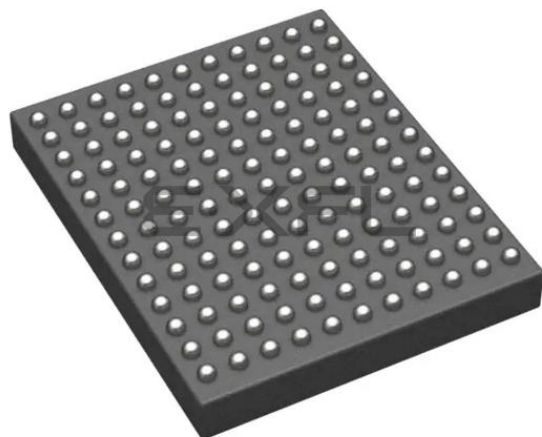




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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I ² C, IrDA, LINbus, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I ² S, LCD, POR, PWM, WDT
Number of I/O	114
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	143-UFBGA, WLCSP
Supplier Device Package	143-WLCSP (4.52x5.55)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f429zgy6tr

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3.26 Inter-integrated sound (I²S)

Two standard I²S interfaces (multiplexed with SPI2 and SPI3) are available. They can be operated in master or slave mode, in full duplex and simplex communication modes, and can be configured to operate with a 16-/32-bit resolution as an input or output channel. Audio sampling frequencies from 8 kHz up to 192 kHz are supported. When either or both of the I²S interfaces is/are configured in master mode, the master clock can be output to the external DAC/CODEC at 256 times the sampling frequency.

All I2Sx can be served by the DMA controller.

Note: For I2S2 full-duplex mode, I2S2_CK and I2S2_WS signals can be used only on GPIO Port B and GPIO Port D.

3.27 Serial Audio interface (SAI1)

The serial audio interface (SAI1) is based on two independent audio sub-blocks which can operate as transmitter or receiver with their FIFO. Many audio protocols are supported by each block: I2S standards, LSB or MSB-justified, PCM/DSP, TDM, AC'97 and SPDIF output, supporting audio sampling frequencies from 8 kHz up to 192 kHz. Both sub-blocks can be configured in master or in slave mode.

In master mode, the master clock can be output to the external DAC/CODEC at 256 times of the sampling frequency.

The two sub-blocks can be configured in synchronous mode when full-duplex mode is required.

SAI1 can be served by the DMA controller.

3.28 Audio PLL (PLLI2S)

The devices feature an additional dedicated PLL for audio I²S and SAI applications. It allows to achieve error-free I²S sampling clock accuracy without compromising on the CPU performance, while using USB peripherals.

The PLLI2S configuration can be modified to manage an I²S/SAI sample rate change without disabling the main PLL (PLL) used for CPU, USB and Ethernet interfaces.

The audio PLL can be programmed with very low error to obtain sampling rates ranging from 8 KHz to 192 KHz.

In addition to the audio PLL, a master clock input pin can be used to synchronize the I²S/SAI flow with an external PLL (or Codec output).

3.29 Audio and LCD PLL(PLLSAI)

An additional PLL dedicated to audio and LCD-TFT is used for SAI1 peripheral in case the PLLI2S is programmed to achieve another audio sampling frequency (49.152 MHz or 11.2896 MHz) and the audio application requires both sampling frequencies simultaneously.

The PLLSAI is also used to generate the LCD-TFT clock.

Table 10. STM32F427xx and STM32F429xx pin and ball definitions (continued)

Pin number								Pin name (function after reset) ⁽¹⁾	Pin type	I / O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA169	UFBGA176	LQFP176	WLCSP143	LQFP208	TFBGA216						
51	73	N12	P12	92	M2	104	L13	PB12	I/O	FT	-	TIM1_BKIN, I2C2_SMBA, SPI2_NSS/I2S2_WS, USART3_CK, CAN2_RX, OTG_HS_ULPI_D5, ETH_MII_TXD0/ETH_R MII_TXD0, OTG_HS_ID, EVENTOUT	-
52	74	M12	P13	93	N1	105	K14	PB13	I/O	FT	-	TIM1_CH1N, SPI2_SCK/I2S2_CK, USART3_CTS, CAN2_TX, OTG_HS_ULPI_D6, ETH_MII_TXD1/ETH_R MII_TXD1, EVENTOUT	OTG_HS_VBUS
53	75	M13	R14	94	K3	106	R14	PB14	I/O	FT	-	TIM1_CH2N, TIM8_CH2N, SPI2_MISO, I2S2ext_SD, USART3_RTS, TIM12_CH1, OTG_HS_DM, EVENTOUT	-
54	76	L13	R15	95	J3	107	R15	PB15	I/O	FT	-	RTC_REFIN, TIM1_CH3N, TIM8_CH3N, SPI2_MOSI/I2S2_SD, TIM12_CH2, OTG_HS_DP, EVENTOUT	-
55	77	L12	P15	96	L2	108	L15	PD8	I/O	FT	-	USART3_TX, FMC_D13, EVENTOUT	-
56	78	K13	P14	97	M1	109	L14	PD9	I/O	FT	-	USART3_RX, FMC_D14, EVENTOUT	-
57	79	K11	N15	98	H4	110	K15	PD10	I/O	FT	-	USART3_CK, FMC_D15, LCD_B3, EVENTOUT	-



Table 12. STM32F427xx and STM32F429xx alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/ 10/11	I2C1/ 2/3	SPI1/2/ 3/4/5/6	SPI2/3/ SAI1	SPI3/ USART1/ 2/3	USART6/ UART4/5/7 /8	CAN1/2/ TIM12/13/14 /LCD	OTG2_HS /OTG1_ FS	ETH	FMC/SDIO /OTG2_FS	DCMI	LCD	SYS
Port A	PA13	JTMS- SWDI O	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVEN TOUT
	PA14	JTCK- SWCL K	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVEN TOUT
	PA15	JTDI	TIM2_ CH1/TIM2 _ETR	-	-	-	SPI1_ NSS	SPI3_ NSS/ I2S3_WS	-	-	-	-	-	-	-	-	EVEN TOUT
Port B	PB0	-	TIM1_ CH2N	TIM3_ CH3	TIM8_ CH2N	-	-	-	-	-	LCD_R3	OTG_HS_ ULPI_D1	ETH_MII_ RXD2	-	-	-	EVEN TOUT
	PB1	-	TIM1_ CH3N	TIM3_ CH4	TIM8_ CH3N	-	-	-	-	-	LCD_R6	OTG_HS_ ULPI_D2	ETH_MII_ RXD3	-	-	-	EVEN TOUT
	PB2	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVEN TOUT
	PB3	JTDO/ TRAC ESWO	TIM2_ CH2	-	-	-	SPI1_ SCK	SPI3_ SCK/ I2S3_CK	-	-	-	-	-	-	-	-	EVEN TOUT
	PB4	NJTR ST	-	TIM3_ CH1	-	-	SPI1_ MISO	SPI3_ MISO	I2S3ext_ SD	-	-	-	-	-	-	-	EVEN TOUT
	PB5	-	-	TIM3_ CH2	-	I2C1_ SMBA	SPI1_ MOSI	SPI3_ MOSI/ I2S3_SD	-	-	CAN2_RX	OTG_HS_ ULPI_D7	ETH_PPS_ OUT	FMC_ SDCKE1	DCMI_ D10	-	EVEN TOUT
	PB6	-	-	TIM4_ CH1	-	I2C1_ SCL	-	-	USART1_ TX	-	CAN2_TX	-	-	FMC_ SDNE1	DCMI_ D5	-	EVEN TOUT
	PB7	-	-	TIM4_ CH2	-	I2C1_ SDA	-	-	USART1_ RX	-	-	-	-	FMC_NL	DCMI_ VSYNC	-	EVEN TOUT
	PB8	-	-	TIM4_ CH3	TIM10_ CH1	I2C1_ SCL	-	-	-	-	CAN1_RX	-	ETH_MII_ TXD3	SDIO_D4	DCMI_ D6	LCD_B6	EVEN TOUT
	PB9	-	-	TIM4_ CH4	TIM11_ CH1	I2C1_ SDA	SPI2_ NSS/I2 S2_WS	-	-	-	CAN1_TX	-	-	SDIO_D5	DCMI_ D7	LCD_B7	EVEN TOUT
	PB10	-	TIM2_ CH3	-	-	I2C2_ SCL	SPI2_ SCK/I2 S2_CK	-	USART3_ TX	-	-	OTG_HS_ ULPI_D3	ETH_MII_ RX_ER	-	-	LCD_G4	EVEN TOUT



Table 12. STM32F427xx and STM32F429xx alternate function mapping (continued)

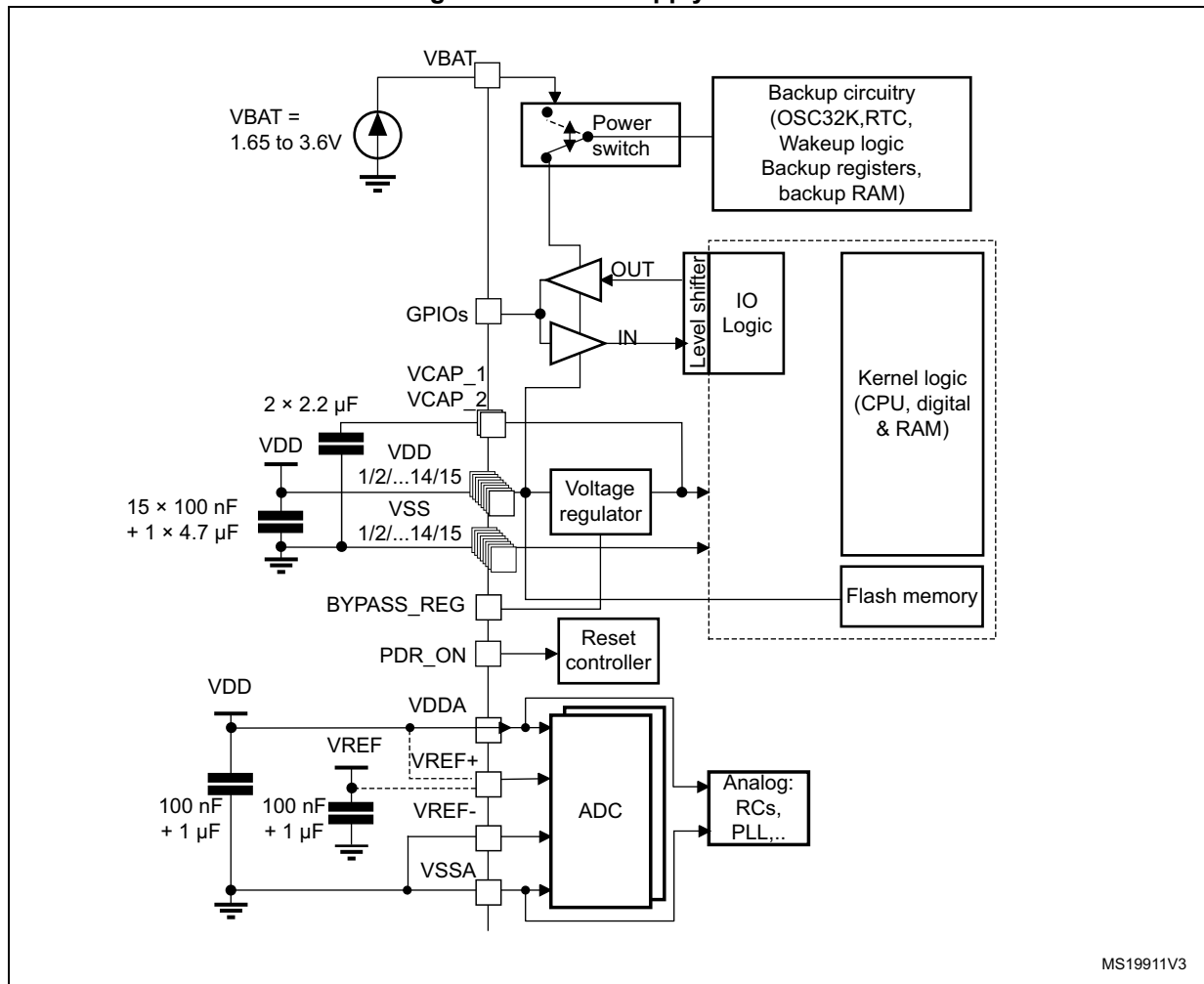
Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/ 10/11	I2C1/ 2/3	SPI1/2/ 3/4/5/6	SPI2/3/ SAI1	SPI3/ USART1/ 2/3	USART6/ UART4/5/7 /8	CAN1/2/ TIM12/13/14 /LCD	OTG2_HS /OTG1_ FS	ETH	FMC/SDIO /OTG2_FS	DCMI	LCD	SYS
Port I	PI7	-	-	-	TIM8_ CH3	-	-	-	-	-	-	-	-	FMC_D29	DCMI_ D7	LCD_B7	EVEN TOUT
	PI8	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVEN TOUT
	PI9	-	-	-	-	-	-	-	-	-	CAN1_RX	-	-	FMC_D30	-	LCD_ VSYNC	EVEN TOUT
	PI10	-	-	-	-	-	-	-	-	-	-	-	ETH_MII_ RX_ER	FMC_D31	-	LCD_ HSYNC	EVEN TOUT
	PI11	-	-	-	-	-	-	-	-	-	-	OTG_HS_ ULPI_DIR	-	-	-	-	EVEN TOUT
	PI12	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_ HSYNC	EVEN TOUT
	PI13	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_ VSYNC	EVEN TOUT
	PI14	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_ CLK	EVEN TOUT
	PI15	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_R0	EVEN TOUT
Port J	PJ0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_R1	EVEN TOUT
	PJ1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_R2	EVEN TOUT
	PJ2	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_R3	EVEN TOUT
	PJ3	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_R4	EVEN TOUT
	PJ4	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_R5	EVEN TOUT
	PJ5	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_R6	EVEN TOUT
	PJ6	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_R7	EVEN TOUT
	PJ7	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_G0	EVEN TOUT

Table 13. STM32F427xx and STM32F429xx register boundary addresses (continued)

Bus	Boundary address	Peripheral
	0x4000 8000 - 0x4000 FFFF	Reserved
APB1	0x4000 7C00 - 0x4000 7FFF	UART8
	0x4000 7800 - 0x4000 7BFF	UART7
	0x4000 7400 - 0x4000 77FF	DAC
	0x4000 7000 - 0x4000 73FF	PWR
	0x4000 6C00 - 0x4000 6FFF	Reserved
	0x4000 6800 - 0x4000 6BFF	CAN2
	0x4000 6400 - 0x4000 67FF	CAN1
	0x4000 6000 - 0x4000 63FF	Reserved
	0x4000 5C00 - 0x4000 5FFF	I2C3
	0x4000 5800 - 0x4000 5BFF	I2C2
	0x4000 5400 - 0x4000 57FF	I2C1
	0x4000 5000 - 0x4000 53FF	UART5
	0x4000 4C00 - 0x4000 4FFF	UART4
	0x4000 4800 - 0x4000 4BFF	USART3
	0x4000 4400 - 0x4000 47FF	USART2
	0x4000 4000 - 0x4000 43FF	I2S3ext
	0x4000 3C00 - 0x4000 3FFF	SPI3 / I2S3
	0x4000 3800 - 0x4000 3BFF	SPI2 / I2S2
	0x4000 3400 - 0x4000 37FF	I2S2ext
	0x4000 3000 - 0x4000 33FF	IWDG
	0x4000 2C00 - 0x4000 2FFF	WWDG
	0x4000 2800 - 0x4000 2BFF	RTC & BKP Registers
	0x4000 2400 - 0x4000 27FF	Reserved
	0x4000 2000 - 0x4000 23FF	TIM14
	0x4000 1C00 - 0x4000 1FFF	TIM13
	0x4000 1800 - 0x4000 1BFF	TIM12
	0x4000 1400 - 0x4000 17FF	TIM7
	0x4000 1000 - 0x4000 13FF	TIM6
	0x4000 0C00 - 0x4000 0FFF	TIM5
	0x4000 0800 - 0x4000 0BFF	TIM4
	0x4000 0400 - 0x4000 07FF	TIM3
	0x4000 0000 - 0x4000 03FF	TIM2

6.1.6 Power supply scheme

Figure 22. Power supply scheme



1. To connect BYPASS_REG and PDR_ON pins, refer to [Section 3.17: Power supply supervisor](#) and [Section 3.18: Voltage regulator](#)
2. The two 2.2 μF ceramic capacitors should be replaced by two 100 nF decoupling capacitors when the voltage regulator is OFF.
3. The 4.7 μF ceramic capacitor must be connected to one of the V_{DD} pin.
4. $V_{DDA}=V_{DD}$ and $V_{SSA}=V_{SS}$.

Caution: Each power supply pair (V_{DD}/V_{SS} , V_{DDA}/V_{SSA} ...) must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB to ensure good operation of the device. It is not recommended to remove filtering capacitors to reduce PCB size or cost. This might cause incorrect operation of the device.

6.3.7 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

The current consumption is measured as described in [Figure 23: Current consumption measurement scheme](#).

All the run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to CoreMark code.

Typical and maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load).
- All peripherals are disabled except if it is explicitly mentioned.
- The Flash memory access time is adjusted both to f_{HCLK} frequency and V_{DD} range (see [Table 18: Limitations depending on the operating power supply range](#)).
- Regulator ON
- The voltage scaling and over-drive mode are adjusted to f_{HCLK} frequency as follows:
 - Scale 3 for $f_{HCLK} \leq 120$ MHz
 - Scale 2 for $120 \text{ MHz} < f_{HCLK} \leq 144$ MHz
 - Scale 1 for $144 \text{ MHz} < f_{HCLK} \leq 180$ MHz. The over-drive is only ON at 180 MHz.
- The system clock is HCLK, $f_{PCLK1} = f_{HCLK}/4$, and $f_{PCLK2} = f_{HCLK}/2$.
- External clock frequency is 4 MHz and PLL is ON when f_{HCLK} is higher than 25 MHz.
- The maximum values are obtained for $V_{DD} = 3.6$ V and a maximum ambient temperature (T_A), and the typical values for $T_A = 25$ °C and $V_{DD} = 3.3$ V unless otherwise specified.

Table 32. Typical current consumption in Sleep mode, regulator ON, $V_{DD}=1.7\text{ V}^{(1)}$

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Typ	Unit
I_{DD}	Supply current in Sleep mode from V_{DD} supply	All Peripherals enabled	168	65.5	mA
			150	55.5	
			144	53.5	
			120	39.0	
			90	31.6	
			60	21.7	
			30	9.8	
			25	8.8	
		All Peripherals disabled	168	15.7	
			150	13.7	
			144	12.7	
			120	9.7	
			90	7.7	
			60	5.7	
			30	4.7	
			25	2.8	

1. When peripherals are enabled, the power consumption corresponding to the analog part of the peripherals (such as ADC, or DAC) is not included.

On-chip peripheral current consumption

The MCU is placed under the following conditions:

- At startup, all I/O pins are in analog input configuration.
- All peripherals are disabled unless otherwise mentioned.
- I/O compensation cell enabled.
- The ART accelerator is ON.
- Scale 1 mode selected, internal digital voltage V12 = 1.32 V.
- HCLK is the system clock. $f_{PCLK1} = f_{HCLK}/4$, and $f_{PCLK2} = f_{HCLK}/2$.

The given value is calculated by measuring the difference of current consumption

- with all peripherals clocked off
- with only one peripheral clocked on
- $f_{HCLK} = 180$ MHz (Scale1 + over-drive ON), $f_{HCLK} = 144$ MHz (Scale 2), $f_{HCLK} = 120$ MHz (Scale 3)"
- Ambient operating temperature is 25 °C and $V_{DD}=3.3$ V.

Table 35. Peripheral current consumption

Peripheral		I_{DD} (Typ) ⁽¹⁾			Unit
		Scale 1	Scale 2	Scale 3	
AHB1 (up to 180 MHz)	GPIOA	2.50	2.36	2.08	$\mu A/MHz$
	GPIOB	2.56	2.36	2.08	
	GPIOC	2.44	2.29	2.00	
	GPIOD	2.50	2.36	2.08	
	GPIOE	2.44	2.29	2.00	
	GPIOF	2.44	2.29	2.00	
	GPIOG	2.39	2.22	2.00	
	GPIOH	2.33	2.15	1.92	
	GPIOI	2.39	2.22	2.00	
	GPIOJ	2.33	2.15	1.92	
	GPIOK	2.33	2.15	1.92	
	OTG_HS+ULPI	27.00	24.86	21.92	
	CRC	0.44	0.42	0.33	
	BKPSRAM	0.78	0.69	0.58	
	DMA1	25.33	23.26	20.50	
	DMA2	24.72	22.71	20.00	
	DMA2D	28.50	26.32	23.33	
	ETH_MAC ETH_MAC_TX ETH_MAC_RX ETH_MAC_PTP	21.56	20.07	17.75	

6.3.12 PLL spread spectrum clock generation (SSCG) characteristics

The spread spectrum clock generation (SSCG) feature allows to reduce electromagnetic interferences (see [Table 52: EMI characteristics](#)). It is available only on the main PLL.

Table 46. SSCG parameters constraint

Symbol	Parameter	Min	Typ	Max ⁽¹⁾	Unit
f_{Mod}	Modulation frequency	-	-	10	KHz
md	Peak modulation depth	0.25	-	2	%
MODEPER * INCSTEP		-	-	$2^{15} - 1$	-

1. Guaranteed by design.

Equation 1

The frequency modulation period (MODEPER) is given by the equation below:

$$\text{MODEPER} = \text{round}[f_{\text{PLL_IN}} / (4 \times f_{\text{Mod}})]$$

$f_{\text{PLL_IN}}$ and f_{Mod} must be expressed in Hz.

As an example:

If $f_{\text{PLL_IN}} = 1$ MHz, and $f_{\text{MOD}} = 1$ kHz, the modulation depth (MODEPER) is given by equation 1:

$$\text{MODEPER} = \text{round}[10^6 / (4 \times 10^3)] = 250$$

Equation 2

Equation 2 allows to calculate the increment step (INCSTEP):

$$\text{INCSTEP} = \text{round}[(2^{15} - 1) \times \text{md} \times \text{PLLN}] / (100 \times 5 \times \text{MODEPER})$$

$f_{\text{VCO_OUT}}$ must be expressed in MHz.

With a modulation depth (md) = $\pm 2\%$ (4 % peak to peak), and PLLN = 240 (in MHz):

$$\text{INCSTEP} = \text{round}[(2^{15} - 1) \times 2 \times 240] / (100 \times 5 \times 250) = 126 \text{md}(\text{quantitized})\%$$

An amplitude quantization error may be generated because the linear modulation profile is obtained by taking the quantized values (rounded to the nearest integer) of MODPER and INCSTEP. As a result, the achieved modulation depth is quantized. The percentage quantized modulation depth is given by the following formula:

$$\text{md}_{\text{quantized}}\% = (\text{MODEPER} \times \text{INCSTEP} \times 100 \times 5) / ((2^{15} - 1) \times \text{PLLN})$$

As a result:

$$\text{md}_{\text{quantized}}\% = (250 \times 126 \times 100 \times 5) / ((2^{15} - 1) \times 240) = 2.002\%(\text{peak})$$

6.3.17 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in [Table 56: I/O static characteristics](#) are derived from tests performed under the conditions summarized in [Table 17](#). All I/Os are CMOS and TTL compliant.

Table 56. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{IL}	FT, TTa and NRST I/O input low level voltage	1.7 V≤V _{DD} ≤3.6 V	-	-	0.35V _{DD} (1) - 0.04	V
					0.3V _{DD} (2)	
	BOOT0 I/O input low level voltage	1.75 V≤V _{DD} ≤3.6 V, -40 °C≤T _A ≤105 °C	-	-	0.1V _{DD} +0.1(1)	
		1.7 V≤V _{DD} ≤3.6 V, 0 °C≤T _A ≤105 °C	-	-		
V _{IH}	FT, TTa and NRST I/O input high level voltage(5)	1.7 V≤V _{DD} ≤3.6 V	0.45V _{DD} +0.3(1)	-	-	V
			0.7V _{DD} (2)			
	BOOT0 I/O input high level voltage	1.75 V≤V _{DD} ≤3.6 V, -40 °C≤T _A ≤105 °C	0.17V _{DD} +0.7(1)	-	-	
		1.7 V≤V _{DD} ≤3.6 V, 0 °C≤T _A ≤105 °C				
V _{HYS}	FT, TTa and NRST I/O input hysteresis	1.7 V≤V _{DD} ≤3.6 V	10%V _{DD} (3)	-	-	V
	BOOT0 I/O input hysteresis	1.75 V≤V _{DD} ≤3.6 V, -40 °C≤T _A ≤105 °C	0.1	-	-	
		1.7 V≤V _{DD} ≤3.6 V, 0 °C≤T _A ≤105 °C				
I _{lkg}	I/O input leakage current (4)	V _{SS} ≤V _{IN} ≤V _{DD}	-	-	±1	μA
	I/O FT input leakage current (5)	V _{IN} = 5 V	-	-	3	

Table 58. I/O AC characteristics⁽¹⁾⁽²⁾ (continued)

OSPEEDRy [1:0] bit value ⁽¹⁾	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
11	$f_{\max(\text{IO})\text{out}}$	Maximum frequency ⁽³⁾	$C_L = 30 \text{ pF}, V_{DD} \geq 2.7 \text{ V}$	-	-	100 ⁽⁴⁾	MHz
			$C_L = 30 \text{ pF}, V_{DD} \geq 1.8 \text{ V}$	-	-	50	
			$C_L = 30 \text{ pF}, V_{DD} \geq 1.7 \text{ V}$	-	-	42.5	
			$C_L = 10 \text{ pF}, V_{DD} \geq 2.7 \text{ V}$	-	-	180 ⁽⁴⁾	
			$C_L = 10 \text{ pF}, V_{DD} \geq 1.8 \text{ V}$	-	-	100	
			$C_L = 10 \text{ pF}, V_{DD} \geq 1.7 \text{ V}$	-	-	72.5	
	$t_{f(\text{IO})\text{out}} / t_{r(\text{IO})\text{out}}$	Output high to low level fall time and output low to high level rise time	$C_L = 30 \text{ pF}, V_{DD} \geq 2.7 \text{ V}$	-	-	4	ns
			$C_L = 30 \text{ pF}, V_{DD} \geq 1.8 \text{ V}$	-	-	6	
			$C_L = 30 \text{ pF}, V_{DD} \geq 1.7 \text{ V}$	-	-	7	
			$C_L = 10 \text{ pF}, V_{DD} \geq 2.7 \text{ V}$	-	-	2.5	
			$C_L = 10 \text{ pF}, V_{DD} \geq 1.8 \text{ V}$	-	-	3.5	
			$C_L = 10 \text{ pF}, V_{DD} \geq 1.7 \text{ V}$	-	-	4	
-	$t_{\text{EXTI}pw}$	Pulse width of external signals detected by the EXTI controller	-	10	-	-	ns

1. Guaranteed by design.
2. The I/O speed is configured using the OSPEEDRy[1:0] bits. Refer to the STM32F4xx reference manual for a description of the GPIOx_SPEEDR GPIO port output speed register.
3. The maximum frequency is defined in [Figure 36](#).
4. For maximum frequencies above 50 MHz and $V_{DD} > 2.4 \text{ V}$, the compensation cell should be used.

Figure 36. I/O AC characteristics definition

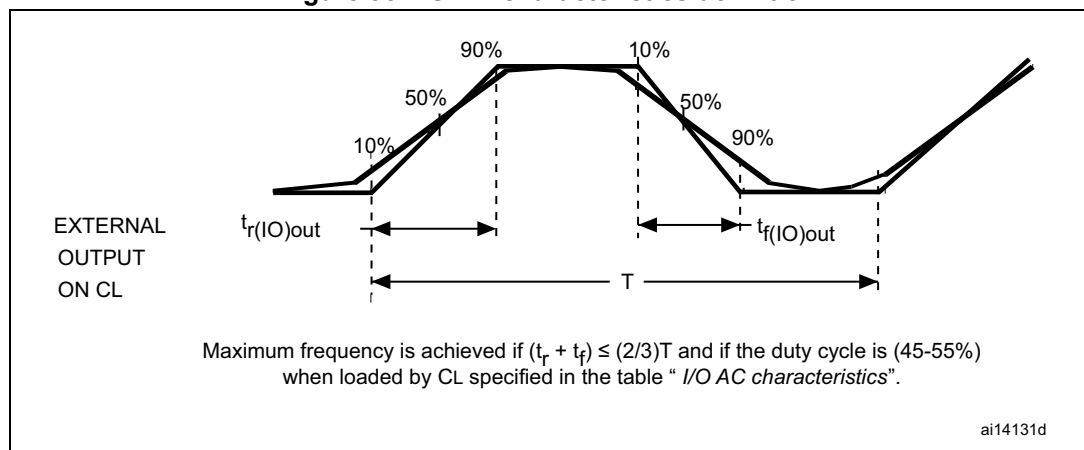
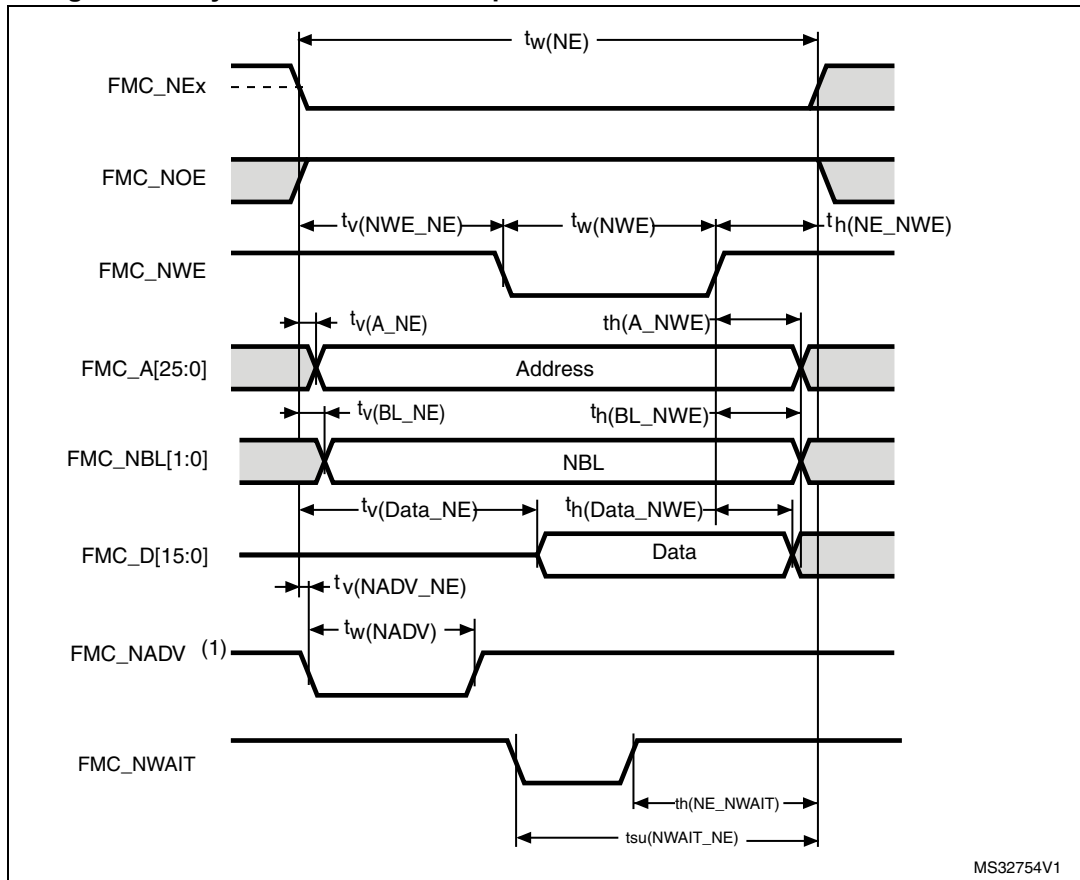


Figure 56. Asynchronous non-multiplexed SRAM/PSRAM/NOR write waveforms

1. Mode 2/B, C and D only. In Mode 1, FMC_NADV is not used.

Table 88. Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings⁽¹⁾⁽²⁾

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$3T_{HCLK}$	$3T_{HCLK}+1$	ns
$t_{v(NWE_NE)}$	FMC_NEx low to FMC_NWE low	$T_{HCLK} - 0.5$	$T_{HCLK}+0.5$	ns
$t_{w(NWE)}$	FMC_NWE low time	T_{HCLK}	$T_{HCLK}+0.5$	ns
$t_{h(NE_NWE)}$	FMC_NWE high to FMC_NE high hold time	$T_{HCLK} + 1.5$	-	ns
$t_{v(A_NE)}$	FMC_NEx low to FMC_A valid	-	0	ns
$t_{h(A_NWE)}$	Address hold time after FMC_NWE high	$T_{HCLK}+0.5$	-	ns
$t_{v(BL_NE)}$	FMC_NEx low to FMC_BL valid	-	1.5	ns
$t_{h(BL_NWE)}$	FMC_BL hold time after FMC_NWE high	$T_{HCLK}+0.5$	-	ns
$t_{v(Data_NE)}$	Data to FMC_NEx low to Data valid	-	$T_{HCLK}+2$	ns
$t_{h(Data_NWE)}$	Data hold time after FMC_NWE high	$T_{HCLK}+0.5$	-	ns
$t_{v(NADV_NE)}$	FMC_NEx low to FMC_NADV low	-	0.5	ns
$t_{w(NADV)}$	FMC_NADV low time	-	$T_{HCLK}+0.5$	ns

1. $C_L = 30$ pF.

2. Guaranteed by characterization results.

Table 93. Asynchronous multiplexed PSRAM/NOR write-NWAIT timings⁽¹⁾⁽²⁾

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$9T_{HCLK}$	$9T_{HCLK}+0.5$	ns
$t_{w(NWE)}$	FMC_NWE low time	$7T_{HCLK}$	$7T_{HCLK}+2$	ns
$t_{su(NWAIT_NE)}$	FMC_NWAIT valid before FMC_NEx high	$6T_{HCLK}+1.5$	-	ns
$t_{h(NE_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$4T_{HCLK}-1$	-	ns

1. $C_L = 30$ pF.

2. Guaranteed by characterization results.

Synchronous waveforms and timings

[Figure 59](#) through [Figure 62](#) represent synchronous waveforms and [Table 94](#) through [Table 97](#) provide the corresponding timings. The results shown in these tables are obtained with the following FMC configuration:

- BurstAccessMode = FMC_BurstAccessMode_Enable;
- MemoryType = FMC_MemoryType_CRAM;
- WriteBurst = FMC_WriteBurst_Enable;
- CLKDivision = 1; (0 is not supported, see the STM32F4xx reference manual : RM0090)
- DataLatency = 1 for NOR Flash; DataLatency = 0 for PSRAM

In all timing tables, the T_{HCLK} is the HCLK clock period (with maximum FMC_CLK = 90 MHz).

Figure 69. NAND controller waveforms for read access

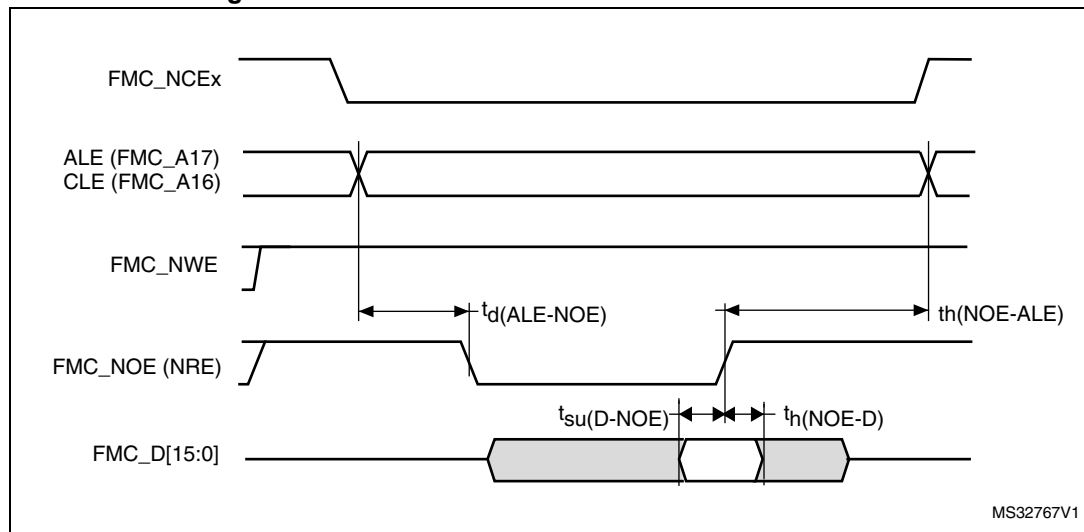


Figure 70. NAND controller waveforms for write access

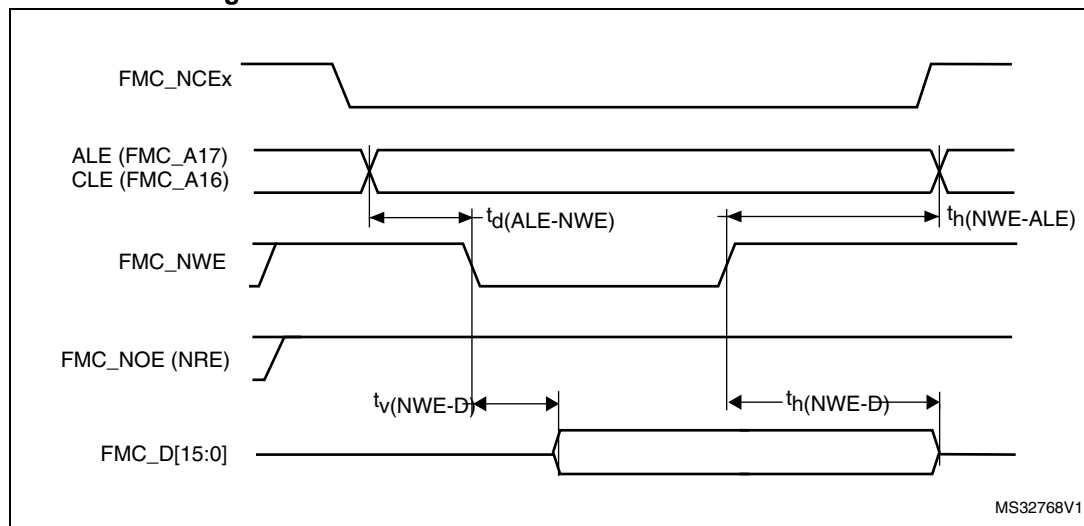


Table 104. SDRAM write timings⁽¹⁾⁽²⁾

Symbol	Parameter	Min	Max	Unit
$t_{w(SDCLK)}$	FMC_SDCLK period	$2T_{HCLK} - 0.5$	$2T_{HCLK} + 0.5$	ns
$t_{d(SDCLKL_Data)}$	Data output valid time	-	3.5	
$t_{h(SDCLKL_Data)}$	Data output hold time	0	-	
$t_{d(SDCLKL_Add)}$	Address valid time	-	1.5	
$t_{d(SDCLKL_SDNWE)}$	SDNWE valid time	-	1	
$t_{h(SDCLKL_SDNWE)}$	SDNWE hold time	0	-	
$t_{d(SDCLKL_SDNE)}$	Chip select valid time	-	0.5	
$t_{h(SDCLKL_SDNE)}$	Chip select hold time	0	-	
$t_{d(SDCLKL_SDNRAS)}$	SDNRAS valid time	-	2	
$t_{h(SDCLKL_SDNRAS)}$	SDNRAS hold time	0	-	
$t_{d(SDCLKL_SDNCAS)}$	SDNCAS valid time	-	0.5	
$t_{d(SDCLKL_SDNCAS)}$	SDNCAS hold time	0	-	
$t_{d(SDCLKL_NBL)}$	NBL valid time	-	0.5	
$t_{h(SDCLKL_NBL)}$	NBL output time	0	-	

1. CL = 30 pF on data and address lines. CL=15pF on FMC_SDCLK.

2. Guaranteed by characterization results.

Table 105. LPDDR SDRAM write timings⁽¹⁾⁽²⁾

Symbol	Parameter	Min	Max	Unit
$t_{w(SDCLK)}$	FMC_SDCLK period	$2T_{HCLK} - 0.5$	$2T_{HCLK} + 0.5$	ns
$t_{d(SDCLKL_Data)}$	Data output valid time	-	5	
$t_{h(SDCLKL_Data)}$	Data output hold time	2	-	
$t_{d(SDCLKL_Add)}$	Address valid time	-	2.8	
$t_{d(SDCLKL_SDNWE)}$	SDNWE valid time	-	2	
$t_{h(SDCLKL_SDNWE)}$	SDNWE hold time	1	-	
$t_{d(SDCLKL_SDNE)}$	Chip select valid time	-	1.5	
$t_{h(SDCLKL_SDNE)}$	Chip select hold time	1	-	
$t_{d(SDCLKL_SDNRAS)}$	SDNRAS valid time	-	1.5	
$t_{h(SDCLKL_SDNRAS)}$	SDNRAS hold time	1.5	-	
$t_{d(SDCLKL_SDNCAS)}$	SDNCAS valid time	-	1.5	
$t_{d(SDCLKL_SDNCAS)}$	SDNCAS hold time	1.5	-	
$t_{d(SDCLKL_NBL)}$	NBL valid time	-	1.5	
$t_{h(SDCLKL_NBL)}$	NBL output time	1.5	-	

1. CL = 10 pF.

2. Guaranteed by characterization results.

6.3.27 Camera interface (DCMI) timing specifications

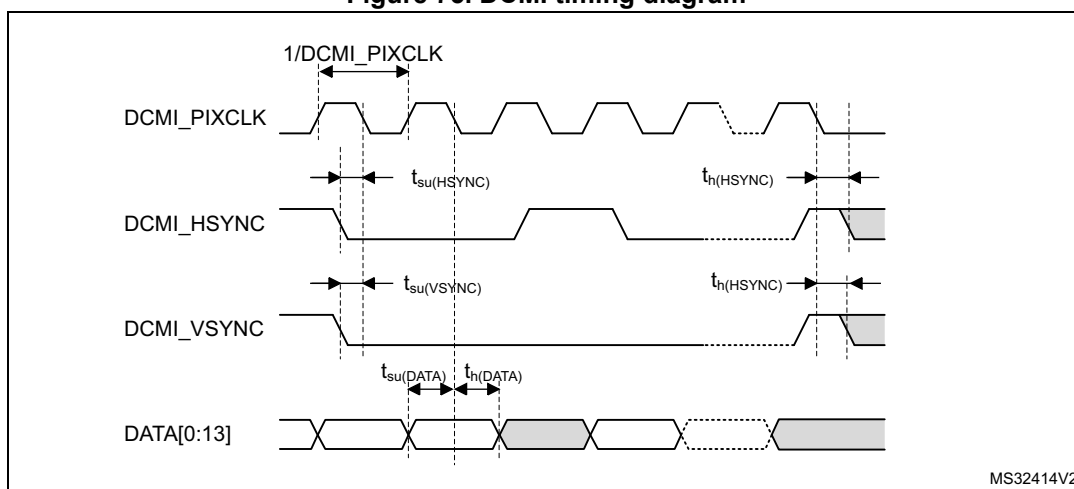
Unless otherwise specified, the parameters given in [Table 106](#) for DCMI are derived from tests performed under the ambient temperature, f_{HCLK} frequency and V_{DD} supply voltage summarized in [Table 17](#), with the following configuration:

- DCMI_PIXCLK polarity: falling
- DCMI_VSYNC and DCMI_HSYNC polarity: high
- Data formats: 14 bits

Table 106. DCMI characteristics

Symbol	Parameter	Min	Max	Unit
	Frequency ratio DCMI_PIXCLK/ f_{HCLK}	-	0.4	
DCMI_PIXCLK	Pixel clock input	-	54	MHz
D_{Pixel}	Pixel clock input duty cycle	30	70	%
$t_{su}(DATA)$	Data input setup time	2	-	ns
$t_h(DATA)$	Data input hold time	2.5	-	
$t_{su}(HSYNC)$ $t_{su}(VSYNC)$	DCMI_HSYNC/DCMI_VSYNC input setup time	0.5	-	
$t_h(HSYNC)$ $t_h(VSYNC)$	DCMI_HSYNC/DCMI_VSYNC input hold time	1	-	

Figure 75. DCMI timing diagram



**Table 114. LQFP176 - 176-pin, 24 x 24 mm low-profile quad flat package
mechanical data (continued)**

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
ZD	-	1.250	-	-	0.0492	-
E	23.900	-	24.100	0.9409	-	0.9488
HE	25.900	-	26.100	1.0197	-	1.0276
ZE	-	1.250	-	-	0.0492	-
e	-	0.500	-	-	0.0197	-
L ⁽²⁾	0.450	-	0.750	0.0177	-	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	-	7°	0°	-	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

2. L dimension is measured at gauge plane at 0.25 mm above the seating plane.

Table 120. TFBGA216 - 216 ball 13 × 13 mm 0.8 mm pitch thin fine pitch ball grid array package mechanical data (continued)

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.080	-	-	0.0031

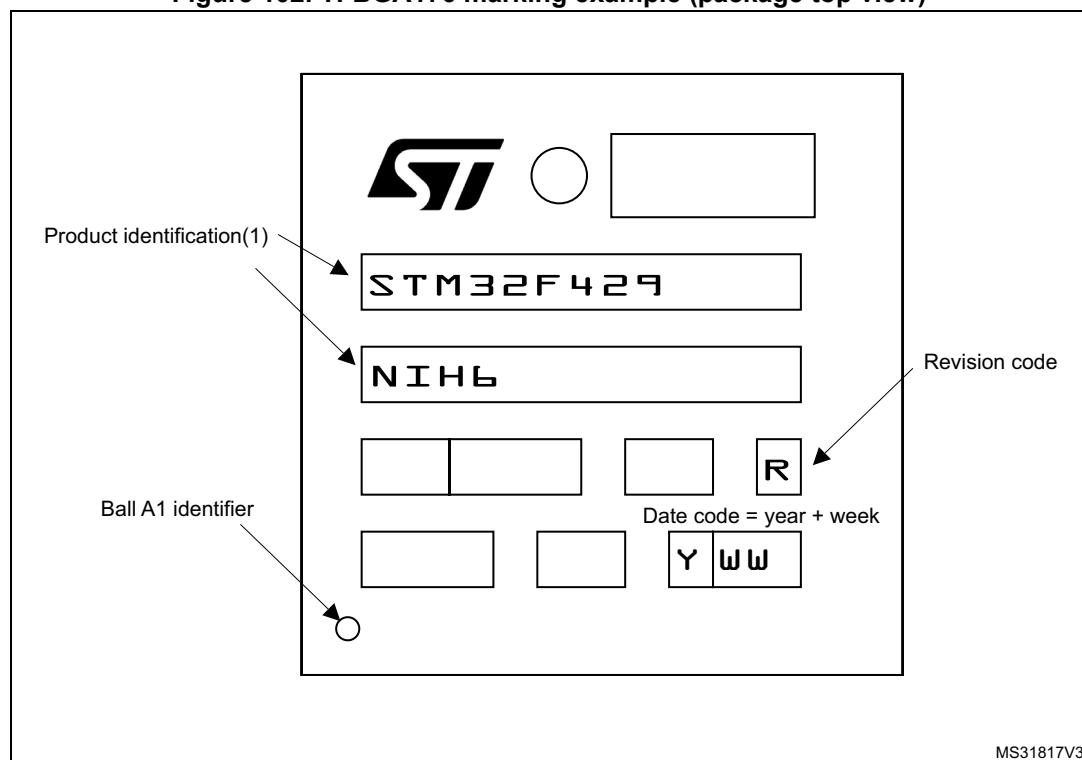
1. Values in inches are converted from mm and rounded to 4 decimal digits.

Device marking for TFBGA176

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

Other optional marking or inset/upset marks, which depends assembly location, are not indicated below.

Figure 102. TFBGA176 marking example (package top view)



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.