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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

#### Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I <sup>2</sup> C, IrDA, LINbus, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I <sup>2</sup> S, LCD, POR, PWM, WDT
Number of I/O	114
Program Memory Size	2MB (2M × 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f429zit6g

Email: info@E-XFL.COM

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1. The timers connected to APB2 are clocked from TIMxCLK up to 180 MHz, while the timers connected to APB1 are clocked from TIMxCLK either up to 90 MHz or 180 MHz depending on TIMPRE bit configuration in the RCC\_DCKCFGR register.

2. The LCD-TFT is available only on STM32F429xx devices.





Figure 5. STM32F427xx and STM32F429xx Multi-AHB matrix

## 3.8 DMA controller (DMA)

The devices feature two general-purpose dual-port DMAs (DMA1 and DMA2) with 8 streams each. They are able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. They feature dedicated FIFOs for APB/AHB peripherals, support burst transfer and are designed to provide the maximum peripheral bandwidth (AHB/APB).

The two DMA controllers support circular buffer management, so that no specific code is needed when the controller reaches the end of the buffer. The two DMA controllers also have a double buffering feature, which automates the use and switching of two memory buffers without requiring any special code.

Each stream is connected to dedicated hardware DMA requests, with support for software trigger on each stream. Configuration is made by software and transfer sizes between source and destination are independent.



## 3.11 Chrom-ART Accelerator<sup>™</sup> (DMA2D)

The Chrom-Art Accelerator <sup>™</sup> (DMA2D) is a graphic accelerator which offers advanced bit blitting, row data copy and pixel format conversion. It supports the following functions:

- Rectangle filling with a fixed color
- Rectangle copy
- Rectangle copy with pixel format conversion
- Rectangle composition with blending and pixel format conversion.

Various image format coding are supported, from indirect 4bpp color mode up to 32bpp direct color. It embeds dedicated memory to store color lookup tables.

An interrupt can be generated when an operation is complete or at a programmed watermark.

All the operations are fully automatized and are running independently from the CPU or the DMAs.

## 3.12 Nested vectored interrupt controller (NVIC)

The devices embed a nested vectored interrupt controller able to manage 16 priority levels, and handle up to 91 maskable interrupt channels plus the 16 interrupt lines of the  $Cortex^{\$}$ -M4 with FPU core.

- Closely coupled NVIC gives low-latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Allows early processing of interrupts
- Processing of late arriving, higher-priority interrupts
- Support tail chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimum interrupt latency.

## 3.13 External interrupt/event controller (EXTI)

The external interrupt/event controller consists of 23 edge-detector lines used to generate interrupt/event requests. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the Internal APB2 clock period. Up to 168 GPIOs can be connected to the 16 external interrupt lines.

## 3.14 Clocks and startup

On reset the 16 MHz internal RC oscillator is selected as the default CPU clock. The 16 MHz internal RC oscillator is factory-trimmed to offer 1% accuracy over the full temperature range. The application can then select as system clock either the RC oscillator or an external 4-26 MHz clock source. This clock can be monitored for failure. If a failure is



	Pin number												
LQFP100	LQFP144	UFBGA169	UFBGA176	LQFP176	WLCSP143	LQFP208	TFBGA216	Pin name (function after reset) <sup>(1)</sup>	Pin type	I / O structure	Notes	Alternate functions	Additional functions
82	115	C9	C12	143	C4	165	C12	PD1	I/O	FT	-	CAN1_TX, FMC_D3, EVENTOUT	-
83	116	В9	D12	144	A3	166	D12	PD2	I/O	FT	-	TIM3_ETR, UART5_RX, SDIO_CMD, DCMI_D11, EVENTOUT	-
84	117	A9	D11	145	B4	167	C11	PD3	I/O	FT	-	SPI2_SCK/I2S2_CK, USART2_CTS, FMC_CLK, DCMI_D5, LCD_G7, EVENTOUT	-
85	118	D8	D10	146	B5	168	D11	PD4	I/O	FT	-	USART2_RTS, FMC_NOE, EVENTOUT	-
86	119	C8	C11	147	A4	169	C10	PD5	I/O	FT	-	USART2_TX, FMC_NWE, EVENTOUT	-
-	120	-	D8	148	-	170	F8	V <sub>SS</sub>	S		-	-	-
-	121	D6	C8	149	C5	171	E9	V <sub>DD</sub>	S		-	-	-
87	122	B8	B11	150	F4	172	B11	PD6	I/O	FT	-	SPI3_MOSI/I2S3_SD, SAI1_SD_A, USART2_RX, FMC_NWAIT, DCMI_D10, LCD_B2, EVENTOUT	-
88	123	A8	A11	151	A5	173	A11	PD7	I/O	FT	-	USART2_CK, FMC_NE1/FMC_NCE2, EVENTOUT	-
-	-	-	-	-	-	174	B10	PJ12	I/O	FT	-	LCD_B0, EVENTOUT	-
_	-	-	-	-	-	175	B9	PJ13	I/O	FT	-	LCD_B1, EVENTOUT	-
-	-	-	-	-	-	176	C9	PJ14	I/O	FT	-	LCD_B2, EVENTOUT	-
_	-	-	-	-	-	177	D10	PJ15	I/O	FT	-	LCD_B3, EVENTOUT	-
-	124	NC (2)	C10	152	E5	178	D9	PG9	I/O	FT	-	USART6_RX, FMC_NE2/FMC_NCE3, DCMI_VSYNC <sup>(8)</sup> , EVENTOUT	-

 Table 10. STM32F427xx and STM32F429xx pin and ball definitions (continued)



Pin name	CF	NOR/PSRAM/ SRAM	NOR/PSRAM Mux	NAND16	SDRAM
PF6	NIORD				
PF7	NREG				
PF8	NIOWR				
PF9	CD				
PF10	INTR				
PG6				INT2	
PG7				INT3	
PE0		NBL0	NBL0		NBL0
PE1		NBL1	NBL1		NBL1
PI4		NBL2			NBL2
PI5		NBL3			NBL3
PG8					SDCLK
PC0					SDNWE
PF11					SDNRAS
PG15					SDNCAS
PH2					SDCKE0
PH3					SDNE0
PH6					SDNE1
PH7					SDCKE1
PH5					SDNWE
PC2					SDNE0
PC3					SDCKE0
PB5					SDCKE1
PB6					SDNE1

Table 11. FMC pin definition (continued)



Symbol	Ratings	Max.	Unit
$\Sigma I_{VDD}$	Total current into sum of all $V_{DD_x}$ power lines (source) <sup>(1)</sup>	270	
$\Sigma I_{VSS}$	Total current out of sum of all $V_{SS_x}$ ground lines $(sink)^{(1)}$	- 270	
I <sub>VDD</sub>	Maximum current into each V <sub>DD_x</sub> power line (source) <sup>(1)</sup>	100	
I <sub>VSS</sub>	Maximum current out of each V <sub>SS_x</sub> ground line (sink) <sup>(1)</sup>	- 100	
1	Output current sunk by any I/O and control pin	25	
Ι <sub>ΙΟ</sub>	Output current sourced by any I/Os and control pin	- 25	
ΣI	Total output current sunk by sum of all I/O and control pins <sup>(2)</sup>	120	mA
2110	Total output current sourced by sum of all I/Os and control pins <sup>(2)</sup>	- 120	
I <sub>INJ(PIN)</sub> <sup>(3)</sup>	Injected current on FT pins <sup>(4)</sup>		
	Injected current on NRST and BOOT0 pins <sup>(4)</sup>	- 5/+0	
	Injected current on TTa pins <sup>(5)</sup>	±5	
$\Sigma I_{\rm INJ(PIN)}^{(5)}$	Total injected current (sum of all I/O and control pins) <sup>(6)</sup>	±25	

1. All main power (V<sub>DD</sub>, V<sub>DDA</sub>) and ground (V<sub>SS</sub>, V<sub>SSA</sub>) pins must always be connected to the external power supply, in the permitted range.

2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count LQFP packages.

3. Negative injection disturbs the analog performance of the device. See note in Section 6.3.21: 12-bit ADC characteristics.

4. Positive injection is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.

5. A positive injection is induced by  $V_{IN} > V_{DDA}$  while a negative injection is induced by  $V_{IN} < V_{SS}$ .  $I_{INJ(PIN)}$  must never be exceeded. Refer to *Table 14* for the values of the maximum allowed input voltage.

6. When several inputs are submitted to a current injection, the maximum  $\Sigma I_{INJ(PIN)}$  is the absolute sum of the positive and negative injected currents (instantaneous values).

#### Table 16. Thermal characteristics

Symbol	Ratings	Value	Unit
T <sub>STG</sub>	Storage temperature range	– 65 to +150	°C
TJ	Maximum junction temperature	125	°C



## 6.3.5 Reset and power control block characteristics

The parameters given in *Table 22* are derived from tests performed under ambient temperature and  $V_{DD}$  supply voltage conditions summarized in *Table 17*.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
		PLS[2:0]=000 (rising edge)	2.09	2.14	2.19	V
SymbolParameterConditionsNumberPLS[2:0]=000 (rising edge)2PLS[2:0]=000 (rising edge)2PLS[2:0]=001 (rising edge)2PLS[2:0]=001 (rising edge)2PLS[2:0]=001 (rising edge)2PLS[2:0]=010 (rising edge)2PLS[2:0]=100 (rising edge)2PLS[2:0]=110 (rising edge)2PLS[2:0]=110 (rising edge)2PLS[2:0]=111 (rising edge)2PLS[2:0]=111 (rising edge)2VPOR/PDRPOR hysteresisVPOR/PDRPOR hysteresisVBOR1PDR hysteresisPLSPAHATFalling edgeVBOR2Falling edgeVBOR3Brownout level 2 thresholdPLSING edge2PLSING edge2PLSING edge2PLSING edge2PLSING edge2PLSING edge2PLSING edge <td< td=""><td></td><td>PLS[2:0]=000 (falling edge)</td><td>1.98</td><td>2.04</td><td>2.08</td><td>V</td></td<>		PLS[2:0]=000 (falling edge)	1.98	2.04	2.08	V
		PLS[2:0]=001 (rising edge)	2.23	2.30	2.37	V
		PLS[2:0]=001 (falling edge)	2.13	2.19	2.25	V
		PLS[2:0]=010 (rising edge)	2.39	2.45	2.51	V
		PLS[2:0]=010 (falling edge)	2.29	2.35	2.39	V
	2.54	2.60	2.65	V		
	Programmable voltage	PLS[2:0]=011 (falling edge)	2.44	2.51	2.56	V
	detector level selection	PLS[2:0]=100 (rising edge)	2.70	2.76	2.82	V
		PLS[2:0]=100 (falling edge)	2.59	2.66	2.71	V
		PLS[2:0]=101 (rising edge)	2.86	2.93	2.99	V
		PLS[2:0]=101 (falling edge)	2.65	2.84	2.92	V
		PLS[2:0]=110 (rising edge)	2.96	3.03	3.10	V
		PLS[2:0]=110 (falling edge)	2.85	2.93	2.99	V
		PLS[2:0]=111 (rising edge)	3.07	3.14	3.21	V
		PLS[2:0]=111 (falling edge)	2.95	3.03	3.09	V
V <sub>PVDhyst</sub> <sup>(1)</sup>	PVD hysteresis		-	100	-	mV
V <sub>PVD</sub> V <sub>PVDhyst</sub> <sup>(1)</sup> V <sub>POR/PDR</sub> V <sub>PORhyst</sub> <sup>(1)</sup> V <sub>BOR1</sub> V <sub>BOR2</sub> V <sub>BOR3</sub> V <sub>BORhyst</sub> <sup>(1)</sup> T <sub>RSTTE</sub> MPO	Power-on/power-down	Falling edge	1.60	1.68	1.76	V
	reset threshold	Rising edge	1.64	1.72	1.80	V
V <sub>PDRhyst</sub> <sup>(1)</sup>	PDR hysteresis		-	40	-	mV
M	Brownout level 1	Falling edge	2.13	2.19	2.24	V
VBOR1	threshold	Rising edge	MinTypMaxUnit2.092.142.19V1.982.042.08V2.232.302.37V2.132.192.25V2.392.452.51V2.292.352.39V2.542.602.65V2.702.762.82V2.592.662.71V2.862.932.99V2.852.932.99V2.963.033.10V2.852.932.99V3.073.143.21V2.953.033.09V1.601.681.76V1.641.721.80V2.132.192.24V2.132.192.24V2.132.192.24V2.132.192.24V2.132.192.33V2.132.192.442.502.132.192.44V2.132.922.33V2.132.192.63V2.132.192.852.922.852.922.97V2.852.922.97V2.852.922.97V0.51.53.0ms			
M	Brownout level 2	Falling edge	2.44	2.50	2.56	V
VPVD VPVDhyst <sup>(1)</sup> VPOR/PDR VPDRhyst <sup>(1)</sup> VBOR1 VBOR2 VBOR3 VBORhyst <sup>(1)</sup> TRSTTEMPO	threshold	Rising edge	2.53	2.59	2.63	V
VPVD VPVDvitin VPOR/PDR VPOR/PDR VBOR1 VBOR1 VBOR2 VBOR3 VBORhyst <sup>(1)</sup> TRSTTEMPO	Brownout level 3	Falling edge	2.75	2.83	2.88	V
	threshold	Rising edge	2.85	2.92	2.97	V
V <sub>BORhyst</sub> <sup>(1)</sup>	BOR hysteresis		-	100	-	mV
T <sub>RSTTEMPO</sub>	POR reset temporization		0.5	1.5	3.0	ms

Table 22.	reset and	power	control block	characteristics
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Table 24. Typical and maximum current consumption in Run mode, code with data processing
running from Flash memory (ART accelerator enabled except prefetch) or RAM <sup>(1)</sup>

		Conditions	f <sub>HCLK</sub> (MHz)					
Symbol	Parameter			Тур	T <sub>A</sub> = 25 °C	T <sub>A</sub> = 85 °C	T <sub>A</sub> = 105 °C	Unit
			180	98	104 <sup>(5)</sup>	123	141 <sup>(5)</sup>	
			168	89	98 <sup>(5)</sup>	116	133 <sup>(5)</sup>	
			150	75	84	100	115	
			144	72	81	96	112	
			120	54	58	72	85	
		All	90	43	45	56	66	
		Peripherals	60	29	30	38	45	
		enabled	30	16	20	34	46	
			25	13	16	30	43	
	Supply current in RUN mode	· · · · · · · · · · · · · · · · · · ·	16	11	13	27	39	- - - mΔ
			8	5	9	23	36	
			4	4	8	21	34	
			2	2	7	20	33	
'DD			180	44	47 <sup>(5)</sup>	69	87 <sup>(5)</sup>	
			168	41	45 <sup>(5)</sup>	66	83 <sup>(5)</sup>	
			150	36	39	57	73	
			144	33	37	56	72	
			120	25	29	43	56	
		All	90	20	21	32	41	
		Peripherals	60	14	15	22	28	
		disabled(0)	30	8	8	12	26	
			25	7	7	10	24	
			16	7	9	22	35	
			8	3	7	21	34	
			4	3	6	20	33	
			2	2	6	20	33	

1. Code and data processing running from SRAM1 using boot pins.

2. Guaranteed by characterization.

3. When analog peripheral blocks such as ADCs, DACs, HSE, LSE, HSI, or LSI are ON, an additional power consumption should be considered.

4. When the ADC is ON (ADON bit set in the ADC\_CR2 register), add an additional power consumption of 1.6 mA per ADC for the analog part.

5. Guaranteed by test in production.



				Typ <sup>(1)</sup>			Max <sup>(2)</sup>			
Symbol	Parameter	Conditions	T <sub>A</sub> = 25 °C			T <sub>A</sub> = 25 °C	T <sub>A</sub> = 85 °C	T <sub>A</sub> = 105 °C	Unit	
			V <sub>DD</sub> = 1.7 V	V <sub>DD</sub> = 2.4 V	V <sub>DD</sub> = 3.3 V	V <sub>DD</sub> = 3.6 V				
I <sub>DD_STBY</sub>	Supply current in Standby mode	Backup SRAM ON, low-speed oscillator (LSE) and RTC ON	2.80	3.00	3.60	7.00	19.00	36.00		
		Backup SRAM OFF, low- speed oscillator (LSE) and RTC ON	2.30	2.60	3.10	6.00	16.00	31.00	μA	
		Backup SRAM ON, RTC and LSE OFF	2.30	2.50	2.90	6.00 <sup>(3)</sup>	18.00 <sup>(3)</sup>	35.00 <sup>(3)</sup>		
		Backup SRAM OFF, RTC and LSE OFF	1.70	1.90	2.20	5.00 <sup>(3)</sup>	15.00 <sup>(3)</sup>	30.00 <sup>(3)</sup>		

#### Table 28. Typical and maximum current consumptions in Standby mode

The typical current consumption values are given with PDR OFF (internal reset OFF). When the PDR is OFF (internal reset OFF), the typical current consumption is reduced by additional 1.2 μA.

2. Based on characterization, not tested in production unless otherwise specified.

3. Based on characterization, tested in production.

#### Table 29. Typical and maximum current consumptions in $\ensuremath{\mathsf{V}_{\mathsf{BAT}}}$ mode

				Тур			Max <sup>(2)</sup>		
Symbol	Parameter	r Conditions <sup>(1)</sup>	T <sub>A</sub> = 25 °C			T <sub>A</sub> = 85 °C T <sub>A</sub> = 105 °C		Unit	
			V <sub>BAT</sub> = 1.7 V	V <sub>BAT</sub> = 2.4 V	V <sub>BAT</sub> = 3.3 V	V <sub>BAT</sub> =	= 3.6 V		
I <sub>DD_VBAT</sub> Bacł dom curre		Backup SRAM ON, low-speed oscillator (LSE) and RTC ON	1.28	1.40	1.62	6	11		
	Backup	Backup SRAM OFF, low-speed oscillator (LSE) and RTC ON	0.66	0.76	0.97	3	5		
	current	Backup SRAM ON, RTC and LSE OFF	0.70	0.72	0.74	5	10	μΛ	
		Backup SRAM OFF, RTC and LSE OFF	0.10	0.10	0.10	2	4		

1. Crystal used: Abracon ABS07-120-32.768 kHz-T with a  $C_L$  of 6 pF for typical values.

2. Guaranteed by characterization results.



### 6.3.16 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below  $V_{SS}$  or above  $V_{DD}$  (for standard, 3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

#### Functional susceptibilty to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (>5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of – 5  $\mu$ A/+0  $\mu$ A range), or other functional failure (for example reset, oscillator frequency deviation).

Negative induced leakage current is caused by negative injection and positive induced leakage current by positive injection.

The test results are given in Table 55.

		Functional s		
Symbol	Description	Negative injection	Positive injection	Unit
	Injected current on BOOT0 pin	- 0	NA	
	Injected current on NRST pin	- 0	NA	
I <sub>INJ</sub>	Injected current on PA0, PA1, PA2, PA3, PA6, PA7, PB0, PC0, PC1, PC2, PC3, PC4, PC5, PH1, PH2, PH3, PH4, PH5	- 0	NA	mA
	Injected current on TTa pins: PA4 and PA5	- 0	+5	
	Injected current on any other FT pin	- 5	NA	

### Table 55. I/O current injection susceptibility<sup>(1)</sup>

1. NA = not applicable.

*Note:* It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents.





Figure 51. Typical connection diagram using the ADC

1. Refer to Table 74 for the values of  $\mathsf{R}_{\mathsf{AIN}},\,\mathsf{R}_{\mathsf{ADC}}\,\mathsf{and}\,\mathsf{C}_{\mathsf{ADC}}.$ 

 $C_{parasitic}$  represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 5 pF). A high  $C_{parasitic}$  value downgrades conversion accuracy. To remedy this, f<sub>ADC</sub> should be reduced. 2.





Figure 53. Power supply and reference decoupling (V<sub>REF+</sub> connected to V<sub>DDA</sub>)

1.  $V_{REF+}$  and  $V_{REF-}$  inputs are both available on UFBGA176.  $V_{REF+}$  is also available on LQFP100, LQFP144, and LQFP176. When  $V_{REF+}$  and  $V_{REF-}$  are not available, they are internally connected to  $V_{DDA}$  and  $V_{SSA}$ .

### 6.3.22 Temperature sensor characteristics

Table 80. Temperature sensor characteristics	5	
Parameter	Min	-

Symbol	Parameter		Тур	Max	Unit
T <sub>L</sub> <sup>(1)</sup>	V <sub>SENSE</sub> linearity with temperature	-	±1	±2	°C
Avg_Slope <sup>(1)</sup>	Average slope	-	2.5		mV/°C
V <sub>25</sub> <sup>(1)</sup>	Voltage at 25 °C	-	0.76		V
t <sub>START</sub> <sup>(2)</sup>	Startup time	-	6	10	μs
T <sub>S_temp</sub> <sup>(2)</sup>	ADC sampling time when reading the temperature (1 °C accuracy)	10	-	-	μs

1. Guaranteed by characterization results.

2. Guaranteed by design.

Symbol	Parameter	Memory address
TS_CAL1	TS ADC raw data acquired at temperature of 30 °C, $V_{DDA}$ = 3.3 V	0x1FFF 7A2C - 0x1FFF 7A2D
TS_CAL2	TS ADC raw data acquired at temperature of 110 °C, V <sub>DDA</sub> = 3.3 V	0x1FFF 7A2E - 0x1FFF 7A2F

#### Table 81. Temperature sensor calibration values





Figure 65. PC Card/CompactFlash controller waveforms for attribute memory read access

1. Only data bits 0...7 are read (bits 8...15 are disregarded).



		-		
Symbol	Parameter	Min	Max	Unit
t <sub>w(SDCLK)</sub>	FMC_SDCLK period	2T <sub>HCLK</sub> – 0.5	2T <sub>HCLK</sub> +0.5	
t <sub>d(SDCLKL_Data</sub> )	Data output valid time	-	3.5	
t <sub>h(SDCLKL</sub> _Data)	Data output hold time	0	-	
t <sub>d(SDCLKL_Add)</sub>	Address valid time	-	1.5	
t <sub>d(SDCLKL_SDNWE)</sub>	SDNWE valid time	-	1	
t <sub>h(SDCLKL_SDNWE)</sub>	SDNWE hold time	0	-	
t <sub>d(SDCLKL_SDNE)</sub>	Chip select valid time	-	0.5	
t <sub>h(SDCLKLSDNE)</sub>	Chip select hold time	0	-	115
t <sub>d(SDCLKL_SDNRAS)</sub>	SDNRAS valid time	-	2	
t <sub>h(SDCLKL_SDNRAS)</sub>	SDNRAS hold time	0	-	
t <sub>d(SDCLKL_SDNCAS)</sub>	SDNCAS valid time	SDNCAS valid time - 0		
t <sub>d(SDCLKL_SDNCAS)</sub> SDNCAS hold time		0	-	
t <sub>d(SDCLKL_NBL)</sub>	NBL valid time	-	0.5	
t <sub>h(SDCLKL_NBL)</sub>	NBLoutput time	0	-	1

## Table 104. SDRAM write timings<sup>(1)(2)</sup>

1. CL = 30 pF on data and address lines. CL=15pF on FMC\_SDCLK.

2. Guaranteed by characterization results.

## Table 105. LPSDR SDRAM write timings<sup>(1)(2)</sup>

Symbol Parameter		Min	Мах	Unit
t <sub>w(SDCLK)</sub>	FMC_SDCLK period	2T <sub>HCLK</sub> – 0.5	2T <sub>HCLK</sub> +0.5	
t <sub>d(SDCLKL_Data</sub> )	Data output valid time	-	5	
t <sub>h(SDCLKL</sub> _Data)	Data output hold time	2	-	
t <sub>d(SDCLKL_Add)</sub>	Address valid time	-	2.8	
t <sub>d(SDCLKL-SDNWE)</sub>	SDNWE valid time	-	2	
t <sub>h(SDCLKL-SDNWE)</sub>	SDNWE hold time	1	-	
t <sub>d(SDCLKL-SDNE)</sub>	Chip select valid time	-	1.5	
t <sub>h(SDCLKL</sub> - SDNE)	Chip select hold time	1	-	ns
t <sub>d(SDCLKL-SDNRAS)</sub>	SDNRAS valid time	-	1.5	
t <sub>h(SDCLKL-SDNRAS)</sub>	SDNRAS hold time	1.5	-	
t <sub>d(SDCLKL-SDNCAS)</sub>	SDNCAS valid time	-	1.5	
t <sub>d(SDCLKL-SDNCAS)</sub>	SDNCAS hold time	1.5	-	
t <sub>d(SDCLKL_NBL)</sub>	NBL valid time	-	1.5	
t <sub>h(SDCLKL-NBL)</sub>	NBL output time	1.5	-	

1. CL = 10 pF.

2. Guaranteed by characterization results.



### Device marking for LQFP100

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which depends assembly location, are not indicated below.





 Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.



## 7.4 LQFP176 package information

Figure 89. LQFP176 - 176-pin, 24 x 24 mm low-profile quad flat package outline



1. Drawing is not to scale.

# Table 114. LQFP176 - 176-pin, 24 x 24 mm low-profile quad flat packagemechanical data

Symbol	millimeters			inches <sup>(1)</sup>			
Symbol	Min	Тур	Мах	Min	Тур	Мах	
А	-	-	1.600	-	-	0.0630	
A1	0.050	-	0.150	0.0020	-	0.0059	
A2	1.350	-	1.450	0.0531	-	0.0571	
b	0.170	-	0.270	0.0067	-	0.0106	
С	0.090	-	0.200	0.0035	-	0.0079	
D	23.900	-	24.100	0.9409	-	0.9488	
HD	25.900	-	26.100	1.0197	-	1.0276	



# Table 120. TFBGA216 - 216 ball 13 × 13 mm 0.8 mm pitch thin fine pitch ball grid array package mechanical data (continued)

Symbol	millimeters			inches <sup>(1)</sup>			
	Min	Тур	Мах	Min	Тур	Мах	
eee	-	-	0.150	-	-	0.0059	
fff	-	-	0.080	-	-	0.0031	

1. Values in inches are converted from mm and rounded to 4 decimal digits.

#### **Device marking for TFBGA176**

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

Other optional marking or inset/upset marks, which depends assembly location, are not indicated below.



#### Figure 102. TFBGA176 marking example (package top view)

 Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.



#### STM32F427xx STM32F429xx

Date	Revision	Changes
24-Jan-2014	3	Added STM32F429xE part numbers featuring 512 Mbytes of Flash memory and UFBGA169 package. Added LPSDR SDRAM. Changed INTN into INTR in <i>Figure 4: STM32F427xx and</i> <i>STM32F429xx block diagram</i> . Added note 4 in <i>Table 2: STM32F427xx and STM32F429xx features</i> <i>and peripheral counts</i> . Updated Section 3.15: Boot modes. Updated for PA4 and PA5 in <i>Table 10: STM32F427xx and</i> <i>STM32F429xx pin and ball definitions</i> . Added V <sub>IN</sub> for BOOT0 pins in <i>Table 14: Voltage characteristics</i> . Updated Note 6, added Note 1, and updated maximum V <sub>IN</sub> for B pins in <i>Table 17: General operating conditions</i> . Updated maximum Flash memory access frequency with wait states for V <sub>DD</sub> =1.8 to 2.1 V in <i>Table 18: Limitations depending on the</i> <i>operating power supply range</i> . Updated Table 24: Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (ART accelerator enabled except prefetch) or RAM and Table 25: Typical and maximum current consumption in Run mode, code with data processing running from Flash memory or RAM, regulator ON (ART accelerator enabled except prefetch), VDD=1.7 V, Table 31: Typical current consumption in Run mode, code with data processing running from Flash memory or RAM, regulator ON (ART accelerator enabled except prefetch), vDD=1.7 V, Table 31: Typical current consumption in Run mode, code with data processing running from Flash memory, regulator OFF (ART accelerator enabled except prefetch), and Table 32: Typical current consumption in Sleep mode, regulator ON, VDD=1.7 V. Updated Table 58: I/O AC characteristics. Added Figure 35. Updated Table 58: I/O AC characteristics. USB ULPI. Updated Table 57: Output voltage characteristics. Updated Table 57: Output voltage characteristics. Updated Table 57: Dynamic characteristics conditions. Updated Figure 73: SDRAM read access waveforms (CL = 1) and Figure 74: SDRAM write access waveforms. Added Table 103: LPSDR SDRAM read timings and Table 106: DPSDR SDRAM write timings and added note 2. Table 108: Dynamic characteristics: SD /

	Table 124.	Document	revision	historv
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