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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

#### Applications of "[Embedded - Microcontrollers](#)"

##### Details

Product Status	Obsolete
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, LINbus, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	114
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	143-UFBGA, WLCSP
Supplier Device Package	143-WLCSP (4.52x5.55)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f429ziy6jtr">https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f429ziy6jtr</a>

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3.22	Timers and watchdogs . . . . .	33
3.22.1	Advanced-control timers (TIM1, TIM8) . . . . .	35
3.22.2	General-purpose timers (TIMx) . . . . .	35
3.22.3	Basic timers TIM6 and TIM7 . . . . .	35
3.22.4	Independent watchdog . . . . .	36
3.22.5	Window watchdog . . . . .	36
3.22.6	SysTick timer . . . . .	36
3.23	Inter-integrated circuit interface (I <sup>2</sup> C) . . . . .	36
3.24	Universal synchronous/asynchronous receiver transmitters (USART) . . . . .	36
3.25	Serial peripheral interface (SPI) . . . . .	37
3.26	Inter-integrated sound (I <sup>2</sup> S) . . . . .	38
3.27	Serial Audio interface (SAI1) . . . . .	38
3.28	Audio PLL (PLLI2S) . . . . .	38
3.29	Audio and LCD PLL(PLLSAI) . . . . .	38
3.30	Secure digital input/output interface (SDIO) . . . . .	39
3.31	Ethernet MAC interface with dedicated DMA and IEEE 1588 support . . . . .	39
3.32	Controller area network (bxCAN) . . . . .	39
3.33	Universal serial bus on-the-go full-speed (OTG_FS) . . . . .	40
3.34	Universal serial bus on-the-go high-speed (OTG_HS) . . . . .	40
3.35	Digital camera interface (DCMI) . . . . .	41
3.36	Random number generator (RNG) . . . . .	41
3.37	General-purpose input/outputs (GPIOs) . . . . .	41
3.38	Analog-to-digital converters (ADCs) . . . . .	41
3.39	Temperature sensor . . . . .	42
3.40	Digital-to-analog converter (DAC) . . . . .	42
3.41	Serial wire JTAG debug port (SWJ-DP) . . . . .	42
3.42	Embedded Trace Macrocell™ . . . . .	43
4	<b>Pinouts and pin description . . . . .</b>	<b>44</b>
5	<b>Memory mapping . . . . .</b>	<b>85</b>
6	<b>Electrical characteristics . . . . .</b>	<b>90</b>
6.1	Parameter conditions . . . . .	90
6.1.1	Minimum and maximum values . . . . .	90

6.1.2	Typical values .....	90
6.1.3	Typical curves .....	90
6.1.4	Loading capacitor .....	90
6.1.5	Pin input voltage .....	90
6.1.6	Power supply scheme .....	91
6.1.7	Current consumption measurement .....	92
6.2	Absolute maximum ratings .....	92
6.3	Operating conditions .....	94
6.3.1	General operating conditions .....	94
6.3.2	VCAP1/VCAP2 external capacitor .....	96
6.3.3	Operating conditions at power-up / power-down (regulator ON) .....	97
6.3.4	Operating conditions at power-up / power-down (regulator OFF) .....	97
6.3.5	Reset and power control block characteristics .....	98
6.3.6	Over-drive switching characteristics .....	99
6.3.7	Supply current characteristics .....	100
6.3.8	Wakeup time from low-power modes .....	116
6.3.9	External clock source characteristics .....	117
6.3.10	Internal clock source characteristics .....	121
6.3.11	PLL characteristics .....	123
6.3.12	PLL spread spectrum clock generation (SSCG) characteristics .....	126
6.3.13	Memory characteristics .....	128
6.3.14	EMC characteristics .....	130
6.3.15	Absolute maximum ratings (electrical sensitivity) .....	132
6.3.16	I/O current injection characteristics .....	133
6.3.17	I/O port characteristics .....	134
6.3.18	NRST pin characteristics .....	140
6.3.19	TIM timer characteristics .....	141
6.3.20	Communications interfaces .....	141
6.3.21	12-bit ADC characteristics .....	156
6.3.22	Temperature sensor characteristics .....	162
6.3.23	V <sub>BAT</sub> monitoring characteristics .....	163
6.3.24	Reference voltage .....	163
6.3.25	DAC electrical characteristics .....	164
6.3.26	FMC characteristics .....	167
6.3.27	Camera interface (DCMI) timing specifications .....	192
6.3.28	LCD-TFT controller (LTDC) characteristics .....	192
6.3.29	SD/SDIO MMC card host interface (SDIO) characteristics .....	195

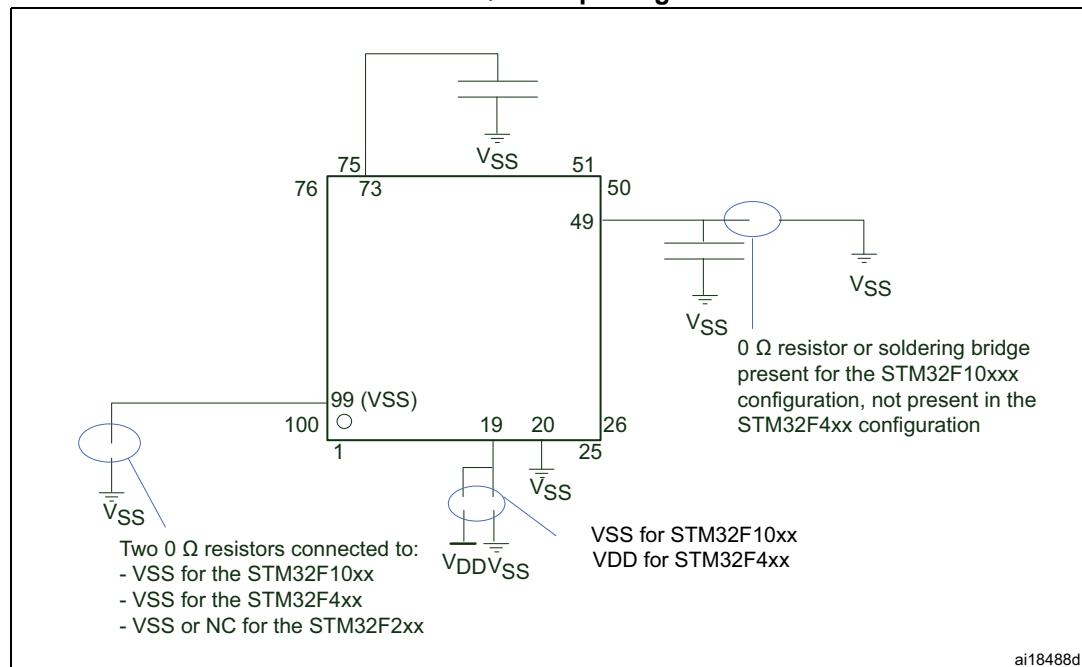
## 2.1 Full compatibility throughout the family

The STM32F427xx and STM32F429xx devices are part of the STM32F4 family. They are fully pin-to-pin, software and feature compatible with the STM32F2xx devices, allowing the user to try different memory densities, peripherals, and performances (FPU, higher frequency) for a greater degree of freedom during the development cycle.

The STM32F427xx and STM32F429xx devices maintain a close compatibility with the whole STM32F10xx family. All functional pins are pin-to-pin compatible. The STM32F427xx and STM32F429xx, however, are not drop-in replacements for the STM32F10xx devices: the two families do not have the same power scheme, and so their power pins are different. Nonetheless, transition from the STM32F10xx to the STM32F42x family remains simple as only a few pins are impacted.

*Figure 1*, *Figure 2*, and *Figure 3*, give compatible board designs between the STM32F4xx, STM32F2xx, and STM32F10xx families.

**Figure 1. Compatible board design STM32F10xx/STM32F2xx/STM32F4xx for LQFP100 package**



Additional 32-bit registers contain the programmable alarm subseconds, seconds, minutes, hours, day, and date.

Like backup SRAM, the RTC and backup registers are supplied through a switch that is powered either from the V<sub>DD</sub> supply when present or from the V<sub>BAT</sub> pin.

## 3.20 Low-power modes

The devices support three low-power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

- **Sleep mode**

In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

- **Stop mode**

The Stop mode achieves the lowest power consumption while retaining the contents of SRAM and registers. All clocks in the 1.2 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled.

The voltage regulator can be put either in main regulator mode (MR) or in low-power mode (LPR). Both modes can be configured as follows (see [Table 5: Voltage regulator modes in stop mode](#)):

- Normal mode (default mode when MR or LPR is enabled)
- Under-drive mode.

The device can be woken up from the Stop mode by any of the EXTI line (the EXTI line source can be one of the 16 external lines, the PVD output, the RTC alarm / wakeup / tamper / time stamp events, the USB OTG FS/HS wakeup or the Ethernet wakeup).

**Table 5. Voltage regulator modes in stop mode**

Voltage regulator configuration	Main regulator (MR)	Low-power regulator (LPR)
Normal mode	MR ON	LPR ON
Under-drive mode	MR in under-drive mode	LPR in under-drive mode

- **Standby mode**

The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.2 V domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering Standby mode, the SRAM and register contents are lost except for registers in the backup domain and the backup SRAM when selected.

The device exits the Standby mode when an external reset (NRST pin), an IWDG reset, a rising edge on the WKUP pin, or an RTC alarm / wakeup / tamper /time stamp event occurs.

The standby mode is not supported when the embedded voltage regulator is bypassed and the 1.2 V domain is controlled by an external power.

MS30422V2

Figure 15. STM32F42x LQFP208 pinout

PE2	53	1	208	P17
PE3	54	2	207	P16
PE4	54	3	206	P15
PE5	55	4	205	P14
PE6	55	5	204	VDD
VBAT	56		203	PDR_ON
PI8	57		202	VSS
PC13	58		201	PE1
PC14	59		200	PE0
PC15	60	10	199	PB8
PI9	61	11	198	PB8
PI10	62	12	197	BOOT0
PI11	63	13	196	PB7
VSS	64	14	195	PB6
VDD	65	15	194	PB5
PF0	66	16	193	PB4
PF1	67	17	192	PB3
PF2	68	18	191	PB15
PI12	69	19	190	PK7
PI13	70	20	189	PK6
PI14	71	21	188	PK5
PF3	72	22	187	PK4
PF4	73	23	186	PK3
PF5	74	24	185	VDD
VSS	75	25	184	VSS
VDD	76	26	183	PG14
PF6	77	27	182	PG13
PF7	78	28	181	PG12
PF8	79	29	180	PG11
PF9	80	30	179	PG10
PF10	81	31	178	PG9
PH0	82	32	177	PJ15
PH1	83	33	176	PJ14
NRST	84	34	175	PJ13
PC0	85		174	PJ12
PC1	86		173	PD7
PC2	87		172	PD6
PC3	88		171	VDD
VDD	89	39	170	VSS
VSSA	90	40	169	PD5
VREF+	91	41	168	PD4
VDDA	92	42	167	PD3
PA0	93	43	166	PD2
PA1	94	44	165	PD1
PA2	95	45	164	PDO
PH2	96	46	163	PC12
PH3	97	47	162	PC11
PH4	98	48	161	PC10
PH5	99	49	160	PA15
PA3	100	50	159	PA14
VSS	101	51	158	VDD
VDD	102	52	157	P13

- The above figure shows the package top view.

Table 10. STM32F427xx and STM32F429xx pin and ball definitions (continued)

Pin number								Pin name (function after reset) <sup>(1)</sup>	Pin type	I / O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA169	UFBGA176	LQFP176	WL CSP143	LQFP208	TFBGA216						
-	-	C11	D14	132	-	155	D14	PI1	I/O	FT	-	SPI2_SCK/I2S2_CK <sup>(7)</sup> , FMC_D25, DCMI_D8, LCD_G6, EVENTOUT	-
-	-	B12	C14	133	-	156	C14	PI2	I/O	FT	-	TIM8_CH4, SPI2_MISO, I2S2ext_SD, FMC_D26, DCMI_D9, LCD_G7, EVENTOUT	-
-	-	A12	C13	134	-	157	C13	PI3	I/O	FT	-	TIM8_ETR, SPI2_MOSI/I2S2_SD, FMC_D27, DCMI_D10, EVENTOUT	-
-	-	D11	D9	135	F5	-	F9	V <sub>SS</sub>	S		-	-	-
-	-	D3	C9	136	A1	158	E10	V <sub>DD</sub>	S		-	-	-
76	109	A11	A14	137	B1	159	A14	PA14 (JTCK-SWCLK)	I/O	FT	-	JTCK-SWCLK/ EVENTOUT	-
77	110	B11	A13	138	C2	160	A13	PA15 (JTDI)	I/O	FT	-	JTDI, TIM2_CH1/TIM2_ETR, SPI1_NSS, SPI3_NSS/I2S3_WS, EVENTOUT	-
78	111	C10	B14	139	A2	161	B14	PC10	I/O	FT	-	SPI3_SCK/I2S3_CK, USART3_TX, UART4_TX, SDIO_D2, DCMI_D8, LCD_R2, EVENTOUT	-
79	112	B10	B13	140	B2	162	B13	PC11	I/O	FT	-	I2S3ext_SD, SPI3_MISO, USART3_RX, UART4_RX, SDIO_D3, DCMI_D4, EVENTOUT	-
80	113	A10	A12	141	C3	163	A12	PC12	I/O	FT	-	SPI3_MOSI/I2S3_SD, USART3_CK, UART5_TX, SDIO_CK, DCMI_D9, EVENTOUT	-
81	114	D9	B12	142	B3	164	B12	PD0	I/O	FT	-	CAN1_RX, FMC_D2, EVENTOUT	-

Table 10. STM32F427xx and STM32F429xx pin and ball definitions (continued)

Pin number									Pin name (function after reset) <sup>(1)</sup>	Pin type	I / O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA169	UFBGA176	LQFP176	WL CSP143	LQFP208	TFBGA216							
89	133	B6	A10	161	B7	192	A10	PB3 (JTDO/TRACE SWO)	I/O	FT	-	JTDO/TRACESWO, TIM2_CH2, SPI1_SCK, SPI3_SCK/I2S3_CK, EVENTOUT	-	
90	134	A6	A9	162	C7	193	A9	PB4 (NJTRST)	I/O	FT	-	NJTRST, TIM3_CH1, SPI1_MISO, SPI3_MISO, I2S3ext_SD, EVENTOUT	-	
91	135	D5	A6	163	C8	194	A8	PB5	I/O	FT	-	TIM3_CH2, I2C1_SMBA, SPI1_MOSI, SPI3_MOSI/I2S3_SD, CAN2_RX, OTG_HS_ULPI_D7, ETH_PPS_OUT, FMC_SDCKE1, DCMI_D10, EVENTOUT	-	
92	136	C5	B6	164	A8	195	B6	PB6	I/O	FT	-	TIM4_CH1, I2C1_SCL, USART1_TX, CAN2_TX, FMC_SDNE1, DCMI_D5, EVENTOUT	-	
93	137	B5	B5	165	B8	196	B5	PB7	I/O	FT	-	TIM4_CH2, I2C1_SDA, USART1_RX, FMC_NL, DCMI_VSYNC, EVENTOUT	-	
94	138	A5	D6	166	C9	197	E6	BOOT0	I	B	-		V <sub>PP</sub>	
95	139	D4	A5	167	A9	198	A7	PB8	I/O	FT	-	TIM4_CH3, TIM10_CH1, I2C1_SCL, CAN1_RX, ETH_MII_TXD3, SDIO_D4, DCMI_D6, LCD_B6, EVENTOUT	-	

**Table 13. STM32F427xx and STM32F429xx register boundary addresses**

Bus	Boundary address	Peripheral
	0xE00F FFFF - 0xFFFF FFFF	Reserved
Cortex-M4	0xE000 0000 - 0xE00F FFFF	Cortex-M4 internal peripherals
AHB3	0xD000 0000 - 0xDFFF FFFF	FMC bank 6
	0xC000 0000 - 0xCFFF FFFF	FMC bank 5
	0xA000 1000 - 0xBFFF FFFF	Reserved
	0xA000 0000- 0xA000 0FFF	FMC control register
	0x9000 0000 - 0x9FFF FFFF	FMC bank 4
	0x8000 0000 - 0x8FFF FFFF	FMC bank 3
	0x7000 0000 - 0x7FFF FFFF	FMC bank 2
	0x6000 0000 - 0x6FFF FFFF	FMC bank 1
	0x5006 0C00- 0x5FFF FFFF	Reserved
AHB2	0x5006 0800 - 0X5006 0BFF	RNG
	0x5005 0400 - X5006 07FF	Reserved
	0x5005 0000 - 0X5005 03FF	DCMI
	0x5004 0000- 0x5004 FFFF	Reserved
	0x5000 0000 - 0X5003 FFFF	USB OTG FS

**Table 13. STM32F427xx and STM32F429xx register boundary addresses (continued)**

Bus	Boundary address	Peripheral
	0x4000 8000- 0x4000 FFFF	Reserved
APB1	0x4000 7C00 - 0x4000 7FFF	UART8
	0x4000 7800 - 0x4000 7BFF	UART7
	0x4000 7400 - 0x4000 77FF	DAC
	0x4000 7000 - 0x4000 73FF	PWR
	0x4000 6C00 - 0x4000 6FFF	Reserved
	0x4000 6800 - 0x4000 6BFF	CAN2
	0x4000 6400 - 0x4000 67FF	CAN1
	0x4000 6000 - 0x4000 63FF	Reserved
	0x4000 5C00 - 0x4000 5FFF	I2C3
	0x4000 5800 - 0x4000 5BFF	I2C2
	0x4000 5400 - 0x4000 57FF	I2C1
	0x4000 5000 - 0x4000 53FF	UART5
	0x4000 4C00 - 0x4000 4FFF	UART4
	0x4000 4800 - 0x4000 4BFF	USART3
	0x4000 4400 - 0x4000 47FF	USART2
	0x4000 4000 - 0x4000 43FF	I2S3ext
	0x4000 3C00 - 0x4000 3FFF	SPI3 / I2S3
	0x4000 3800 - 0x4000 3BFF	SPI2 / I2S2
	0x4000 3400 - 0x4000 37FF	I2S2ext
	0x4000 3000 - 0x4000 33FF	IWDG
	0x4000 2C00 - 0x4000 2FFF	WWDG
	0x4000 2800 - 0x4000 2BFF	RTC & BKP Registers
	0x4000 2400 - 0x4000 27FF	Reserved
	0x4000 2000 - 0x4000 23FF	TIM14
	0x4000 1C00 - 0x4000 1FFF	TIM13
	0x4000 1800 - 0x4000 1BFF	TIM12
	0x4000 1400 - 0x4000 17FF	TIM7
	0x4000 1000 - 0x4000 13FF	TIM6
	0x4000 0C00 - 0x4000 0FFF	TIM5
	0x4000 0800 - 0x4000 0BFF	TIM4
	0x4000 0400 - 0x4000 07FF	TIM3
	0x4000 0000 - 0x4000 03FF	TIM2

Table 26. Typical and maximum current consumption in Sleep mode

Symbol	Parameter	Conditions	$f_{HCLK}$ (MHz)	Typ	Max <sup>(1)</sup>			Unit
					$T_A = 25^\circ\text{C}$	$T_A = 85^\circ\text{C}$	$T_A = 105^\circ\text{C}$	
$I_{DD}$	Supply current in Sleep mode	All Peripherals enabled <sup>(2)</sup>	180	78	89 <sup>(3)</sup>	110	130 <sup>(3)</sup>	mA
			168	66	75 <sup>(3)</sup>	93	110 <sup>(3)</sup>	
			150	56	61	80	96	
			144	54	58	78	94	
			120	40	44	59	72	
			90	32	34	46	56	
			60	22	23	31	38	
			30	10	16	30	43	
			25	9	14	28	40	
			16	5	12	25	40	
			8	3	8	22	35	
			4	3	7	21	34	
		All Peripherals disabled	2	2	6.5	20	33	
			180	21	26 <sup>(3)</sup>	54	76 <sup>(3)</sup>	
			168	16	20 <sup>(3)</sup>	41	58 <sup>(3)</sup>	
			150	14	17	36	52	
			144	13	16.5	35	51	
			120	10	14	28	41	
			90	8	13	26	37	
			60	6	9	17	25	
			30	5	8	22	35	
			25	3	7	21	34	

1. Guaranteed by characterization unless otherwise specified.
2. When analog peripheral blocks such as ADCs, DACs, HSE, LSE, HSI, or LSI are ON, an additional power consumption should be considered.
3. Based on characterization, tested in production.

Table 27. Typical and maximum current consumptions in Stop mode

Symbol	Parameter	Conditions	Typ	Max <sup>(1)</sup>			Unit
				$V_{DD} = 3.6 \text{ V}$			
			$T_A = 25^\circ\text{C}$	$T_A = 25^\circ\text{C}$	$T_A = 85^\circ\text{C}$	$T_A = 105^\circ\text{C}$	
$I_{DD\_STOP\_NM}$ (normal mode)	Supply current in Stop mode with voltage regulator in main regulator mode	Flash memory in Stop mode, all oscillators OFF, no independent watchdog	0.40	1.50	14.00	25.00	mA
		Flash memory in Deep power down mode, all oscillators OFF, no independent watchdog	0.35	1.50	14.00	25.00	
	Supply current in Stop mode with voltage regulator in Low Power regulator mode	Flash memory in Stop mode, all oscillators OFF, no independent watchdog	0.29	1.10	10.00	18.00	
		Flash memory in Deep power down mode, all oscillators OFF, no independent watchdog	0.23	1.10	10.00	18.00	
$I_{DD\_STOP\_UDM}$ (under-drive mode)	Supply current in Stop mode with voltage regulator in main regulator and under-drive mode	Flash memory in Deep power down mode, main regulator in under-drive mode, all oscillators OFF, no independent watchdog	0.19	0.50	6.00	9.00	
	Supply current in Stop mode with voltage regulator in Low Power regulator and under-drive mode	Flash memory in Deep power down mode, Low Power regulator in under-drive mode, all oscillators OFF, no independent watchdog	0.10	0.40	4.00	7.00	

1. Data based on characterization, tested in production.

Table 35. Peripheral current consumption (continued)

Peripheral	I <sub>DD</sub> ( Typ) <sup>(1)</sup>			Unit
	Scale 1	Scale 2	Scale 3	
APB2 (up to 90 MHz)	SDIO	8.11	8.75	7.83
	TIM1	17.11	15.97	14.17
	TIM8	17.33	16.11	14.33
	TIM9	7.22	6.67	6.00
	TIM10	4.56	4.31	3.83
	TIM11	4.78	4.44	4.00
	ADC1 <sup>(5)</sup>	4.67	4.31	3.83
	ADC2 <sup>(5)</sup>	4.78	4.44	4.00
	ADC3 <sup>(5)</sup>	4.56	4.17	3.67
	SPI1	1.44	1.39	1.17
	USART1	4.00	3.75	3.33
	USART6	4.00	3.75	3.33
	SPI4	1.44	1.39	1.17
	SPI5	1.44	1.39	1.17
	SPI6	1.44	1.39	1.17
	SYSCFG	0.78	0.69	0.67
	LCD_TFT	39.89	37.22	33.17
	SAI1	3.78	3.47	3.17

- When the I/O compensation cell is ON, I<sub>DD</sub> typical value increases by 0.22 mA.
- The BusMatrix is automatically active when at least one master is ON.
- To enable an I2S peripheral, first set the I2SMOD bit and then the I2SE bit in the SPI\_I2SCFGR register.
- When the DAC is ON and EN1/2 bits are set in DAC\_CR register, add an additional power consumption of 0.8 mA per DAC channel for the analog part.
- When the ADC is ON (ADON bit set in the ADC\_CR2 register), add an additional power consumption of 1.6 mA per ADC for the analog part.

### Low-speed external user clock generated from an external source

In bypass mode the LSE oscillator is switched off and the input pin is a standard I/O. The external clock signal has to respect the [Table 56: I/O static characteristics](#). However, the recommended clock input waveform is shown in [Figure 28](#).

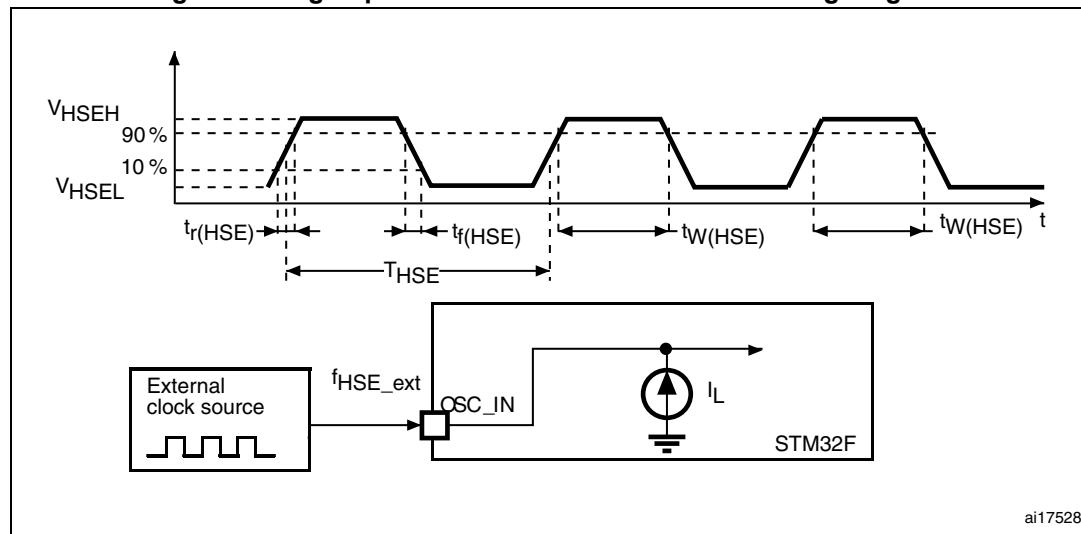
The characteristics given in [Table 38](#) result from tests performed using a low-speed external clock source, and under ambient temperature and supply voltage conditions summarized in [Table 17](#).

**Table 38. Low-speed external user clock characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{LSE\_ext}$	User External clock source frequency <sup>(1)</sup>		-	32.768	1000	kHz
$V_{LSEH}$	OSC32_IN input pin high level voltage		0.7 $V_{DD}$	-	$V_{DD}$	V
$V_{LSEL}$	OSC32_IN input pin low level voltage		$V_{SS}$	-	0.3 $V_{DD}$	
$t_w(LSE)$ $t_f(LSE)$	OSC32_IN high or low time <sup>(1)</sup>		450	-	-	ns
$t_r(LSE)$ $t_f(LSE)$	OSC32_IN rise or fall time <sup>(1)</sup>		-	-	50	
$C_{in}(LSE)$	OSC32_IN input capacitance <sup>(1)</sup>		-	5	-	pF
$DuCy_{(LSE)}$	Duty cycle		30	-	70	%
$I_L$	OSC32_IN Input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	$\pm 1$	$\mu A$

1. Guaranteed by design.

**Figure 27. High-speed external clock source AC timing diagram**



ai17528

**Table 44. PLLI2S (audio PLL) characteristics (continued)**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{DD(PLLI2S)}^{(4)}$	PLLI2S power consumption on $V_{DD}$	VCO freq = 100 MHz VCO freq = 432 MHz	0.15 0.45	-	0.40 0.75	mA
$I_{DDA(PLLI2S)}^{(4)}$	PLLI2S power consumption on $V_{DDA}$	VCO freq = 100 MHz VCO freq = 432 MHz	0.30 0.55	-	0.40 0.85	mA

1. Take care of using the appropriate division factor M to have the specified PLL input clock values.
2. Guaranteed by design.
3. Value given with main PLL running.
4. Guaranteed by characterization results.

**Table 45. PLLISAI (audio and LCD-TFT PLL) characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{PLLSAI\_IN}$	PLLSAI input clock <sup>(1)</sup>		0.95 <sup>(2)</sup>	1	2.10	MHz
$f_{PLLSAI\_OUT}$	PLLSAI multiplier output clock		-	-	216	MHz
$f_{VCO\_OUT}$	PLLSAI VCO output		100	-	432	MHz
$t_{LOCK}$	PLLSAI lock time	VCO freq = 100 MHz	75	-	200	$\mu s$
		VCO freq = 432 MHz	100	-	300	
Jitter <sup>(3)</sup>	Main SAI clock jitter	Cycle to cycle at 12.288 MHz on 48KHz period, N=432, R=5	RMS  peak to peak	-  -	90  $\pm 280$	-  ps
		Average frequency of 12.288 MHz N = 432, R = 5 on 1000 samples		-	90	- ps
		FS clock jitter	Cycle to cycle at 48 KHz on 1000 samples	-	400	- ps
$I_{DD(PLLSAI)}^{(4)}$	PLLSAI power consumption on $V_{DD}$	VCO freq = 100 MHz VCO freq = 432 MHz	0.15 0.45	-	0.40 0.75	mA
$I_{DDA(PLLSAI)}^{(4)}$	PLLSAI power consumption on $V_{DDA}$	VCO freq = 100 MHz VCO freq = 432 MHz	0.30 0.55	-	0.40 0.85	mA

1. Take care of using the appropriate division factor M to have the specified PLL input clock values.
2. Guaranteed by design.
3. Value given with main PLL running.
4. Guaranteed by characterization results.

**Table 50. Flash memory endurance and data retention**

Symbol	Parameter	Conditions	Value	Unit
			Min <sup>(1)</sup>	
N <sub>END</sub>	Endurance	T <sub>A</sub> = -40 to +85 °C (6 suffix versions) T <sub>A</sub> = -40 to +105 °C (7 suffix versions)	10	kcycles
t <sub>RET</sub>	Data retention	1 kcycle <sup>(2)</sup> at T <sub>A</sub> = 85 °C	30	Years
		1 kcycle <sup>(2)</sup> at T <sub>A</sub> = 105 °C	10	
		10 kcycles <sup>(2)</sup> at T <sub>A</sub> = 55 °C	20	

1. Guaranteed by characterization results.
2. Cycling performed over the whole temperature range.

### 6.3.14 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

#### Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports), the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A burst of fast transient voltage (positive and negative) is applied to V<sub>DD</sub> and V<sub>SS</sub> through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in [Table 51](#). They are based on the EMS levels and classes defined in application note AN1709.

**Table 51. EMS characteristics**

Symbol	Parameter	Conditions	Level/ Class
V <sub>FESD</sub>	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V <sub>DD</sub> = 3.3 V, LQFP176, T <sub>A</sub> = +25 °C, f <sub>HCLK</sub> = 168 MHz, conforms to IEC 61000-4-2	2B
V <sub>EFTB</sub>	Fast transient voltage burst limits to be applied through 100 pF on V <sub>DD</sub> and V <sub>SS</sub> pins to induce a functional disturbance	V <sub>DD</sub> = 3.3 V, LQFP176, T <sub>A</sub> = +25 °C, f <sub>HCLK</sub> = 168 MHz, conforms to IEC 61000-4-2	4A

When the application is exposed to a noisy environment, it is recommended to avoid pin exposition to disturbances. The pins showing a middle range robustness are: PA0, PA1, PA2, PH2, PH3, PH4, PH5, PA3, PA4, PA5, PA6, PA7, PC4, and PC5.

As a consequence, it is recommended to add a serial resistor (1 kΩ) located as close as possible to the MCU to the pins exposed to noise (connected to tracks longer than 50 mm on PCB).

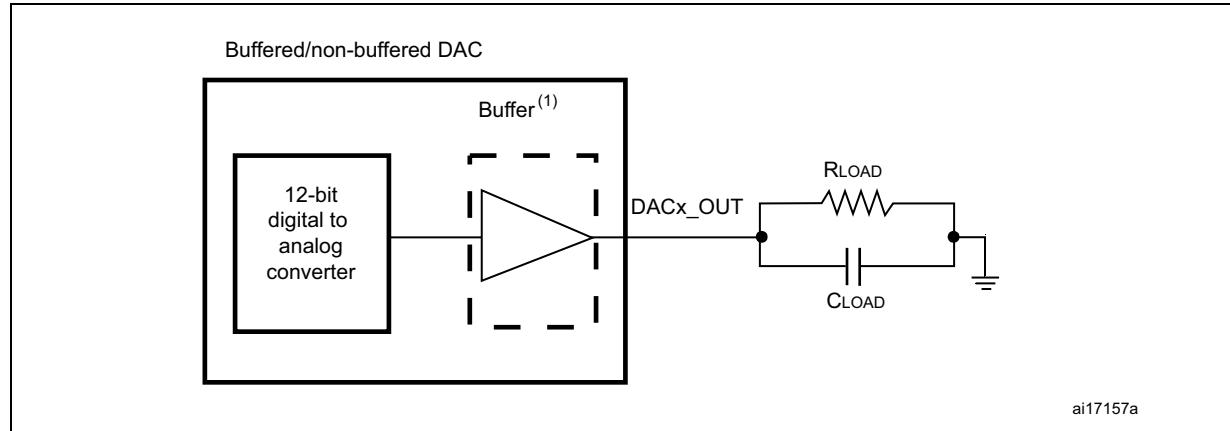
Table 85. DAC characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Comments
$t_{WAKEUP_4}$	Wakeup time from off state (Setting the ENx bit in the DAC Control register)	-	-	6.5	10	μs	$C_{LOAD} \leq 50 \text{ pF}$ , $R_{LOAD} \geq 5 \text{ k}\Omega$ input code between lowest and highest possible ones.
PSRR <sup>(2)</sup>	Power supply rejection ratio (to $V_{DDA}$ ) (static DC measurement)	-	-	-67	-40	dB	No $R_{LOAD}$ , $C_{LOAD} = 50 \text{ pF}$

1.  $V_{DDA}$  minimum value of 1.7 V is obtained with the use of an external power supply supervisor (refer to [Section 3.17.2: Internal reset OFF](#)).

2. Guaranteed by design.
3. The quiescent mode corresponds to a state where the DAC maintains a stable output level to ensure that no dynamic consumption occurs.
4. Guaranteed by characterization.

Figure 54. 12-bit buffered /non-buffered DAC



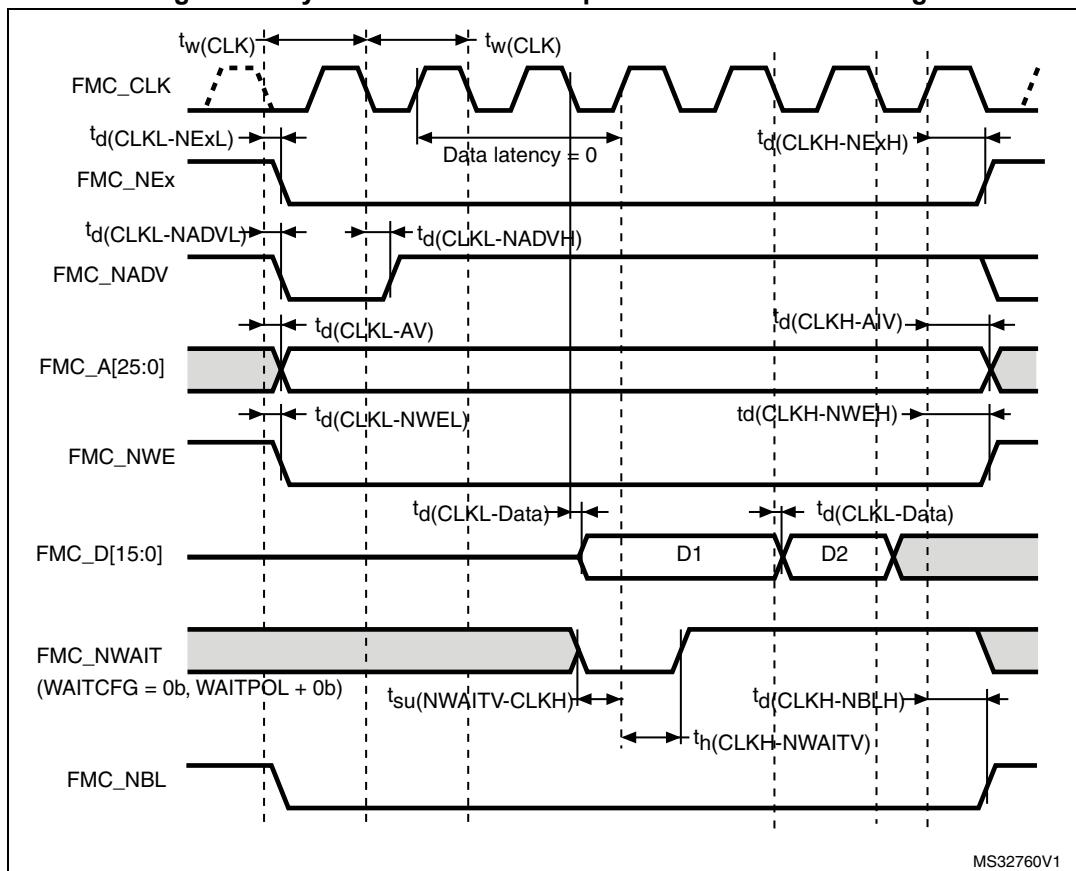
1. The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC\_CR register.

**Table 96. Synchronous non-multiplexed NOR/PSRAM read timings<sup>(1)(2)</sup> (continued)**

Symbol	Parameter	Min	Max	Unit
$t_h(CLKH-DV)$	FMC_D[15:0] valid data after FMC_CLK high	0	-	ns
$t_{(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	4		
$t_h(CLKH-NWAIT)$	FMC_NWAIT valid after FMC_CLK high	0		

1.  $C_L = 30 \text{ pF}$ .

2. Guaranteed by characterization results.

**Figure 62. Synchronous non-multiplexed PSRAM write timings****Table 97. Synchronous non-multiplexed PSRAM write timings<sup>(1)(2)</sup>**

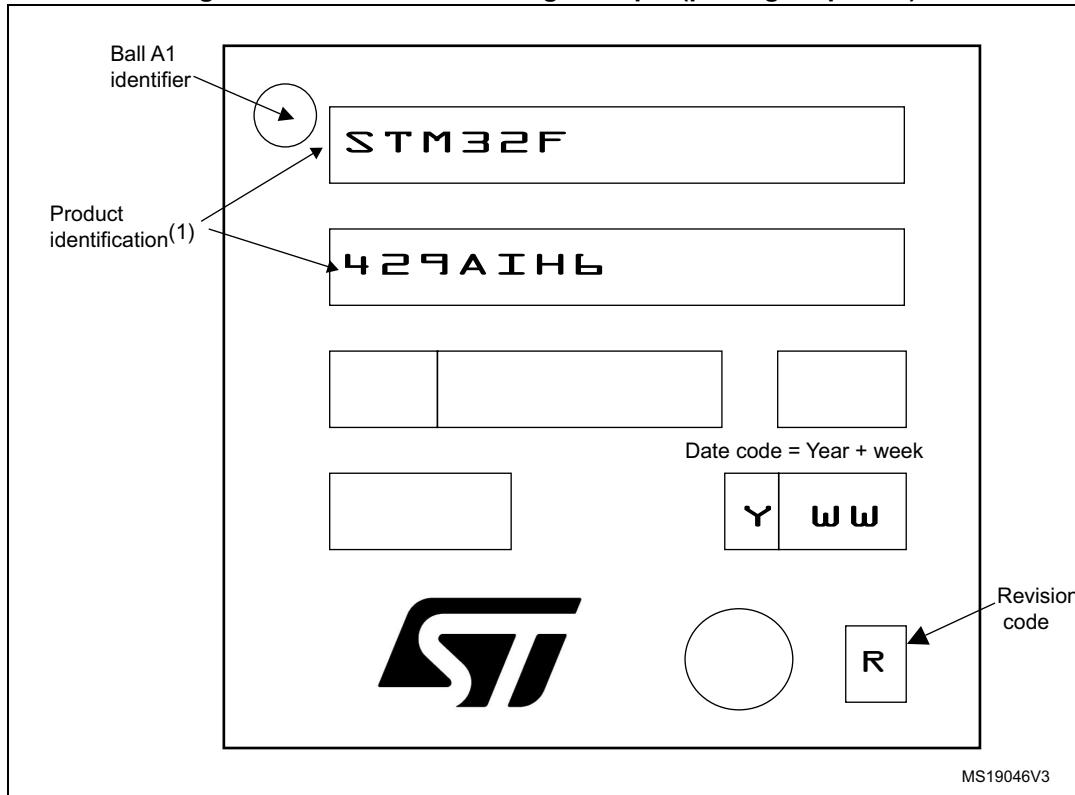
Symbol	Parameter	Min	Max	Unit
$t_{(CLK)}$	FMC_CLK period	$2T_{HCLK} - 1$	-	ns
$t_d(CLKL-NExL)$	FMC_CLK low to FMC_NEx low (x=0..2)	-	0.5	ns
$t_{(CLKH-NExH)}$	FMC_CLK high to FMC_NEx high (x= 0..2)	$T_{HCLK}$	-	ns
$t_d(CLKL-NADV)$	FMC_CLK low to FMC_NADV low	-	0	ns
$t_d(CLKL-NADVH)$	FMC_CLK low to FMC_NADV high	0	-	ns
$t_d(CLKL-AV)$	FMC_CLK low to FMC_Ax valid (x=16...25)	-	0	ns

### Device marking for UFBGA169

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

Other optional marking or inset/upset marks, which depends assembly location, are not indicated below.

Figure 97. UFBGA169 marking example (package top view)



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

**Table 124. Document revision history**

Date	Revision	Changes
21-Jan-2016	8	<p>Updated <a href="#">Figure 22: Power supply scheme</a>.            Added <math>t_{d(TXD)}</math> values corresponding to <math>1.71 \text{ V} &lt; V_{DD} &lt; 3.6 \text{ V}</math> in <a href="#">Table 72: Dynamics characteristics: Ethernet MAC signals for RMII</a>.</p>
18-Jul-2016	9	<p>Updated <a href="#">Figure 1: Compatible board design</a>  <a href="#">STM32F10xx/STM32F2xx/STM32F4xx for LQFP100 package</a>.            Added mission profile compliance with JEDEC JESD47 in <a href="#">Section 6.2: Absolute maximum ratings</a>.            Changed <a href="#">Figure 31 HSI deviation versus temperature to ACCHSI versus temperature</a>.            Updated <math>R_{LOAD}</math> in <a href="#">Table 85: DAC characteristics</a>.            Added note 2. related to the position of the 0.1 <math>\mu\text{F}</math> capacitor below <a href="#">Figure 37: Recommended NRST pin protection</a>.            Updated <a href="#">Figure 40: SPI timing diagram - master mode</a>.            Added reference to optional marking or inset/upset marks in all package device marking sections. Updated <a href="#">Figure 85: WLCSP143 marking example (package top view)</a>, <a href="#">Figure 88: LQFP144 marking example (package top view)</a>, <a href="#">Figure 91: LQFP176 marking (package top view)</a>, <a href="#">Figure 94: LQFP208 marking example (package top view)</a>.            Updated <a href="#">Figure 98: UFBGA176+25 - ball 10 x 10 mm, 0.65 mm pitch ultra thin fine pitch ball grid array package outline</a> and <a href="#">Table 118: UFBGA176+25 - ball, 10 x 10 mm, 0.65 mm pitch, ultra fine pitch ball grid array package mechanical data</a>.</p>

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