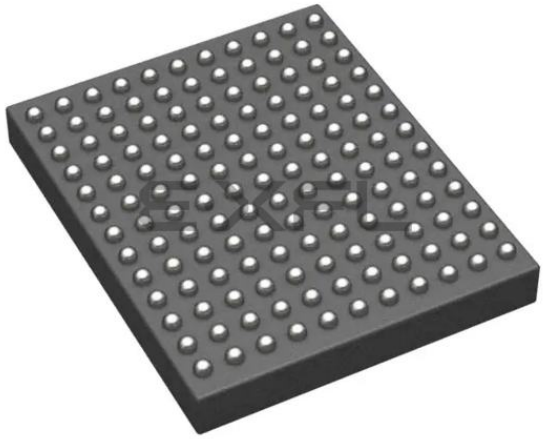

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | ARM® Cortex®-M4 |
| Core Size | 32-Bit Single-Core |
| Speed | 180MHz |
| Connectivity | CANbus, EBI/EMI, Ethernet, I²C, IrDA, LINbus, SPI, UART/USART, USB OTG |
| Peripherals | Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT |
| Number of I/O | 114 |
| Program Memory Size | 2MB (2M x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 256K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 3.6V |
| Data Converters | A/D 24x12b; D/A 2x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 143-UFBGA, WLCSP |
| Supplier Device Package | 143-WLCSP (4.52x5.55) |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f429ziy6jtr |

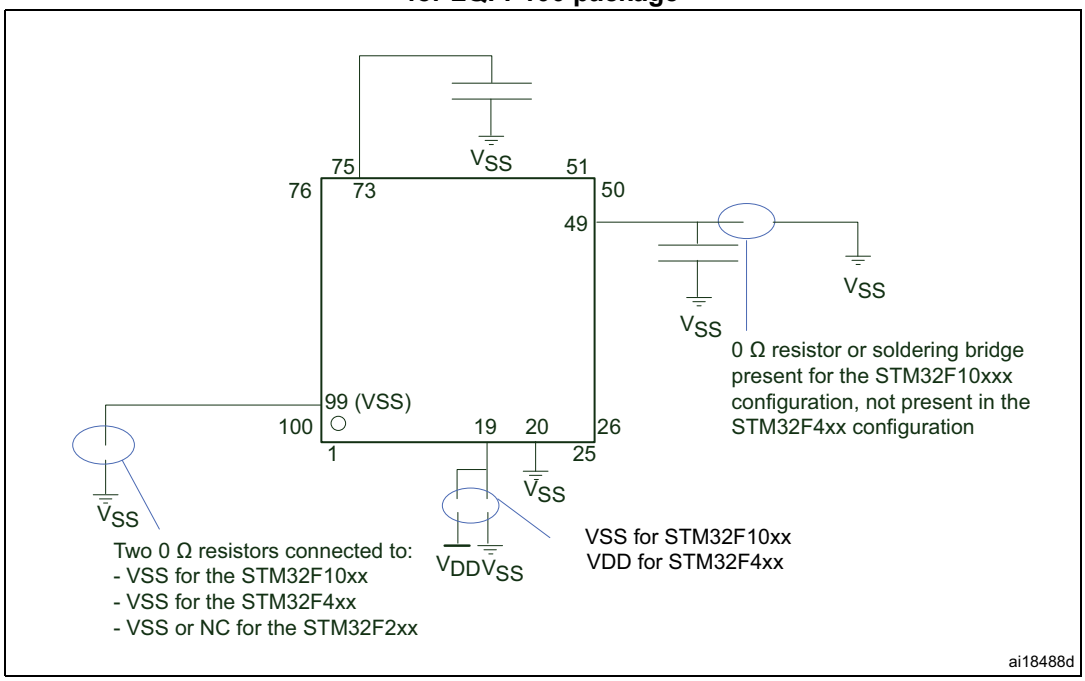
## 2.1 Full compatibility throughout the family

The STM32F427xx and STM32F429xx devices are part of the STM32F4 family. They are fully pin-to-pin, software and feature compatible with the STM32F2xx devices, allowing the user to try different memory densities, peripherals, and performances (FPU, higher frequency) for a greater degree of freedom during the development cycle.

The STM32F427xx and STM32F429xx devices maintain a close compatibility with the whole STM32F10xx family. All functional pins are pin-to-pin compatible. The STM32F427xx and STM32F429xx, however, are not drop-in replacements for the STM32F10xx devices: the two families do not have the same power scheme, and so their power pins are different. Nonetheless, transition from the STM32F10xx to the STM32F42x family remains simple as only a few pins are impacted.

*Figure 1*, *Figure 2*, and *Figure 3*, give compatible board designs between the STM32F4xx, STM32F2xx, and STM32F10xx families.

**Figure 1. Compatible board design STM32F10xx/STM32F2xx/STM32F4xx for LQFP100 package**



Additional 32-bit registers contain the programmable alarm subseconds, seconds, minutes, hours, day, and date.

Like backup SRAM, the RTC and backup registers are supplied through a switch that is powered either from the $V_{DD}$ supply when present or from the $V_{BAT}$ pin.

## 3.20 Low-power modes

The devices support three low-power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

- **Sleep mode**

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

- **Stop mode**

  The Stop mode achieves the lowest power consumption while retaining the contents of SRAM and registers. All clocks in the 1.2 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled.

  The voltage regulator can be put either in main regulator mode (MR) or in low-power mode (LPR). Both modes can be configured as follows (see *Table 5: Voltage regulator modes in stop mode*):

  – Normal mode (default mode when MR or LPR is enabled)

  – Under-drive mode.

  The device can be woken up from the Stop mode by any of the EXTI line (the EXTI line source can be one of the 16 external lines, the PVD output, the RTC alarm / wakeup / tamper / time stamp events, the USB OTG FS/HS wakeup or the Ethernet wakeup).

**Table 5. Voltage regulator modes in stop mode**

| Voltage regulator configuration | Main regulator (MR) | Low-power regulator (LPR) |
|---|---|---|
| Normal mode | MR ON | LPR ON |
| Under-drive mode | MR in under-drive mode | LPR in under-drive mode |

- **Standby mode**

  The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.2 V domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering Standby mode, the SRAM and register contents are lost except for registers in the backup domain and the backup SRAM when selected.

  The device exits the Standby mode when an external reset (NRST pin), an IWDG reset, a rising edge on the WKUP pin, or an RTC alarm / wakeup / tamper /time stamp event occurs.

  The standby mode is not supported when the embedded voltage regulator is bypassed and the 1.2 V domain is controlled by an external power.

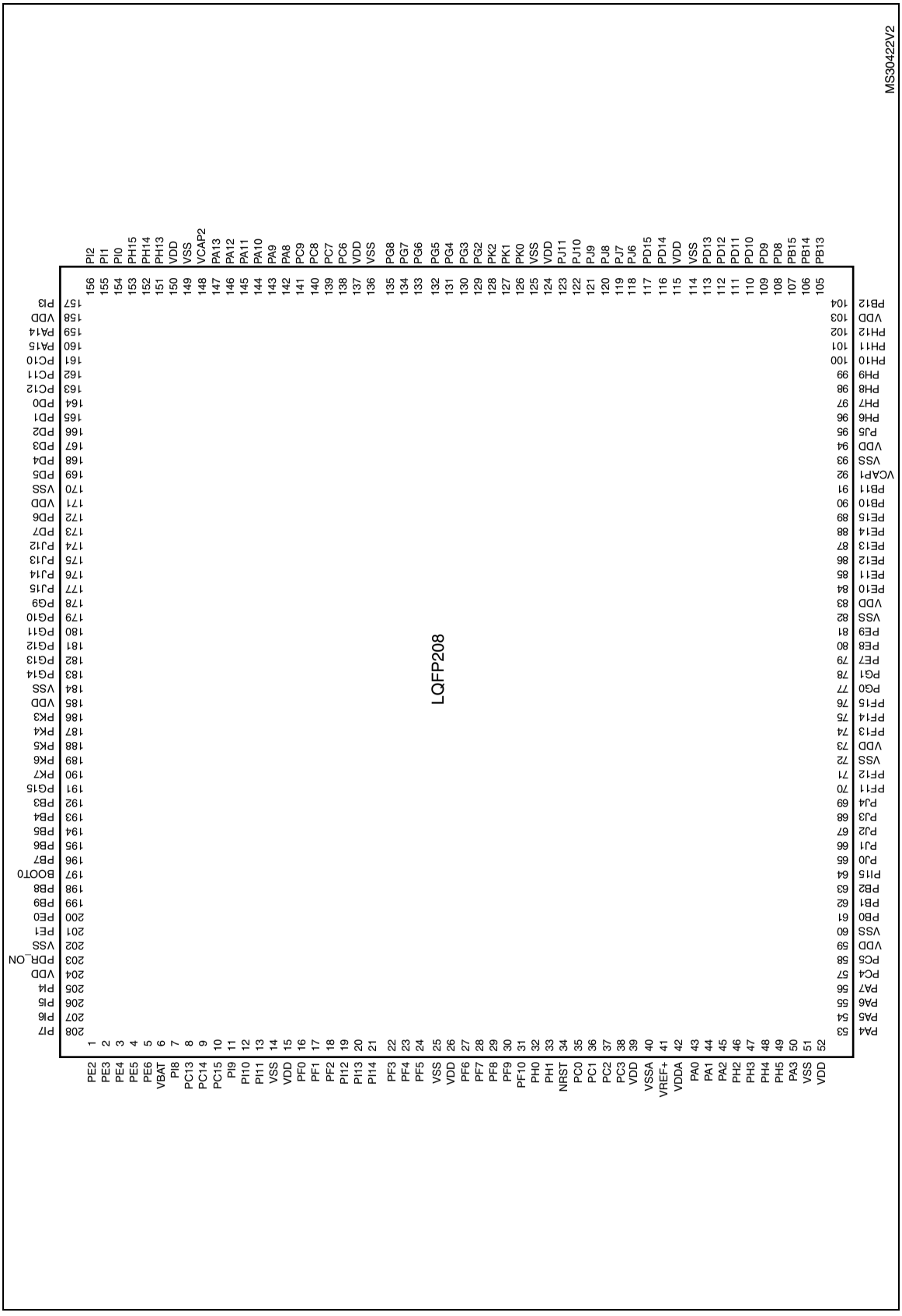



Figure 15. STM32F42x LQFP208 pinout

1. The above figure shows the package top view.

Table 10. STM32F427xx and STM32F429xx pin and ball definitions (continued)

| Pin number | | | | | | | | Pin name (function after reset)(1) | Pin type | I / O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LQFP100 | LQFP144 | UFBGA169 | UFBGA176 | LQFP176 | WLCSP143 | LQFP208 | TFBGA216 | | | | | | |
| - | - | C11 | D14 | 132 | - | 155 | D14 | PI1 | I/O | FT | - | SPI2_SCK/I2S2_CK(7), FMC_D25, DCMI_D8, LCD_G6, EVENTOUT | - |
| - | - | B12 | C14 | 133 | - | 156 | C14 | PI2 | I/O | FT | - | TIM8_CH4, SPI2_MISO, I2S2ext_SD, FMC_D26, DCMI_D9, LCD_G7, EVENTOUT | - |
| - | - | A12 | C13 | 134 | - | 157 | C13 | PI3 | I/O | FT | - | TIM8_ETR, SPI2_MOSI/I2S2_SD, FMC_D27, DCMI_D10, EVENTOUT | - |
| - | - | D11 | D9 | 135 | F5 | - | F9 | $V_{SS}$ | S | | - | - | - |
| - | - | D3 | C9 | 136 | A1 | 158 | E10 | $V_{DD}$ | S | | - | - | - |
| 76 | 109 | A11 | A14 | 137 | B1 | 159 | A14 | PA14 (JTCK-SWCLK) | I/O | FT | - | JTCK-SWCLK/ EVENTOUT | - |
| 77 | 110 | B11 | A13 | 138 | C2 | 160 | A13 | PA15 (JTDI) | I/O | FT | - | JTDI, TIM2_CH1/TIM2_ETR, SPI1_NSS, SPI3_NSS/I2S3_WS, EVENTOUT | - |
| 78 | 111 | C10 | B14 | 139 | A2 | 161 | B14 | PC10 | I/O | FT | - | SPI3_SCK/I2S3_CK, USART3_TX, UART4_TX, SDIO_D2, DCMI_D8, LCD_R2, EVENTOUT | - |
| 79 | 112 | B10 | B13 | 140 | B2 | 162 | B13 | PC11 | I/O | FT | - | I2S3ext_SD, SPI3_MISO, USART3_RX, UART4_RX, SDIO_D3, DCMI_D4, EVENTOUT | - |
| 80 | 113 | A10 | A12 | 141 | C3 | 163 | A12 | PC12 | I/O | FT | - | SPI3_MOSI/I2S3_SD, USART3_CK, UART5_TX, SDIO_CK, DCMI_D9, EVENTOUT | - |
| 81 | 114 | D9 | B12 | 142 | B3 | 164 | B12 | PD0 | I/O | FT | - | CAN1_RX, FMC_D2, EVENTOUT | - |

Table 10. STM32F427xx and STM32F429xx pin and ball definitions (continued)

| Pin number | | | | | | | | Pin name (function after reset)(1) | Pin type | I / O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LQFP100 | LQFP144 | UFBGA169 | UFBGA176 | LQFP176 | WLCSP143 | LQFP208 | TFBGA216 | | | | | | |
| 89 | 133 | B6 | A10 | 161 | B7 | 192 | A10 | PB3 (JTDO/TRACESWO) | I/O | FT | - | JTDO/TRACESWO, TIM2_CH2, SPI1_SCK, SPI3_SCK/I2S3_CK, EVENTOUT | - |
| 90 | 134 | A6 | A9 | 162 | C7 | 193 | A9 | PB4 (NJTRST) | I/O | FT | - | NJTRST, TIM3_CH1, SPI1_MISO, SPI3_MISO, I2S3ext_SD, EVENTOUT | - |
| 91 | 135 | D5 | A6 | 163 | C8 | 194 | A8 | PB5 | I/O | FT | - | TIM3_CH2, I2C1_SMBA, SPI1_MOSI, SPI3_MOSI/I2S3_SD, CAN2_RX, OTG_HS_ULPI_D7, ETH_PPS_OUT, FMC_SDCKE1, DCMI_D10, EVENTOUT | - |
| 92 | 136 | C5 | B6 | 164 | A8 | 195 | B6 | PB6 | I/O | FT | - | TIM4_CH1, I2C1_SCL, USART1_TX, CAN2_TX, FMC_SDNE1, DCMI_D5, EVENTOUT | - |
| 93 | 137 | B5 | B5 | 165 | B8 | 196 | B5 | PB7 | I/O | FT | - | TIM4_CH2, I2C1_SDA, USART1_RX, FMC_NL, DCMI_VSYNC, EVENTOUT | - |
| 94 | 138 | A5 | D6 | 166 | C9 | 197 | E6 | BOOT0 | I | B | - | | $V_{PP}$ |
| 95 | 139 | D4 | A5 | 167 | A9 | 198 | A7 | PB8 | I/O | FT | - | TIM4_CH3, TIM10_CH1, I2C1_SCL, CAN1_RX, ETH_MII_TXD3, SDIO_D4, DCMI_D6, LCD_B6, EVENTOUT | - |

**Table 13. STM32F427xx and STM32F429xx register boundary addresses**

| Bus | Boundary address | Peripheral |
|---|---|---|
| | 0xE00F FFFF - 0xFFFF FFFF | Reserved |
| Cortex-M4 | 0xE000 0000 - 0xE00F FFFF | Cortex-M4 internal peripherals |
| AHB3 | 0xD000 0000 - 0xDFFF FFFF | FMC bank 6 |
| | 0xC000 0000 - 0xCFFF FFFF | FMC bank 5 |
| | 0xA000 1000 - 0xBFFF FFFF | Reserved |
| | 0xA000 0000- 0xA000 0FFF | FMC control register |
| | 0x9000 0000 - 0x9FFF FFFF | FMC bank 4 |
| | 0x8000 0000 - 0x8FFF FFFF | FMC bank 3 |
| | 0x7000 0000 - 0x7FFF FFFF | FMC bank 2 |
| | 0x6000 0000 - 0x6FFF FFFF | FMC bank 1 |
| | 0x5006 0C00- 0x5FFF FFFF | Reserved |
| AHB2 | 0x5006 0800 - 0X5006 0BFF | RNG |
| | 0x5005 0400 - X5006 07FF | Reserved |
| | 0x5005 0000 - 0X5005 03FF | DCMI |
| | 0x5004 0000- 0x5004 FFFF | Reserved |
| | 0x5000 0000 - 0X5003 FFFF | USB OTG FS |

Table 13. STM32F427xx and STM32F429xx register boundary addresses (continued)

| Bus | Boundary address | Peripheral |
|---|---|---|
| | 0x4000 8000- 0x4000 FFFF | Reserved |
| APB1 | 0x4000 7C00 - 0x4000 7FFF | UART8 |
| | 0x4000 7800 - 0x4000 7BFF | UART7 |
| | 0x4000 7400 - 0x4000 77FF | DAC |
| | 0x4000 7000 - 0x4000 73FF | PWR |
| | 0x4000 6C00 - 0x4000 6FFF | Reserved |
| | 0x4000 6800 - 0x4000 6BFF | CAN2 |
| | 0x4000 6400 - 0x4000 67FF | CAN1 |
| | 0x4000 6000 - 0x4000 63FF | Reserved |
| | 0x4000 5C00 - 0x4000 5FFF | I2C3 |
| | 0x4000 5800 - 0x4000 5BFF | I2C2 |
| | 0x4000 5400 - 0x4000 57FF | I2C1 |
| | 0x4000 5000 - 0x4000 53FF | UART5 |
| | 0x4000 4C00 - 0x4000 4FFF | UART4 |
| | 0x4000 4800 - 0x4000 4BFF | USART3 |
| | 0x4000 4400 - 0x4000 47FF | USART2 |
| | 0x4000 4000 - 0x4000 43FF | I2S3ext |
| | 0x4000 3C00 - 0x4000 3FFF | SPI3 / I2S3 |
| | 0x4000 3800 - 0x4000 3BFF | SPI2 / I2S2 |
| | 0x4000 3400 - 0x4000 37FF | I2S2ext |
| | 0x4000 3000 - 0x4000 33FF | IWDG |
| | 0x4000 2C00 - 0x4000 2FFF | WWDG |
| | 0x4000 2800 - 0x4000 2BFF | RTC & BKP Registers |
| | 0x4000 2400 - 0x4000 27FF | Reserved |
| | 0x4000 2000 - 0x4000 23FF | TIM14 |
| | 0x4000 1C00 - 0x4000 1FFF | TIM13 |
| | 0x4000 1800 - 0x4000 1BFF | TIM12 |
| | 0x4000 1400 - 0x4000 17FF | TIM7 |
| | 0x4000 1000 - 0x4000 13FF | TIM6 |
| | 0x4000 0C00 - 0x4000 0FFF | TIM5 |
| | 0x4000 0800 - 0x4000 0BFF | TIM4 |
| | 0x4000 0400 - 0x4000 07FF | TIM3 |
| | 0x4000 0000 - 0x4000 03FF | TIM2 |

**Table 26. Typical and maximum current consumption in Sleep mode**

| Symbol | Parameter | Conditions | $f_{HCLK}$ (MHz) | Typ | Max(1) | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | $T_A$ = 25 °C | $T_A$ = 85 °C | $T_A$ = 105 °C | |
| $I_{DD}$ | Supply current in Sleep mode | All Peripherals enabled(2) | 180 | 78 | 89(3) | 110 | 130(3) | mA |
| | | | 168 | 66 | 75(3) | 93 | 110(3) | |
| | | | 150 | 56 | 61 | 80 | 96 | |
| | | | 144 | 54 | 58 | 78 | 94 | |
| | | | 120 | 40 | 44 | 59 | 72 | |
| | | | 90 | 32 | 34 | 46 | 56 | |
| | | | 60 | 22 | 23 | 31 | 38 | |
| | | | 30 | 10 | 16 | 30 | 43 | |
| | | | 25 | 9 | 14 | 28 | 40 | |
| | | | 16 | 5 | 12 | 25 | 40 | |
| | | | 8 | 3 | 8 | 22 | 35 | |
| | | | 4 | 3 | 7 | 21 | 34 | |
| | | | 2 | 2 | 6.5 | 20 | 33 | |
| | | All Peripherals disabled | 180 | 21 | 26(3) | 54 | 76(3) | |
| | | | 168 | 16 | 20(3) | 41 | 58(3) | |
| | | | 150 | 14 | 17 | 36 | 52 | |
| | | | 144 | 13 | 16.5 | 35 | 51 | |
| | | | 120 | 10 | 14 | 28 | 41 | |
| | | | 90 | 8 | 13 | 26 | 37 | |
| | | | 60 | 6 | 9 | 17 | 25 | |
| | | | 30 | 5 | 8 | 22 | 35 | |
| | | | 25 | 3 | 7 | 21 | 34 | |
| | | | 16 | 3 | 7 | 21 | 34 | |
| | | | 8 | 2 | 6 | 20 | 33 | |
| | | | 4 | 2 | 6 | 20 | 33 | |
| | | | 2 | 2 | 6 | 20 | 33 | |

1. Guaranteed by characterization unless otherwise specified.
2. When analog peripheral blocks such as ADCs, DACs, HSE, LSE, HSI, or LSI are ON, an additional power consumption should be considered.
3. Based on characterization, tested in production.

**Table 27. Typical and maximum current consumptions in Stop mode**

| Symbol | Parameter | Conditions | Typ | Max(1) | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | $V_{DD}$ = 3.6 V | | | |
| | | | $T_A$ = 25 °C | $T_A$ = 25 °C | $T_A$ = 85 °C | $T_A$ = 105 °C | |
| $I_{DD\_STOP\_NM}$ (normal mode) | Supply current in Stop mode with voltage regulator in main regulator mode | Flash memory in Stop mode, all oscillators OFF, no independent watchdog | 0.40 | 1.50 | 14.00 | 25.00 | mA |
| | | Flash memory in Deep power down mode, all oscillators OFF, no independent watchdog | 0.35 | 1.50 | 14.00 | 25.00 | |
| | Supply current in Stop mode with voltage regulator in Low Power regulator mode | Flash memory in Stop mode, all oscillators OFF, no independent watchdog | 0.29 | 1.10 | 10.00 | 18.00 | |
| | | Flash memory in Deep power down mode, all oscillators OFF, no independent watchdog | 0.23 | 1.10 | 10.00 | 18.00 | |
| $I_{DD\_STOP\_UDM}$ (under-drive mode) | Supply current in Stop mode with voltage regulator in main regulator and under-drive mode | Flash memory in Deep power down mode, main regulator in under-drive mode, all oscillators OFF, no independent watchdog | 0.19 | 0.50 | 6.00 | 9.00 | |
| | Supply current in Stop mode with voltage regulator in Low Power regulator and under-drive mode | Flash memory in Deep power down mode, Low Power regulator in under-drive mode, all oscillators OFF, no independent watchdog | 0.10 | 0.40 | 4.00 | 7.00 | |

1. Data based on characterization, tested in production.

**Table 35. Peripheral current consumption (continued)**

| Peripheral | | $I_{DD}$( Typ)(1) | | | Unit |
|---|---|---|---|---|---|
| | | Scale 1 | Scale 2 | Scale 3 | |
| APB2 (up to 90 MHz) | SDIO | 8.11 | 8.75 | 7.83 | µA/MHz |
| | TIM1 | 17.11 | 15.97 | 14.17 | |
| | TIM8 | 17.33 | 16.11 | 14.33 | |
| | TIM9 | 7.22 | 6.67 | 6.00 | |
| | TIM10 | 4.56 | 4.31 | 3.83 | |
| | TIM11 | 4.78 | 4.44 | 4.00 | |
| | ADC1(5) | 4.67 | 4.31 | 3.83 | |
| | ADC2(5) | 4.78 | 4.44 | 4.00 | |
| | ADC3(5) | 4.56 | 4.17 | 3.67 | |
| | SPI1 | 1.44 | 1.39 | 1.17 | |
| | USART1 | 4.00 | 3.75 | 3.33 | |
| | USART6 | 4.00 | 3.75 | 3.33 | |
| | SPI4 | 1.44 | 1.39 | 1.17 | |
| | SPI5 | 1.44 | 1.39 | 1.17 | |
| | SPI6 | 1.44 | 1.39 | 1.17 | |
| | SYSCFG | 0.78 | 0.69 | 0.67 | |
| | LCD_TFT | 39.89 | 37.22 | 33.17 | |
| | SAI1 | 3.78 | 3.47 | 3.17 | |

1. When the I/O compensation cell is ON, $I_{DD}$ typical value increases by 0.22 mA.
2. The BusMatrix is automatically active when at least one master is ON.
3. To enable an I2S peripheral, first set the I2SMOD bit and then the I2SE bit in the SPI_I2SCFGR register.
4. When the DAC is ON and EN1/2 bits are set in DAC_CR register, add an additional power consumption of 0.8 mA per DAC channel for the analog part.
5. When the ADC is ON (ADON bit set in the ADC_CR2 register), add an additional power consumption of 1.6 mA per ADC for the analog part.

### Low-speed external user clock generated from an external source

In bypass mode the LSE oscillator is switched off and the input pin is a standard I/O. The external clock signal has to respect the *Table 56: I/O static characteristics*. However, the recommended clock input waveform is shown in *Figure 28*.

The characteristics given in *Table 38* result from tests performed using an low-speed external clock source, and under ambient temperature and supply voltage conditions summarized in *Table 17*.

**Table 38. Low-speed external user clock characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{LSE\_ext}$ | User External clock source frequency(1) | | - | 32.768 | 1000 | kHz |
| $V_{LSEH}$ | OSC32_IN input pin high level voltage | | $0.7V_{DD}$ | - | $V_{DD}$ | V |
| $V_{LSEL}$ | OSC32_IN input pin low level voltage | | $V_{SS}$ | - | $0.3V_{DD}$ | |
| $t_{w(LSE)}$ $t_{f(LSE)}$ | OSC32_IN high or low time(1) | | 450 | - | - | ns |
| $t_{r(LSE)}$ $t_{f(LSE)}$ | OSC32_IN rise or fall time(1) | | - | - | 50 | |
| $C_{in(LSE)}$ | OSC32_IN input capacitance(1) | | - | 5 | - | pF |
| $DuCy_{(LSE)}$ | Duty cycle | | 30 | - | 70 | % |
| $I_L$ | OSC32_IN Input leakage current | $V_{SS} \leq V_{IN} \leq V_{DD}$ | - | - | ±1 | µA |

1. Guaranteed by design.

**Figure 27. High-speed external clock source AC timing diagram**

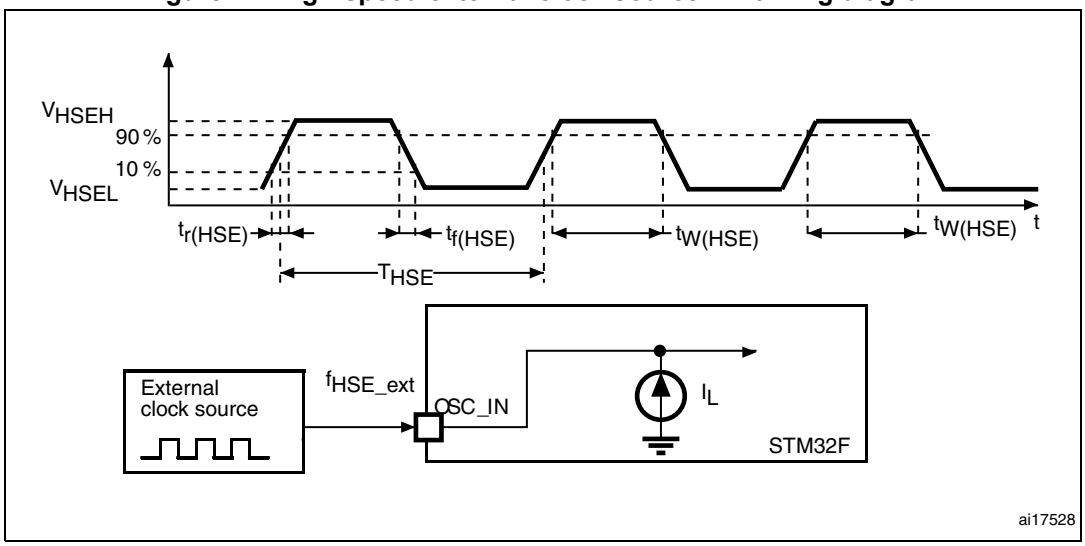


**Table 44. PLLI2S (audio PLL) characteristics (continued)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{DD(PLLI2S)}$(4) | PLLI2S power consumption on $V_{DD}$ | VCO freq = 100 MHz<br>VCO freq = 432 MHz | 0.15<br>0.45 | - | 0.40<br>0.75 | mA |
| $I_{DDA(PLLI2S)}$(4) | PLLI2S power consumption on $V_{DDA}$ | VCO freq = 100 MHz<br>VCO freq = 432 MHz | 0.30<br>0.55 | - | 0.40<br>0.85 | mA |

1. Take care of using the appropriate division factor M to have the specified PLL input clock values.
2. Guaranteed by design.
3. Value given with main PLL running.
4. Guaranteed by characterization results.

**Table 45. PLLISAI (audio and LCD-TFT PLL) characteristics**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $f_{PLLSAI\_IN}$ | PLLSAI input clock(1) | | | 0.95(2) | 1 | 2.10 | MHz |
| $f_{PLLSAI\_OUT}$ | PLLSAI multiplier output clock | | | - | - | 216 | MHz |
| $f_{VCO\_OUT}$ | PLLSAI VCO output | | | 100 | - | 432 | MHz |
| $t_{LOCK}$ | PLLSAI lock time | VCO freq = 100 MHz | | 75 | - | 200 | µs |
| | | VCO freq = 432 MHz | | 100 | - | 300 | |
| Jitter(3) | Main SAI clock jitter | Cycle to cycle at 12.288 MHz on 48KHz period, N=432, R=5 | RMS | - | 90 | - | ps |
| | | | peak to peak | - | ±280 | - | |
| | | Average frequency of 12.288 MHz<br>N = 432, R = 5<br>on 1000 samples | | - | 90 | - | ps |
| | FS clock jitter | Cycle to cycle at 48 KHz on 1000 samples | | - | 400 | - | ps |
| $I_{DD(PLLSAI)}$(4) | PLLSAI power consumption on $V_{DD}$ | VCO freq = 100 MHz<br>VCO freq = 432 MHz | | 0.15<br>0.45 | - | 0.40<br>0.75 | mA |
| $I_{DDA(PLLSAI)}$(4) | PLLSAI power consumption on $V_{DDA}$ | VCO freq = 100 MHz<br>VCO freq = 432 MHz | | 0.30<br>0.55 | - | 0.40<br>0.85 | mA |

1. Take care of using the appropriate division factor M to have the specified PLL input clock values.
2. Guaranteed by design.
3. Value given with main PLL running.
4. Guaranteed by characterization results.

**Table 50. Flash memory endurance and data retention**

| Symbol | Parameter | Conditions | Value | Unit |
|---|---|---|---|---|
| | | | Min(1) | |
| $N_{END}$ | Endurance | $T_A$ = –40 to +85 °C (6 suffix versions)<br>$T_A$ = –40 to +105 °C (7 suffix versions) | 10 | kcycles |
| $t_{RET}$ | Data retention | 1 kcycle(2) at $T_A$ = 85 °C | 30 | Years |
| | | 1 kcycle(2) at $T_A$ = 105 °C | 10 | |
| | | 10 kcycles(2) at $T_A$ = 55 °C | 20 | |

1. Guaranteed by characterization results.
2. Cycling performed over the whole temperature range.

## 6.3.14 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

### Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A burst of fast transient voltage (positive and negative) is applied to $V_{DD}$ and $V_{SS}$ through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 51*. They are based on the EMS levels and classes defined in application note AN1709.

**Table 51. EMS characteristics**

| Symbol | Parameter | Conditions | Level/ Class |
|---|---|---|---|
| $V_{FESD}$ | Voltage limits to be applied on any I/O pin to induce a functional disturbance | $V_{DD}$ = 3.3 V, LQFP176, $T_A$ = +25 °C, $f_{HCLK}$ = 168 MHz, conforms to IEC 61000-4-2 | 2B |
| $V_{EFTB}$ | Fast transient voltage burst limits to be applied through 100 pF on $V_{DD}$ and $V_{SS}$ pins to induce a functional disturbance | $V_{DD}$ = 3.3 V, LQFP176, $T_A$ =+25 °C, $f_{HCLK}$ = 168 MHz, conforms to IEC 61000-4-2 | 4A |

When the application is exposed to a noisy environment, it is recommended to avoid pin exposition to disturbances. The pins showing a middle range robustness are: PA0, PA1, PA2, PH2, PH3, PH4, PH5, PA3, PA4, PA5, PA6, PA7, PC4, and PC5.

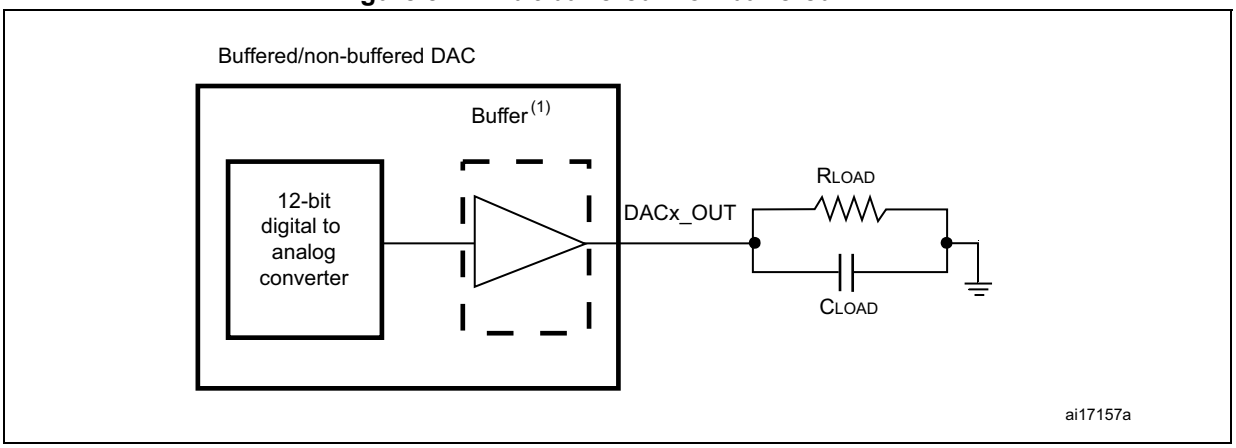
As a consequence, it is recommended to add a serial resistor (1 kΩ) located as close as possible to the MCU to the pins exposed to noise (connected to tracks longer than 50 mm on PCB).

**Table 85. DAC characteristics (continued)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit | Comments |
|---|---|---|---|---|---|---|---|
| $t_{WAKEUP}$(4) | Wakeup time from off state (Setting the ENx bit in the DAC Control register) | - | - | 6.5 | 10 | µs | $C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ input code between lowest and highest possible ones. |
| PSRR+ (2) | Power supply rejection ratio (to $V_{DDA}$) (static DC measurement) | - | - | –67 | –40 | dB | No $R_{LOAD}$, $C_{LOAD}$ = 50 pF |

1. $V_{DDA}$ minimum value of 1.7 V is obtained with the use of an external power supply supervisor (refer to *Section 3.17.2: Internal reset OFF*).
2. Guaranteed by design.
3. The quiescent mode corresponds to a state where the DAC maintains a stable output level to ensure that no dynamic consumption occurs.
4. Guaranteed by characterization.

**Figure 54. 12-bit buffered /non-buffered DAC**




1. The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC_CR register.

**Table 96. Synchronous non-multiplexed NOR/PSRAM read timings(1)(2) (continued)**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{h(CLKH-DV)}$ | FMC_D[15:0] valid data after FMC_CLK high | 0 | - | ns |
| $t_{(NWAIT-CLKH)}$ | FMC_NWAIT valid before FMC_CLK high | 4 | | |
| $t_{h(CLKH-NWAIT)}$ | FMC_NWAIT valid after FMC_CLK high | 0 | | |

1. $C_L$ = 30 pF.
2. Guaranteed by characterization results.

**Figure 62. Synchronous non-multiplexed PSRAM write timings**

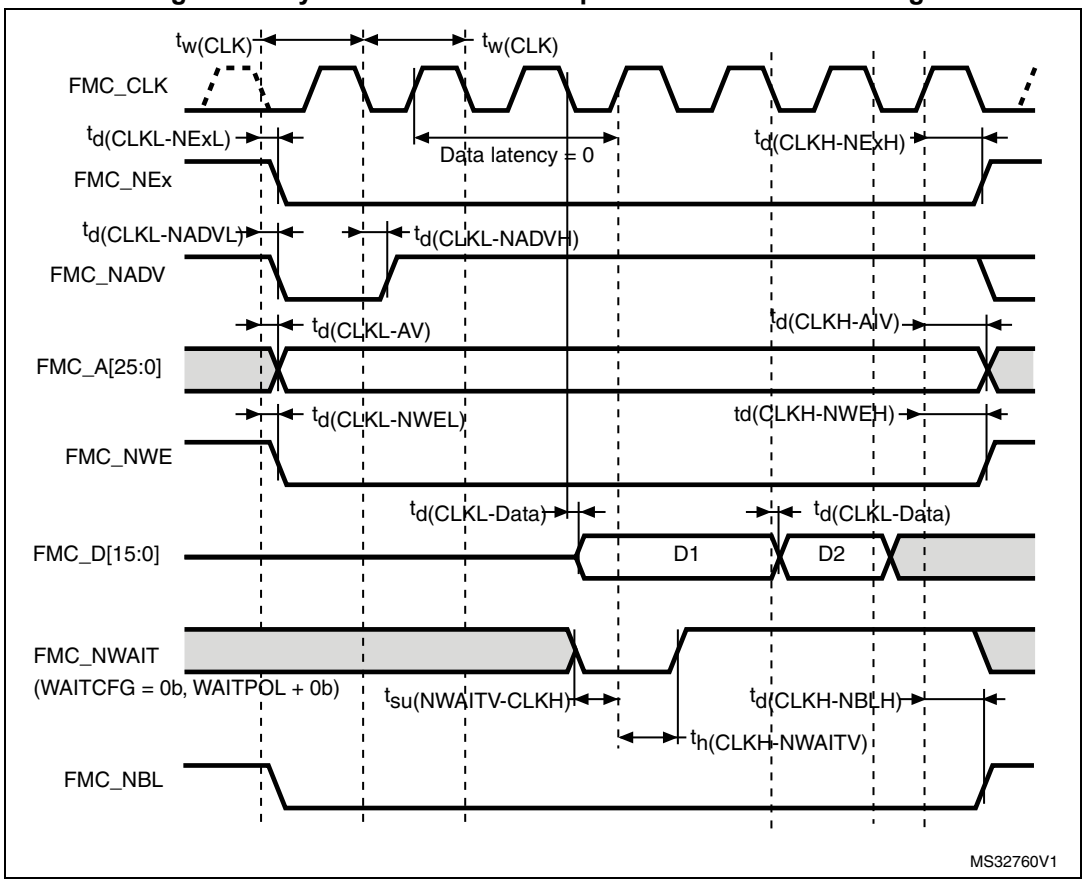



**Table 97. Synchronous non-multiplexed PSRAM write timings(1)(2)**

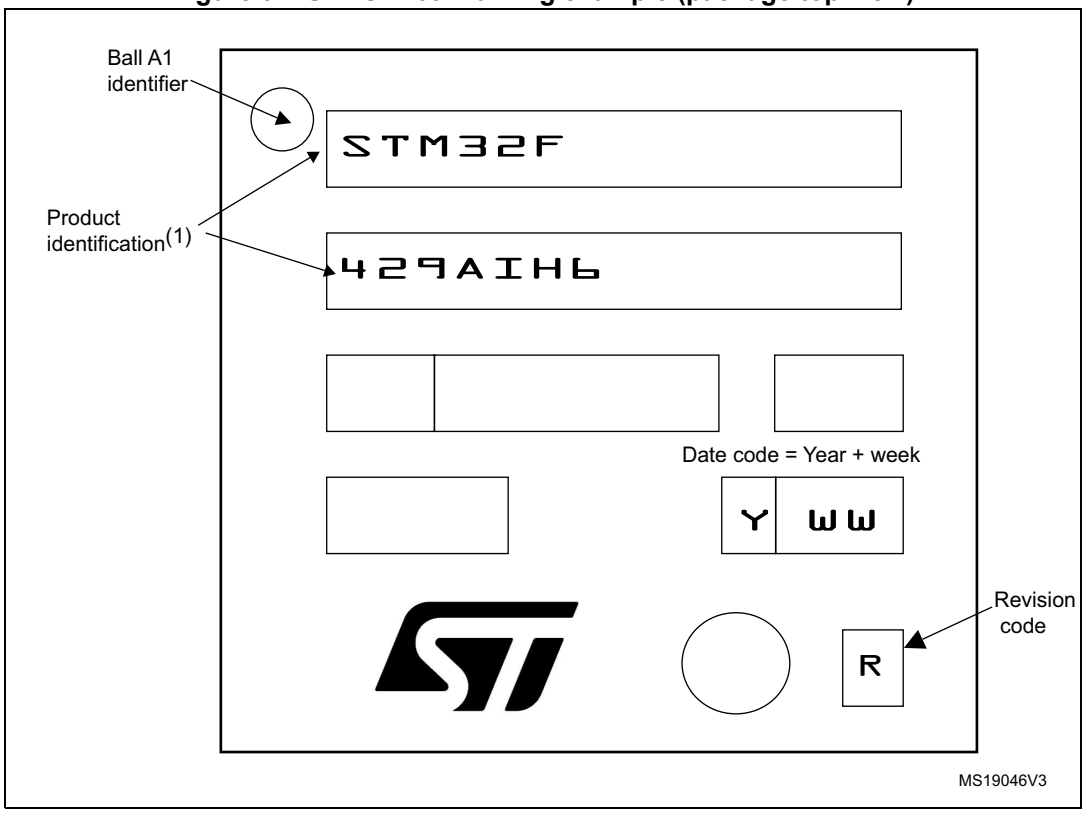
| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{(CLK)}$ | FMC_CLK period | $2T_{HCLK} - 1$ | - | ns |
| $t_{d(CLKL-NExL)}$ | FMC_CLK low to FMC_NEx low (x=0..2) | - | 0.5 | ns |
| $t_{(CLKH-NExH)}$ | FMC_CLK high to FMC_NEx high (x= 0…2) | $T_{HCLK}$ | - | ns |
| $t_{d(CLKL-NADVL)}$ | FMC_CLK low to FMC_NADV low | - | 0 | ns |
| $t_{d(CLKL-NADVH)}$ | FMC_CLK low to FMC_NADV high | 0 | - | ns |
| $t_{d(CLKL-AV)}$ | FMC_CLK low to FMC_Ax valid (x=16…25) | - | 0 | ns |

### Device marking for UFBGA169

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

Other optional marking or inset/upset marks, which depends assembly location, are not indicated below.

**Figure 97. UFBGA169 marking example (package top view)**




1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

**Table 124. Document revision history**

| Date | Revision | Changes |
|---|---|---|
| 21-Jan-2016 | 8 | Updated *Figure 22: Power supply scheme*.<br>Added $t_{d(TXD)}$ values corresponding to 1.71 V < $V_{DD}$ < 3.6 V in *Table 72: Dynamics characteristics: Ethernet MAC signals for RMII*. |
| 18-Jul-2016 | 9 | Updated *Figure 1: Compatible board design STM32F10xx/STM32F2xx/STM32F4xx for LQFP100 package*.<br>Added mission profile compliance with JEDEC JESD47 in *Section 6.2: Absolute maximum ratings*.<br>Changed *Figure 31 HSI deviation versus temperature to ACCHSI versus temperature.*<br>Updated $R_{LOAD}$ in *Table 85: DAC characteristics*.<br>Added note *2.* related to the position of the 0.1 µF capacitor below *Figure 37: Recommended NRST pin protection*.<br>Updated *Figure 40: SPI timing diagram - master mode*.<br>Added reference to optional marking or inset/upset marks in all package device marking sections. Updated *Figure 85: WLCSP143 marking example (package top view)*, *Figure 88: LQFP144 marking example (package top view)*, *Figure 91: LQFP176 marking (package top view)*, *Figure 94: LQFP208 marking example (package top view)*.<br>Updated *Figure 98: UFBGA176+25 - ball 10 x 10 mm, 0.65 mm pitch ultra thin fine pitch ball grid array package outline* and *Table 118: UFBGA176+25 - ball, 10 x 10 mm, 0.65 mm pitch, ultra fine pitch ball grid array package mechanical data*. |