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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	24
Program Memory Size	4KB (4K x 8)
Program Memory Type	ROM
EEPROM Size	-
RAM Size	236 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.600", 15.24mm)
Supplier Device Package	28-DIP
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z87c3304pecr53a7

Pin Description

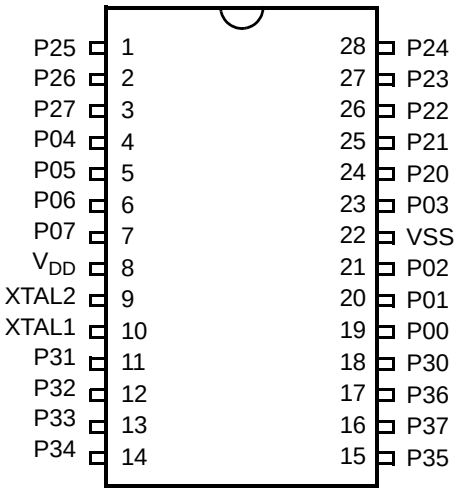


Figure 2.28-Pin DIP/SOIC Pin Configuration

Table 2. 28-Pin DIP/SOIC Pin Configuration

Pin #	Symbol	Function	Direction
1–3	P25-27	Port 2, Pins 5,6,7	Input/Output
4-7	P04-07	Port 0, Pins 4-7	Input/Output
8	V_{DD}	Power Supply	
9	XTAL2	Crystal Oscillator	Output
10	XTAL1	Crystal Oscillator	Input
11-13	P31-33	Port 3, Pins 1,2,3	Fixed Input
14-15	P34-35	Port 3, Pins 4,5	Fixed Output
16	P37	Port 3, Pin 7	Fixed Output
17	P36	Port 3, Pin 6	Fixed Output
18	P30	Port 3, Pin 0	Fixed Input
19-21	P00-02	Port 0, Pins 0,1,2	Input/Output
22	V_{SS}	Ground	
23	P03	Port 0, Pin 3	Input/Output
24-28	P20-24	Port 2, Pins 0,1,2,3,4	Input/Output

Mode Register (P3M bit 1). For interrupt functions, Port 3, bit 0 and pin 3 are falling-edge interrupt inputs. P31 and P32 are programmable as rising, falling, or both edge-triggered interrupts (IRQ register bits 6 and 7). P33 is the comparator reference voltage input when in Analog mode. Access to Counter/Timer 1 is made through P31 (T_{IN}) and P36 (T_{OUT}). Handshake lines for Ports 0, 1, and 2 are available on P31 through P36.

Port 3 also provides the following control functions: four external interrupt request signals (IRQ3–IRQ0) and timer input and output signals (T_{IN} and T_{OUT}).

Table 3. Port 3 Pin Assignments

Pin	I/O	Control Timer	Analog	Interrupt
P30	IN			IRQ3
P31	IN	T_{IN}	AN1	IRQ2
P32	IN		AN2	IRQ0
P33	IN		REF	IRQ1
P34	OUT		AN1–OUT	
P35	OUT			
P36	OUT	T_{OUT}		
P37	OUT		AN2–OUT	

Comparator Inputs and Outputs. Port 3, pins P31 and P32 each feature a comparator front end. The comparator reference voltage, pin P33, is common to both comparators. In ANALOG mode, the P31 and P32 are the positive inputs to the comparators, and P33 is the reference voltage supplied to both comparators. In DIGITAL mode, pin P33 is used as a P33 register input or IRQ1 source. P34 and P37 can provide the comparator output directly by software-programming the PCON register bit D0 to 1 (see Figure 5).

Note: The user must add a two-NOP delay after setting the P3M bit D1 to 1 before the comparator output is valid. IRQ0, IRQ1, and IRQ2 must be cleared in the IRQ register when the comparator is enabled or disabled.

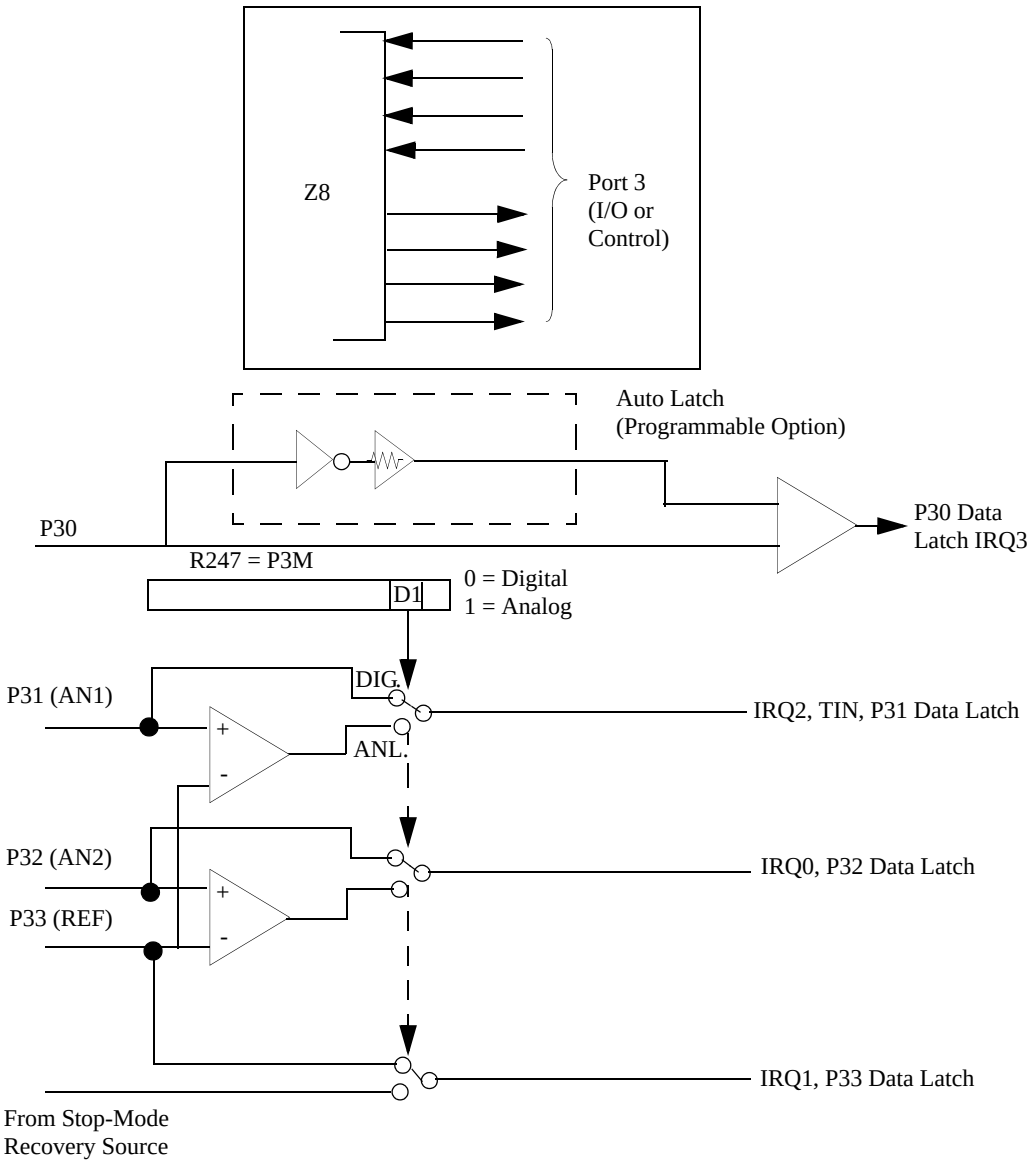


Figure 5. Port 3 Configuration

interrupts. Address 12 to address 4095 consists of on-chip mask-programmed ROM.

The 4 KB program memory is mask programmable. A ROM protect feature prevents dumping of the ROM contents by inhibiting execution of LDC, LDCI, LDE, and LDEI instructions to program memory in external program mode. ROM look-up tables can be used with this feature. The ROM Protect option is mask-programmable, to be selected by the customer when the ROM code is submitted.

See Figure 7.

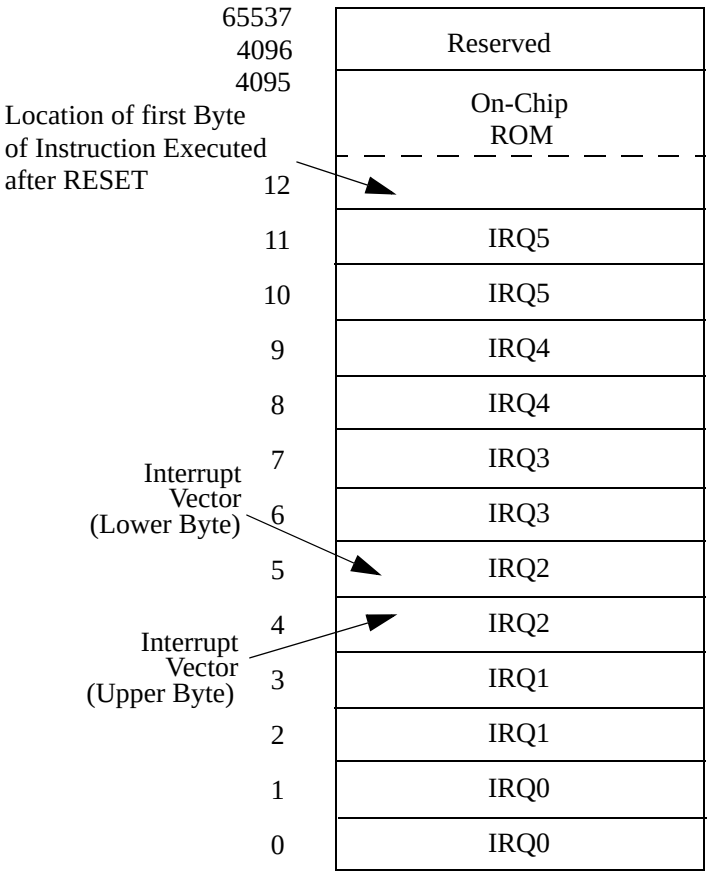


Figure 7.Program Memory Map

ROM Protect. ROM PROTECT provides an additional security function. When the ROM PROTECT option bit is selected, and executing out of Internal Program

Table 5. Interrupt Types, Sources, and Vectors

Name	Source	Vector Location	Comments
IRQ0	IRQ0	0,1	External (P32), Rising and Falling Edges Triggered
IRQ1,	IRQ1	2,3	External (P33), Falling Edge Triggered
IRQ2	IRQ2, T_{IN}	4,5	External (P31), Rising and Falling Edges Triggered
IRQ3	IRQ3	6,7	External (P30), Falling Edge Triggered
IRQ4	T0	8,9	Internal
IRQ5	T1	10,11	Internal

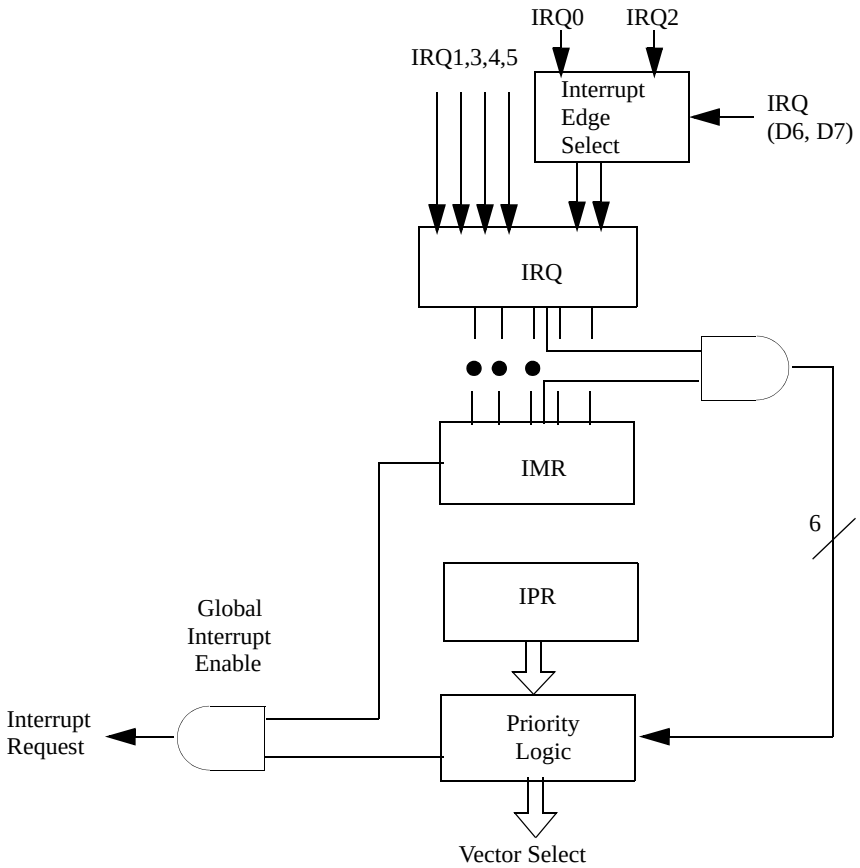


Figure 11.Interrupt Block Diagram

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority register. An interrupt machine cycle activates when an interrupt request is granted. This action disables all subsequent interrupts, saves the Program Counter and Status Flags, and then branches to the program memory vector location reserved for that interrupt.

All Z8 interrupts are vectored through locations in the program memory. This memory location and the next byte contain the 16-bit address of the interrupt service routine for that particular interrupt request. To accommodate polled interrupt systems, interrupt inputs are masked and the Interrupt Request register is polled to determine which of the interrupt requests require service.

When in ANALOG mode, an interrupt resulting from AN1 maps to IRQ2, and an interrupt from AN2 maps to IRQ0. Interrupts IRQ2 and IRQ0 may be rising, falling, or both edge-triggered, and are programmed in the IRQ register. The software polls to identify the state of the pin. When in ANALOG mode, IRQ1 is generated by the Stop-Mode Recovery source selected by SMR Register bits D4, D3, D2, or SMR2 D1 or D0.

Programming bits for the Interrupt Edge Select are located in the IRQ register, bits D7 and D6. The configuration is indicated in Table 7.

Table 6. IRQ Register*

IRQ		Interrupt Edge	
D7	**D6**	**P31**	**P32**
0	0	F	F
	1	F	R
1	0	R	F
1	1	R/F	R/F

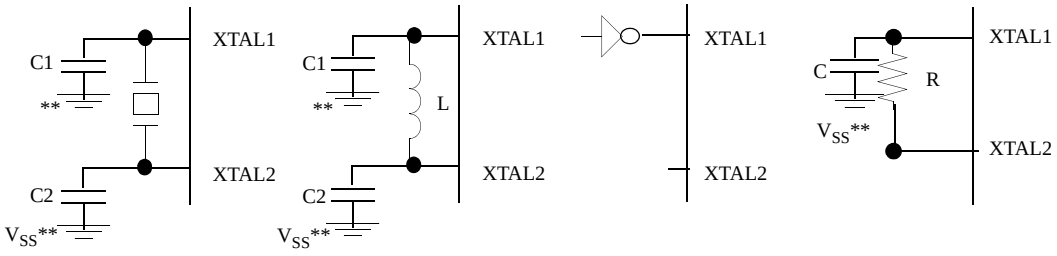
Notes:
F = Falling Edge
R = Rising Edge

Clock. The Z8 on-chip oscillator features a high-gain, parallel-resonant amplifier for connection to a crystal, LC, RC, ceramic resonator, or any suitable external clock source (X_{IN} = INPUT, X_{OUT} = OUTPUT). The crystal should be AT-cut, 4 MHz maximum, with a series resistance (RS) of less than or equal to 100Ω when oscillating from 1MHz to 4MHz.

The crystal should be connected across XTAL1 and XTAL2 using the vendor’s recommended capacitor values from each pin directly to the device Ground pin to reduce ground-noise injection into the oscillator. The RC oscillator option is mask-

programmable and is selectable by the customer at the time the ROM code is submitted.

Notes: The RC option is available up to 4MHz. The RC oscillator configuration must be an external resistor connected from X_{IN} to X_{OUT}, with a frequency-setting capacitor from X_{IN} to Ground (Figure 12).
For better noise immunity, the capacitors should be tied directly to the device Ground pin (V_{SS}).



Ceramic Resonator or Crystal
C1, C2 = 47µfd*
f = 4MHz

LC Clock
C1, C2 = 22 pf
L =130 µH*
f = 3 MHz*

External Clock

RC Clock
@5V V_{CC} (TYP)
C1 = 44pF*
R = 4K ohm
f = 3 MHz*

*Preliminary value, including pin parasitics
** Device Ground Pin

Figure 12.Oscillator Configuration

Power-On Reset (POR). A timer circuit clocked by a dedicated on-board RC oscillator is used for the Power-On Reset (POR) timer function. The POR time allows V_{CC} and the oscillator circuit to stabilize before instruction execution begins.

The POR timer circuit is a one-shot timer triggered by one of three conditions:

1. Power fail to Power OK status.
2. Stop-Mode Recovery (if D5 of SMR = 1).
3. WDT time-out.

The POR time is specified as TPOR. Bit 5 of the Stop-Mode Register determines whether the POR timer is bypassed after Stop-Mode Recovery (typical for external clock, RC/LC oscillators).

HALT. HALT turns off the internal CPU clock, but not the CRYSTAL oscillation. The counter/timers, analog comparators, and external interrupts IRQ0, IRQ1, IRQ2, and IRQ3 remain active. The devices are recovered by interrupts and are either externally or internally generated. This also includes WDT time-out Reset

Table 19. Counter/Timer 0 Register—T0 F4h/R244 Bank 0h: READ/WRITE

Bit	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset State	X	X	X	X	X	X	X	X
Note: R = Read, W = Write, X = Indeterminate.								

Bit Position	Bit Field	R/W	Reset State	Description
D7–D0	T0	R	X	T0 Current Value
		W	X	T0 automatic Reload Value Range = 1–256 decimal; 01h - 00h

Prescaler 0 Register

The Prescaler 0 Register PRE0 controls clocking functions. WRITE and reset states for bits D7–D0 are listed in Table 20.

Table 20. Prescaler 0 Register—PRE0 F5h/R245 Bank 0h: WRITE ONLY

Bit	D7	D6	D5	D4	D3	D2	D1	D0
R/W	W	W	W	W	W	W	W	W
Reset State	X	X	X	X	X	X	X	0
Note: W = Write, X = Indeterminate.								

Bit Position	Bit Field	R/W	Reset State	Description
D7–D2	Prescaler	W	X	**Prescaler Modulo** Range = 1–64 decimal; 01h–00h
D1	Reserved	W	X	Reserved—must be 0
D0	Count	W	0	**Count Mode** 0: T0 Single Pass 1: T0 Modulo N

Bit Position	Bit Field	R/W	Reset State	Description
D7–D6	Interrupt Edge	R/W	00	**Interrupt Edge** 00: P31 ↓ P32 ↓ 01: P31 ↓ P32 ↑ 10: P31 ↑ P32 ↓ 11: P31 ↑↓ P32 ↑↓
D5	IRQ5	R/W	0	**Interrupt** IRQ5 = T1 0: No Interrupt pending 1: Interrupt pending
D4	IRQ4	R/W	0	**Interrupt** IRQ4 = T0 0: No Interrupt pending 1: Interrupt pending
D3	IRQ3	R/W	0	**Interrupt** IRQ3 = P30 Input 0: No Interrupt pending 1: Interrupt pending
D2	IRQ2	R/W	0	**Interrupt** IRQ2 = P31 Input 0: No Interrupt pending 1: Interrupt pending
D1	IRQ1	R/W	0	**Interrupt** IRQ1 = P33 Input 0: No Interrupt pending 1: Interrupt pending
D0	IRQ0	R/W	0	**Interrupt** IRQ0 = P32 Input 0: No Interrupt pending 1: Interrupt pending

Interrupt Mask Register

The Interrupt Mask Register, IMR, controls interrupt functions. READ/WRITE and reset states for bits D7–D0 are listed in Table 26.

Table 26. Interrupt Mask Register—IMR FBh/R251 Bank 0h: READ/WRITE

Bit	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit Position	Bit Field	R/W	Reset State	Description
D4	Reserved	W	1	**Reserved** 1: Reserved must be "1"
D3	Port 0 I/O	W	1	**Port 0†** 0: Low EMI 1: Standard
D2	Port 0 I/O	W	1	**Port 0** 0: Open-Drain 1: Push-Pull Active
D1	Reserved	W	1	**Reserved** 1: Reserved must be "1"
D0	Port 3	W	0	**Port 3 Comparator Output** 0: P34, P37 Standard Output 1: P34, P37 Comparator Output

Stop-Mode Recovery Register

The Stop-Mode Recovery Register, SMR, controls clocking functions. READ/WRITE and reset states for bits D7–D0 are listed in Table 33.

Table 33. Stop-Mode Recovery Register—SMR 0Bh/R11 Bank Fh:READ/WRITE

Bit	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R	W	W	W	W	W	W	W
Reset	0	0	1	0	0	0	0	0
Note: R = Read, W = Write.								

Bit Position	Bit Field	R/W	Reset State	Description
D7	Stop	R	0	**Stop Flag**[3] 0: POR 1: Stop Recovery
D6	Stop-Mode Recovery	W	0	**Stop-Mode Recovery Level** 0: Low 1: High

Notes:
1. For the Stop-Mode Recovery Source, either SMR or SMR2 can be selected. If SMR is used to select the Stop-Mode Recovery Source, bits D1–D0 of SMR2 must be 0.
2. Cleared by RESET and SMR.
3. Not reset after Stop-Mode Recovery.

Bit Position	Bit Field	R/W	Reset State	Description
D5	Stop Delay	W	1	**Stop Delay** 0: Off 1: On
D4–D2	Stop Mode	W	000	**Stop-Mode Recovery Source**[2] 000: POR only and/or external $\overline{\text{RESET}}$ 001: P30 010: P31 011: P32 100: P33 101: P27 110: P2 NOR 0–3 111: P2 NOR 0–7
D1	Clock	W	0	**External Clock Divide-by-2** 0: SCLK &TCLK = $X_{IN} \div 2$ 1: SCLK &TCLK = X_{IN}
D0	SCLK/TCLK	W	0	**SCLK/TCLK Divide-by-16** 0: Off 1: On

Notes:
1. For the Stop-Mode Recovery Source, either SMR or SMR2 can be selected. If SMR is used to select the Stop-Mode Recovery Source, bits D1–D0 of SMR2 must be 0.
2. Cleared by $\overline{\text{RESET}}$ and SMR.
3. Not reset after Stop-Mode Recovery.

Table 37. DC Electrical Characteristics at Standard Temperature (Continued)

Sym	Parameter	V_{CC1}	T_A = 0°C to +70°C Min	T_A = 0°C to +70°C Max	Typical[2] @25°C	Units	Conditions	Notes
I_{CC1}	Standby Current (HALT mode)	3.0V		4.3	1.5	mA	V_{IN} = 0V, V_{CC} @ 16 MHz	6
		5.5V		7	3.4	mA	V_{IN} = 0V, V_{CC} @ 16 MHz	6
I_{CC2}	Standby Current (STOP Mode)	3.0V		8	2	µA	WDT is not Running	7,8
		5.5V		10	4	µA	WDT is not Running	7,8
		3.0V		500	310	µA	WDT is Running	7,8,9
		5.5V		800	600	µA	WDT is Running	7,8,9
V_{ICR}	Input Common Mode Voltage Range	3.0V	0	V_{CC}–1.0V		V		5
		5.5V	0	V_{CC}–1.0V		V		5
I_{ALL}	Autolatch Low Current	3.0V	0.7	8	3	µA	0V<V_{IN}<V_{CC}	10
		5.5V	1.4	15	5	µA	0V<V_{IN}<V_{CC}	10
I_{ALH}	Autolatch High Current	3.0V	–0.6	–5	–3	µA	0V<V_{IN}<V_{CC}	10
		5.5V	–1.0	–8	–6	µA	0V<V_{IN}<V_{CC}	10

Notes:
1. The V_{CC} voltage specification of 3.0V guarantees 3.3V ±0.3V with typicals at V_{CC} = 3.3V, and the V_{CC} voltage specification of 5.5V guarantees 5.0V ±0.5V with typicals at V_{CC} = 5.0V.
2. Typical voltage is V_{CC} = 5.0V and 3.3V.
3. STANDARD Mode (not Low-EMI Mode).
4. Low-EMI Mode (Not Standard Mode).
5. For analog comparator, inputs when analog comparators are enabled.
6. All outputs unloaded, I/O pins floating, inputs at rail.
7. Same as note 6, except inputs at V_{CC}.
8. Clock must be forced Low, when X_{IN} is clock-driven and X_{OUT} is floating.
9. 0ºC to 70ºC (standard temperature).
10. Autolatch (Mask Option) selected.
11. The V_{LV} voltage increases as the temperature decreases and overlaps lower V_{CC} operating region. See Figure 15.
12. –40°C to 105°C (extended temperature).

Table 38. DC Electrical Characteristics at Extended Temperature (Continued)

Sym	Parameter	V_{CC1}	T_A = –40°C to +105°C Min	Max	Typical[2] @25°C	Units	Conditions	Notes
V_{OL}	Output Low Voltage	3.0V		0.6	0.2	V	I_{OL} = 1.0 mA	4
		5.0V		0.4	0.1	V	I_{OL} = 1.0 mA	4
V_{OL1}	Output Low Voltage	3.0V		0.6	0.2	V	I_{OL} = +4.0 mA	3
		5.5V		0.4	0.1	V	I_{OL} = +4.0 mA	3
V_{OL2}	Output Low Voltage	3.0V		1.2	0.3	V	I_{OL} = +6 mA	3
		5.5V		1.2	0.4	V	I_{OL} = +12 mA	3
V_{OFFSET}	Comparator Input Offset Voltage	3.0V		25	10	mV		5
		5.5V		25	10	mV		5
I_{IL}	Input Leakage	3.0V	–1	2	0.04	µA	V_{IN} = 0V, V_{CC}	
		5.5V	–1	2	0.04	µA	V_{IN} = 0V, V_{CC}	
I_{OL}	Output Leakage	3.0V	–1	2	0.04	µA	V_{IN} = 0V, V_{CC}	
		5.5V	–1	2	0.04	µA	V_{IN} = 0V, V_{CC}	
I_{CC}	Supply Current	3.0V		10	4	mA	@ 4 MHz	6
		5.5V		15	9	mA	@ 4 MHz	6
I_{CC1}	Standby Current (HALT mode)	3.0V		4.3	1.5	mA	V_{IN} = 0V, V_{CC} @ 4 MHz	6
		5.5V		7	3.4	mA	V_{IN} = 0V, V_{CC} @ 4 MHz	6

Notes:
1. The V_{CC} voltage specification of 3.0V guarantees 3.3V ±0.3V with typicals at V_{CC} = 3.3V, and the V_{CC} voltage specification of 5.5V guarantees 5.0V ±0.5V with typicals at V_{CC} = 5.0V.
2. Typical voltage is V_{CC} = 5.0V and 3.3V.
3. STANDARD Mode (not Low-EMI Mode).
4. Low-EMI Mode (Not Standard Mode).
5. For analog comparator, inputs when analog comparators are enabled.
6. All outputs unloaded, I/O pins floating, inputs at rail.
7. Same as note 6, except inputs at V_{CC}.
8. Clock must be forced Low, when X_{IN} is clock-driven and X_{OUT} is floating.
9. 0ºC to 70ºC (standard temperature).
10. Autolatch (Mask Option) selected.
11. The V_{LV} voltage increases as the temperature decreases and overlaps lower V_{CC} operating region. See Figure 15.
12. –40°C to 105°C (extended temperature).

Table 39. Additional Timing at Standard Temperature

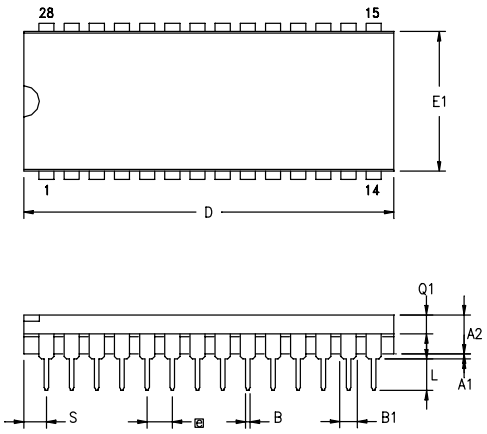
				T_A = 0ºC to +70ºC 4 MHz				
No	**Sym**	**Parameter**	**V_{CC}[1]**	**Min**	**Max**	**Units**	**Notes**	**D1,D0**
1	T_PC	Input Clock Period	3.0V	250	DC	ns	2,3,4	
			5.5V	250	DC	ns	2,3,4	
2	T_RC, T_FC	Clock Input Rise & Fall Times	3.0V		25	ns	2,3	
			5.5V		25	ns	2,3	
3	T_WC	Input Clock Width	3.0V	125		ns	2,3,4	
			5.5V	125		ns	2,3,4	
4	$T_WT_{IN}L$	Timer Input Low Width	3.0V	100		ns	2,3	
			5.5V	70		ns	2,3	
5	$T_WT_{IN}H$	Timer Input High Width	3.0V	$3T_PC$			2,3	
			5.5V	$3T_PC$			2,3	
6	T_PT_{IN}	Timer Input Period	3.0V	$4T_PC$			2,3	
			5.5V	$4T_PC$			2,3	
7	T_RT_{IN}, T_FT_{IN}	Timer Input Rise & Fall Timer	3.0V		100	ns	2,3	
			5.5V		100	ns	2,3	
8A	T_WIL	Interrupt Request Low Time	3.0V	100		ns	2,3,5	
			5.5V	70		ns	2,3,5	
8B	T_WIL	Interrupt Request Low Time	3.0V	$3T_PC$			2,3,6	
			5.5V	$3T_PC$			2,3,6	

Notes:
1. The V_{CC} voltage specification of 3.0V guarantees 3.3V ±0.3V, and the V_{CC} voltage specification of 5.5V guarantees 5.0V ±0.5V.
2. Timing reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
3. SMR: D1 = 0.
4. The maximum frequency for the external crystal clock is 4 MHz when using LOW-EMI OSCILLATOR mode.
5. The interrupt request via Port 3 (P31–P33).
6. The interrupt request via Port 3 (P30).
7. SMR: D5 = 1, and the POR Stop-Mode Delay is on.
8. For RC and LC oscillators, and for an oscillator driven by a clock driver.
9. The D1,D0 column applies to the Watch-Dog Timer Mode Register tap selection.
10. 12 µs is the typical delay time; only applies when SMR Register bit D5 is cleared to 0

Table 40. Additional Timing at Extended Temperature

				T_A = –40ºC to +105ºC 4 MHz				
No	**Sym**	**Parameter**	**V_{CC}[1]**	**Min**	**Max**	**Units**	**Notes**	**D1,D0**
1	T_PC	Input Clock Period	3.0V	250	DC	ns	2,3,4	
			5.5V	250	DC	ns	2,3,4	
2	T_RC, T_FC	Clock Input Rise & Fall Times	3.0V		25	ns	2,3	
			5.5V		25	ns	2,3	
3	T_WC	Input Clock Width	3.0V	125		ns	2,3,4	
			5.5V	125		ns	2,3,4	
4	$T_WT_{IN}L$	Timer Input Low Width	3.0V	100		ns	2,3	
			5.5V	70		ns	2,3	
5	$T_WT_{IN}H$	Timer Input High Width	3.0V	$3T_PC$			2,3	
			5.5V	$3T_PC$			2,3	
6	T_PT_{IN}	Timer Input Period	3.0V	$4T_PC$			2,3	
			5.5V	$4T_PC$			2,3	
7	T_RT_{IN}, T_FT_{IN}	Timer Input Rise & Fall Timer	3.0V		100	ns	2,3	
			5.5V		100	ns	2,3	
8A	T_WIL	Interrupt Request Low Time	3.0V	100		ns	2,3,5	
			5.5V	70		ns	2,3,5	
8B	T_WIL	Interrupt Request Low Time	3.0V	$3T_PC$			2,3,6	
			5.5V	$3T_PC$			2,3,6	

Notes:
1. The V_{CC} voltage specification of 5.5V guarantees 5.0V ±0.5V.
2. The timing reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
3. SMR: D1 = 0.
4. The maximum frequency for the external crystal clock is 4 MHz when using LOW-EMI OSCILLATOR mode.
5. The interrupt request via Port 3 (P31–P33).
6. The interrupt request via Port 3 (P30).
7. SMR: D5 = 1, and the POR Stop-Mode Delay is on.
8. For RC and LC oscillators, and for an oscillator driven by a clock driver.
9. The D1,D0 column applies to the Watch-Dog Timer Mode Register tap selection.
10. 12 µs is the typical delay time.



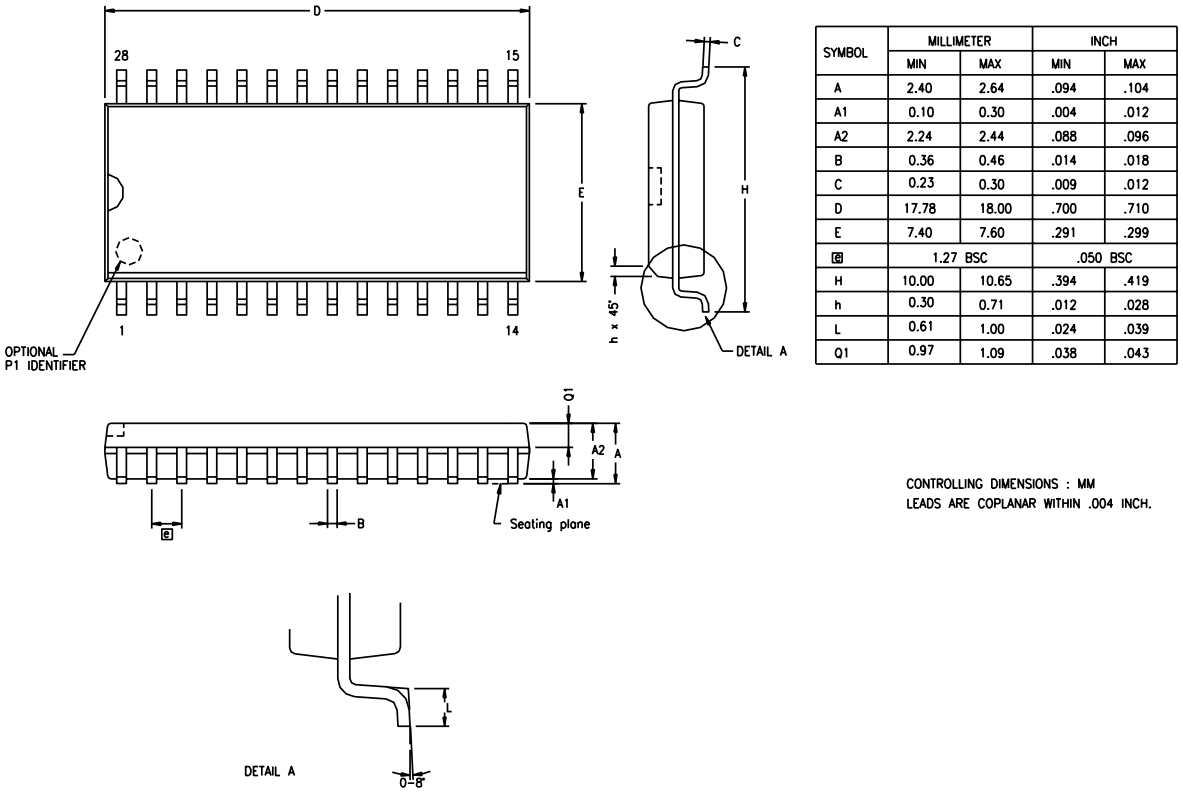
SYMBOL	OPT #	MILLIMETER		INCH	
		MIN	MAX	MIN	MAX
A1		0.38	1.02	.015	.040
A2		3.18	4.19	.125	.165
B		0.38	0.53	.015	.021
B1	01	1.40	1.65	.055	.065
	02	1.14	1.40	.045	.055
C		0.23	0.38	.009	.015
D	01	36.58	37.34	1.440	1.470
	02	35.31	35.94	1.390	1.415
E		15.24	15.75	.600	.620
E1	01	13.59	14.10	.535	.555
	02	12.83	13.08	.505	.515
e		2.54 TYP		.100 TYP	
eA		15.49	16.76	.610	.660
L		3.05	3.81	.120	.150
Q1	01	1.40	1.91	.055	.075
	02	1.40	1.78	.055	.070
S	01	1.52	2.29	.060	.090
	02	1.02	1.52	.040	.060

CONTROLLING DIMENSIONS : INCH

OPTION TABLE	
OPTION #	PACKAGE
01	STANDARD
02	IDF

Figure 18.28-Pin DIP Package Diagram

Figure 19 illustrates the 28-pin SOIC package.



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	2.40	2.64	.094	.104
A1	0.10	0.30	.004	.012
A2	2.24	2.44	.088	.096
B	0.36	0.46	.014	.018
C	0.23	0.30	.009	.012
D	17.78	18.00	.700	.710
E	7.40	7.60	.291	.299
e	1.27 BSC		.050 BSC	
H	10.00	10.65	.394	.419
h	0.30	0.71	.012	.028
L	0.61	1.00	.024	.039
Q1	0.97	1.09	.038	.043

Figure 19.28-Pin SOIC Package Diagram

Ordering Information

Table 42. Ordering Information

Temperature	Speed (4MHz)	Pin Count	Package	Order Number*
Standard	4	28	DIP	Z87C3304PSC
Standard	4	28	SOIC	Z87C3304SSC
Extended	4	28	DIP	Z87C3304PEC

Table 42. Ordering Information

Temperature	Speed (4MHz)	Pin Count	Package	Order Number*
Extended	4	28	SOIC	Z87C3304SEC

Note: *The Standard temperature range is 0ºC to 70ºC. For parts that operate in the Extended temperature range of –40ºC to 105ºC, substitute the letter E for the letter S. For example, the Order Number for a 28-pin DIP operating in the Extended temperature range is Z87C3304PEC.

For fast results, contact your local ZiLOG sale office for assistance in ordering the part(s) desired.

Part Number Description

ZiLOG part numbers consist of a number of components. For example, part number Z87C3304PEC is a 4-MHz 28-pin DIP that operates in the –40ºC to +105ºC temperature range, with Plastic Standard Flow. The Z87C3304PEC part number corresponds to the code segments indicated in the following table.

Z	ZiLOG Prefix
86	Z8 Product
C	ROM Product
33	Product Number
04	Speed (MHz)
P	Package
E	Temperature
C	Environmental Flow

For fast results, contact your local ZiLOG sales office for assistance in ordering the part required.

Precharacterization Product

The product represented by this document is newly introduced and ZiLOG has not completed the full characterization of the product. The document states what ZiLOG knows about this product at this time, but additional features or non-conformance with some aspects of the document may be found, either by ZiLOG or its customers in the course of further application and characterization work. In addition, ZiLOG cautions that delivery may be uncertain at times, due to start-up yield issues.

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Document Information

Document Number Description

The Document Control Number that appears in the footer of each page of this document contains unique identifying attributes, as indicated in the following table:

PS	Product Specification
00156	Unique Document Number
01	Revision Number
1003	Month and Year Published

Customer Feedback Form

Z87C33 Product Specification

If you experience any problems while operating this product, or if you note any inaccuracies while reading this Product Specification, please copy and complete this form, then mail or fax it to ZiLOG (see *Return Information*, below). We also welcome your suggestions!

Customer Information

Name	Country
Company	Phone
Address	Fax
City/State/Zip	E-Mail