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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	24
Program Memory Size	4KB (4K x 8)
Program Memory Type	ROM
EEPROM Size	-
RAM Size	236 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.600", 15.24mm)
Supplier Device Package	28-DIP
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z87c3304pecr53a8

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Architectural Overview

ZiLOG’s large Z8® family of 8-bit microcontrollers now includes the Z87C33 product line, featuring an enhanced wake-up circuitry, programmable Watch-Dog Timers (WDT), and low-noise/EMI options. These enhancements to the Z8 offers a more efficient, cost-effective design and provides the user with increased design flexibility over the standard Z8 microcontroller core. The low-power-consumption CMOS microcontroller offers fast execution, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, and easy hardware/software system expansion.

The Z87C33 subfamily features an Expanded Register File (ERF) to allow access to register-mapped peripheral and I/O circuits. Four basic address spaces are available to support this wide range of configurations: Program Memory, Register File, and ERF. The Register File is composed of 237 bytes of general-purpose registers, three I/O port registers, 15 control and status registers. The ERF consists of four control registers.

For applications demanding powerful I/O capabilities, the Z87C33 offers 24 pins dedicated to input and output. These lines are configurable under software control.

The Z87C33 family operates at 4 MHz with a voltage range of 3.0 to 5.5 V_{DC}.

To unburden the system from coping with real-time tasks such as counting/timing, the Z8 offers two on-chip counter/timers with a large number of user-selectable modes.

Note: All signals with an overline are active Low. For example, B/$\overline{W}$, for which WORD is active Low, and $\overline{B}$/W, for which BYTE is active Low.

Power connections follow these conventional descriptions:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

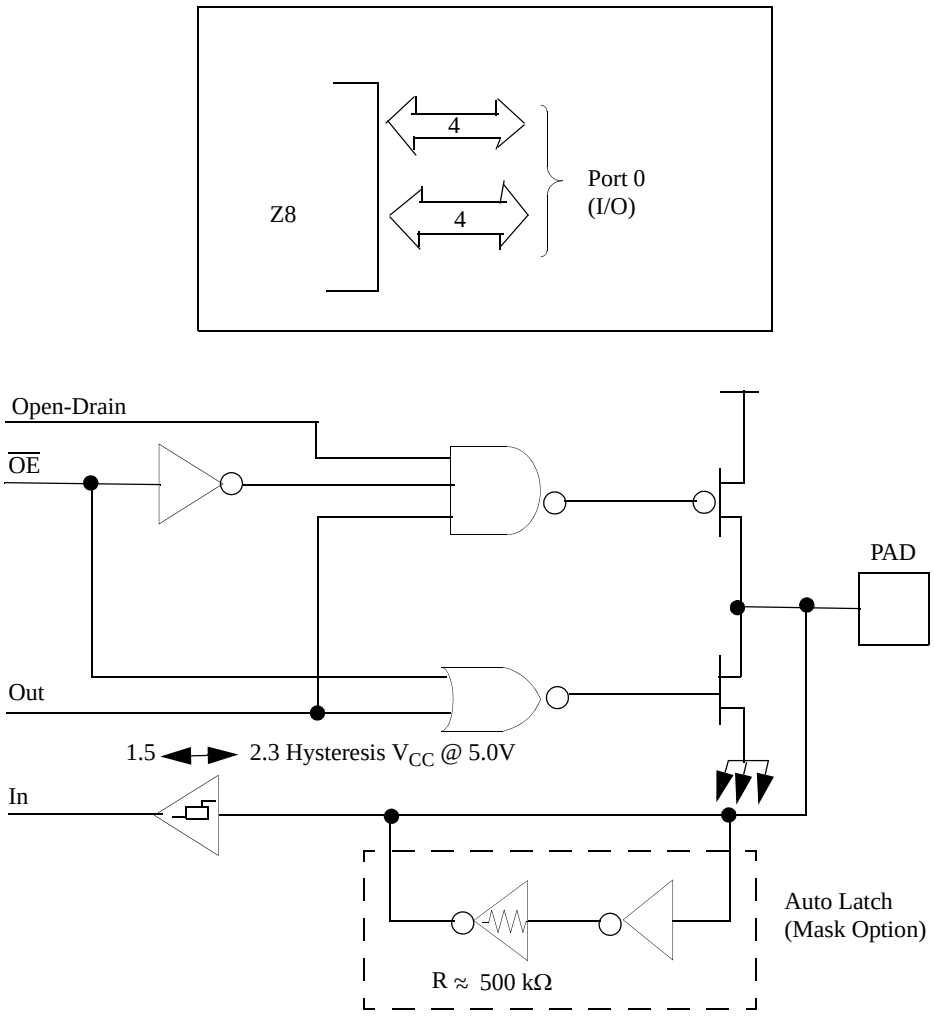

Figure 3. Port 0 Configuration

Port 2 (P27–P20). Port 2 is an 8-bit, bidirectional, CMOS-compatible I/O port. These eight I/O lines are configured under software control as an input or output, independently. Port 2 is always available for I/O operation. The input buffers are Schmitt-triggered. Bits programmed as outputs may be globally programmed as either push-pull or open-drain. Low-EMI output buffers are globally programmed by the software. See Figure 5.

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority register. An interrupt machine cycle activates when an interrupt request is granted. This action disables all subsequent interrupts, saves the Program Counter and Status Flags, and then branches to the program memory vector location reserved for that interrupt.

All Z8 interrupts are vectored through locations in the program memory. This memory location and the next byte contain the 16-bit address of the interrupt service routine for that particular interrupt request. To accommodate polled interrupt systems, interrupt inputs are masked and the Interrupt Request register is polled to determine which of the interrupt requests require service.

When in ANALOG mode, an interrupt resulting from AN1 maps to IRQ2, and an interrupt from AN2 maps to IRQ0. Interrupts IRQ2 and IRQ0 may be rising, falling, or both edge-triggered, and are programmed in the IRQ register. The software polls to identify the state of the pin. When in ANALOG mode, IRQ1 is generated by the Stop-Mode Recovery source selected by SMR Register bits D4, D3, D2, or SMR2 D1 or D0.

Programming bits for the Interrupt Edge Select are located in the IRQ register, bits D7 and D6. The configuration is indicated in Table 7.

Table 6. IRQ Register*

IRQ		Interrupt Edge	
D7	**D6**	**P31**	**P32**
0	0	F	F
	1	F	R
1	0	R	F
1	1	R/F	R/F

Notes:
F = Falling Edge
R = Rising Edge

Clock. The Z8 on-chip oscillator features a high-gain, parallel-resonant amplifier for connection to a crystal, LC, RC, ceramic resonator, or any suitable external clock source (X_{IN} = INPUT, X_{OUT} = OUTPUT). The crystal should be AT-cut, 4 MHz maximum, with a series resistance (RS) of less than or equal to 100Ω when oscillating from 1MHz to 4MHz.

The crystal should be connected across XTAL1 and XTAL2 using the vendor’s recommended capacitor values from each pin directly to the device Ground pin to reduce ground-noise injection into the oscillator. The RC oscillator option is mask-

and V_{LV} Reset. An interrupt request must be enabled and executed to exit HALT mode. After the interrupt service routine, the program continues from the instruction after the HALT.

In order to enter STOP (or HALT) mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. The user must execute a NOP (Op Code = FFh) immediately before the appropriate sleep instruction. For example:

```
FF    NOP    ; clear the pipeline
6F    STOP   ; enter STOP mode
```

or

```
FF    NOP    ; clear the pipeline
7F    HALT   ; enter HALT mode
```

STOP. This instruction turns off the internal clock and external crystal oscillation. The STOP instruction also reduces the standby current to 10 µA or less. The analog comparators are automatically powered down in STOP-Mode. STOP mode is terminated either by WDT time-out, POR, Stop-Mode Recovery, or any Reset. As a result, the processor restarts the application program at address 000Ch. A WDT time-out in STOP mode affects all registers the same as if a Stop-Mode Recovery occurred via a selected Stop-Mode Recovery source except that the POR delay is enabled even if the delay is selected for disable.

Note: If a permanent WDT is selected, the WDT runs in all modes and cannot be stopped or disabled if the onboard RC oscillator is selected to drive the WDT.

Port Configuration Register (PCON). The PCON register configures the ports individually; comparator output on Port 3, open-drain on Port 0 and Port 1, low EMI on Ports 0, 1, 2, and 3, and low-EMI oscillator. The PCON register is located in the expanded register file at Bank F, location 00h (Table 8).

Table 7. Port Configuration Register—PCON 00h/R0 Bank Fh: WRITE ONLY

Bit	D7	D6	D5	D4	D3	D2	D1	D0
R/W	W	W	W	W	W	W	W	W
Reset	1	1	1	1	1	1	1	0
Note: R = Read, W = Write, X = Indeterminate.								

Bit Position	Bit Field	R/W	Reset State	Description
D7	Oscillator	W	1	**Low-EMI Oscillator** 0: Low EMI 1: Standard
D6	Port 3 I/O	W	1	**Port 3** 0: Low EMI 1: Standard
D5	Port 2 I/O	W	1	**Port 2** 0: Low EMI 1: Standard
D4	Reserved	W	1	**Reserved*** 1: Must be "1"
D3	Port 0 I/O	W	1	**Port 0*** 0: Low EMI 1: Standard
D2	Port 0 I/O	W	1	**Port 0** 0: Open-Drain 1: Push-Pull Active
D1	Reserved	W	1	**Reserved*** 1: Must be "1"
D0	Port 3	W	0	**Port 3 Comparator Output** 0: P34, P37 Standard Output 1: P34, P37 Comparator Output

Comparator Output Port 3 (D0). Bit 0 controls the comparator use in Port 3. A 1 in this location brings the comparator outputs to P34 and P37, and a 0 releases the Port to its standard I/O configuration. The default value is 0.

Port 0 Open-Drain (D2). Port 0 is configured as an open-drain by resetting this bit (D2 = 0) or configured as push-pull active by setting this bit (D2 = 1). The default value is 1.

Low-EMI Port 0 (D3). Port 0 is configured as a low-EMI port by resetting this bit (D3 = 0) or configured as a Standard Port by setting this bit (D3 = 1). The default value is 1.

Low-EMI Port 2 (D5). Port 2 is configured as a low-EMI port by resetting this bit (D5 = 0) or configured as a Standard Port by setting this bit (D5 = 1). The default value is 1.

Low-EMI Port 3 (D6). Port 3 is configured as a low-EMI port by resetting this bit (D6 = 0) or configured as a Standard Port by setting this bit (D6 = 1). The default value is 1.

Low-EMI OSC (D7). This bit of the PCON register controls the low-EMI noise oscillator. A 1 in this location configures the oscillator, $\overline{DS}$, $\overline{AS}$ and R/$\overline{W}$ with standard drive, while a 0 configures the oscillator, $\overline{DS}$, $\overline{AS}$ and R/$\overline{W}$ with low noise drive. LOW-EMI mode reduces the drive of the oscillator (OSC). The default value is 1.

Note: Maximum external clock frequency of 4 MHz when running in LOW-EMI OSCILLATOR mode.

Low-EMI Emission. The Z8 is programmed to operate in a low-EMI emission mode in the PCON register. The oscillator and all I/O ports is programmed as LOW-EMI EMISSION mode independently. Use of this feature results in:

- The pre-drivers slew rate reduced to 10 ns (typical)
- Low-EMI output drivers exhibit resistance of 200Ω (typical)
- Low-EMI Oscillator
- Internal SCLK = X_{IN} operation limited to a maximum of 4 MHz–250 ns cycle time, when LOW EMI OSCILLATOR is selected and system clock (SMR Register Bit D1 = 1)

Stop-Mode Recovery Registers (SMR1 and SMR2). These registers select the clock divide value and determine the mode of Stop-Mode Recovery (Tables 8 and 11). All bits are WRITE ONLY, except bit 7 of SMR1, which is READ ONLY. SMR1 bit 7 is a flag bit that is set by hardware on a Stop-Mode Recovery condition and reset by a power-on cycle. For SMR1, bit 6 controls whether a Low level or a High level is required from the recovery source. Bit 5 controls the reset delay after Stop-Mode Recovery. Bits 2, 3, and 4 of the SMR1 register specify the source of the Stop-Mode Recovery signal. Bits 0 and 1 determine the time-out period of the WDT. The SMR registers are located in Bank F of the Expanded Register File at addresses `0Bh` and `0Dh`, respectively.

For SMR2, bits 7 to 2 are reserved. Bits 1 and 0 of the SMR2 register specify the source of the Stop-Mode Recovery signal.

Table 8. Stop-Mode Recovery Register 1—SMR1 0Bh/R11 Bank Fh: WRITE ONLY, except Bit D7, which is READ ONLY

Bit	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R	W	W	W	W	W	W	W

External Clock Divide-by-Two (D1). This bit can eliminate the oscillator divide-by-two circuitry. When this bit is 0, the system clock (SCLK) and timer clock (TCLK) are equal to the external clock frequency divided by 2. The SCLK is equal to the external clock frequency when this bit is set (D1 = 1). Using this bit together with D7 of PCON further helps lower EMI (that is, D7 (PCON) = 0, D1 (SMR) = 1). The default setting is 0. Maximum external clock frequency is 4 MHz when SMR bit D1 = 1 where SCLK & TCLK = X_{IN}.

Stop-Mode Recovery Source (D2, D3, and D4). These three bits of the SMR specify the wake-up source of the Stop-Mode Recovery (Figure and Stop-Mode Recovery Source). When the Stop-Mode Recovery Sources are selected in this register, then SMR2 register bits D0,D1 must be set to 0.

Note: If the Port 2 pin is configured as an output, this output level is read by the SMR circuitry.

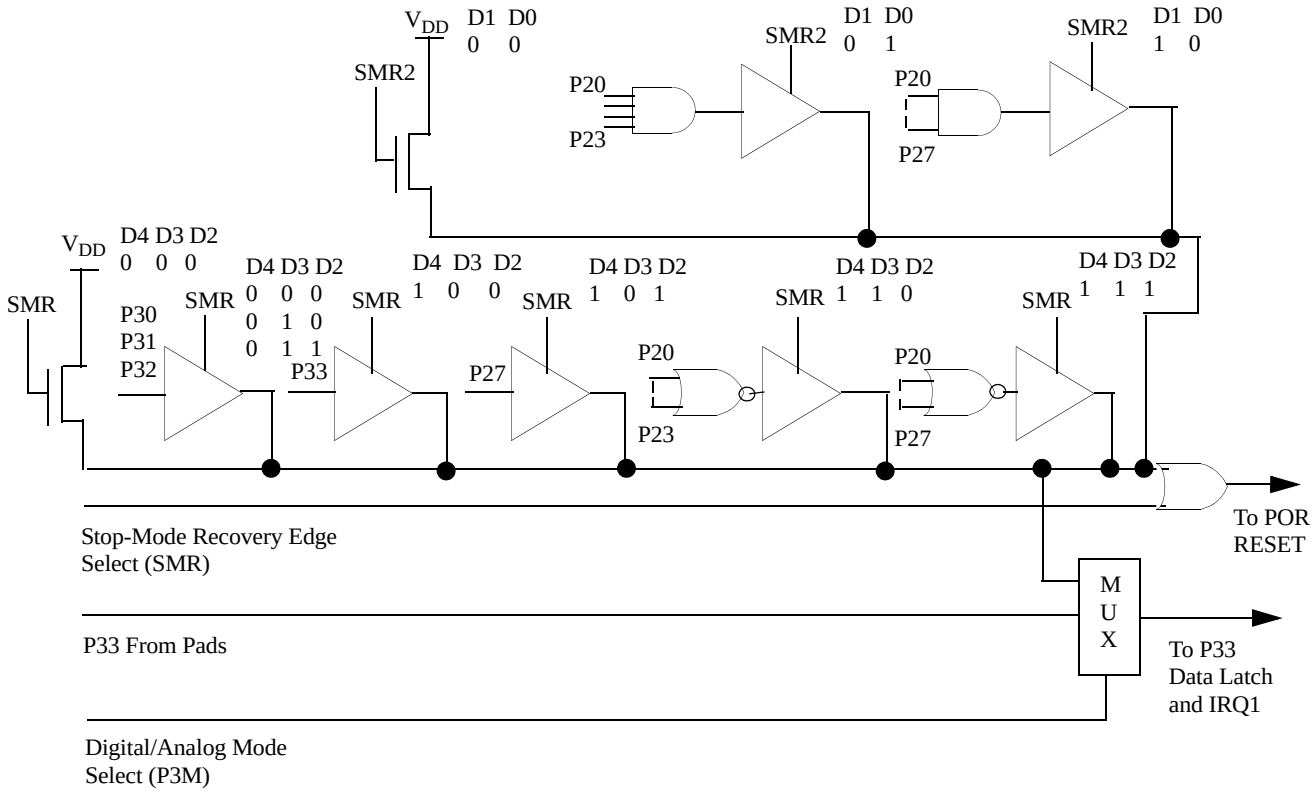

Figure 13.Stop-Mode Recovery Source

Table 12. Watch-Dog Timer Mode Register—WDTMR 0Fh/R15: WRITE ONLY

Bit	D7	D6	D5	D4	D3	D2	D1	D0
R/W	W	W	W	W	W	W	W	W
Reset	X	X	X	0	1	1	0	1
Note: R = Read, W = Write, X = Indeterminate.								

Bit/ Field	Bit Position	R/W	Reset State	Description
D7–D5	Reserved	W	X	Reserved—must be 0
D4	X_{IN}	W	0	**XIN/INT RC Select for WDT** 0: On-Board RC 1: X_{IN}
D3	WDT	W	1	WDT During STOP
D2	WDT	W	1	WDT During HALT
D1–D0	WDT Tap	W	01	**WDT Tap Int RC OSC System Clock** 00: 3.5 ms 128 SCLK 01: 7.0 ms 256 SCLK 10: 14.0 ms 512 SCLK 11: 56.0 ms 2048 SCLK

Note: Not used in conjunction with SMR Source.

WDT Time Select (D0,D1). Selects the WDT time period and is configured as indicated in Table 14.

Table 13. WDT Time Select

D1	D0	Timeout of Internal RC OSC	Timeout of System Clock
0	0	3.5 ms min	128 SCLK
0	1	7 ms min	256 SCLK
1	0	14 ms min	512 SCLK
1	1	56 ms min	2048 SCLK

Note: SCLK = system bus clock cycle. The default on RESET is 7 ms. Values provided are for V_{CC} = 5.0V.

WDTMR During HALT (D2). This bit determines whether or not the WDT is active during HALT mode. A 1 indicates active during HALT. The default is 1.

WDTMR During STOP (D3). This bit determines whether or not the WDT is active during STOP mode. Because the X_{IN} clock is stopped during STOP mode, the on-board RC must be selected as the clock source to the POR counter. A 1 indicates active during STOP. The default is 1.

Note: If the permanent WDT programming option is selected, the WDT runs in all modes and cannot be stopped or disabled if the on board RC oscillator is selected as the clock source for WDT.

Clock Source for WDT (D4). This bit determines which oscillator source is used to clock the internal POR and WDT counter chain. If the bit is a 1, the internal RC oscillator is bypassed and the POR and WDT clock source is driven from the external pin, X_{IN}. The default configuration of this bit is 0 which selects the internal RC oscillator.

WDTMR Register Accessibility. The WDTMR register is accessible only during the first 64 internal system clock cycles from the execution of the first instruction after Power-On Reset, Watch-Dog Reset, or Stop-Mode Recovery. After this point, the register cannot be modified by any means, intentional or otherwise. The WDTMR cannot be read and is located in Bank Fh of the Expanded Register File at address location 0Fh (Figure 14).

Note: The WDT is permanently enabled (automatically enabled after RESET) through a programmable option. The option is selected when the device is programmed. In this mode, WDT is always activated when the device comes out of RESET. Execution of the WDT instruction serves to refresh the WDT time-out period. WDT operation in the HALT and STOP modes is controlled by WDTMR programming. If this option is not selected when the device is programmed, the WDT must be activated by the user through the WDT instruction and is always disabled by any reset to the device.

Table 16. Timer Mode Register—TMR F1h/R241 Bank 0h: READ/WRITE

Bit	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset State	0	0	0	0	0	0	0	0
Note: R = Read, W = Write.								

Bit Position	Bit Field	R/W	Reset State	Description
D7–D6	T_{OUT} Mode	R/W	00	**T_{OUT} Mode** 00: Off 01: T0 Output 10: T1 Output 11: Internal Clock Output
D5–D4	T_{IN} Mode	R/W	00	**T_{IN} Mode** 00: External Clock Input 01: Gate Input 10: Trigger Input (nonretriggerable) 11: Trigger Input (retriggerable)
D3	T1 Count	R/W	0	**T1 Count** 0: Disable 1: Enable
D2	T1	R/W	0	**T1** 0: No Function 1: Load T1
D1	T0 Count	R/W	0	**T0 Count** 0: Disable 1: Enable
D0	T0	R/W	0	**T0** 0: No Function 1: Load T0

Counter/Timer 1 Register

The Counter/Timer 1 Register, T1, controls timing and counter functions. READ/WRITE and reset states for bits D7–D0 are listed in Table 17.

Table 17. Counter/Timer 1 Register—T1 F2h/R242 Bank 0h: READ/WRITE

Bit	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 26. Interrupt Mask Register—IMR FBh/R251 Bank 0h: READ/WRITE

Reset	0	X	X	X	X	X	X	X
Note: R = Read, W = Write, X = Indeterminate.								

Bit Position	Bit Field	R/W	Reset State	Description
D7	MIE	R/W	0	**Master Interrupt Enable** 1: Enable interrupts 0: Disable interrupts
D6	RAM Protect	R/W	X	**RAM Protect** 1: Enable RAM Protect* 0: Disable RAM Protect
D5–D0	IRQ5–IRQ0	R/W	X	**Interrupt Request** 1: Enable IRQ0–IRQ5 0: Disable IRQ0–IRQ5
Note: * Must select RAM Protect Mask Option				

Flags Register

The CPU sets flags in the Flags Register, FLAGS, to allow the user to perform tests based on differing logical states. READ/WRITE and reset states for bits D7–D0 are listed in Table 27.

Table 27. Flags Register—FLAGS FCh/R252 Bank 0h: READ/WRITE

Bit	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	X	X	X	X	X	X	X	X
Note: R = Read, W = Write, X = Indeterminate.								

Bit Position	Bit Field	R/W	Reset State	Description
D7	Carry	R/W	X	Carry Flag
D6	Zero	R/W	X	Zero Flag
D5	Sign	R/W	X	Sign Flag
D4	Overflow	R/W	X	Overflow Flag
D3	Decimal Adjust	R/W	X	Decimal Adjust Flag
D2	Half Carry	R/W	X	Half Carry Flag

Note: *Not affected by $\overline{\text{RESET}}$.

Bit Position	Bit Field	R/W	Reset State	Description
D1	User	R/W	X	User Flag F2*
D0	User	R/W	X	User Flag F1*

Note: *Not affected by $\overline{\text{RESET}}$.

Register Pointer Register

The Register Pointer Register, RP, controls pointer functions in the working registers. READ/WRITE and reset states for bits D7–D0 are listed in Table 28.

Table 28. Register Pointer—RP FDh/R253 Bank 0h: READ/WRITE

Bit	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Note: R = Read, W = Write.								

Bit Position	Bit Field	R/W	Reset State	Description
D7–D4	Working Register Pointer	R/W	0	Working Register Pointer
D3–D0	Expanded Register File Bank	R/W	0	Expanded Register File Bank

General Purpose Register

The General Purpose Register (GPR) READ/WRITE and reset states for bits D7–D0 are listed in Table 29.

Table 29. General Purpose—GPR FEh/R254 Bank 0h: READ/WRITE

Bit	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Note: R = Read, W = Write.								

Table 31. Expanded Register File Registers—Reset States (Continued)

		D7	D6	D5	D4	D3	D2	D1	D0
07h	Reserved								
08h	Reserved								
09h	Reserved								
0Ah	Reserved								
0Bh	SMR**	0	0	1	0	0	0	0	0
0Ch	Reserved								
0Dh	SMR2*	X	X	X	X	X	X	0	0
0Eh	Reserved								
0Fh	WDTMR*	X	X	X	0	1	1	0	1

Note: *Not reset with a Stop-Mode Recovery.
Note: **Not reset with a Stop-Mode Recovery except Bit D7.

Port Configuration Register

The Port Configuration Register, PCON, controls the configurations of Ports 0, 2, and 3. WRITE and reset states for bits D7–D0 are listed in Table 32.

Table 32. Port Configuration Register—PCON 00h/R0 Bank Fh: WRITE ONLY

Bit	D7	D6	D5	D4	D3	D2	D1	D0
R/W	W	W	W	W	W	W	W	W
Reset	1	1	1	1	1	1	1	0
Note: W = Write.								

Bit Position	Bit Field	R/W	Reset State	Description
D7	Oscillator	W	1	**Low-EMI Oscillator** 0: Low EMI 1: Standard
D6	Port 3 I/O	W	1	**Port 3** 0: Low EMI 1: Standard
D5	Port 2 I/O	W	1	**Port 2** 0: Low EMI 1: Standard

Table 36. Absolute Maximum Ratings (Continued)

Parameter	Min	Max	Units	Notes
Maximum Allowable Current out of V_{SS}		220	mA	
Maximum Allowable Current into V_{DD}		180	mA	
Maximum Allowable Current into an Input Pin	–600	+600	µA	3
Maximum Allowable Current into an Open-Drain Pin	–600	+600	µA	4
Maximum Allowable Output Current Sunk by Any I/O Pin		25	mA	
Maximum Allowable Output Current Sourced by Any I/O Pin		25	mA	

Notes:
1. Applies to all pins except Crystal pins and where otherwise noted.
2. There is no input protection diode from pin to V_{DD} and current into pin is limited to ±600 µA.
3. Excludes X_{IN} and X_{OUT} pins.
4. Device pin is not at an output Low state.

Total power dissipation should not exceed 1.21 W for the package. Power dissipation is calculated as follows:

$$\text{Total Power Dissipation} = V_{DD} \times [I_{DD} - (\text{sum of } I_{OH}), + \text{sum of } [(V_{DD} - V_{OH}) \times I_{OH}] + \text{sum of } (V_{OL} \times I_{OL})$$

Table 37. DC Electrical Characteristics at Standard Temperature (Continued)

Sym	Parameter	V_{CC1}	T_A = 0°C to +70°C Min	T_A = 0°C to +70°C Max	Typical[2] @25°C	Units	Conditions	Notes
I_{CC1}	Standby Current (HALT mode)	3.0V		4.3	1.5	mA	V_{IN} = 0V, V_{CC} @ 16 MHz	6
		5.5V		7	3.4	mA	V_{IN} = 0V, V_{CC} @ 16 MHz	6
I_{CC2}	Standby Current (STOP Mode)	3.0V		8	2	µA	WDT is not Running	7,8
		5.5V		10	4	µA	WDT is not Running	7,8
		3.0V		500	310	µA	WDT is Running	7,8,9
		5.5V		800	600	µA	WDT is Running	7,8,9
V_{ICR}	Input Common Mode Voltage Range	3.0V	0	V_{CC}–1.0V		V		5
		5.5V	0	V_{CC}–1.0V		V		5
I_{ALL}	Autolatch Low Current	3.0V	0.7	8	3	µA	0V<V_{IN}<V_{CC}	10
		5.5V	1.4	15	5	µA	0V<V_{IN}<V_{CC}	10
I_{ALH}	Autolatch High Current	3.0V	–0.6	–5	–3	µA	0V<V_{IN}<V_{CC}	10
		5.5V	–1.0	–8	–6	µA	0V<V_{IN}<V_{CC}	10

Notes:
1. The V_{CC} voltage specification of 3.0V guarantees 3.3V ±0.3V with typicals at V_{CC} = 3.3V, and the V_{CC} voltage specification of 5.5V guarantees 5.0V ±0.5V with typicals at V_{CC} = 5.0V.
2. Typical voltage is V_{CC} = 5.0V and 3.3V.
3. STANDARD Mode (not Low-EMI Mode).
4. Low-EMI Mode (Not Standard Mode).
5. For analog comparator, inputs when analog comparators are enabled.
6. All outputs unloaded, I/O pins floating, inputs at rail.
7. Same as note 6, except inputs at V_{CC}.
8. Clock must be forced Low, when X_{IN} is clock-driven and X_{OUT} is floating.
9. 0ºC to 70ºC (standard temperature).
10. Autolatch (Mask Option) selected.
11. The V_{LV} voltage increases as the temperature decreases and overlaps lower V_{CC} operating region. See Figure 15.
12. –40°C to 105°C (extended temperature).

AC Electrical Characteristics

The timing characteristics with respect to external input/output sources are provided in the following pages.

Additional Timing

Figure 16 illustrates the timing characteristics with respect to system clock functions. See Tables 39 and 40 for descriptions of the numbered timing parameters in the figure.

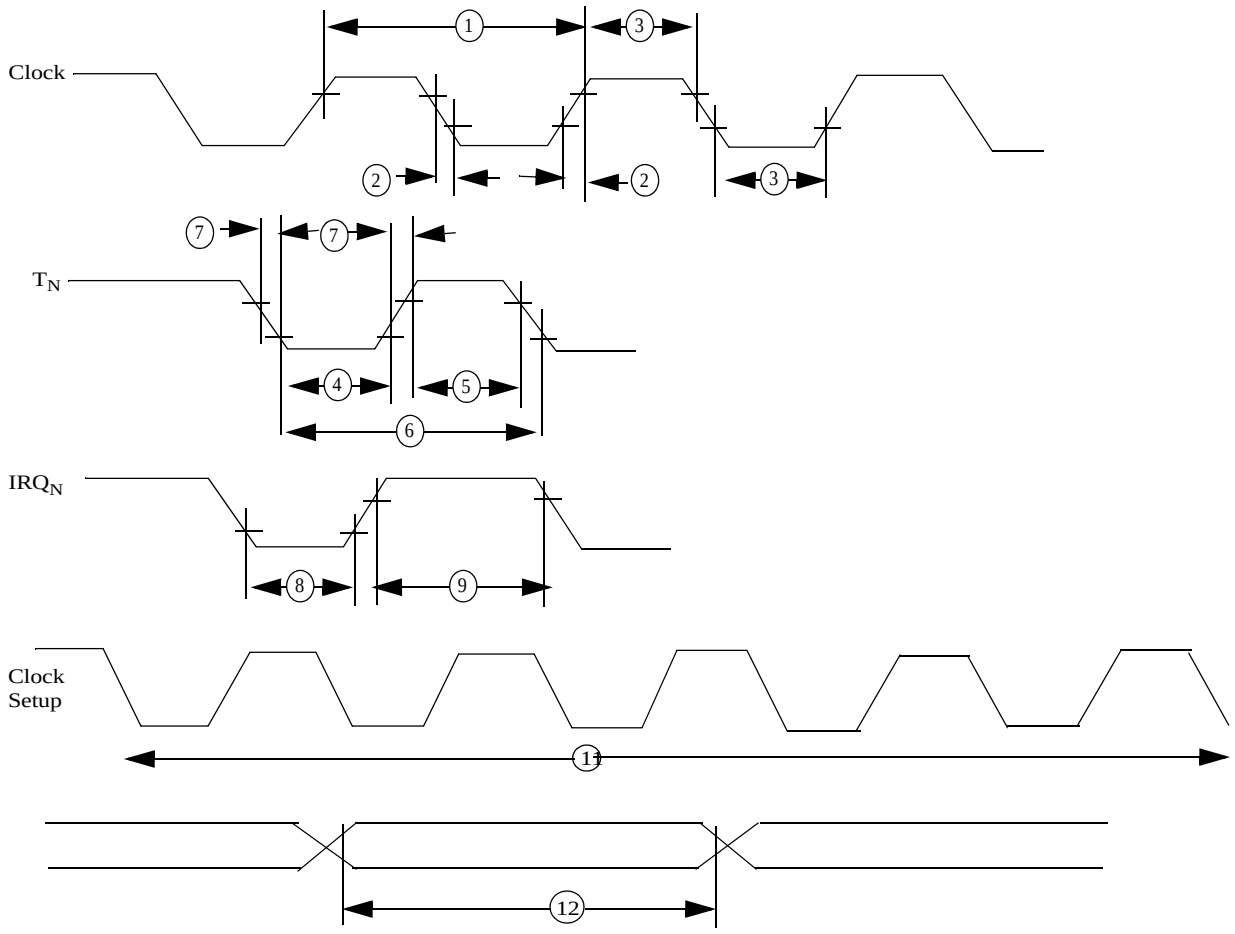

Figure 16.Additional Timing

The values presented in Table 39 are within a standard temperature range of 0ºC to 70ºC.

Table 40. Additional Timing at Extended Temperature (Continued)

				T_A = –40ºC to +105ºC 4 MHz				
No	**Sym**	**Parameter**	**V_{CC}[1]**	**Min**	**Max**	**Units**	**Notes**	**D1,D0**
9	T_WIH	Interrupt Request Input High Time	3.0V	$3T_PC$			2,3,5	
			5.5V	$3T_PC$			2,3,5	
10	T_{WSM}	Stop-Mode Recovery Width Spec	3.0V	12		ns	7	
			5.5V	12		ns	7	
11	T_{OST}	Oscillator Startup Time	3.0V		$5T_PC$		7,8	
			5.5V		$5T_PC$		7,8	
12	T_{WDT}	Watch-Dog Timer Delay Timer before time-out	3.0V	7		ms	9	0,0
			5.5V	3.5		ms	9	0,0
			3.0V	14		ms	9	0,1
			5.5V	7		ms	9	0,1
			3.0V	28		ms	9	1,0
			5.5V	14		ms	9	1,0
			3.0V	112		ms	9	1,1
			5.5V	56		ms	9	1,1
13	T_{POR}	Power-On Reset Delay	3.0V	2	32	ms		
			5.5V	1	16	ms		

Notes:
1. The V_{CC} voltage specification of 5.5V guarantees 5.0V ±0.5V.
2. The timing reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
3. SMR: D1 = 0.
4. The maximum frequency for the external crystal clock is 4 MHz when using LOW-EMI OSCILLATOR mode.
5. The interrupt request via Port 3 (P31–P33).
6. The interrupt request via Port 3 (P30).
7. SMR: D5 = 1, and the POR Stop-Mode Delay is on.
8. For RC and LC oscillators, and for an oscillator driven by a clock driver.
9. The D1,D0 column applies to the Watch-Dog Timer Mode Register tap selection.
10. 12 µs is the typical delay time.

Product Information

Serial # or Board Fab #/Rev. #
Software Version
Document Number
Host Computer Description/Type

Return Information

ZiLOG
System Test/Customer Support
532 Race Street
San Jose, CA 95126-3432
Fax: (408) 558-8536
Email:www.zilog.com

Problem Description or Suggestion

Provide a complete description of the problem or your suggestion. If you are reporting a specific problem, include all steps leading up to the occurrence of the problem. Attach additional pages as necessary.

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