Zilog - Z87C3304PECR53KM Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	24
Program Memory Size	4KB (4K x 8)
Program Memory Type	ROM
EEPROM Size	-
RAM Size	236 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.600", 15.24mm)
Supplier Device Package	28-DIP
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z87c3304pecr53km

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Architectural Overview

ZiLOG’s large Z8® family of 8-bit microcontrollers now includes the Z87C33 product line, featuring an enhanced wake-up circuitry, programmable Watch-Dog Timers (WDT), and low-noise/EMI options. These enhancements to the Z8 offers a more efficient, cost-effective design and provides the user with increased design flexibility over the standard Z8 microcontroller core. The low-power-consumption CMOS microcontroller offers fast execution, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, and easy hardware/software system expansion.

The Z87C33 subfamily features an Expanded Register File (ERF) to allow access to register-mapped peripheral and I/O circuits. Four basic address spaces are available to support this wide range of configurations: Program Memory, Register File, and ERF. The Register File is composed of 237 bytes of general-purpose registers, three I/O port registers, 15 control and status registers. The ERF consists of four control registers.

For applications demanding powerful I/O capabilities, the Z87C33 offers 24 pins dedicated to input and output. These lines are configurable under software control.

The Z87C33 family operates at 4 MHz with a voltage range of 3.0 to 5.5 V_{DC}.

To unburden the system from coping with real-time tasks such as counting/timing, the Z8 offers two on-chip counter/timers with a large number of user-selectable modes.

Note: All signals with an overline are active Low. For example, B/$\overline{W}$, for which WORD is active Low, and $\overline{B}$/W, for which BYTE is active Low.

Power connections follow these conventional descriptions:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

Pin Description

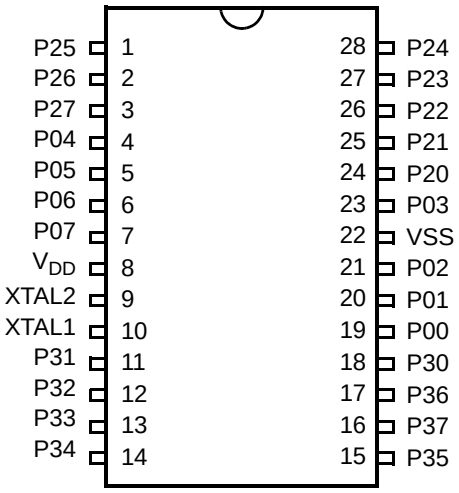

Figure 2.28-Pin DIP/SOIC Pin Configuration

Table 2. 28-Pin DIP/SOIC Pin Configuration

Pin #	Symbol	Function	Direction
1–3	P25-27	Port 2, Pins 5,6,7	Input/Output
4-7	P04-07	Port 0, Pins 4-7	Input/Output
8	V_{DD}	Power Supply	
9	XTAL2	Crystal Oscillator	Output
10	XTAL1	Crystal Oscillator	Input
11-13	P31-33	Port 3, Pins 1,2,3	Fixed Input
14-15	P34-35	Port 3, Pins 4,5	Fixed Output
16	P37	Port 3, Pin 7	Fixed Output
17	P36	Port 3, Pin 6	Fixed Output
18	P30	Port 3, Pin 0	Fixed Input
19-21	P00-02	Port 0, Pins 0,1,2	Input/Output
22	V_{SS}	Ground	
23	P03	Port 0, Pin 3	Input/Output
24-28	P20-24	Port 2, Pins 0,1,2,3,4	Input/Output

Pin Functions

The following pages describe the function of each available Z87C33 family pin.

X_{IN} Crystal Input. This pin connects a parallel-resonant crystal, ceramic resonator, LC, or RC network, or an external single-phase clock to the on-chip oscillator input.

X_{OUT} Crystal Output. This pin connects a parallel-resonant crystal, ceramic resonant, LC, or RC network to the on-chip oscillator output.

Port 0 (P00–P07). Port 0 is an 8-bit, bidirectional, CMOS-compatible port. These eight I/O lines are configured under software control as a nibble I/O port (P03–P00 input/output and P07–P04 input/output), or as an address port for interfacing external memory. The input buffers are Schmitt-triggered and nibble-programmed as outputs and can be globally programmed as either push-pull or open-drain. Low-EMI output buffers are globally programmed by the software.

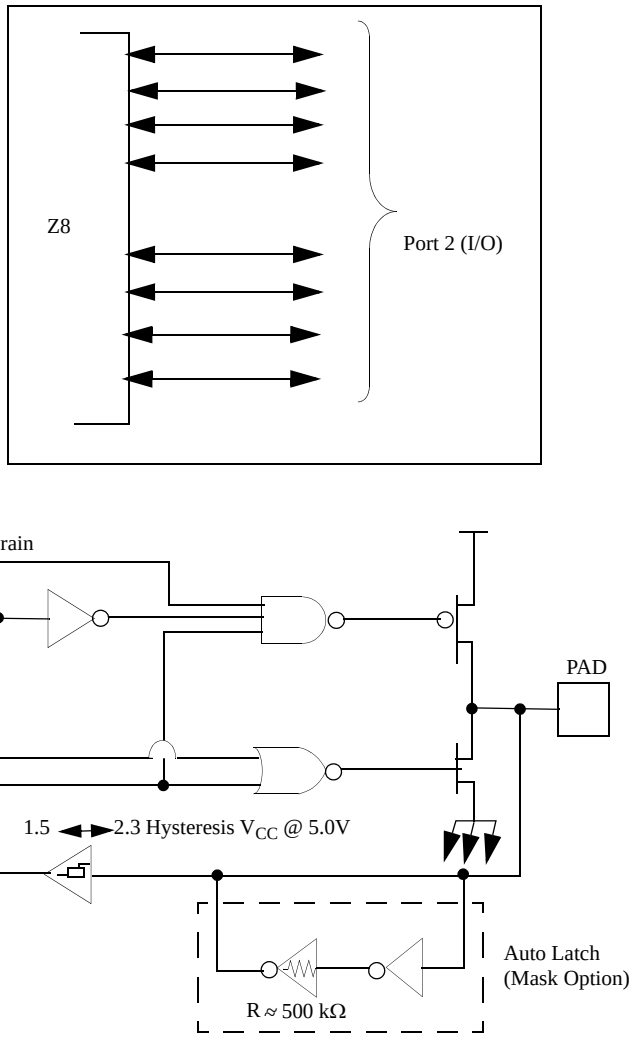

Figure 4.Port 2 Configuration

Port 3 (P37–P30). Port 3 is an 8-bit, CMOS-compatible port, with four fixed inputs (P33–P30) and four fixed outputs (P34–P37). Port 3 is configured under software control for Input/Output, Counter/Timers, interrupt, and UART. Port 3, bit 0 input is Schmitt-triggered, and pins P31, P32, and P33 are standard CMOS inputs (no autolatches). Pins P34, P35, P36, P37 are push-pull output lines. Low-EMI output buffers are globally programmed by the software.

Two onboard comparators process analog signals on P31 and P32 with reference to the voltage on P33. The analog function is enabled by programming Port 3

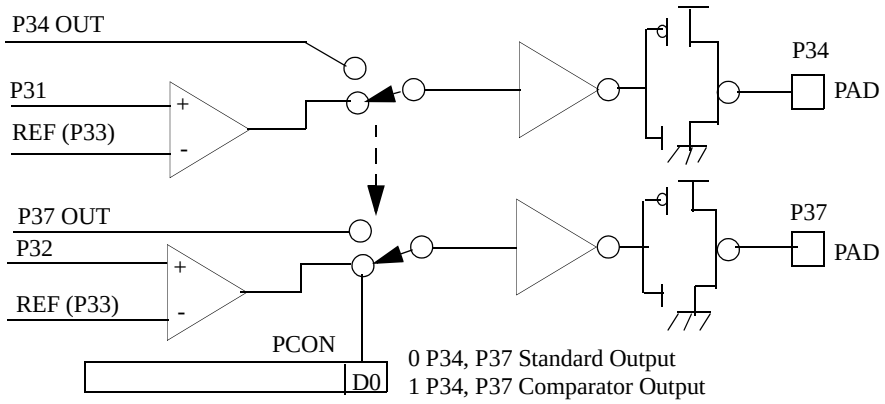

Figure 6.Port 3 Configuration—PCON Register Detail

Autolatch. The autolatch places valid CMOS levels on all CMOS inputs (except P33–P31) that are not externally driven. Whether this level is 0 or 1 cannot be determined. A valid CMOS level, rather than a floating node, reduces excessive supply current flow in the input buffer. Autolatches are available on Port 0, Port 1, Port 2, and P30. There are no auto latches on P31, P32, and P33.

Note: Deletion of all port autolatches is available as an option when the device is programmed. The AUTOLATCH DISABLE option is selected by the customer when the device is programmed.

Functional Description

The Z8 MCU incorporates the following functions that enhance the standard Z8® architecture and provide the user with increased design flexibility:

- Program Memory
- ROM Protect
- RAM Protect
- Working Register File
- Expanded Register File
- General-Purpose Registers
- Stack Pointer
- Counter/Timers
- Interrupts
- Clock
- Power-On Reset
- HALT and STOP Modes
- Port Configuration Register
- Comparator
- Stop-Mode Recovery
- Watch-Dog Timer
- Voltage Comparator (V_{LV})

RESET. The device is reset in one of the following conditions.

- Power-On Reset
- Watch-Dog Timer
- Stop-Mode Recovery Source
- Low Voltage Recovery

Automatic Power-On Reset circuitry is built into the Z87C33 eliminating the requirement for an external reset circuit to reset upon power-up.

Program Memory. The Program Memory addresses up to 4 KB of internal memory. The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available

Table 5. Interrupt Types, Sources, and Vectors

Name	Source	Vector Location	Comments
IRQ0	IRQ0	0,1	External (P32), Rising and Falling Edges Triggered
IRQ1,	IRQ1	2,3	External (P33), Falling Edge Triggered
IRQ2	IRQ2, T_{IN}	4,5	External (P31), Rising and Falling Edges Triggered
IRQ3	IRQ3	6,7	External (P30), Falling Edge Triggered
IRQ4	T0	8,9	Internal
IRQ5	T1	10,11	Internal

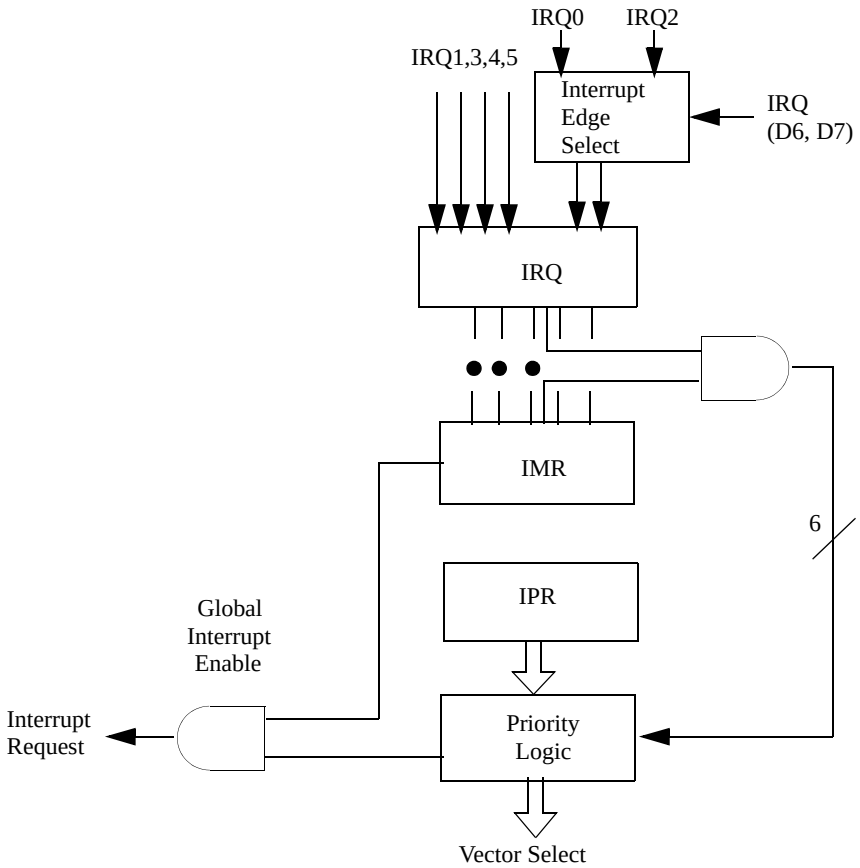

Figure 11.Interrupt Block Diagram

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority register. An interrupt machine cycle activates when an interrupt request is granted. This action disables all subsequent interrupts, saves the Program Counter and Status Flags, and then branches to the program memory vector location reserved for that interrupt.

All Z8 interrupts are vectored through locations in the program memory. This memory location and the next byte contain the 16-bit address of the interrupt service routine for that particular interrupt request. To accommodate polled interrupt systems, interrupt inputs are masked and the Interrupt Request register is polled to determine which of the interrupt requests require service.

When in ANALOG mode, an interrupt resulting from AN1 maps to IRQ2, and an interrupt from AN2 maps to IRQ0. Interrupts IRQ2 and IRQ0 may be rising, falling, or both edge-triggered, and are programmed in the IRQ register. The software polls to identify the state of the pin. When in ANALOG mode, IRQ1 is generated by the Stop-Mode Recovery source selected by SMR Register bits D4, D3, D2, or SMR2 D1 or D0.

Programming bits for the Interrupt Edge Select are located in the IRQ register, bits D7 and D6. The configuration is indicated in Table 7.

Table 6. IRQ Register*

IRQ		Interrupt Edge	
D7	**D6**	**P31**	**P32**
0	0	F	F
	1	F	R
1	0	R	F
1	1	R/F	R/F

Notes:
F = Falling Edge
R = Rising Edge

Clock. The Z8 on-chip oscillator features a high-gain, parallel-resonant amplifier for connection to a crystal, LC, RC, ceramic resonator, or any suitable external clock source (X_{IN} = INPUT, X_{OUT} = OUTPUT). The crystal should be AT-cut, 4 MHz maximum, with a series resistance (RS) of less than or equal to 100Ω when oscillating from 1MHz to 4MHz.

The crystal should be connected across XTAL1 and XTAL2 using the vendor’s recommended capacitor values from each pin directly to the device Ground pin to reduce ground-noise injection into the oscillator. The RC oscillator option is mask-

Low-EMI Port 2 (D5). Port 2 is configured as a low-EMI port by resetting this bit (D5 = 0) or configured as a Standard Port by setting this bit (D5 = 1). The default value is 1.

Low-EMI Port 3 (D6). Port 3 is configured as a low-EMI port by resetting this bit (D6 = 0) or configured as a Standard Port by setting this bit (D6 = 1). The default value is 1.

Low-EMI OSC (D7). This bit of the PCON register controls the low-EMI noise oscillator. A 1 in this location configures the oscillator, $\overline{DS}$, $\overline{AS}$ and R/$\overline{W}$ with standard drive, while a 0 configures the oscillator, $\overline{DS}$, $\overline{AS}$ and R/$\overline{W}$ with low noise drive. LOW-EMI mode reduces the drive of the oscillator (OSC). The default value is 1.

Note: Maximum external clock frequency of 4 MHz when running in LOW-EMI OSCILLATOR mode.

Low-EMI Emission. The Z8 is programmed to operate in a low-EMI emission mode in the PCON register. The oscillator and all I/O ports is programmed as LOW-EMI EMISSION mode independently. Use of this feature results in:

- The pre-drivers slew rate reduced to 10 ns (typical)
- Low-EMI output drivers exhibit resistance of 200Ω (typical)
- Low-EMI Oscillator
- Internal SCLK = X_{IN} operation limited to a maximum of 4 MHz–250 ns cycle time, when LOW EMI OSCILLATOR is selected and system clock (SMR Register Bit D1 = 1)

Stop-Mode Recovery Registers (SMR1 and SMR2). These registers select the clock divide value and determine the mode of Stop-Mode Recovery (Tables 8 and 11). All bits are WRITE ONLY, except bit 7 of SMR1, which is READ ONLY. SMR1 bit 7 is a flag bit that is set by hardware on a Stop-Mode Recovery condition and reset by a power-on cycle. For SMR1, bit 6 controls whether a Low level or a High level is required from the recovery source. Bit 5 controls the reset delay after Stop-Mode Recovery. Bits 2, 3, and 4 of the SMR1 register specify the source of the Stop-Mode Recovery signal. Bits 0 and 1 determine the time-out period of the WDT. The SMR registers are located in Bank F of the Expanded Register File at addresses `0Bh` and `0Dh`, respectively.

For SMR2, bits 7 to 2 are reserved. Bits 1 and 0 of the SMR2 register specify the source of the Stop-Mode Recovery signal.

Table 8. Stop-Mode Recovery Register 1—SMR1 0Bh/R11 Bank Fh: WRITE ONLY, except Bit D7, which is READ ONLY

Bit	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R	W	W	W	W	W	W	W

External Clock Divide-by-Two (D1). This bit can eliminate the oscillator divide-by-two circuitry. When this bit is 0, the system clock (SCLK) and timer clock (TCLK) are equal to the external clock frequency divided by 2. The SCLK is equal to the external clock frequency when this bit is set (D1 = 1). Using this bit together with D7 of PCON further helps lower EMI (that is, D7 (PCON) = 0, D1 (SMR) = 1). The default setting is 0. Maximum external clock frequency is 4 MHz when SMR bit D1 = 1 where SCLK & TCLK = X_{IN}.

Stop-Mode Recovery Source (D2, D3, and D4). These three bits of the SMR specify the wake-up source of the Stop-Mode Recovery (Figure and Stop-Mode Recovery Source). When the Stop-Mode Recovery Sources are selected in this register, then SMR2 register bits D0,D1 must be set to 0.

Note: If the Port 2 pin is configured as an output, this output level is read by the SMR circuitry.

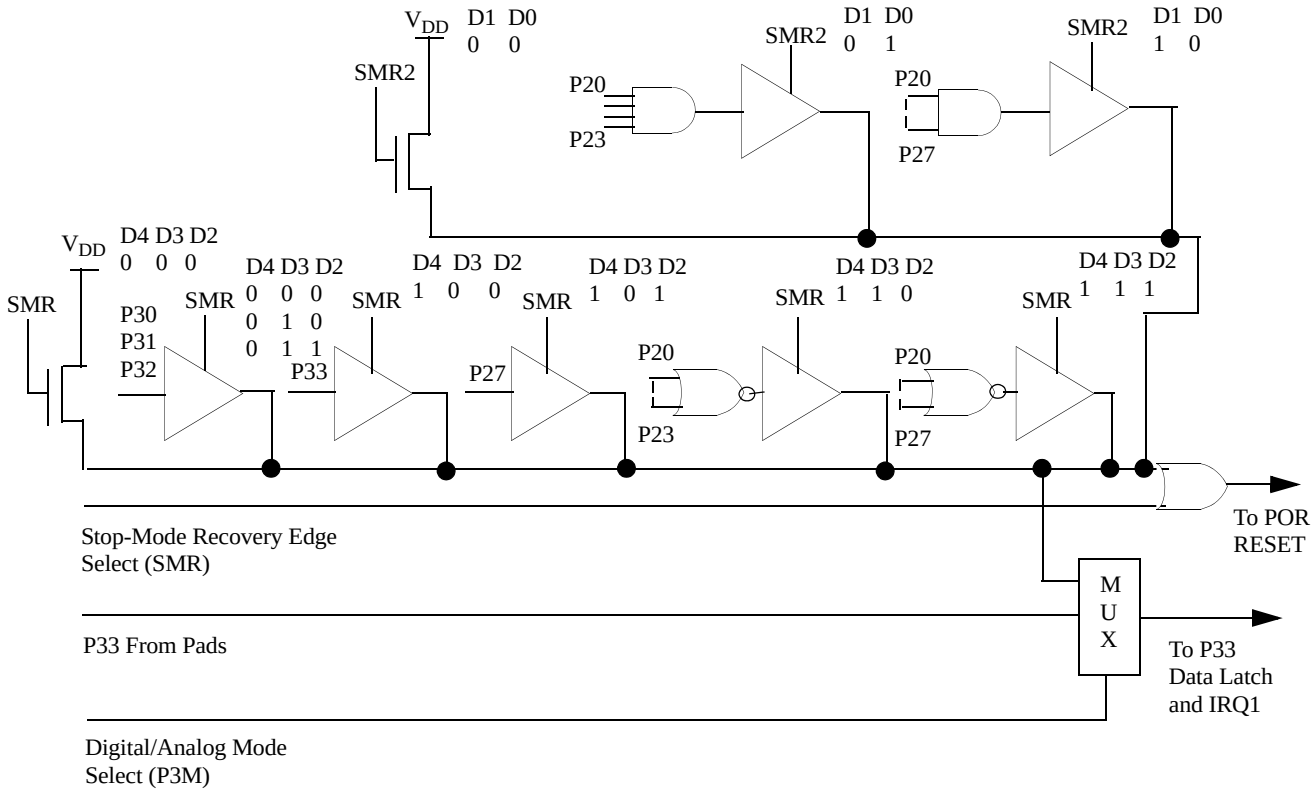

Figure 13.Stop-Mode Recovery Source

Table 12. Watch-Dog Timer Mode Register—WDTMR 0Fh/R15: WRITE ONLY

Bit	D7	D6	D5	D4	D3	D2	D1	D0
R/W	W	W	W	W	W	W	W	W
Reset	X	X	X	0	1	1	0	1
Note: R = Read, W = Write, X = Indeterminate.								

Bit/ Field	Bit Position	R/W	Reset State	Description
D7–D5	Reserved	W	X	Reserved—must be 0
D4	X_{IN}	W	0	**XIN/INT RC Select for WDT** 0: On-Board RC 1: X_{IN}
D3	WDT	W	1	WDT During STOP
D2	WDT	W	1	WDT During HALT
D1–D0	WDT Tap	W	01	**WDT Tap Int RC OSC System Clock** 00: 3.5 ms 128 SCLK 01: 7.0 ms 256 SCLK 10: 14.0 ms 512 SCLK 11: 56.0 ms 2048 SCLK

Note: Not used in conjunction with SMR Source.

WDT Time Select (D0,D1). Selects the WDT time period and is configured as indicated in Table 14.

Table 13. WDT Time Select

D1	D0	Timeout of Internal RC OSC	Timeout of System Clock
0	0	3.5 ms min	128 SCLK
0	1	7 ms min	256 SCLK
1	0	14 ms min	512 SCLK
1	1	56 ms min	2048 SCLK

Note: SCLK = system bus clock cycle. The default on RESET is 7 ms. Values provided are for V_{CC} = 5.0V.

WDTMR During HALT (D2). This bit determines whether or not the WDT is active during HALT mode. A 1 indicates active during HALT. The default is 1.

Control Registers

The Z87C33 offers 2 banks of registers, as detailed in the following pages.

Expanded Register File, Bank 0h

Bank 0h of the Expanded Register File contains 15 Control registers that perform the Timer, Prescaler, Port, Interrupt, Flag, and Pointer functions, as shown in Tables 16 through 30. Table 15 lists the reset states of all 15 Bank 0h Control registers.

Table 15. Expanded Register File Registers—Reset States

		D7	D6	D5	D4	D3	D2	D1	D0
F0h	Reserved								
F1h	TMR	0	0	0	0	0	0	0	0
F2h	T1	X	X	X	X	X	X	X	X
F3h	PRE1	X	X	X	X	X	X	0	0
F4h	T0	X	X	X	X	X	X	X	X
F5h	PRE0	X	X	X	X	X	X	X	0
F6h	P2M*	1	1	1	1	1	1	1	1
F7h	P3M*	0	0	0	0	0	0	0	0
F8h	P01M	0	1	0	0	1	1	0	1
F9h	IPR	X	X	X	X	X	X	X	X
FAh	IRQ	0	0	0	0	0	0	0	0
FBh	IMR	0	X	X	X	X	X	X	X
FCh	FLAGS	X	X	X	X	X	X	X	X
FDh	RP	0	0	0	0	0	0	0	0
FEh	SPH	0	0	0	0	0	0	0	0
FFh	SPL	0	0	0	0	0	0	0	0

Note: *Not reset with a Stop-Mode Recovery.

Timer Mode Register

The Timer Mode Register, TMR, controls timing and counter functions. READ/WRITE and reset states for bits D7–D0 are listed in Table 16.

Table 16. Timer Mode Register—TMR F1h/R241 Bank 0h: READ/WRITE

Bit	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset State	0	0	0	0	0	0	0	0
Note: R = Read, W = Write.								

Bit Position	Bit Field	R/W	Reset State	Description
D7–D6	T_{OUT} Mode	R/W	00	**T_{OUT} Mode** 00: Off 01: T0 Output 10: T1 Output 11: Internal Clock Output
D5–D4	T_{IN} Mode	R/W	00	**T_{IN} Mode** 00: External Clock Input 01: Gate Input 10: Trigger Input (nonretriggerable) 11: Trigger Input (retriggerable)
D3	T1 Count	R/W	0	**T1 Count** 0: Disable 1: Enable
D2	T1	R/W	0	**T1** 0: No Function 1: Load T1
D1	T0 Count	R/W	0	**T0 Count** 0: Disable 1: Enable
D0	T0	R/W	0	**T0** 0: No Function 1: Load T0

Counter/Timer 1 Register

The Counter/Timer 1 Register, T1, controls timing and counter functions. READ/WRITE and reset states for bits D7–D0 are listed in Table 17.

Table 17. Counter/Timer 1 Register—T1 F2h/R242 Bank 0h: READ/WRITE

Bit	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 17. Counter/Timer 1 Register—T1 F2h/R242 Bank 0h: READ/WRITE

Reset State	X	X	X	X	X	X	X	X
Note: R = Read, W = Write, X = Indeterminate.								

Bit Position	Bit Field	R/W	Reset State	Description
D7–D0	T1	R	X	T1 Current Value
		W	X	T1 Automatic Reload Value Range = 1–256 decimal; 01h–00h

Prescaler 1 Register

The Prescaler 1 Register, PRE1, controls clocking functions. READ/WRITE and reset states for bits D7–D0 are listed in Table 18.

Table 18. Prescaler 1 Register—PRE1 F3h/R243 Bank 0h: WRITE ONLY

Bit	D7	D6	D5	D4	D3	D2	D1	D0
R/W	W	W	W	W	W	W	W	W
Reset State	X	X	X	X	X	X	0	0
Note: W = Write, X = Indeterminate.								

Bit Position	Bit Field	R/W	Reset State	Description
D7–D2	Prescaler	W	X	**Prescaler Modulo** Range = 1–64 decimal; 01h–00h
D1	Clock	W	0	**Clock Source** 0: T1 External Timing Input (T_{IN}) Mode 1: T1 Internal
D0	Count	W	0	**Count Mode** 0: T1 Single Pass 1: T1 Modulo N

Counter/Timer 0 Register

The Counter/Timer 0 Register, T0, controls timing and counter functions. READ/WRITE and reset states for bits D7–D0 are listed in Table 19.

Table 31. Expanded Register File Registers—Reset States (Continued)

		D7	D6	D5	D4	D3	D2	D1	D0
07h	Reserved								
08h	Reserved								
09h	Reserved								
0Ah	Reserved								
0Bh	SMR**	0	0	1	0	0	0	0	0
0Ch	Reserved								
0Dh	SMR2*	X	X	X	X	X	X	0	0
0Eh	Reserved								
0Fh	WDTMR*	X	X	X	0	1	1	0	1

Note: *Not reset with a Stop-Mode Recovery.
Note: **Not reset with a Stop-Mode Recovery except Bit D7.

Port Configuration Register

The Port Configuration Register, PCON, controls the configurations of Ports 0, 2, and 3. WRITE and reset states for bits D7–D0 are listed in Table 32.

Table 32. Port Configuration Register—PCON 00h/R0 Bank Fh: WRITE ONLY

Bit	D7	D6	D5	D4	D3	D2	D1	D0
R/W	W	W	W	W	W	W	W	W
Reset	1	1	1	1	1	1	1	0
Note: W = Write.								

Bit Position	Bit Field	R/W	Reset State	Description
D7	Oscillator	W	1	**Low-EMI Oscillator** 0: Low EMI 1: Standard
D6	Port 3 I/O	W	1	**Port 3** 0: Low EMI 1: Standard
D5	Port 2 I/O	W	1	**Port 2** 0: Low EMI 1: Standard

Bit Position	Bit Field	R/W	Reset State	Description
D7–D5	Reserved	W	X	Reserved—must be 0
D4	X_{IN}	W	0	**X_{IN} Input/Internal RC Select for WDT** 0: On-Board RC 1: X_{IN}
D3	WDT	W	1	**WDT During STOP** 0: WDT disabled during STOP mode 1: WDT enabled during STOP mode
D2	WDT	W	1	**WDT During HALT** 0: WDT disabled during HALT mode 1: WDT enabled during HALT mode
D1–D0	WDT Tap	W	01	**WDT Tap Int. RC Osc. System Clock** 00: 3.5 ms 128 SCLK 01: 7 ms 256 SCLK 10: 14 ms 512 SCLK 11: 56 ms 2048 SCLK

Note: Not used in conjunction with SMR Source.

Electrical Characteristics

Absolute Maximum Ratings

Stresses greater than the Absolute Maximum Ratings listed in Table 36 may cause permanent damage to the device. This rating is a stress rating only. Functional operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability.

Table 36. Absolute Maximum Ratings

Parameter	Min	Max	Units	Notes
Ambient Temperature under Bias	–40	+105	C	
Storage Temperature	–65	+150	C	
Voltage on any Pin with Respect to V_{SS}	–0.6	+7	V	1
Voltage on V_{DD} Pin with Respect to V_{SS}	–0.3	+7	V	
Voltage on X_{IN} Pin with Respect to V_{SS}	–0.6	V_{DD}+1	V	2
Total Power Dissipation		1.21	W	

DC Electrical Characteristics

Standard Temperature Range

Table 37. DC Electrical Characteristics at Standard Temperature

Sym	Parameter	V_{CC1}	T_A = 0°C to +70°C Min	T_A = 0°C to +70°C Max	Typical[2] @25°C	Units	Conditions	Notes
V_{CH}	Clock Input High Voltage	3.0V	0.7 V_{CC}	V_{CC}+0.3	1.8	V	Driven by External Clock Generator	
		5.5V	0.7 V_{CC}	V_{CC}+0.3	2.6	V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	3.0V	GND–0.3	0.2 V_{CC}	1.2	V	Driven by External Clock Generator	
		5.5V	GND–0.3	0.2 V_{CC}	2.1	V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	3.0V	0.7 V_{CC}	V_{CC}+0.3	1.8	V		
		5.5V	0.7 V_{CC}	V_{CC}+0.3	2.6	V		
V_{IL}	Input Low Voltage	3.0V	GND–0.3	0.2 V_{CC}	1.1	V		
		5.5V	GND–0.3	0.2 V_{CC}	1.6	V		
V_{OH}	Output High Voltage	3.0V	V_{CC}–0.4		3.1	V	I_{OH} = –0.5 mA	4
		5.0V	V_{CC}–0.4		4.8	V	I_{OH} = –0.5 mA	4

Notes:
1. The V_{CC} voltage specification of 3.0V guarantees 3.3V ±0.3V with typicals at V_{CC} = 3.3V, and the V_{CC} voltage specification of 5.5V guarantees 5.0V ±0.5V with typicals at V_{CC} = 5.0V.
2. Typical voltage is V_{CC} = 5.0V and 3.3V.
3. STANDARD Mode (not Low-EMI Mode).
4. Low-EMI Mode (Not Standard Mode).
5. For analog comparator, inputs when analog comparators are enabled.
6. All outputs unloaded, I/O pins floating, inputs at rail.
7. Same as note 6, except inputs at V_{CC}.
8. Clock must be forced Low, when X_{IN} is clock-driven and X_{OUT} is floating.
9. 0ºC to 70ºC (standard temperature).
10. Autolatch (Mask Option) selected.
11. The V_{LV} voltage increases as the temperature decreases and overlaps lower V_{CC} operating region. See Figure 15.
12. –40°C to 105°C (extended temperature).

Table 38. DC Electrical Characteristics at Extended Temperature (Continued)

Sym	Parameter	V_{CC1}	T_A = –40°C to +105°C Min	Max	Typical[2] @25°C	Units	Conditions	Notes
I_{CC2}	Standby Current (STOP Mode)	3.0V		8	2	µA	WDT is not Running	7,8
		5.5V		10	4	µA	WDT is not Running	7,8
		3.0V		600	310	µA	WDT is Running	7,8
		5.5V		1000	600	µA	WDT is Running	7,8
V_{ICR}	Input Common Mode Voltage Range	3.0V	0	V_{CC}–1.5V		V		5
		5.5V	0	V_{CC}–1.5V		V		5
I_{ALL}	Autolatch Low Current	3.0V	0.7	10	3	µA	$0V<V_{IN}<V_{CC}$	10
		5.5V	1.4	20	5	µA	$0V<V_{IN}<V_{CC}$	10
I_{ALH}	Autolatch High Current	3.0V	–0.6	–7	–3	µA	$0V<V_{IN}<V_{CC}$	10
		5.5V	–1.0	–10	–6	µA	$0V<V_{IN}<V_{CC}$	10
V_{LV}	V_{CC} Low Voltage Protection Voltage		2.0	3.3	2.8	V	4 MHz max Internal CLK Freq.	11,12

Notes:
1. The V_{CC} voltage specification of 3.0V guarantees 3.3V ±0.3V with typicals at V_{CC} = 3.3V, and the V_{CC} voltage specification of 5.5V guarantees 5.0V ±0.5V with typicals at V_{CC} = 5.0V.
2. Typical voltage is V_{CC} = 5.0V and 3.3V.
3. STANDARD Mode (not Low-EMI Mode).
4. Low-EMI Mode (Not Standard Mode).
5. For analog comparator, inputs when analog comparators are enabled.
6. All outputs unloaded, I/O pins floating, inputs at rail.
7. Same as note 6, except inputs at V_{CC}.
8. Clock must be forced Low, when X_{IN} is clock-driven and X_{OUT} is floating.
9. 0ºC to 70ºC (standard temperature).
10. Autolatch (Mask Option) selected.
11. The V_{LV} voltage increases as the temperature decreases and overlaps lower V_{CC} operating region. See Figure 15.
12. –40°C to 105°C (extended temperature).

Product Information

Serial # or Board Fab #/Rev. #
Software Version
Document Number
Host Computer Description/Type

Return Information

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Problem Description or Suggestion

Provide a complete description of the problem or your suggestion. If you are reporting a specific problem, include all steps leading up to the occurrence of the problem. Attach additional pages as necessary.

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