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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	24
Program Memory Size	4KB (4K x 8)
Program Memory Type	ROM
EEPROM Size	-
RAM Size	236 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.600", 15.24mm)
Supplier Device Package	28-DIP
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z87c3304pecr5467

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Architectural Overview

ZiLOG’s large Z8® family of 8-bit microcontrollers now includes the Z87C33 product line, featuring an enhanced wake-up circuitry, programmable Watch-Dog Timers (WDT), and low-noise/EMI options. These enhancements to the Z8 offers a more efficient, cost-effective design and provides the user with increased design flexibility over the standard Z8 microcontroller core. The low-power-consumption CMOS microcontroller offers fast execution, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, and easy hardware/software system expansion.

The Z87C33 subfamily features an Expanded Register File (ERF) to allow access to register-mapped peripheral and I/O circuits. Four basic address spaces are available to support this wide range of configurations: Program Memory, Register File, and ERF. The Register File is composed of 237 bytes of general-purpose registers, three I/O port registers, 15 control and status registers. The ERF consists of four control registers.

For applications demanding powerful I/O capabilities, the Z87C33 offers 24 pins dedicated to input and output. These lines are configurable under software control.

The Z87C33 family operates at 4 MHz with a voltage range of 3.0 to 5.5 V_{DC}.

To unburden the system from coping with real-time tasks such as counting/timing, the Z8 offers two on-chip counter/timers with a large number of user-selectable modes.

Note: All signals with an overline are active Low. For example, B/$\overline{W}$, for which WORD is active Low, and $\overline{B}$/W, for which BYTE is active Low.

Power connections follow these conventional descriptions:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

Features

Table 1. Family Features

Device	ROM (KB)	RAM* (Bytes)	Speed (MHz—Standard and Extended Temperature)
Z87C33	4	236	4

Note: *General-Purpose.

- 28-Pin DIP and 28-Pin SOIC
- 3.0- to 5.5-Volt Operating Range
- Operating Temperature Ranges:
  Standard: 0ºC to 70ºC
  Extended: –40ºC to +105ºC
- Expanded Register File (ERF)
- 24 Input/Output Lines
- Vectored, Prioritized Interrupts with Programmable Polarity
- Two Analog Comparators
- Two Programmable 8-Bit Counter/Timers, each with two 6-Bit Programmable Prescalers
- VBO/Power-On Reset (POR)
- Clock-Free Watch-Dog Timer (WDT) Reset
- On-Chip Oscillator that accepts a Crystal, Ceramic Resonator, LC, RC, or External Clock
- RAM and ROM Protect

Pin Description

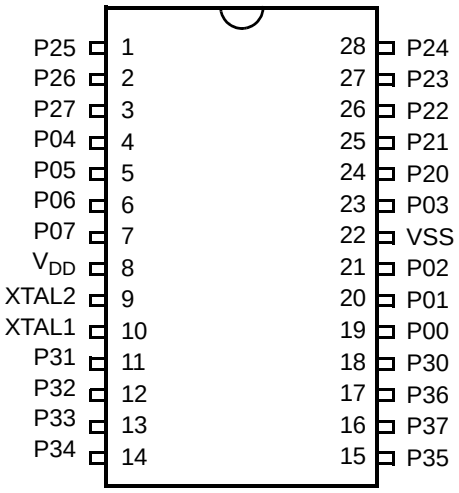


Figure 2.28-Pin DIP/SOIC Pin Configuration

Table 2. 28-Pin DIP/SOIC Pin Configuration

Pin #	Symbol	Function	Direction
1–3	P25-27	Port 2, Pins 5,6,7	Input/Output
4-7	P04-07	Port 0, Pins 4-7	Input/Output
8	V_{DD}	Power Supply	
9	XTAL2	Crystal Oscillator	Output
10	XTAL1	Crystal Oscillator	Input
11-13	P31-33	Port 3, Pins 1,2,3	Fixed Input
14-15	P34-35	Port 3, Pins 4,5	Fixed Output
16	P37	Port 3, Pin 7	Fixed Output
17	P36	Port 3, Pin 6	Fixed Output
18	P30	Port 3, Pin 0	Fixed Input
19-21	P00-02	Port 0, Pins 0,1,2	Input/Output
22	V_{SS}	Ground	
23	P03	Port 0, Pin 3	Input/Output
24-28	P20-24	Port 2, Pins 0,1,2,3,4	Input/Output

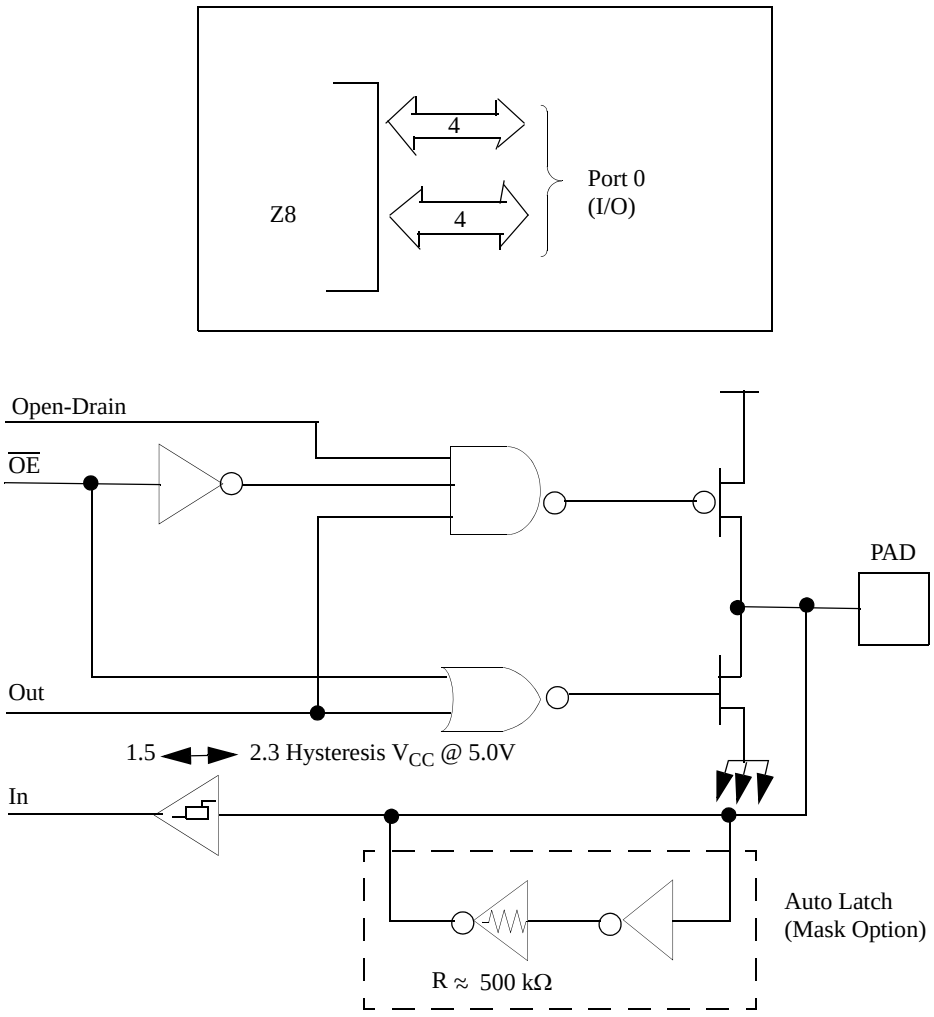


Figure 3. Port 0 Configuration

Port 2 (P27–P20). Port 2 is an 8-bit, bidirectional, CMOS-compatible I/O port. These eight I/O lines are configured under software control as an input or output, independently. Port 2 is always available for I/O operation. The input buffers are Schmitt-triggered. Bits programmed as outputs may be globally programmed as either push-pull or open-drain. Low-EMI output buffers are globally programmed by the software. See Figure 5.

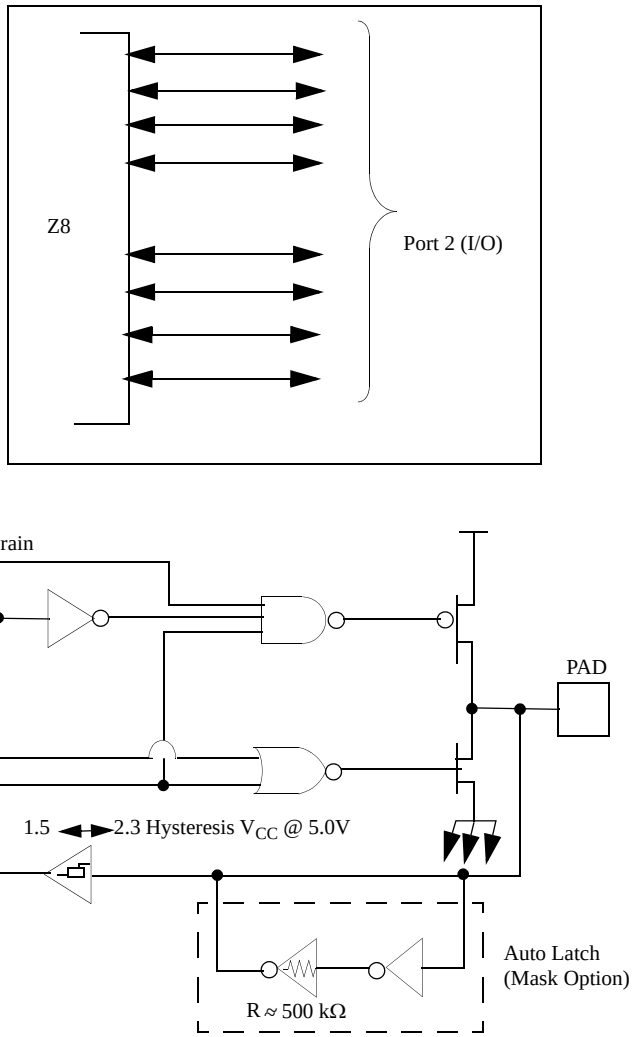


Figure 4.Port 2 Configuration

Port 3 (P37–P30). Port 3 is an 8-bit, CMOS-compatible port, with four fixed inputs (P33–P30) and four fixed outputs (P34–P37). Port 3 is configured under software control for Input/Output, Counter/Timers, interrupt, and UART. Port 3, bit 0 input is Schmitt-triggered, and pins P31, P32, and P33 are standard CMOS inputs (no autolatches). Pins P34, P35, P36, P37 are push-pull output lines. Low-EMI output buffers are globally programmed by the software.

Two onboard comparators process analog signals on P31 and P32 with reference to the voltage on P33. The analog function is enabled by programming Port 3

Memory, instructions LDC, LDCI, LDE, and LDEI can read Internal Program Memory.

RAM Protect. The upper portion of the RAM’s address spaces 80h to EFh (excluding the control registers) can be protected from writing. The RAM Protect option bit can be selected when the device is programmed. After the mask option is selected, the user activates this feature from the internal ROM code to turn off/on the RAM Protect by loading either a 0 or a 1 into the IMR register, bit D6. A 1 in bit D6 enables the RAM Protect option.

Working Register File. The Z8 standard register file (Bank 0) contains 3 I/O port registers, 237 general-purpose registers, and 15 control and status registers. Expanded register file Bank Fh contains 4 system-configuration registers. The working registers are accessed directly or indirectly via an 8-bit address field. As a result, a short 4-bit register address can use the Register Pointer (Table 5 and Figure 9). In the 4-bit mode, the working register file is divided into 16 working register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working register group.

Throughout this document, Bank 0 is referred to as the Z8 Standard Register File.

Table 4. Register Pointer Register—RP FDh/R253 Bank 0h: READ/WRITE

Bit	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Note: R = Read, W = Write, X = Indeterminate.								

Bit Position	Bit Field	R/W	Reset State	Description
D7–D4	Working Registers	R/W	0	Working Register Group Pointer
D3–D0	ERF	R/W	0	Expanded Register File

Expanded Register File (ERF). The Z8 register file is expanded to allow for additional system control registers, and for mapping of additional peripheral devices, along with the I/O ports, into the register address area. The Z8 register address space 0 through 255 is implemented as 16 groups of 16 registers per bank (Figures 8 and 9). There are 16 banks known as the Expanded Register File (ERF). Bits 7–4 of register RP select the Working Register Group. Bits 3–0 of register RP select the Expanded Register File Bank. Four system configuration registers reside in the Expanded Register File at Bank Fh—PCON, SMR, SMR2, and WDTMR. The remainder of the Expanded Register is not physically implemented, and is open for future expansion.

and V_{LV} Reset. An interrupt request must be enabled and executed to exit HALT mode. After the interrupt service routine, the program continues from the instruction after the HALT.

In order to enter STOP (or HALT) mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. The user must execute a NOP (Op Code = FFh) immediately before the appropriate sleep instruction. For example:

```
FF    NOP    ; clear the pipeline
6F    STOP   ; enter STOP mode
```

or

```
FF    NOP    ; clear the pipeline
7F    HALT   ; enter HALT mode
```

STOP. This instruction turns off the internal clock and external crystal oscillation. The STOP instruction also reduces the standby current to 10 µA or less. The analog comparators are automatically powered down in STOP-Mode. STOP mode is terminated either by WDT time-out, POR, Stop-Mode Recovery, or any Reset. As a result, the processor restarts the application program at address 000Ch. A WDT time-out in STOP mode affects all registers the same as if a Stop-Mode Recovery occurred via a selected Stop-Mode Recovery source except that the POR delay is enabled even if the delay is selected for disable.

Note: If a permanent WDT is selected, the WDT runs in all modes and cannot be stopped or disabled if the onboard RC oscillator is selected to drive the WDT.

Port Configuration Register (PCON). The PCON register configures the ports individually; comparator output on Port 3, open-drain on Port 0 and Port 1, low EMI on Ports 0, 1, 2, and 3, and low-EMI oscillator. The PCON register is located in the expanded register file at Bank F, location 00h (Table 8).

Table 8. Stop-Mode Recovery Register 1—SMR1 0Bh/R11 Bank Fh: WRITE ONLY, except Bit D7, which is READ ONLY

Reset	0	0	1	0	0	0	0	0
Note: R = Read, W = Write, X = Indeterminate.								

Bit Position	Bit Field	R/W	Reset State	Description
D7	STP	R	0	**Stop Flag** 0: POR 1: Stop-Mode Recovery
D6	SMR	W	0	**Stop-Mode Recovery Level** 0: Low 1: High
D5	STPDLY	W	1	**Stop Delay** 0: Off 1: On
D4–D2	SMRSRC	W	000	**Stop-Mode Recovery Source** [1] 000: POR only and/or external $\overline{\text{RESET}}$ 001: P30 010: P31 011: P32 100: P33 101: P27 110: P2 NOR 0–3 111: P2 NOR 0–7
D1	EXTCLK	W	0	**External Clock Divide-by-2** 0: SCLK & TCLK = XTAL ÷ 2 1: SCLK & TCLK = XTAL
D0	CLK	W	0	**SCLK & TCLK Divide-by-16** 0: Off [2] 1: On

Notes:
1. Do not use in conjunction with SMR2 Source.
2. Cleared by $\overline{\text{RESET}}$ and SMR.

SCLK & TCLK Divide-by-16 Select (D0). Bit D0 of the SMR controls a divide-by-16 prescaler of SCLK & TCLK. The purpose of this control is to selectively reduce device power consumption during normal processor execution (SCLK control) and/or HALT mode (where TCLK sources counter/timers and interrupt logic). This bit is reset to D0 = 0 after a Stop-Mode Recovery.

Table 9. Stop-Mode Recovery Source

SMR[4–2]			
D4	**D3**	**D2**	**Operation/Description of Action**
0	0	0	POR and/or external reset recovery
0	0	1	P30 transition
0	1	0	P31 transition (not in ANALOG mode)
0	1	1	P32 transition (not in ANALOG mode)
1	0	0	P33 transition (not in ANALOG mode)
1	0	1	P27 transition
1	1	0	Logical NOR of P20 through P23
1	1	1	Logical NOR of P20 through P27

Stop-Mode Recovery Delay Select (D5). This bit, if High, enables the T_{POR} $\overline{\text{RESET}}$ delay after Stop-Mode Recovery. The default configuration of this bit is 1. If the *fast* wake up (no delay) is selected, the Stop-Mode Recovery source must be kept active for at least 5 T_PC. The clock source must be RC/LC/external clock driven.

Stop-Mode Recovery Edge Select (D6). A 1 in this bit position indicates that a high level on any one of the recovery sources wakes the Z8 from STOP mode. A 0 indicates low-level recovery. The default is 0 on POR (Table 11). This bit is used for either SMR or SMR2.

Cold or Warm Start (D7). This bit is set by the device upon entering STOP mode. A 0 in this bit (cold) indicates that the device resets by POR/WDT RESET. A 1 in this bit (warm) indicates that the device awakens by a Stop-Mode Recovery source.

Note: If the Port 2 pin is configured as an output, this output level is read by the SMR2 circuitry.

Stop-Mode Recovery Register 2 (SMR2). This register contains additional Stop-Mode Recovery sources. When the Stop-Mode Recovery sources are selected in this register then SMR register bits D2, D3, and D4 must be 0.

Table 10. Stop-Mode Recovery Register 2

SMR1–0		
D1	**D0**	**Operation/Description of Action**
0	0	POR and/or external reset recovery

Table 12. Watch-Dog Timer Mode Register—WDTMR 0Fh/R15: WRITE ONLY

Bit	D7	D6	D5	D4	D3	D2	D1	D0
R/W	W	W	W	W	W	W	W	W
Reset	X	X	X	0	1	1	0	1
Note: R = Read, W = Write, X = Indeterminate.								

Bit/ Field	Bit Position	R/W	Reset State	Description
D7–D5	Reserved	W	X	Reserved—must be 0
D4	X_{IN}	W	0	**XIN/INT RC Select for WDT** 0: On-Board RC 1: X_{IN}
D3	WDT	W	1	WDT During STOP
D2	WDT	W	1	WDT During HALT
D1–D0	WDT Tap	W	01	**WDT Tap Int RC OSC System Clock** 00: 3.5 ms 128 SCLK 01: 7.0 ms 256 SCLK 10: 14.0 ms 512 SCLK 11: 56.0 ms 2048 SCLK

Note: Not used in conjunction with SMR Source.

WDT Time Select (D0,D1). Selects the WDT time period and is configured as indicated in Table 14.

Table 13. WDT Time Select

D1	D0	Timeout of Internal RC OSC	Timeout of System Clock
0	0	3.5 ms min	128 SCLK
0	1	7 ms min	256 SCLK
1	0	14 ms min	512 SCLK
1	1	56 ms min	2048 SCLK

Note: SCLK = system bus clock cycle. The default on RESET is 7 ms. Values provided are for V_{CC} = 5.0V.

WDTMR During HALT (D2). This bit determines whether or not the WDT is active during HALT mode. A 1 indicates active during HALT. The default is 1.

Table 16. Timer Mode Register—TMR F1h/R241 Bank 0h: READ/WRITE

Bit	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset State	0	0	0	0	0	0	0	0
Note: R = Read, W = Write.								

Bit Position	Bit Field	R/W	Reset State	Description
D7–D6	T_{OUT} Mode	R/W	00	**T_{OUT} Mode** 00: Off 01: T0 Output 10: T1 Output 11: Internal Clock Output
D5–D4	T_{IN} Mode	R/W	00	**T_{IN} Mode** 00: External Clock Input 01: Gate Input 10: Trigger Input (nonretriggerable) 11: Trigger Input (retriggerable)
D3	T1 Count	R/W	0	**T1 Count** 0: Disable 1: Enable
D2	T1	R/W	0	**T1** 0: No Function 1: Load T1
D1	T0 Count	R/W	0	**T0 Count** 0: Disable 1: Enable
D0	T0	R/W	0	**T0** 0: No Function 1: Load T0

Counter/Timer 1 Register

The Counter/Timer 1 Register, T1, controls timing and counter functions. READ/WRITE and reset states for bits D7–D0 are listed in Table 17.

Table 17. Counter/Timer 1 Register—T1 F2h/R242 Bank 0h: READ/WRITE

Bit	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Stop-Mode Recovery Register 2

The Stop-Mode Recovery Register, SMR2, controls additional Port 2 clocking functions. WRITE and reset states for bits D7–D0 are listed in Table 34.

Table 34. Stop-Mode Recovery Register 2—SMR2 0Dh/R13 Bank Fh: WRITE ONLY

Bit	D7	D6	D5	D4	D3	D2	D1	D0
R/W	W	W	W	W	W	W	W	W
Reset	X	X	X	X	X	X	0	0
Note: W = Write, X = Indeterminate.								

Bit Position	Bit Field	R/W	Reset State	Description
D7–D2	Reserved	W	X	Reserved—must be 0
D1–D0	STOP Mode	W	00	**Stop-Mode Recovery Source 2*** 00: POR only 01: AND P20, P21, P22, P23 10: AND P20, P21, P22, P23, P24, P25, P26, P27 11: Reserved

Note: For the Stop-Mode Recovery Source, either SMR or SMR2 can be selected. If SMR2 is used to select the Stop-Mode Recovery Source, bits D4–D2 of SMR must be 0. Not used in conjunction with SMR Source.

Watch-Dog Timer Mode Register

The Watch-Dog Timer Mode Register, WDTMR, controls Watch-Dog Timer functions. WRITE and reset states for bits D7–D0 are listed in Table 35.

Table 35. Watch-Dog Timer Mode Register—WDTMR 0Fh/R15 Bank Fh: WRITE ONLY

Bit	D7	D6	D5	D4	D3	D2	D1	D0
R/W	W	W	W	W	W	W	W	W
Reset	X	X	X	0	1	1	0	1
Note: W = Write, X = Indeterminate.								

Bit Position	Bit Field	R/W	Reset State	Description
D7–D5	Reserved	W	X	Reserved—must be 0
D4	X_{IN}	W	0	**X_{IN} Input/Internal RC Select for WDT** 0: On-Board RC 1: X_{IN}
D3	WDT	W	1	**WDT During STOP** 0: WDT disabled during STOP mode 1: WDT enabled during STOP mode
D2	WDT	W	1	**WDT During HALT** 0: WDT disabled during HALT mode 1: WDT enabled during HALT mode
D1–D0	WDT Tap	W	01	**WDT Tap Int. RC Osc. System Clock** 00: 3.5 ms 128 SCLK 01: 7 ms 256 SCLK 10: 14 ms 512 SCLK 11: 56 ms 2048 SCLK

Note: Not used in conjunction with SMR Source.

Electrical Characteristics

Absolute Maximum Ratings

Stresses greater than the Absolute Maximum Ratings listed in Table 36 may cause permanent damage to the device. This rating is a stress rating only. Functional operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability.

Table 36. Absolute Maximum Ratings

Parameter	Min	Max	Units	Notes
Ambient Temperature under Bias	–40	+105	C	
Storage Temperature	–65	+150	C	
Voltage on any Pin with Respect to V_{SS}	–0.6	+7	V	1
Voltage on V_{DD} Pin with Respect to V_{SS}	–0.3	+7	V	
Voltage on X_{IN} Pin with Respect to V_{SS}	–0.6	V_{DD}+1	V	2
Total Power Dissipation		1.21	W	

Table 36. Absolute Maximum Ratings (Continued)

Parameter	Min	Max	Units	Notes
Maximum Allowable Current out of V_{SS}		220	mA	
Maximum Allowable Current into V_{DD}		180	mA	
Maximum Allowable Current into an Input Pin	–600	+600	µA	3
Maximum Allowable Current into an Open-Drain Pin	–600	+600	µA	4
Maximum Allowable Output Current Sunk by Any I/O Pin		25	mA	
Maximum Allowable Output Current Sourced by Any I/O Pin		25	mA	

Notes:
1. Applies to all pins except Crystal pins and where otherwise noted.
2. There is no input protection diode from pin to V_{DD} and current into pin is limited to ±600 µA.
3. Excludes X_{IN} and X_{OUT} pins.
4. Device pin is not at an output Low state.

Total power dissipation should not exceed 1.21 W for the package. Power dissipation is calculated as follows:

$$\text{Total Power Dissipation} = V_{DD} \times [I_{DD} - (\text{sum of } I_{OH}), + \text{sum of } [(V_{DD} - V_{OH}) \times I_{OH}] + \text{sum of } (V_{OL} \times I_{OL})$$

Table 37. DC Electrical Characteristics at Standard Temperature (Continued)

Sym	Parameter	V_{CC1}	T_A = 0°C to +70°C Min	Max	Typical[2] @25°C	Units	Conditions	Notes
V_{LV}	V_{CC} Low Voltage Protection Voltage		2.2	3.1	2.8	V		11

Notes:
1. The V_{CC} voltage specification of 3.0V guarantees 3.3V ±0.3V with typicals at V_{CC} = 3.3V, and the V_{CC} voltage specification of 5.5V guarantees 5.0V ±0.5V with typicals at V_{CC} = 5.0V.
2. Typical voltage is V_{CC} = 5.0V and 3.3V.
3. STANDARD Mode (not Low-EMI Mode).
4. Low-EMI Mode (Not Standard Mode).
5. For analog comparator, inputs when analog comparators are enabled.
6. All outputs unloaded, I/O pins floating, inputs at rail.
7. Same as note 6, except inputs at V_{CC}.
8. Clock must be forced Low, when X_{IN} is clock-driven and X_{OUT} is floating.
9. 0ºC to 70ºC (standard temperature).
10. Autolatch (Mask Option) selected.
11. The V_{LV} voltage increases as the temperature decreases and overlaps lower V_{CC} operating region. See Figure 15.
12. –40°C to 105°C (extended temperature).

Table 40. Additional Timing at Extended Temperature

				T_A = –40ºC to +105ºC 4 MHz				
No	**Sym**	**Parameter**	**V_{CC}[1]**	**Min**	**Max**	**Units**	**Notes**	**D1,D0**
1	T_PC	Input Clock Period	3.0V	250	DC	ns	2,3,4	
			5.5V	250	DC	ns	2,3,4	
2	T_RC, T_FC	Clock Input Rise & Fall Times	3.0V		25	ns	2,3	
			5.5V		25	ns	2,3	
3	T_WC	Input Clock Width	3.0V	125		ns	2,3,4	
			5.5V	125		ns	2,3,4	
4	$T_WT_{IN}L$	Timer Input Low Width	3.0V	100		ns	2,3	
			5.5V	70		ns	2,3	
5	$T_WT_{IN}H$	Timer Input High Width	3.0V	$3T_PC$			2,3	
			5.5V	$3T_PC$			2,3	
6	T_PT_{IN}	Timer Input Period	3.0V	$4T_PC$			2,3	
			5.5V	$4T_PC$			2,3	
7	T_RT_{IN}, T_FT_{IN}	Timer Input Rise & Fall Timer	3.0V		100	ns	2,3	
			5.5V		100	ns	2,3	
8A	T_WIL	Interrupt Request Low Time	3.0V	100		ns	2,3,5	
			5.5V	70		ns	2,3,5	
8B	T_WIL	Interrupt Request Low Time	3.0V	$3T_PC$			2,3,6	
			5.5V	$3T_PC$			2,3,6	

Notes:
1. The V_{CC} voltage specification of 5.5V guarantees 5.0V ±0.5V.
2. The timing reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
3. SMR: D1 = 0.
4. The maximum frequency for the external crystal clock is 4 MHz when using LOW-EMI OSCILLATOR mode.
5. The interrupt request via Port 3 (P31–P33).
6. The interrupt request via Port 3 (P30).
7. SMR: D5 = 1, and the POR Stop-Mode Delay is on.
8. For RC and LC oscillators, and for an oscillator driven by a clock driver.
9. The D1,D0 column applies to the Watch-Dog Timer Mode Register tap selection.
10. 12 µs is the typical delay time.

Standard Test Conditions

The characteristics listed in following pages apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (see Figure 17.)

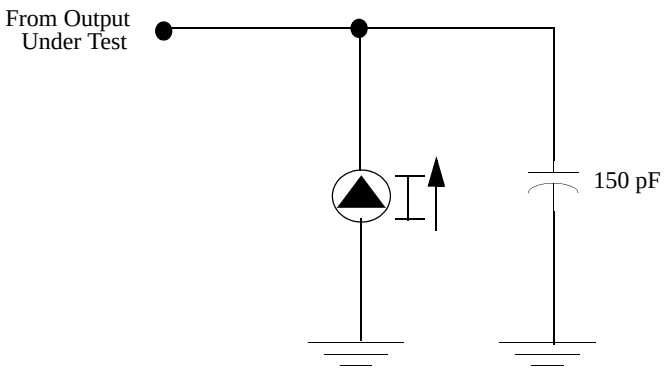


Figure 17.Test Load Diagram

Capacitance

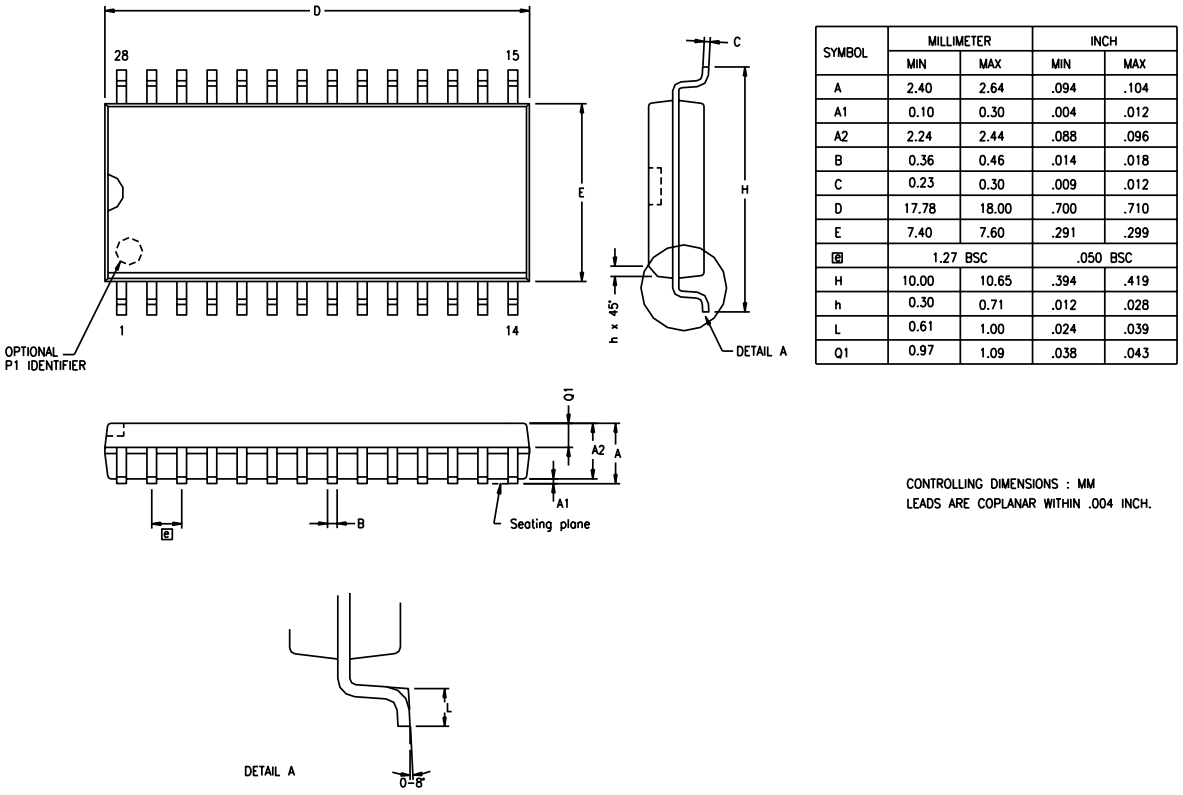
Table 41. Capacitance*

Parameter	Min	Max
Input capacitance	0	12 pF
Output capacitance	0	12 pF
I/O capacitance	0	12 pF

Note: *T_A = 25ºC, V_{CC} = GND = 0V, f = 1.0 MHz, unmeasured pins to GND.

Packaging

Figure 18 illustrates the 28-pin DIP package.



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	2.40	2.64	.094	.104
A1	0.10	0.30	.004	.012
A2	2.24	2.44	.088	.096
B	0.36	0.46	.014	.018
C	0.23	0.30	.009	.012
D	17.78	18.00	.700	.710
E	7.40	7.60	.291	.299
e	1.27 BSC		.050 BSC	
H	10.00	10.65	.394	.419
h	0.30	0.71	.012	.028
L	0.61	1.00	.024	.039
Q1	0.97	1.09	.038	.043

Figure 19.28-Pin SOIC Package Diagram

Ordering Information

Table 42. Ordering Information

Temperature	Speed (4MHz)	Pin Count	Package	Order Number*
Standard	4	28	DIP	Z87C3304PSC
Standard	4	28	SOIC	Z87C3304SSC
Extended	4	28	DIP	Z87C3304PEC