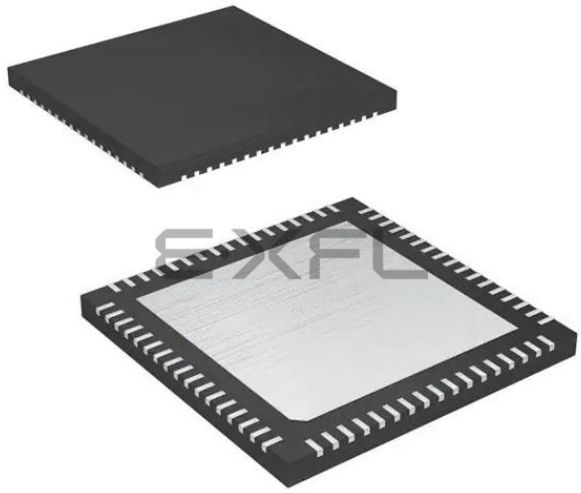

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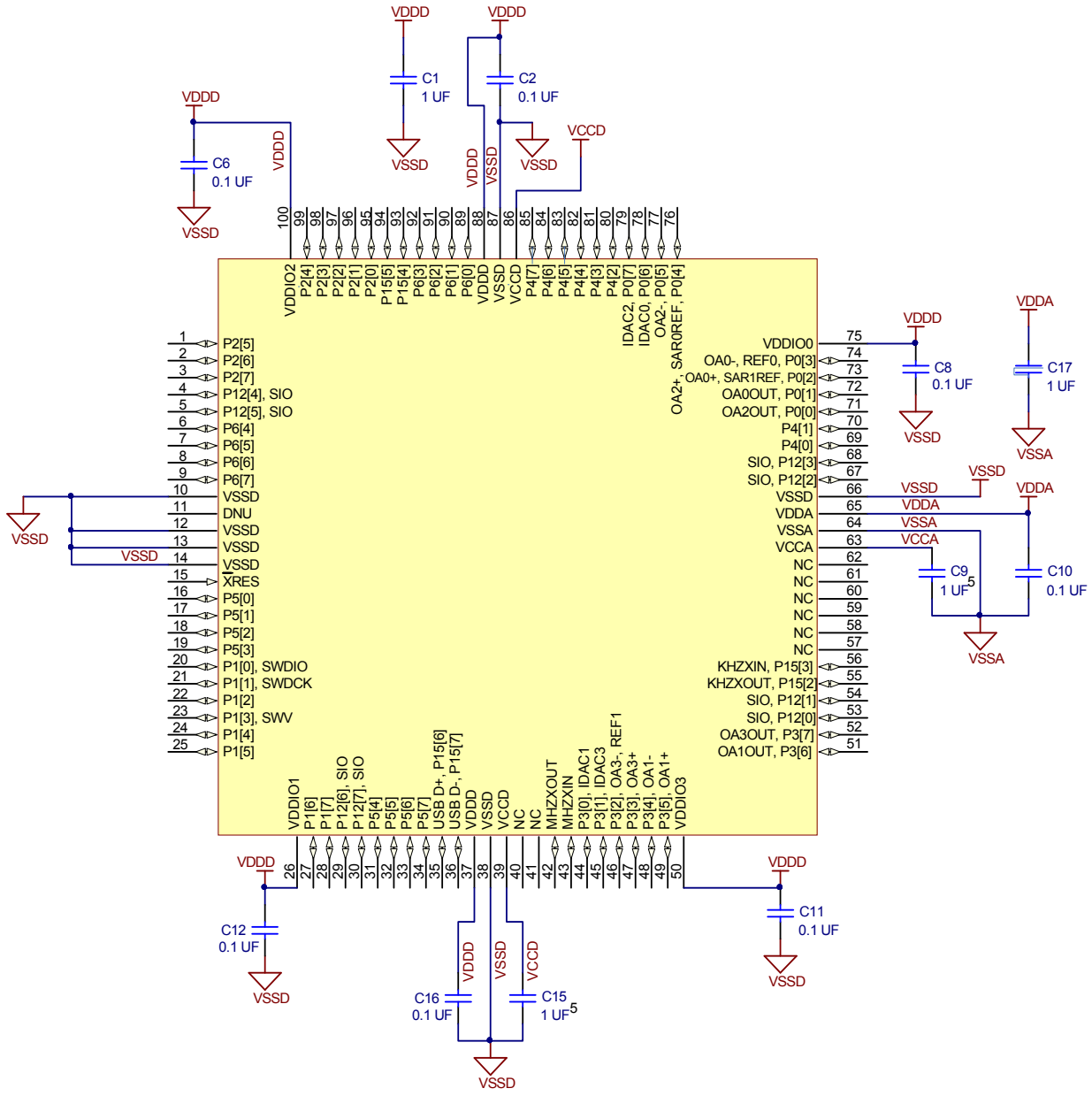
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	67MHz
Connectivity	I²C, LINbus, SPI, UART/USART, USB
Peripherals	CapSense, DMA, LCD, POR, PWM, WDT
Number of I/O	36
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 2x12b; D/A 4x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	68-VFQFN Exposed Pad
Supplier Device Package	68-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c5466lti-063

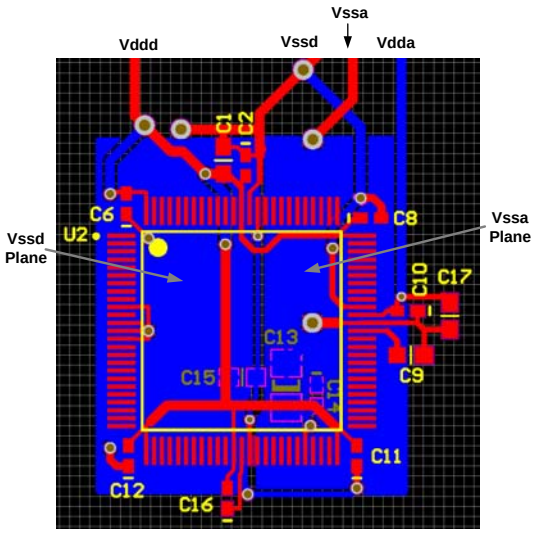
Figure 2-3. Example Schematic for 100-pin TQFP Part with Power Connections



Note The two V_{CCD} pins must be connected together with as short a trace as possible. A trace under the device is recommended, as shown in Figure 2-4.

Note
5. 10 µF is required for sleep mode. See Table 11-3.

Figure 2-4. Example PCB Layout for 100-pin TQFP Part for Optimal Analog Performance



3. Pin Descriptions

IDAC0, IDAC1, IDAC2, IDAC3
Low resistance output pin for high current DACs (IDAC).

OpAmp0out, OpAmp1out, OpAmp2out, OpAmp3out
High current output of uncommitted opamp[6].

Extref0, Extref1
External reference input to the analog system.

OpAmp0–, OpAmp1–, OpAmp2–, OpAmp3–
Inverting input to uncommitted opamp.

OpAmp0+, OpAmp1+, OpAmp2+, OpAmp3+
Noninverting input to uncommitted opamp.

SAR0ref, SAR1ref. External references for SAR ADCs.

GPIO
General purpose I/O pin provides interfaces to the CPU, digital peripherals, analog peripherals, interrupts, LCD segment drive, and CapSense[6].

kHz XTAL: Xo, kHz XTAL: Xi
32.768 kHz crystal oscillator pin.

MHz XTAL: Xo, MHz XTAL: Xi
4 to 25 MHz crystal oscillator pin. If a crystal is not used then Xi must be shorted to ground and Xo must be left floating.

SIO. Special I/O provides interfaces to the CPU, digital peripherals and interrupts with a programmable high threshold voltage, analog comparator, high sink current, and high impedance state when the device is unpowered.

SWDCK
Serial Wire Debug Clock programming and debug port connection. When programming and debugging using SWD is done over USBIOs, the SWDCK pin of port P1[1] is not available for use as a general purpose I/O and should be externally pulled down using a resistor of less than 100 KΩ.

SWDIO
Serial Wire Debug Input and Output programming and debug port connection.

SWV
Single Wire Viewer output.

USBIO, D+
Provides D+ connection directly to a USB 2.0 bus. May be used as a digital I/O pin; it is powered from Vddd instead of from a Vdddio. Pins are Do Not Use (DNU) on devices without USB.

USBIO, D–
Provides D– connection directly to a USB 2.0 bus. May be used as a digital I/O pin; it is powered from Vddd instead of from a Vdddio. Pins are DNU on devices without USB.

V_{CCA}
Output of analog core regulator and input to analog core. Requires a 1 µF capacitor to V_{SSA} (10 µF is required for sleep mode. See Table 11-3). Regulator output not for external use.

V_{CCD}
Output of digital core regulator and input to digital core. The two Vccd pins must be shorted together, with the trace between them as short as possible, and a 1 µF capacitor to V_{SSD} (10 µF is required for sleep mode. See Table 11-3); see Power System on page 21. Regulator output not for external use.

V_{DDA}
Supply for all analog peripherals and analog core regulator. **V_{DDA} must be the highest voltage present on the device. All other supply pins must be less than or equal to V_{DDA}.**[7]

V_{DDD}
Supply for all digital peripherals and digital core regulator. V_{DDD} must be less than or equal to V_{DDA}.[7]

V_{SSA}
Ground for all analog peripherals.

V_{SSD}
Ground for all digital logic and I/O pins.

Vddio0, Vddio1, Vddio2, Vddio3
Supply for I/O pins. Each V_{DDIO} must be tied to a valid operating voltage (2.7 V to 5.5 V), and must be less than or equal to Vdda.

$\overline{XRES}$. External reset pin. Active low with internal pull-up.

RSVD. Reserved pins.

Notes
6. GPIOs with opamp outputs are not recommended for use with CapSense.
7. V_{DDD} and V_{DDA} must be brought up in synchronization with each other, that is, at the same rates and levels. V_{DDA} must be greater than or equal to all other supplies

Table 4-6. Interrupt Vector Table

Interrupt #	Cortex-M3 Exception #	Fixed Function	DMA	UDB
0	16	Low voltage detect (LVD)	phub_termout0[0]	udb_intr[0]
1	17	Cache	phub_termout0[1]	udb_intr[1]
2	18	Reserved	phub_termout0[2]	udb_intr[2]
3	19	Pwr Mgr	phub_termout0[3]	udb_intr[3]
4	20	PICU[0]	phub_termout0[4]	udb_intr[4]
5	21	PICU[1]	phub_termout0[5]	udb_intr[5]
6	22	PICU[2]	phub_termout0[6]	udb_intr[6]
7	23	PICU[3]	phub_termout0[7]	udb_intr[7]
8	24	PICU[4]	phub_termout0[8]	udb_intr[8]
9	25	PICU[5]	phub_termout0[9]	udb_intr[9]
10	26	PICU[6]	phub_termout0[10]	udb_intr[10]
11	27	PICU[12]	phub_termout0[11]	udb_intr[11]
12	28	PICU[15]	phub_termout0[12]	udb_intr[12]
13	29	Comparators Combined	phub_termout0[13]	udb_intr[13]
14	30	Switched Caps Combined	phub_termout0[14]	udb_intr[14]
15	31	I^2C	phub_termout0[15]	udb_intr[15]
16	32	Reserved	phub_termout1[0]	udb_intr[16]
17	33	Reserved	phub_termout1[1]	udb_intr[17]
18	34	Reserved	phub_termout1[2]	udb_intr[18]
19	35	Reserved	phub_termout1[3]	udb_intr[19]
20	36	Reserved	phub_termout1[4]	udb_intr[20]
21	37	USB SOF Int	phub_termout1[5]	udb_intr[21]
22	38	USB Arb Int	phub_termout1[6]	udb_intr[22]
23	39	USB Bus Int	phub_termout1[7]	udb_intr[23]
24	40	USB Endpoint[0]	phub_termout1[8]	udb_intr[24]
25	41	USB Endpoint Data	phub_termout1[9]	udb_intr[25]
26	42	Reserved	phub_termout1[10]	udb_intr[26]
27	43	Reserved	phub_termout1[11]	udb_intr[27]
28	44	DFB Int	phub_termout1[12]	udb_intr[28]
29	45	Decimator Int	phub_termout1[13]	udb_intr[29]
30	46	phub_err_int	phub_termout1[14]	udb_intr[30]
31	47	eeprom_fault_int	phub_termout1[15]	udb_intr[31]

- Eight fully programmable 16-bit clock dividers generate digital system clocks for general use in the digital system, as configured by the design's requirements. Digital system clocks can generate custom clocks derived from any of the seven clock sources for any purpose. Examples include baud rate generators, accurate PWM periods, and timer clocks, and many others. If more than eight digital clock dividers are required, the Universal Digital Blocks (UDBs) and fixed function Timer/Counter/PWMs can also generate clocks.
- Four 16-bit clock dividers generate clocks for the analog system components that require clocking, such as ADCs and mixers. The analog clock dividers include skew control to ensure that critical analog events do not occur simultaneously with digital switching events. This is done to reduce analog system noise.

Each clock divider consists of an 8-input multiplexer, a 16-bit clock divider (divide by 2 and higher) that generates ~50% duty cycle clocks, system clock resynchronization logic, and deglitch logic. The outputs from each digital clock tree can be routed into the digital system interconnect and then brought back into the clock system as an input, allowing clock chaining of up to 32 bits.

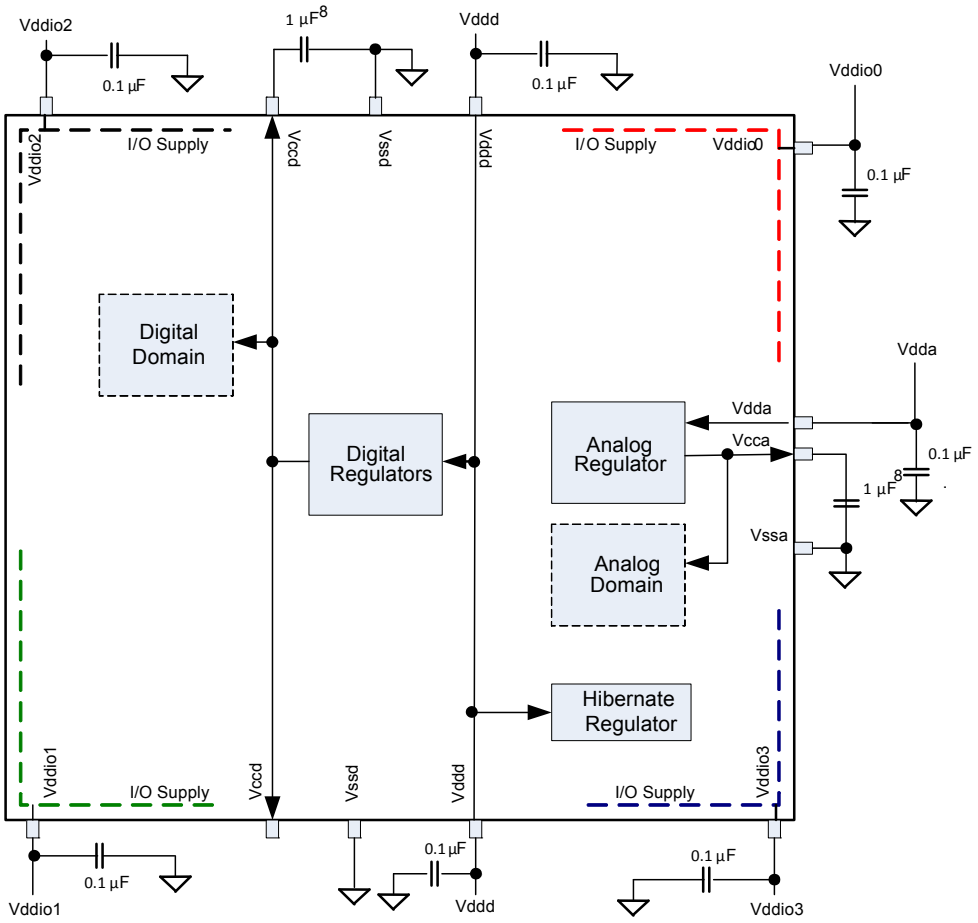
6.1.4 USB Clock Domain

The USB clock domain is unique in that it operates largely asynchronously from the main clock network. The USB logic contains a synchronous bus interface to the chip, while running on an asynchronous clock to process USB data. The USB logic requires a 48 MHz frequency. This frequency can be generated from different sources, including DSI clock at 48 MHz or doubled value of 24 MHz from the MHzECO or DSI signal.

6.2 Power System

The power system consists of separate analog, digital, and I/O supply pins, labeled V_{DDA}, V_{DDD}, and Vddiox, respectively. It also includes two internal 1.8 V regulators that provide the digital (V_{CCD}) and analog (V_{CCA}) supplies for the internal core logic. The output pins of the regulators (V_{CCD} and V_{CCA}) and the V_{DDIO} pins must have capacitors connected as shown in Figure 6-4 (10 µF is required for sleep mode. See Table 11-3). The two V_{CCD} pins must be shorted together, with as short a trace as possible. The power system also contains a hibernate regulator.

Figure 6-4. PSoC Power System



Note The two V_{CCD} pins must be connected together with as short a trace as possible. A trace under the device is recommended, as shown in Figure 2-4.

Note
8. 10 µF is required for sleep mode. See Table 11-3.

Figure 6-8. SIO Input/Output Block Diagram

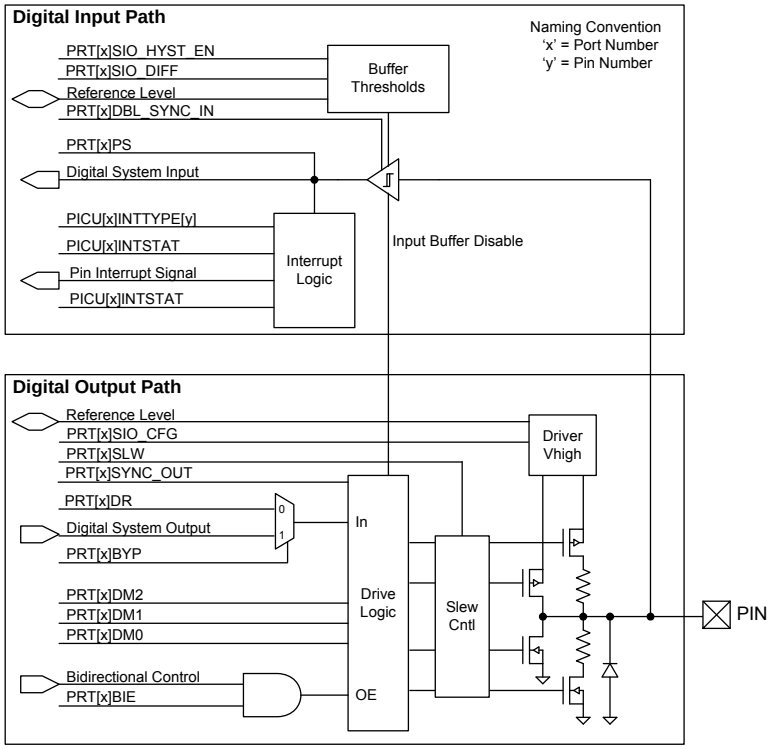
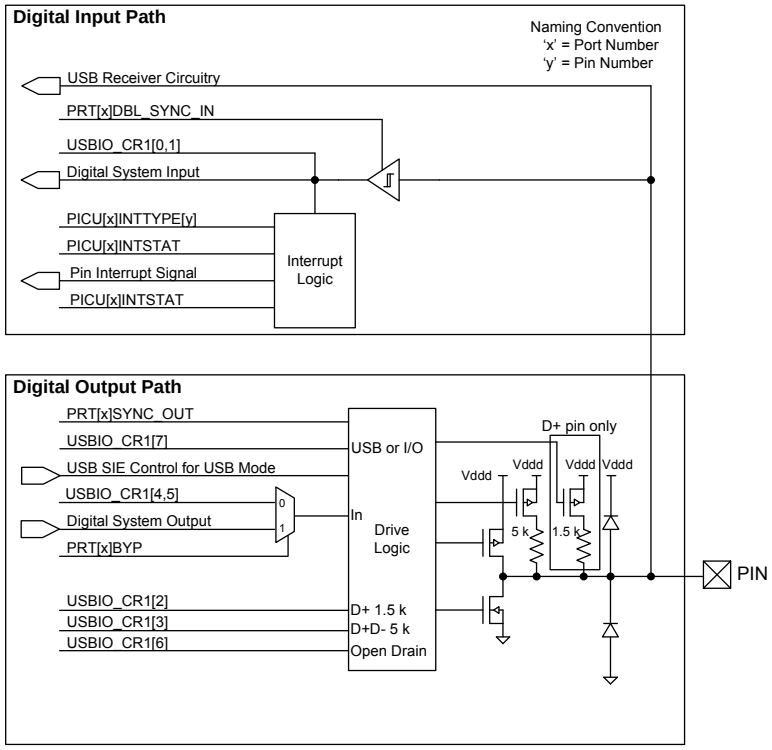


Figure 6-9. USBIO Block Diagram



7.1.2 Example Analog Components

The following is a sample of the analog components available in PSoC Creator for the CY8C54 family. The exact amount of hardware resources (SC/CT blocks, routing, RAM, flash) used by a component varies with the features selected in PSoC Creator for the component.

- Amplifiers
  - TIA
  - PGA
  - opamp
- ADCs
  - Successive Approximation (SAR)
- DACs
  - Current
  - Voltage
  - PWM
- Comparators
- Mixers

7.1.3 Example System Function Components

The following is a sample of the system function components available in PSoC Creator for the CY8C54 family. The exact amount of hardware resources (UDBs, DFB taps, SC/CT blocks, routing, RAM, flash) used by a component varies with the features selected in PSoC Creator for the component.

- CapSense
- LCD Drive
- LCD Control
- Filters

7.1.4 Designing with PSoC Creator

7.1.4.1 More Than a Typical IDE

A successful design tool allows for the rapid development and deployment of both simple and complex designs. It reduces or eliminates any learning curve. It makes the integration of a new design into the production stream straightforward.

PSoC Creator is that design tool.

PSoC Creator is a full featured Integrated Development Environment (IDE) for hardware and software design. It is optimized specifically for PSoC devices and combines a modern, powerful software development platform with a sophisticated graphical design tool. This unique combination of tools makes PSoC Creator the most flexible embedded design platform available.

Graphical design entry simplifies the task of configuring a particular part. You can select the required functionality from an extensive catalog of components and place it in your design. All components are parameterized and have an editor dialog that allows you to tailor functionality to your needs.

PSoC Creator automatically configures clocks and routes the I/O to the selected pins and then generates APIs to give the application complete control over the hardware. Changing the PSoC device configuration is as simple as adding a new component, setting its parameters, and rebuilding the project.

At any stage of development you are free to change the hardware configuration and even the target processor. To retarget your application (hardware and software) to new devices, even from 8- to 32-bit families, just select the new device and rebuild.

You also have the ability to change the C compiler and evaluate an alternative. Components are designed for portability and are validated against all devices, from all families, and against all supported tool chains Switching compilers is as easy as editing the from the project options and rebuilding the application with no errors from the generated APIs or boot code.

7.4.1 I/O Port Routing

There are a total of 20 DSI routes to a typical 8-bit I/O port, 16 for data and four for drive strength control.

When an I/O pin is connected to the routing, there are two primary connections available, an input and an output. In conjunction with drive strength control, this can implement a bidirectional I/O pin. A data output signal has the option to be single synchronized (pipelined) and a data input signal has the option to be double synchronized. The synchronization clock is the system clock (see Figure 6-1). Normally all inputs from pins are synchronized as this is required if the CPU interacts with the signal or any signal derived from it. Asynchronous inputs have rare uses. An example of this is a feed through of combinational PLD logic from input pins to output pins.

Figure 7-15. I/O Pin Synchronization Routing

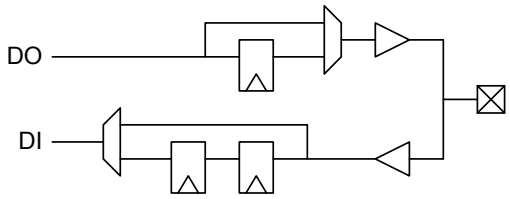
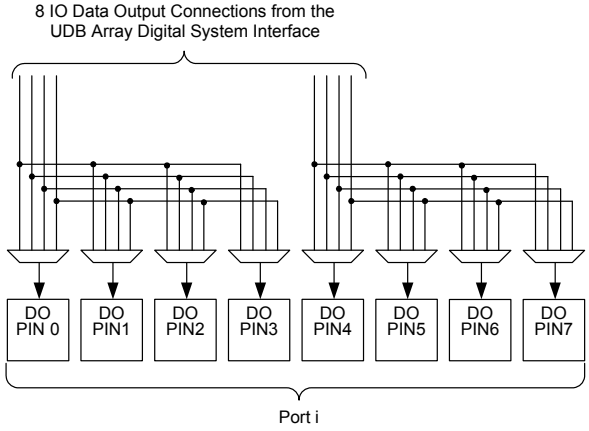
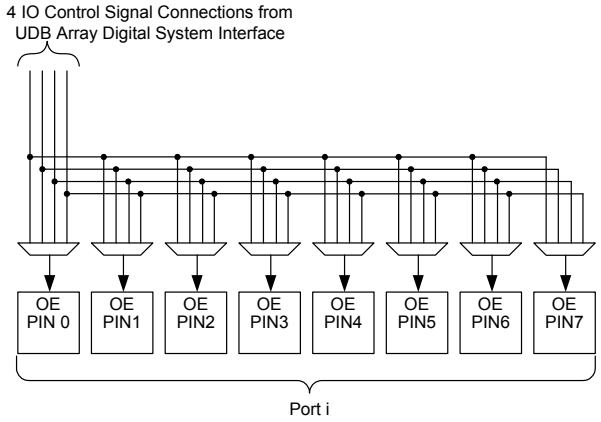


Figure 7-16. I/O Pin Output Connectivity



There are four more DSI connections to a given I/O port to implement dynamic output enable control of pins. This connectivity gives a range of options, from fully ganged 8-bits controlled by one signal, to up to four individually controlled pins. The output enable signal is useful for creating tri-state bidirectional pins and buses.

Figure 7-17. I/O Pin Output Enable Connectivity



7.5 USB

PSoC includes a dedicated FS (12 Mbps) USB 2.0 transceiver supporting all four USB transfer types: control, interrupt, bulk, and isochronous. PSoC Creator provides full configuration support. USB interfaces to hosts through two dedicated USBIO pins, which are detailed in the "I/O System and Routing" section on page 24.

When using USB, either a crystal must be used (24 MHz with MHzECO) or a similar high-accuracy clock source must be provided externally through a pin and the DSI. Also, bus clock must be equal to 33 MHz. See *Section 6.1* on page 18 for details.

USB includes the following features:

- Eight unidirectional data endpoints
- One bidirectional control endpoint 0 (EP0)
- Shared 512-byte buffer for the eight data endpoints
- Dedicated 8-byte buffer for EP0
- Two memory modes
  - Manual Memory Management with No DMA Access
  - Manual Memory Management with Manual DMA Access
- Internal 3.3 V regulator for transceiver
- Interrupts on bus and each endpoint event
- USB Reset, Suspend, and Resume operations
- Bus powered and self powered modes

Figure 7-18. USB

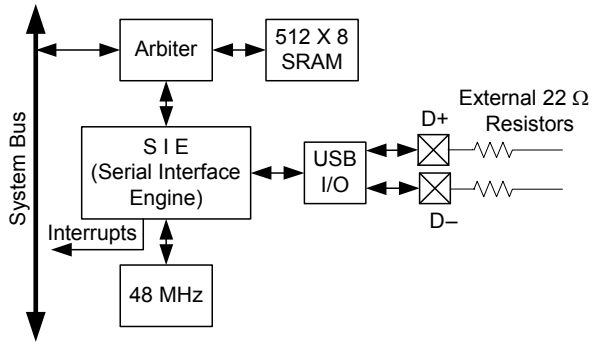
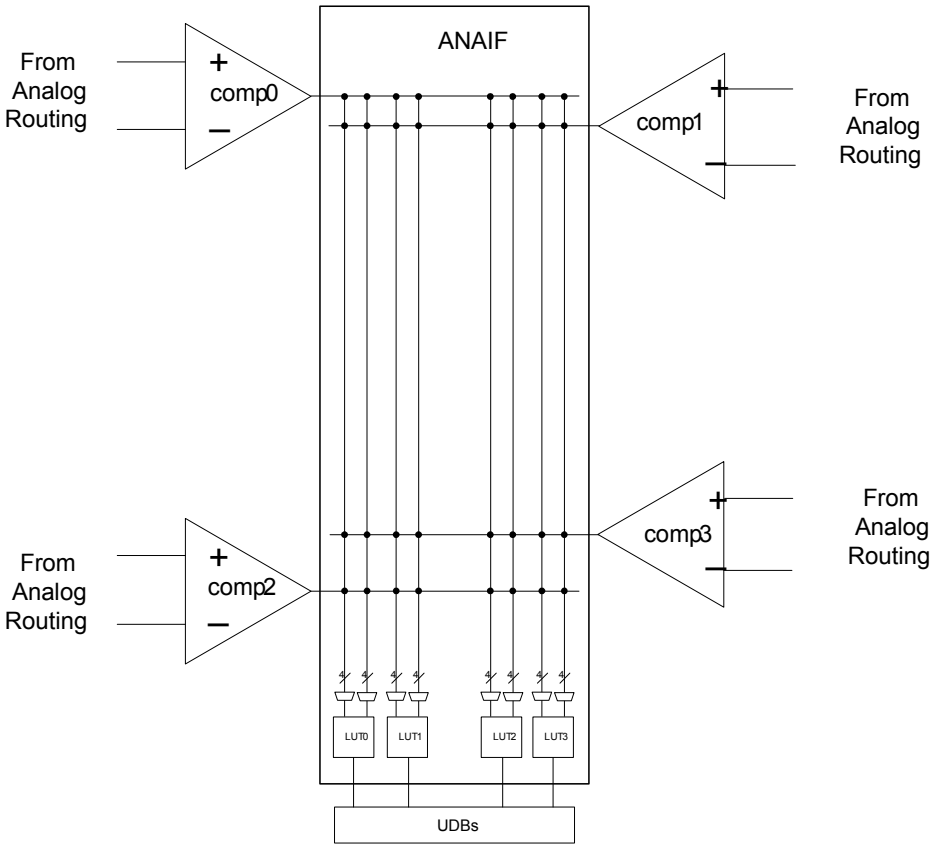


Figure 8-4. Analog Comparator



8.3.2 LUT

The CY8C54 family of devices contains four LUTs. The LUT is a two input, one output lookup table that is driven by any one or two of the comparators in the chip. The output of any LUT is routed to the digital system interface of the UDB array. From the digital system interface of the UDB array, these signals can be connected to UDBs, DMA controller, I/O, or the interrupt controller.

The LUT control word written to a register sets the logic function on the output. The available LUT functions and the associated control word is shown in Table 8-1.

Table 8-1. LUT Function vs. Program Word and Inputs

Control Word	Output (A and B are LUT inputs)
0000b	**FALSE** (‘0’)
0001b	**A** AND **B**
0010b	**A** AND (NOT **B**)
0011b	A
0100b	(NOT **A**) AND **B**
0101b	B
0110b	**A** XOR **B**
0111b	**A** OR **B**
1000b	**A** NOR **B**
1001b	**A** XNOR **B**
1010b	NOT **B**
1011b	**A** OR (NOT **B**)
1100b	NOT **A**
1101b	(NOT **A**) OR **B**
1110b	**A** NAND **B**
1111b	**TRUE** (‘1’)

Figure 11-7. GPIO Output Rise and Fall Times, Fast Strong Mode, V_{DDIO} = 3.3 V, 25 pF Load

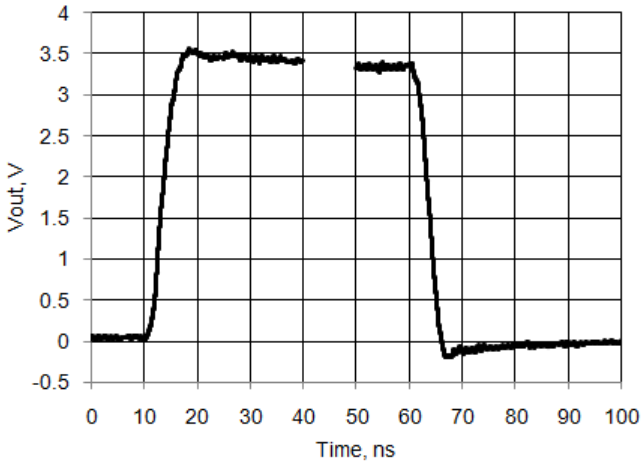
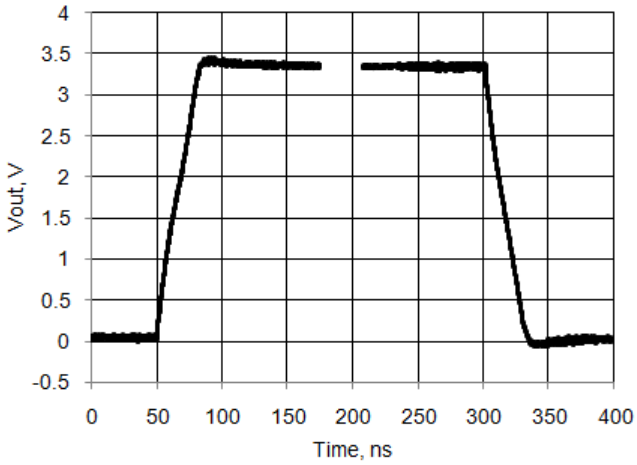


Figure 11-8. GPIO Output Rise and Fall Times, Slow Strong Mode, V_{DDIO} = 3.3 V, 25 pF Load



11.4.2 SIO

Note that under certain conditions an SIO pin may cause up to 1 mA of additional current to be drawn from the related V_{DDIO} pin. If an SIO pin's voltage exceeds its V_{DDIO} supply by 0.5 V, the trigger condition is set. After the trigger condition is set, the SIO pin causes increased current when its voltage is between V_{SSD} + 0.5 V and V_{DDIO} – 0.5 V. The trigger condition is reset when the SIO pin is brought within the range of V_{SSD} to V_{SSD} + 0.5 V. The trigger condition may unknowningly be met during device powerup due to differences in supply ramps.

Table 11-8. SIO DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
Vinmax	Maximum input voltage	All allowed values of Vddio and Vddd, see *Section 11.2.1*	–	–	5.5	V
Vinref	Input voltage reference (Differential input mode)		0.5	–	0.52 ×V_{DDIO}	V
Voutref	Output voltage reference (Regulated output mode)					
		V_{DDIO} > 3.7	1	–	V_{DDIO}–1	V
		V_{DDIO} < 3.7	1	–	V_{DDIO} – 0.5	V
V_{IH}	Input voltage high threshold					
	GPIO mode	CMOS input	0.7 × V_{DDIO}	–	–	V
	Differential input mode[28]	Hysteresis disabled	SIO_ref + 0.2	–	–	V
V_{IL}	Input voltage low threshold					
	GPIO mode	CMOS input	–	–	0.3 × V_{DDIO}	V
	Differential input mode[28]	Hysteresis disabled	–	–	SIO_ref – 0.2	V
V_{OH}	Output voltage high					
	Unregulated mode	I_{OH} = 4 mA, V_{DDIO} = 3.3 V	V_{DDIO} – 0.4	–	–	V
	Regulated mode[28]	I_{OH} = 1 mA	SIO_ref – 0.65	–	SIO_ref + 0.2	V
	Regulated mode[28]	I_{OH} = 0.1 mA	SIO_ref – 0.3	–	SIO_ref + 0.2	V
V_{OL}	Output voltage low	V_{DDIO} = 3.30 V, I_{OL} = 25 mA	–	–	0.8	V
Rpullup	Pull up resistor		3.5	5.6	8.5	kΩ
Rpulldown	Pull down resistor		3.5	5.6	8.5	kΩ

Note
28. See Figure 6-8 on page 26 and Figure 6-11 on page 29 for more information on SIO reference.
29. Based on device characterization (Not production tested).

11.4.3 USBIO

For operation in GPIO mode, the standard range for V_{DDD} applies, see Device Level Specifications on page 55.

Table 11-10. USBIO DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
Rusbi	USB D+ pull-up resistance	With idle bus	0.900	–	1.575	kΩ
Rusba	USB D+ pull-up resistance	While receiving traffic	1.425	–	3.090	kΩ
Vohusb	Static output high	15 kΩ ±5% to Vss, internal pull-up enabled	2.8	–	3.6	V
Volusb	Static output low	15 kΩ ±5% to Vss, internal pull-up enabled	–	–	0.3	V
Vihgpio	Input voltage high, GPIO mode	$V_{DDD} \geq 3$ V	2	–	–	V
Vilgpio	Input voltage low, GPIO mode	$V_{DDD} \geq 3$ V	–	–	0.8	V
Vohgpio	Output voltage high, GPIO mode	I_{OH} = 4 mA, $V_{DDD} \geq 3$ V	2.4	–	–	V
Volgpio	Output voltage low, GPIO mode	I_{OL} = 4 mA, $V_{DDD} \geq 3$ V	–	–	0.3	V
Vdi	Differential input sensitivity	|(D+)–(D–)|	–	–	0.2	V
Vcm	Differential input common mode range		0.8	–	2.5	V
Vse	Single ended receiver threshold		0.8	–	2	V
Rps2	PS/2 pull-up resistance	In PS/2 mode, with PS/2 pull-up enabled	3	–	7	kΩ
Rext	External USB series resistor	In series with each USB pin	21.78 (–1%)	22	22.22 (+1%)	Ω
Zo	USB driver output impedance[32]	Including Rext	28	–	44	Ω
C_{IN}	USB transceiver input capacitance		–	–	20	pF
I_{IL}[33]	Input leakage current (absolute value)	25 °C, V_{DDD} = 3.0 V	–	–	2	nA

Figure 11-14. USBIO Output High Voltage and Current, GPIO Mode

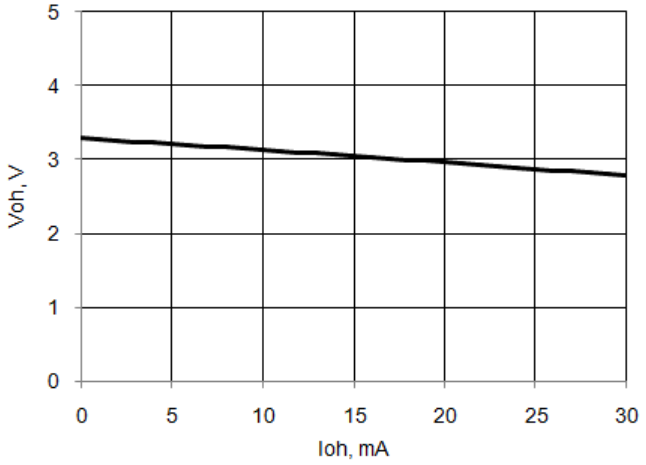
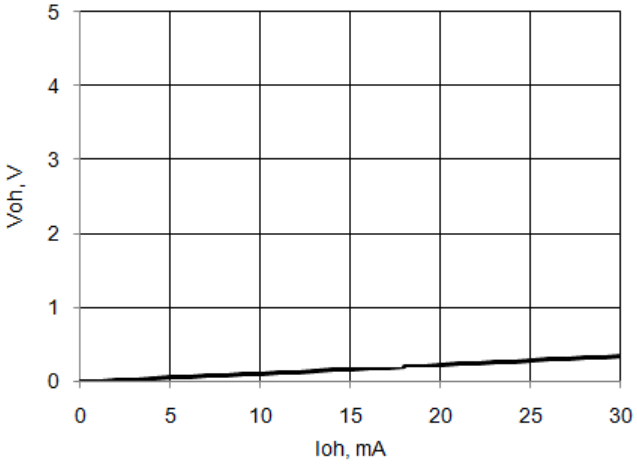


Figure 11-15. USBIO Output Low Voltage and Current, GPIO Mode

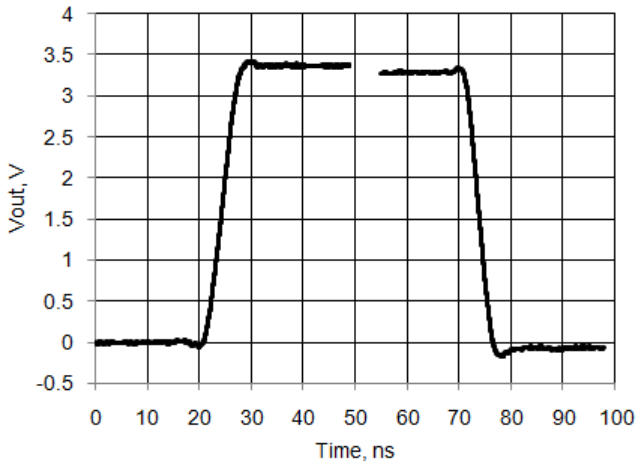


Notes
32. This parameter is not production tested and cannot be guaranteed over all temperatures.
33. Based on device characterization (Not production tested).

Table 11-11. USBIO AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
Tdrate	Full-speed data rate average bit rate	Using external 24 MHz crystal	12 – 0.25%	12	12 + 0.25%	MHz
Tjr1	Receiver data jitter tolerance to next transition		–8	–	8	ns
Tjr2	Receiver data jitter tolerance to pair transition		–5	–	5	ns
Tdj1	Driver differential jitter to next transition		–3.5	–	3.5	ns
Tdj2	Driver differential jitter to pair transition		–4	–	4	ns
Tfdeop	Source jitter for differential transition to SE0 transition		–2	–	5	ns
Tfeopt	Source SE0 interval of EOP		160	–	175	ns
Tfeopr	Receiver SE0 interval of EOP		82	–	–	ns
Tfst	Width of SE0 interval during differential transition		–	–	14	ns
Fgpio_out	GPIO mode output operating frequency	$3\ V \le V_{DDD} \le 5.5\ V$	–	–	20	MHz
		$V_{DDD} = 2.7\ V$	–	–	6	MHz
Tr_gpio	Rise time, GPIO mode, 10%/90% V_{DDD}	$V_{DDD} > 3\ V$, 25 pF load	–	–	12	ns
		$V_{DDD} = 2.7\ V$, 25 pF load	–	–	40	ns
Tf_gpio	Fall time, GPIO mode, 90%/10% V_{DDD}	$V_{DDD} > 3\ V$, 25 pF load	–	–	12	ns
		$V_{DDD} = 2.7\ V$, 25 pF load	–	–	40	ns

Figure 11-16. USBIO Output Rise and Fall Times, GPIO Mode, V_{DDD} = 3.3 V, 25 pF Load



11.5 Analog Peripherals

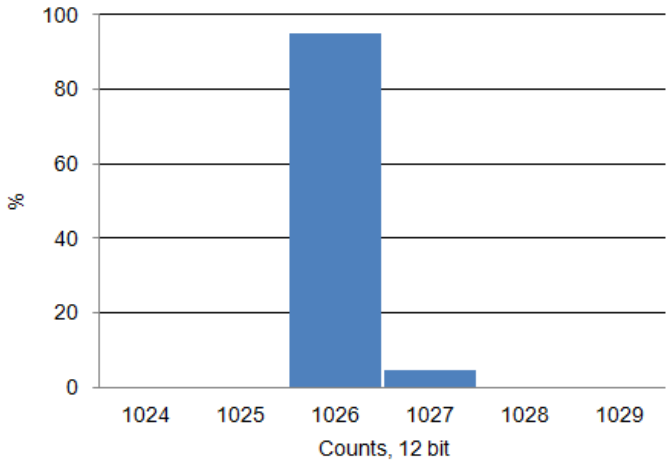
Specifications are valid for –40 °C ≤ T_A ≤ 85 °C and T_J ≤ 100 °C, except where noted. Specifications are valid for 2.7 V to 5.5 V, except where noted.

11.5.1 Opamp

Table 11-15. Opamp DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
V_I	Input voltage range		V_{SSA}	–	V_{DDA}	V
V_{OS}	Input offset voltage	Operating temperature > 70 °C	–	–	3	mV
		Operating temperature –40 °C to 70 °C	–	–	2	mV
TCV_{OS}	Input offset voltage drift with temperature		–	–	±30	µV / °C
Ge1	Gain error, unity gain buffer mode	Rload = 1 kΩ	–	–	±0.1	%
C_{IN}	Input capacitance	Routing from pin	–	–	18	pF
Vo	Output voltage range	1 mA, source or sink	V_{SSA} + 0.05	–	V_{DDA} – 0.05	V
I_{OUT}	Output current, source or sink	V_{SSA} + 500 mV ≤ Vout ≤ V_{DDA} –500 mV	10	–	–	mA
I_{DD}	Quiescent current	Vssa + 50 mV < V_{IN} < V_{DDA}-50 mV	–	1	2.5	mA
CMRR	Common mode rejection ratio		80	–	–	dB
PSRR	Power supply rejection ratio		75	–	–	dB

Figure 11-29. SAR ADC Noise Histogram, 1000 samples, 700 ksps, External Reference, V_{IN} = VREF/2



11.5.4 Analog Globals

Table 11-20. Analog Globals DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
Rppag	Resistance pin-to-pin through analog global	V_{DDA} = 3.0 V	–	1200	1500	Ω
Rppmuxbus	Resistance pin-to-pin through analog mux bus	V_{DDA} = 3.0 V	–	700	1000	Ω

Table 11-24. IDAC AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
F_{DAC}	Update rate		–	–	5.5	Msps
T_{SETTLE}	Settling time to 0.5 LSB	Range = 31.875 µA or 255 µA, full scale transition, fast mode, 600 Ω 15-pF load	–	–	180	ns
	Current noise	Range = 255 µA, source mode, fast mode, Vdda = 5 V, 10 kHz	–	340	–	pA/sqrtHz

Figure 11-40. IDAC Step Response, Codes 0x40 - 0xC0, 255 µA Mode, Source Mode, Fast Mode, Vdda = 5 V

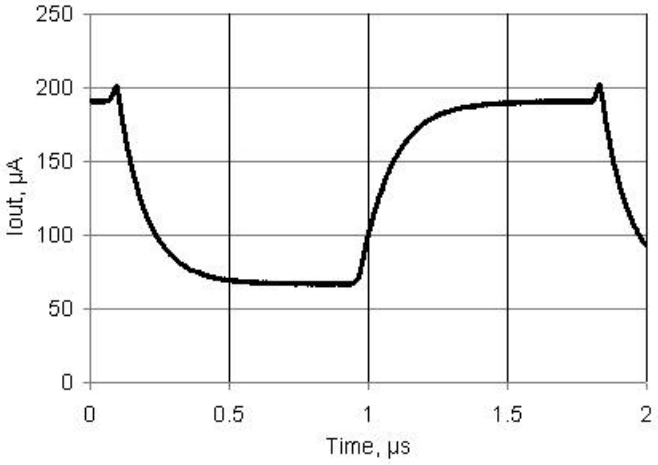


Figure 11-41. IDAC PSRR vs Frequency

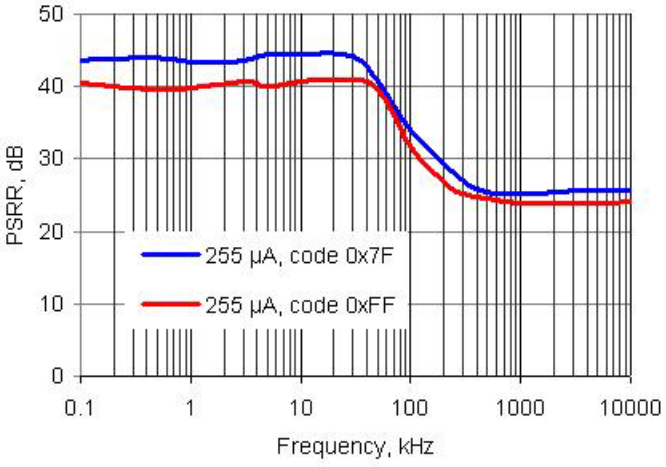


Figure 11-42. IDAC Glitch Response, Codes 0x7F - 0x80, 255 µA Mode, Source Mode, Fast Mode, Vdda = 5 V

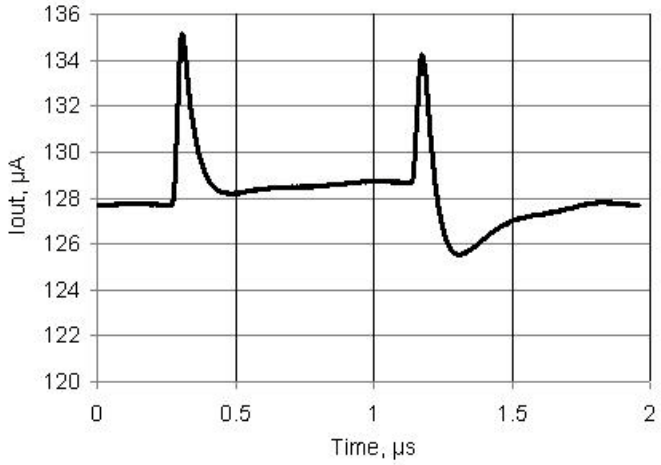


Figure 11-43. IDAC Current Noise, 255 µA Mode, Source Mode, Fast Mode, V_{DDA} = 5 V

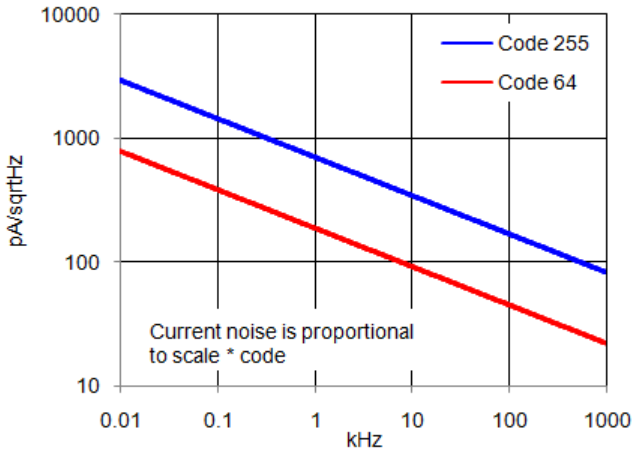


Figure 11-46. VDAC INL vs Temperature, 1 V Mode

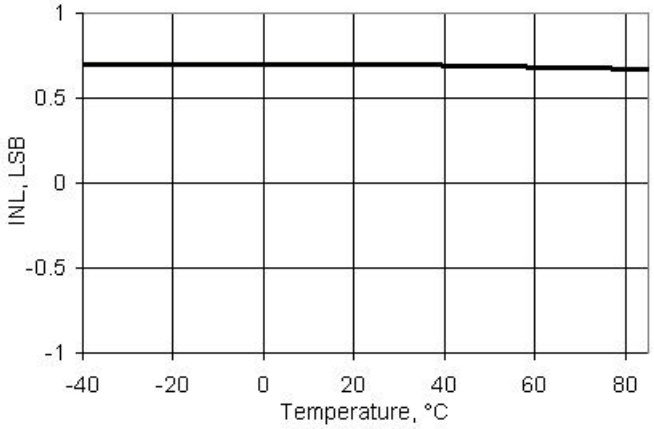


Figure 11-47. VDAC Full Scale Error vs Temperature, 1 V Mode

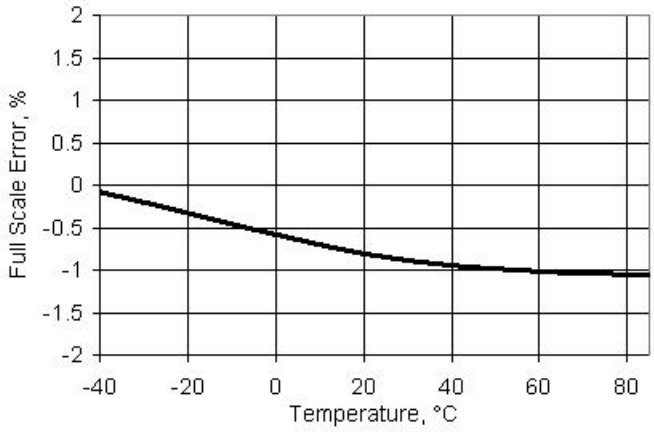


Figure 11-48. VDAC Operating Current vs Temperature, 1 V Mode, Slow Mode

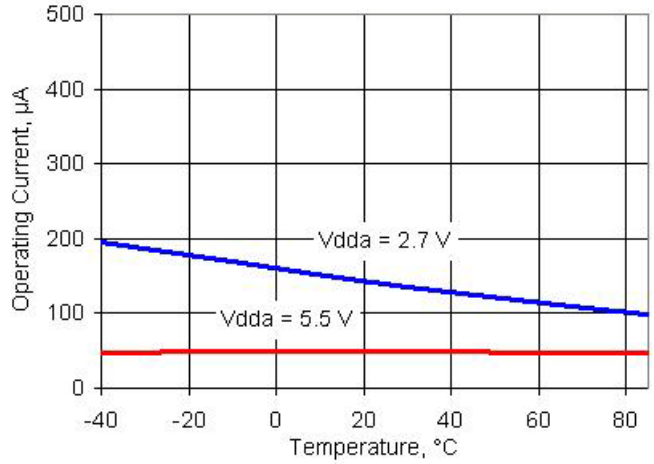


Figure 11-49. VDAC DNL vs Temperature, 1 V Mode

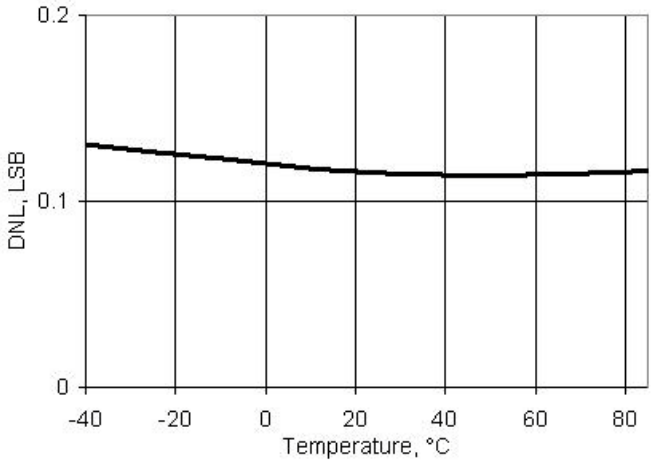


Figure 11-50. VDAC Full Scale Error vs Temperature, 4 V Mode

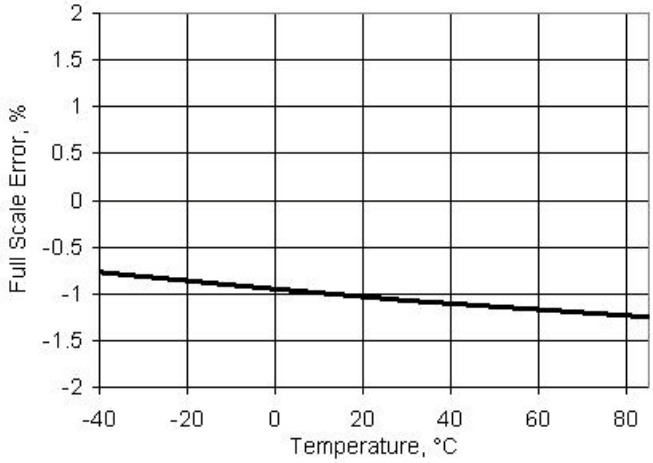
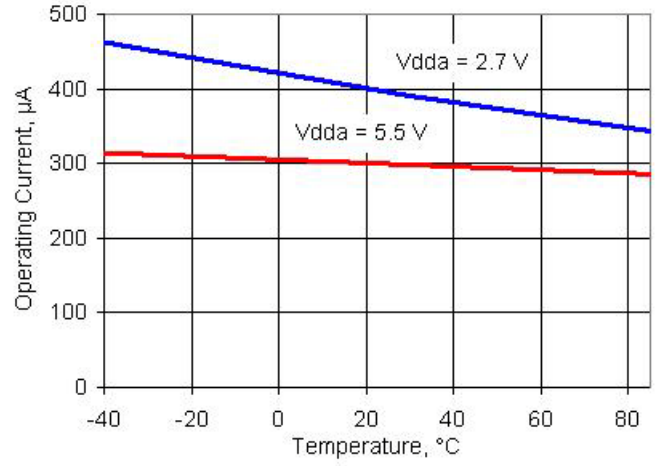


Figure 11-51. VDAC Operating Current vs Temperature, 1 V Mode, Fast Mode



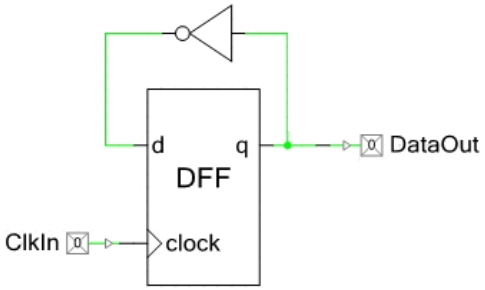
11.6.7 Universal Digital Blocks (UDBs)

PSoC Creator provides a library of pre-built and tested standard digital peripherals (UART, SPI, LIN, PRS, CRC, timer, counter, PWM, AND, OR, and so on) that are mapped to the UDB array. See the component data sheets in PSoC Creator for full AC/DC specifications, APIs, and example code.

Table 11-46. UDB AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
Datapath Performance						
F_{MAX_TIMER}	Maximum frequency of 16-bit timer in a UDB pair		–	–	67.01	MHz
F_{MAX_ADDER}	Maximum frequency of 16-bit adder in a UDB pair		–	–	67.01	MHz
F_{MAX_CRC}	Maximum frequency of 16-bit CRC/PRS in a UDB pair		–	–	67.01	MHz
PLD Performance						
F_{MAX_PLD}	Maximum frequency of a two-pass PLD function in a UDB pair		–	–	67.01	MHz
Clock to Output Performance						
t_{CLK_OUT}	Propagation delay for clock in to data out, see Figure 11-58.	25 °C	–	20	28	ns
t_{CLK_OUT}	Propagation delay for clock in to data out, see Figure 11-58.	Worst-case placement, routing, and pin selection	–	–	55	ns

Figure 11-58. Clock to Output Performance



11.9 Clocking

Specifications are valid for –40 °C ≤ T_A ≤ 85 °C and T_J ≤ 100 °C, except where noted. Specifications are valid for 2.7 V to 5.5 V, except where noted. Unless otherwise specified, all charts and graphs show typical values.

11.9.1 kHz External Crystal Oscillator (kHzECO)

For more information on crystal selection for the kHzECO, refer to application note AN54439: PSoC 3 and PSoC 5 External Oscillators.

Table 11-59. kHz ECO DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
I_{DD}	Oscillator operating current	Low power mode; CL = 6 pF	–	0.25	–	µA
C_{IN}	Capacitance at Pins kHz-XTAL:Xi and kHz-XTAL:Xo[49]		–	5	7	pF

Table 11-60. kHz ECO Crystal Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
F	Crystal frequency		–	32.768	–	kHz
C_L	Crystal load capacitance	Recommended values	–	6 or 12.5	–	pF
D_L	Crystal drive level tolerance		1	–	–	µW

11.9.2 Internal Main Oscillator

Table 11-61. IMO DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Supply current					
	48 MHz		–	465	850	µA
	24 MHz		–	195	500	µA
	12 MHz		–	150	450	µA
	6 MHz		–	120	400	µA
	3 MHz		–	105	300	µA

Note
49. Based on device characterization (Not production tested).

Figure 11-60. IMO Current vs. Frequency

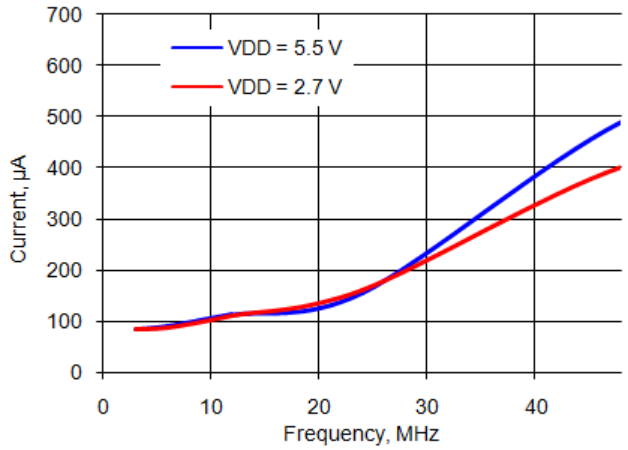


Table 11-62. IMO AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
F_{IMO}	IMO frequency stability (with factory trim)					
	48 MHz		–10	–	10	%
	24 MHz		–8	–	8	%
	12 MHz		–6.25	–	6.25	%
	6 MHz		–5.8	–	5.8	%
	3 MHz		–5	–	5	%
	Startup time[50]	From enable (during normal system operation) or wakeup from low power state	–	–	12	µs
Jp–p	Jitter (peak to peak)[50]					
	F = 24 MHz		–	0.5	–	ns
	F = 3 MHz		–	2.3	–	ns

Figure 11-61. IMO Frequency Variation vs. Temperature

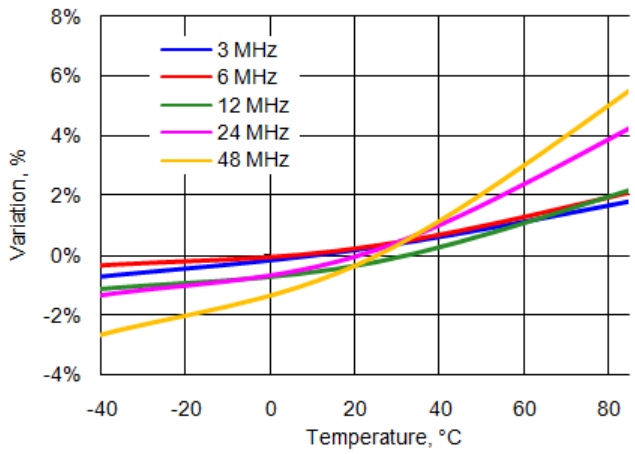
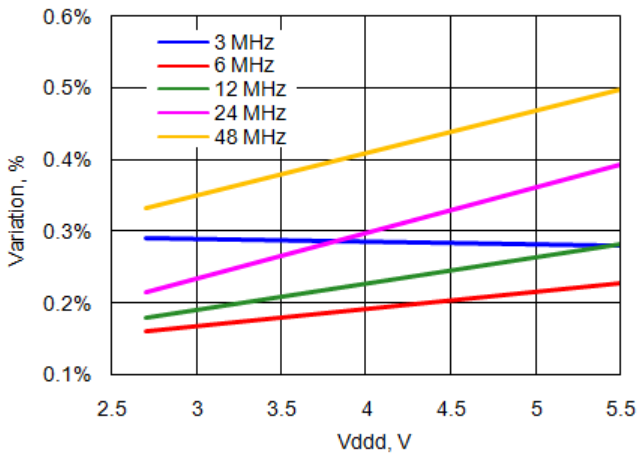


Figure 11-62. IMO Frequency Variation vs. V_{DDD}



Note
50. Based on device characterization (Not production tested).

Description Title: PSoC® 5: CY8C54 Family Datasheet Programmable System-on-Chip (PSoC®) Document Number: 001-66238				
*D	3428148	02/15/2011	WKA/MKEA	Moved status from Preliminary to Final. Changed pins 5, 7, and 8 to VSSD and pin 6 to DNU in 68-pin QFN pinout. Changed pins 10, 12, and 13 to VSSD and pin 11 to DNU in 100-pin TQFP pinout. Changed pins 10, 12, and 13 to VSSD and pin 11 to DNU in Typical Application Schematic. Updated latch up specs in Table 11-1. Updated I_{DD} parameter (Active mode) in Table 11-2. Updated sleep and hibernate current. Updated "DAC" section on page 48. Added note on strobing DAC twice. Updated "SIO" section on page 60. Added note on conditions for SIO to draw excess current. Updated pinout diagrams (Figure 2-1, Figure 2-2, and Figure 2-3). Updated Table 11-2 to include Power consumption details. Updated active, sleep and hibernate modes current specifications (Table 11-2, Table 6-3). Updated latch up current specification (Table 11-1). Updated ESD_{HBM} specification (Table 11-1). Updated "USB" section on page 39. Added note on required clock sources for using USB. Updated GPIO, SIO and USBIO graphs (Figure 11-5, Figure 11-6, Figure 11-7, Figure 11-8, Figure 11-9, Figure 11-10, Figure 11-11, Figure 11-12, Figure 11-13, Figure 11-14, Figure 11-15, and Figure 11-16) Added active mode current graph. (Figure 11-1). Updated LVI / HVI table in Section 6 (Table 6-4, Analog/Digital Low Voltage Interrupt, Analog High Voltage Interrupt). Updated GPIO block diagram (Figure 6-7). Updated Table 11-1 IV_{DDIO} spec to have two sub-rows. Updated note about max V_{DDIO} current sink capability. Updated PGA graphs (Figure 11-55, Figure 11-56, and Figure 11-57). Updated SAR ADC graphs (Figure 11-24, Figure 11-25, Figure 11-26, Figure 11-27, Figure 11-28, and Figure 11-29). Updated Opamp graphs (Figure 11-17, Figure 11-18, Figure 11-19, Figure 11-20, Figure 11-21, Figure 11-22, and Figure 11-23). Updated Table 11-2 to include rows for I_{DDAR} and I_{DDDR}. Updated IDAC and VDAC graphs (Figure 11-30 to Figure 11-55). Updated "Reset" section on page 23. More details given to distinguish External Reset (XRES) from Power-on Reset. Fixed typos: Replaced "CY8C38" with "PSoC 5" and "CY8C32" to "CY8C52". Updated the graphs under "Internal Main Oscillator" section on page 90 section. Updated and clarified specifications and conditions for sleep mode. Updated f_SWDCK, SWDCLK frequency max values. Updated Table 11-3, T_{SLEEP} parameter.

18. Sales, Solutions, and Legal Information

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