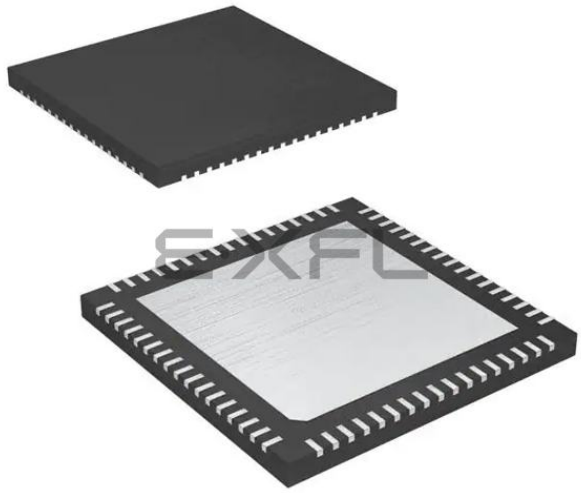


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	67MHz
Connectivity	I²C, LINbus, SPI, UART/USART, USB
Peripherals	CapSense, DMA, LCD, POR, PWM, WDT
Number of I/O	36
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 2x12b; D/A 4x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	68-VFQFN Exposed Pad
Supplier Device Package	68-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c5467lti-007

make the SIO function as a general purpose analog comparator. For devices with FS USB the USB physical interface is also provided (USBIO). When not using USB these pins may also be used for limited digital functionality and device programming. All the features of the PSoC I/Os are covered in detail in the "I/O System and Routing" section on page 24 of this data sheet.

The PSoC device incorporates flexible internal clock generators, designed for high stability and factory trimmed for high accuracy. The Internal Main Oscillator (IMO) is the master clock base for the system, and has 5% accuracy at 3 MHz. The IMO can be configured to run from 3 MHz up to 48 MHz. Multiple clock derivatives can be generated from the main clock frequency to meet application needs. The device provides a PLL to generate system clock frequencies up to 67 MHz from the IMO, external crystal, or external reference clock. It also contains a separate, very low power Internal Low Speed Oscillator (ILO) for the sleep and watchdog timers. A 32.768 kHz external watch crystal is also supported for use in RTC applications. The clocks, together with programmable clock dividers, provide the flexibility to integrate most timing requirements.

The CY8C54 family supports a wide supply operating range from 2.7 to 5.5 V. This allows operation from regulated supplies such as 3.3 V ± 10% or 5.0 V ± 10%, or directly from a wide range of battery types.

PSoC supports a wide range of low power modes. These include a 300-nA hibernate mode with RAM retention and a 2-µA sleep mode.

Power to all major functional blocks, including the programmable digital and analog peripherals, can be controlled independently by firmware. This allows low power background processing when some peripherals are not in use. This, in turn, provides a total device current of only 6 mA when the CPU is running at 6 MHz.

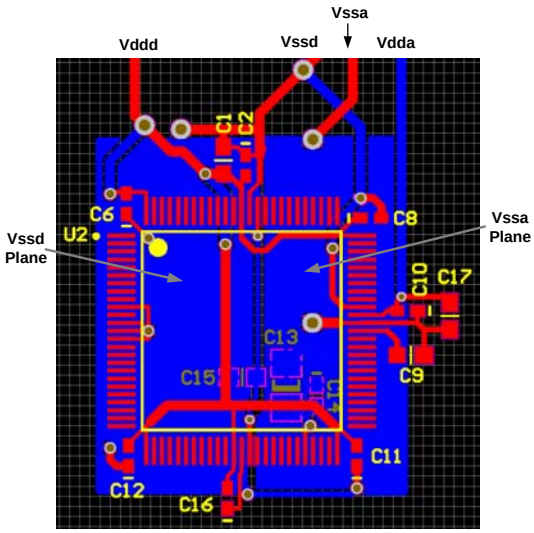
The details of the PSoC power modes are covered in the "Power System" section on page 21 of this data sheet.

PSoC uses a a SWD interface for programming, debug, and test. Using this standard interface enables the designer to debug or program the PSoC with a variety of hardware solutions from Cypress or third party vendors. The Cortex-M3 debug and trace modules include Flash Patch and Breakpoint (FPB), Data Watchpoint and Trace (DWT) and Instrumentation Trace Macrocell (ITM). These modules have many features to help solve difficult debug and trace problems. Details of the programming, test, and debugging interfaces are discussed in the "Programming, Debug Interfaces, Resources" section on page 50 of this data sheet.

2. Pinouts

The VDDIO pin that supplies a particular set of pins is indicated by the black lines drawn on the pinout diagrams in Figure 2-1 and Figure 2-2. Using the VDDIO pins, a single PSoC can support multiple interface voltage levels, eliminating the need for off-chip level shifters. Each VDDIO may sink up to 20 mA total to its associated I/O pins and opamps, and each set of VDDIO associated pins may sink up to 100 mA. .

Figure 2-4. Example PCB Layout for 100-pin TQFP Part for Optimal Analog Performance



3. Pin Descriptions

IDAC0, IDAC1, IDAC2, IDAC3
Low resistance output pin for high current DACs (IDAC).

OpAmp0out, OpAmp1out, OpAmp2out, OpAmp3out
High current output of uncommitted opamp[6].

Extref0, Extref1
External reference input to the analog system.

OpAmp0–, OpAmp1–, OpAmp2–, OpAmp3–
Inverting input to uncommitted opamp.

OpAmp0+, OpAmp1+, OpAmp2+, OpAmp3+
Noninverting input to uncommitted opamp.

SAR0ref, SAR1ref. External references for SAR ADCs.

GPIO
General purpose I/O pin provides interfaces to the CPU, digital peripherals, analog peripherals, interrupts, LCD segment drive, and CapSense[6].

kHz XTAL: Xo, kHz XTAL: Xi
32.768 kHz crystal oscillator pin.

MHz XTAL: Xo, MHz XTAL: Xi
4 to 25 MHz crystal oscillator pin. If a crystal is not used then Xi must be shorted to ground and Xo must be left floating.

SIO. Special I/O provides interfaces to the CPU, digital peripherals and interrupts with a programmable high threshold voltage, analog comparator, high sink current, and high impedance state when the device is unpowered.

SWDCK
Serial Wire Debug Clock programming and debug port connection. When programming and debugging using SWD is done over USBIOs, the SWDCK pin of port P1[1] is not available for use as a general purpose I/O and should be externally pulled down using a resistor of less than 100 KΩ.

SWDIO
Serial Wire Debug Input and Output programming and debug port connection.

SWV
Single Wire Viewer output.

USBIO, D+
Provides D+ connection directly to a USB 2.0 bus. May be used as a digital I/O pin; it is powered from Vddd instead of from a Vdddio. Pins are Do Not Use (DNU) on devices without USB.

USBIO, D–
Provides D– connection directly to a USB 2.0 bus. May be used as a digital I/O pin; it is powered from Vddd instead of from a Vdddio. Pins are DNU on devices without USB.

V_{CCA}
Output of analog core regulator and input to analog core. Requires a 1 µF capacitor to V_{SSA} (10 µF is required for sleep mode. See Table 11-3). Regulator output not for external use.

V_{CCD}
Output of digital core regulator and input to digital core. The two Vccd pins must be shorted together, with the trace between them as short as possible, and a 1 µF capacitor to V_{SSD} (10 µF is required for sleep mode. See Table 11-3); see Power System on page 21. Regulator output not for external use.

V_{DDA}
Supply for all analog peripherals and analog core regulator. **V_{DDA} must be the highest voltage present on the device. All other supply pins must be less than or equal to V_{DDA}.**[7]

V_{DDD}
Supply for all digital peripherals and digital core regulator. V_{DDD} must be less than or equal to V_{DDA}.[7]

V_{SSA}
Ground for all analog peripherals.

V_{SSD}
Ground for all digital logic and I/O pins.

Vddio0, Vddio1, Vddio2, Vddio3
Supply for I/O pins. Each V_{DDIO} must be tied to a valid operating voltage (2.7 V to 5.5 V), and must be less than or equal to Vdda.

$\overline{XRES}$. External reset pin. Active low with internal pull-up.

RSVD. Reserved pins.

Notes
6. GPIOs with opamp outputs are not recommended for use with CapSense.
7. V_{DDD} and V_{DDA} must be brought up in synchronization with each other, that is, at the same rates and levels. V_{DDA} must be greater than or equal to all other supplies

6. System Integration

6.1 Clocking System

The clocking system generates, divides, and distributes clocks throughout the PSoC system. The IMO and PLL together can generate up to a 67 MHz clock, accurate to ±5% over voltage and temperature. Additional internal and external clock sources allow each design to optimize accuracy, power, and cost. All of the system clock sources can be used to generate other clock frequencies in the 16-bit clock dividers and UDBs for anything the user wants, for example a UART baud rate generator.

Clock generation and distribution is automatically configured through the PSoC Creator IDE graphical interface. This is based on the complete system's requirements. It greatly speeds the design process. PSoC Creator allows designers to build clocking systems with minimal input. The designer can specify desired clock frequencies and accuracies, and the software locates or builds a clock that meets the required specifications. This is possible because of the programmability inherent PSoC.

Key features of the clocking system include:

- Seven general purpose clock sources
  - 3 to 48 MHz IMO, ±5% at 3 MHz
  - 4 to 25 MHz External Crystal Oscillator (MHzECO)
  - Clock doubler provides a doubled clock frequency output for the USB block, see USB Clock Domain on page 21
  - DSI signal from an external I/O pin or other logic
  - 24 to 67 MHz fractional Phase-Locked Loop (PLL) sourced from IMO, MHzECO, or DSI
  - 1 kHz, 33 kHz, 100 kHz ILO for Watch Dog Timer (WDT) and Sleep Timer
  - 32.768 kHz External Crystal Oscillator (kHzECO) for Real Time Clock (RTC)
- Independently sourced clock dividers in all clocks
- Eight 16-bit clock dividers for the digital system
- Four 16-bit clock dividers for the analog system
- Dedicated 16-bit divider for the CPU bus and CPU clock
- Automatic clock configuration in PSoC Creator

Table 6-1. Oscillator Summary

Source	Fmin	Tolerance at Fmin	Fmax	Tolerance at Fmax	Startup Time
IMO	3 MHz	±5% over voltage and temperature	48 MHz	±10%	12 µs max
MHzECO	4 MHz	Crystal dependent	25 MHz	Crystal dependent	5 ms typ, max is crystal dependent
DSI	0 MHz	Input dependent	66 MHz	Input dependent	Input dependent
PLL	24 MHz	Input dependent	67 MHz	Input dependent	250 µs max
Doubler	48 MHz	Input dependent	48 MHz	Input dependent	1 µs max
ILO	1 kHz	–50%, +100%	100 kHz	–55%, +100%	15 ms max in lowest power mode
kHzECO	32 kHz	Crystal dependent	32 kHz	Crystal dependent	500 ms typ, max is crystal dependent

The central timewheel can be programmed to wake the system periodically and optionally issue an interrupt. This enables flexible, periodic wakeups from low power modes or coarse timing applications. Systems that require accurate timing should use the Real Time Clock capability instead of the central timewheel. The 100 kHz clock (CLK100K) works as a low power system clock to run the CPU. It can also generate fast time intervals using the fast timewheel.

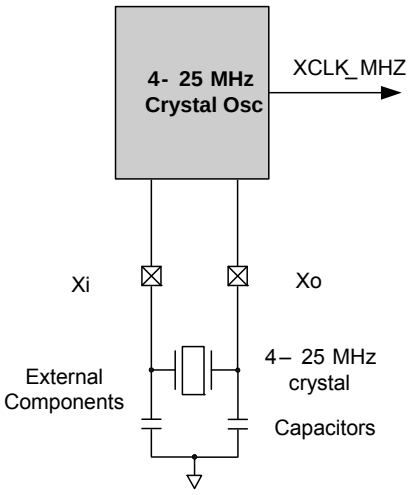
The fast timewheel is a 100 kHz, 5-bit counter clocked by the ILO that can also be used to generate periodic interrupts. The fast timewheel settings are programmable, and the counter automatically resets when the terminal count is reached. This enables flexible, periodic interrupts to the CPU at a higher rate than is allowed using the central timewheel. The fast timewheel can generate an optional interrupt each time the terminal count is reached. The 33 kHz clock (CLK33K) comes from a divide-by-3 operation on CLK100K. This output can be used as a reduced accuracy version of the 32.768 kHz ECO clock with no need for a crystal. The fast timewheel cannot be used as a wakeup source and must be turned off before entering sleep or hibernate mode.

6.1.2 External Oscillators

6.1.2.1 MHz External Crystal Oscillator

The MHzECO provides high frequency, high precision clocking using an external crystal (see Figure 6-2). It supports crystals in the range of 4 to 25 MHz. When used in conjunction with the PLL, it can generate CPU and system clocks up to the device's maximum frequency (see Phase-Locked Loop on page 19). The MHzECO with a 24 MHz crystal can be used with the clock doubler to generate a 48 MHz clock for the USB. If a crystal is not used then Xi must be shorted to ground and Xo must be left floating. MHzECO accuracy depends on the crystal chosen.

Figure 6-2. MHzECO Block Diagram

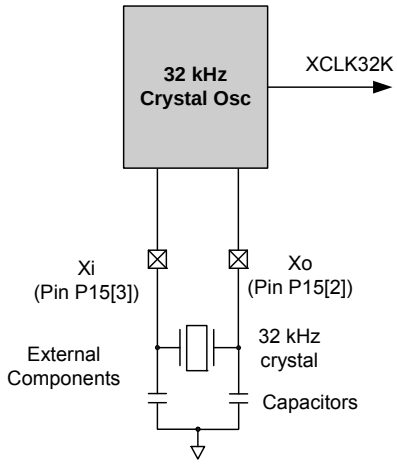


6.1.2.2 32.768 kHz ECO

The 32.768 kHz External Crystal Oscillator (32kHzECO) provides precision timing with minimal power consumption using an external 32.768 kHz watch crystal (see Figure 6-3). The RTC uses a 1 second interrupt to implement the RTC functionality in firmware.

The oscillator works in two distinct power modes. This allows users to trade off power consumption with noise immunity from neighboring circuits. The GPIO pins connected to the external crystal and capacitors are fixed.

Figure 6-3. 32kHzECO Block Diagram



It is recommended that the external 32.768-kHz watch crystal have a load capacitance (CL) of 6 pF or 12.5 pF. Check the crystal manufacturer's datasheet. The two external capacitors, CL1 and CL2, are typically of the same value, and their total capacitance, CL1CL2 / (CL1 + CL2), including pin and trace capacitance, should equal the crystal CL value. For more information, refer to application note AN54439: PSoC 3 and PSoC 5 External Oscillators. See also pin capacitance specifications in the "GPIO" section on page 58.

6.1.2.3 Digital System Interconnect

The DSI provides routing for clocks taken from external clock oscillators connected to I/O. The oscillators can also be generated within the device in the digital system and Universal Digital Blocks.

While the primary DSI clock input provides access to all clocking resources, up to eight other DSI clocks (internally or externally generated) may be routed directly to the eight digital clock dividers. This is only possible if there are multiple precision clock sources.

6.1.3 Clock Distribution

All seven clock sources are inputs to the central clock distribution system. The distribution system is designed to create multiple high precision clocks. These clocks are customized for the design's requirements and eliminate the common problems found with limited resolution prescalers attached to peripherals. The clock distribution system generates several types of clock trees.

- The system clock is used to select and supply the fastest clock in the system for general system clock requirements and clock synchronization of the PSoC device.
- Bus Clock 16-bit divider uses the system clock to generate the system's bus clock used for data transfers and the CPU. The CPU clock is directly derived from the bus clock.

The term **system reset** indicates that the processor as well as analog and digital peripherals and registers are reset.

A reset status register shows some of the resets or power voltage monitoring interrupts. The program may examine this register to detect and report certain exception conditions. This register is cleared after a power-on reset. For details see the Technical Reference Manual.

6.3.1 Power Voltage Level Monitors

- IPOR - Initial Power-on Reset

  At initial power on, IPOR monitors the power voltages V_{DDD} and V_{DDA}, both directly at the pins and at the outputs of the corresponding internal regulators. The trip level is not precise. It is set to approximately 1 volt, which is below the lowest specified operating voltage but high enough for the internal circuits to be reset and to hold their reset state. The monitor generates a reset pulse that is at least 100 ns wide. It may be much wider if one or more of the voltages ramps up slowly.

  To save power the IPOR circuit is disabled when the internal digital supply is stable. When the voltage is high enough, the IMO starts.

- ALVI, DLVI, AHVI - Analog/Digital Low Voltage Interrupt, Analog High Voltage Interrupt

  Interrupt circuits are available to detect when V_{DDA} and V_{DDD} go outside a voltage range. For AHVI, V_{DDA} is compared to a fixed trip level. For ALVI and DLVI, V_{DDA} and V_{DDD} are compared to trip levels that are programmable, as listed in Table 6-4.

Table 6-4. Analog/Digital Low Voltage Interrupt, Analog High Voltage Interrupt

Interrupt	Supply	Normal Voltage Range	Available Trip Settings
DLVI	V_{DDD}	2.7 V–5.5 V	2.45 V–5.45 V in 250 mV increments. The 2.45 V setting is used for LVD.
ALVI	V_{DDA}	2.7 V–5.5 V	2.45 V–5.45 V in 250 mV increments. The 2.45 V setting is used for LVD.
AHVI	V_{DDA}	2.7 V–5.5 V	5.75 V

  The monitors are disabled until after IPOR. The monitors are not available in low-power modes. To monitor voltages in sleep mode, wake up periodically using the CTW. After wakeup, the 2.45 V LVI interrupt may trigger. Voltage monitoring is not available in hibernate mode.

6.3.2 Other Reset Sources

- XRES - External Reset

  CY8C54 has a dedicated XRES pin which holds the part in reset while held active (low). The response to an XRES is the same as to an IPOR reset. The external reset is active low. It includes an internal pull up resistor. XRES is active during sleep and hibernate modes.

- SRES - Software Reset

  A reset can be commanded under program control by setting a bit in the software reset register. This is done either directly by the program or indirectly by DMA access. The response to a SRES is the same as after an IPOR reset.

  Another register bit exists to disable this function.

- WRES - Watchdog Timer Reset

  The watchdog reset detects when the software program is no longer being executed correctly. To indicate to the watchdog timer that it is running correctly, the program must periodically reset the timer. If the timer is not reset before a user-specified amount of time, then a reset is generated.

  Note IPOR disables the watchdog function. The program must enable the watchdog function at an appropriate point in the code by setting a register bit. When this bit is set, it cannot be cleared again except by an IPOR power on reset event. The watchdog timer can be used only when the part remains in active mode.

6.4 I/O System and Routing

PSoC I/Os are extremely flexible. Every GPIO has analog and digital I/O capability. All I/Os have a large number of drive modes, which are set at POR. PSoC also provides up to four individual I/O voltage domains through the V_{DDIO} pins.

There are two types of I/O pins on every device; those with USB provide a third type. Both General Purpose I/O (GPIO) and Special I/O (SIO) provide similar digital functionality. The primary differences are their analog capability and drive strength. Devices that include USB also provide two USBIO pins that support specific USB functionality as well as limited GPIO capability.

All I/O pins are available for use as digital inputs and outputs for both the CPU and digital peripherals. In addition, all I/O pins can generate an interrupt. The flexible and advanced capabilities of the PSoC I/O, combined with any signal to any pin routability, greatly simplify circuit design and board layout. All GPIO pins can be used for analog input, CapSense[6], and LCD segment drive, while SIO pins are used for voltages in excess of V_{DDA} and for programmable output voltages.

- Features supported by both GPIO and SIO:
  - Separate I/O supplies and voltages for up to four groups of I/O
  - Digital peripherals use DSI to connect the pins
  - Input or output or both for CPU and DMA
  - Eight drive modes
  - Every pin can be an interrupt source configured as rising edge, falling edge or both edges. If required, level sensitive interrupts are supported through the DSI
  - Dedicated port interrupt vector for each port
  - Slew rate controlled digital output drive mode
  - Access port control and configuration registers on either port basis or pin basis
  - Separate port read (PS) and write (DR) data registers to avoid read modify write errors
  - Special functionality on a pin by pin basis
- Additional features only provided on the GPIO pins:
  - LCD segment drive on LCD equipped devices
  - CapSense on CapSense equipped devices[11]
  - Analog input and output capability

6.4.1 Drive Modes

Each GPIO and SIO pin is individually configurable into one of the eight drive modes listed in Table 6-5. Three configuration bits are used for each pin (DM[2:0]) and set in the PRTxDM[2:0] registers. Figure 6-10 depicts a simplified pin view based on each of the eight drive modes. Table 6-5 shows the I/O pin's drive state based on the port data register value or digital array signal if bypass mode is selected. Note that the actual I/O pin voltage is determined by a combination of the selected drive mode and the load at the pin. For example, if a GPIO pin is configured for resistive pull up mode and driven high while the pin is floating, the voltage measured at the pin is a high logic state. If the same GPIO pin is externally tied to ground then the voltage unmeasured at the pin is a low logic state.

Figure 6-10. Drive Mode

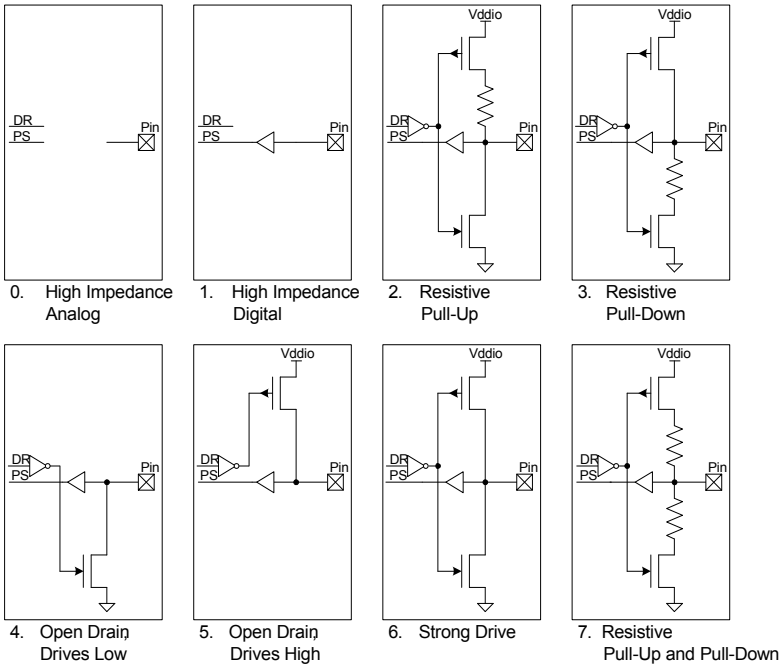


Table 6-5. Drive Modes

Diagram	Drive Mode	PRTxDM2	PRTxDM1	PRTxDM0	PRTxDR = 1	PRTxDR = 0
0	High impedence analog	0	0	0	High Z	High Z
1	High Impedance digital	0	0	1	High Z	High Z
2	Resistive pull up[12]	0	1	0	Res High (5K)	Strong Low
3	Resistive pull down[12]	0	1	1	Strong High	Res Low (5K)
4	Open drain, drives low	1	0	0	High Z	Strong Low
5	Open drain, drive high	1	0	1	Strong High	High Z
6	Strong drive	1	1	0	Strong High	Strong Low
7	Resistive pull up and pull down[12]	1	1	1	Res High (5K)	Res Low (5K)

- High Impedance Analog

  The default reset state with both the output driver and digital input buffer turned off. This prevents any current from flowing in the I/O's digital input buffer due to a floating voltage. This state is recommended for pins that are floating or that support an analog voltage. High impedance analog pins do not provide digital input functionality.

  To achieve the lowest chip current in sleep modes, all I/Os must either be configured to the high impedance analog mode, or have their pins driven to a power supply rail by the PSoC device or by external circuitry.

- High Impedance Digital

  The input buffer is enabled for digital signal input. This is the standard high impedance (HiZ) state recommended for digital inputs.

Note
12. Resistive pull up and pull down are not available with SIO in regulated output mode.

9.3 Debug Features

The CY8C54 supports the following debug features:

- Halt and single-step the CPU
- View and change CPU and peripheral registers, and RAM addresses
- Six program address breakpoints and two literal access breakpoints
- Data watchpoint events to CPU
- Patch and remap instruction from flash to SRAM
- Debugging at the full speed of the CPU
- Compatible with PSoC Creator and MiniProg3 programmer and debugger

9.4 Trace Features

The following trace features are supported:

- Data watchpoint on access to data address, address range, or data value
- Software event monitoring, “printf-style” debugging

9.5 SWV Interface

The SWV interface provides trace data to a debug host via the Cypress MiniProg3 or an external trace port analyzer.

9.6 Programming Features

The SWD interface provides full programming support. The entire device can be erased, programmed, and verified. Designers can increase flash protection levels to protect firmware IP. Flash protection can only be reset after a full device erase. Individual flash blocks can be erased, programmed, and verified, if block security settings permit.

9.7 Device Security

PSoC 5 offers an advanced security feature called device security, which permanently disables all test, programming, and debug ports, protecting your application from external access. The device security is activated by programming a 32-bit key (0x50536F43) to a Write Once Latch (WOL). The WOL must be programmed at $V_{DDD} \leq 3.3$ V and $T_J = 25$ °C ±15 °C.

The Write Once Latch is a type of nonvolatile latch (NVL). The cell itself is an NVL with additional logic wrapped around it. Each WOL device contains four bytes (32 bits) of data. The wrapper outputs a ‘1’ if a super-majority (28 of 32) of its bits match a pre-determined pattern (0x50536F43); it outputs a ‘0’ if this majority is not reached. When the output is 1, the Write Once NV latch locks the part out of Debug and Test modes; it also permanently gates off the ability to erase or alter the contents of the latch. Matching all bits is intentionally not required, so that single (or few) bit failures do not deassert the WOL output. The state of the NVL bits after wafer processing is truly random with no tendency toward 1 or 0.

The WOL only locks the part after the correct 32-bit key (0x50536F43) is loaded into the NVL's volatile memory, programmed into the NVL's nonvolatile cells, and the part is reset. The output of the WOL is only sampled on reset and used to disable the access. This precaution prevents anyone from reading, erasing, or altering the contents of the internal memory.

The user can write the key into the WOL to lock out external access only if no flash protection is set (see “Flash Security” section on page 16). However, after setting the values in the WOL, a user still has access to the part until it is reset. Therefore, a user can write the key into the WOL, program the flash protection data, and then reset the part to lock it.

If the device is protected with a WOL setting, Cypress cannot perform failure analysis and, therefore, cannot accept RMAs from customers. The WOL can be read out via Serial Wire Debug (SWD) port to electrically identify protected parts. The user can write the key in WOL to lock out external access only if no flash protection is set. For more information on how to take full advantage of the security features in PSoC see the PSoC 5 TRM.

Disclaimer

Note the following details of the flash code protection features on Cypress devices.

Cypress products meet the specifications contained in their particular Cypress data sheets. Cypress believes that its family of products is one of the most secure families of its kind on the market today, regardless of how they are used. There may be methods, unknown to Cypress, that can breach the code protection features. Any of these methods, to our knowledge, would be dishonest and possibly illegal. Neither Cypress nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as “unbreakable.”

Cypress is willing to work with the customer who is concerned about the integrity of their code. Code protection is constantly evolving. We at Cypress are committed to continuously improving the code protection features of our products.

11. Electrical Specifications

Specifications are valid for –40 °C ≤ T_A ≤ 85 °C and T_J ≤ 100 °C, except where noted. Specifications are valid for 2.7 V to 5.5 V, except where noted. The unique flexibility of the PSoC UDBs and analog blocks enable many functions to be implemented in PSoC Creator components, see the component data sheets for full AC/DC specifications of individual functions. See the "Example Peripherals" section on page 30 for further explanation of PSoC Creator components.

11.1 Absolute Maximum Ratings

Table 11-1. Absolute Maximum Ratings DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
T_J	Operating die temperature		–55	–	110	°C
T_{STG}	Storage temperature	Recommended storage temperature is +25 °C ±25 °C. Extended duration storage temperatures above 85 °C degrade reliability.	–55	25	100	°C
V_{DDA}	Analog supply voltage relative to V_{SSA}		–0.5	–	6	V
V_{DDD}	Digital supply voltage relative to V_{SSD}		–0.5	–	6	V
V_{DDIO}	I/O supply voltage relative to V_{SSD}		–0.5	–	6	V
V_{CCA}	Direct analog core voltage input		–0.5	–	1.95	V
V_{CCD}	Direct digital core voltage input		–0.5	–	1.95	V
V_{SSA}	Analog ground voltage		V_{SSD} –0.5	–	V_{SSD} + 0.5	V
V_{GPIO}[15]	DC input voltage on GPIO	Includes signals sourced by V_{DDA} and routed internal to the pin.	V_{SSD} –0.5	–	V_{DDIO} + 0.5	V
V_{SIO}	DC input voltage on SIO	Output disabled	V_{SSD} –0.5	–	7	V
		Output enabled	V_{SSD} –0.5	–	6	V
I_{VDDIO}	Current per V_{DDIO} supply pin	Source	–	–	20	mA
		Sink	–	–	100	
LU	Latch up current[16]		–100	–	100	mA
ESD_{HBM}	Electrostatic discharge voltage	Human Body Model	500	–	–	V
ESD_{CDM}	Electrostatic discharge voltage	Charge Device Model	500	–	–	V

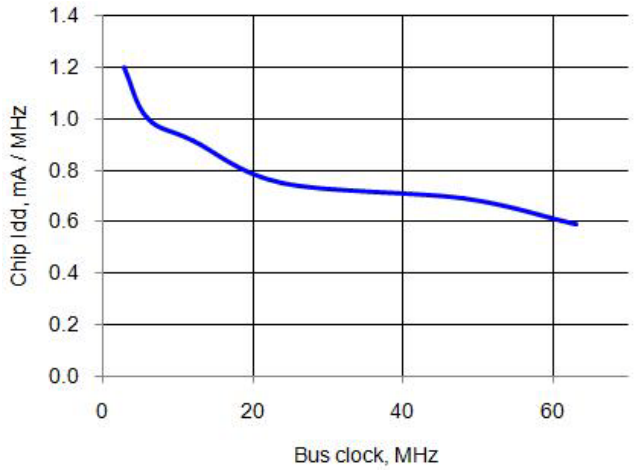
Note Usage above the absolute maximum conditions listed in Table 11-1 may cause permanent damage to the device. Exposure to maximum conditions for extended periods of time may affect device reliability. When used below maximum conditions but above normal operating conditions the device may not operate to specification.

Notes
15. The V_{DDIO} supply voltage must be greater than the maximum analog voltage on the associated GPIO pins. Maximum analog voltage on GPIO pin ≤ V_{DDIO} ≤ V_{DDA}.
16. Meets or exceeds JEDEC Spec EIA/JESD78 IC latch up test, at up to 85 °C.

Table 11-2. DC Specifications (continued)

Parameter	Description	Conditions			Min	Typ	Max	Units
		Device Configuration	$V_{DD} = V_{DDIO}$	Temp				
	Sleep Mode[20]	CPU = OFF SleepTimer=ON POR = ON	4.5 V to 5.5 V	–40 °C	–	1.4	–	µA
				25 °C	–	2.2	–	
				85 °C	–	11	–	
			2.7 V to 3.6 V	–40 °C	–	1.2	–	
				25 °C	–	2	–	
				85 °C	–	10	–	
	Hibernate Mode	All oscillators and regulators off, except hibernate regulator. SRAM retention	4.5 V to 5.5 V	–40 °C	–	0.3	–	µA
				25 °C	–	0.6	–	
				85 °C	–	10	–	
			2.7 V to 3.6 V	–40 °C	–	0.2	–	
				25 °C	–	0.3	–	
				85 °C	–	8	–	
I_{DDAR}	Analog current consumption while device is reset[22]	$V_{DDA} \leq 3.6$ V			–	0.3	–	mA
		$V_{DDA} > 3.6$ V			–	1.4	–	mA
I_{DDDR}	Digital current consumption while device is reset[22]	$V_{DDD} \leq 3.6$ V			–	1.1	–	mA
		$V_{DDD} > 3.6$ V			–	0.7	–	mA

Figure 11-1. Active Mode Device I_{DD}, mA/MHz



Notes
20. Sleep timer generates periodic interrupts to wake up the CPU. This specification applies only to those times that the CPU is off.
21. Based on device characterization (Not production tested).
22. Based on device characterization (not production tested). USBIO pins tied to ground (VSSD).

Table 11-3. AC Specifications[21]

Parameter	Description	Conditions	Min	Typ	Max	Units
F_{CPU}	CPU frequency		DC	–	67.01	MHz
F_{BUSCLK}	Bus frequency		DC	–	67.01	MHz
Svdd	V_{DD} ramp rate		–	–	0.066	V/µs
$T_{STARTUP}$	Time from $V_{DDD}/V_{DDA}/V_{CCD}/V_{CCA}$ ≥ min operating voltage to CPU executing code at reset vector	No PLL used, IMO boot mode 12 MHz typ	–	45	80	µs
T_{SLEEP}	Wakeup from sleep – CTW timeout to beginning of execution of next CPU instruction		–	125	–	µs
T_{SLEEP_INT}	Sleep timer periodic wakeup interval		–	–	128	ms

11.3 Power Regulators

Specifications are valid for –40 °C ≤ T_A ≤ 85 °C and T_J ≤ 100 °C, except where noted. Specifications are valid for 2.7 V to 5.5 V, except where noted.

11.3.1 Digital Core Regulator

Table 11-4. Digital Core Regulator DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{DDD}	Input voltage		2.7	–	5.5	V
V_{CCD}	Output voltage		–	1.80	–	V
	Regulator output capacitor[23]	±10%, X5R ceramic or better. The two V_{CCD} pins must be shorted together, with as short a trace as possible, see Power System on page 21	–	1	10	µF

Figure 11-2. Regulators V_{CC} vs V_{DD}

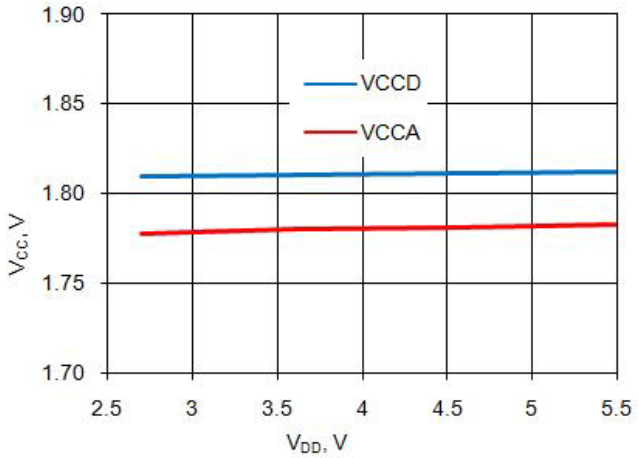
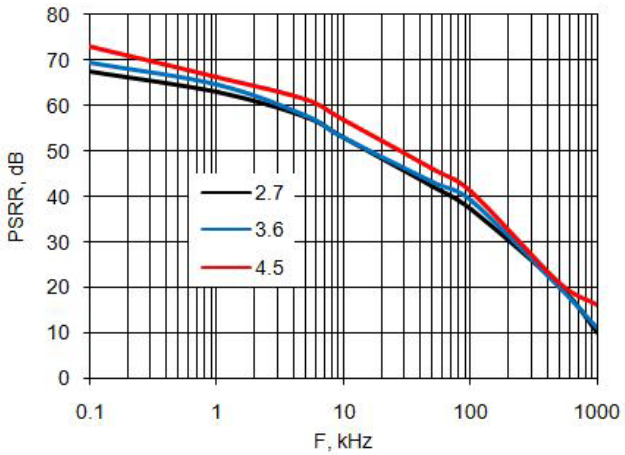


Figure 11-3. Digital Regulator PSRR vs Frequency and V_{DD}



Note
23. 10 µF is required for sleep mode. See Table 11-3.

Figure 11-21. Opamp Step Response, Rising

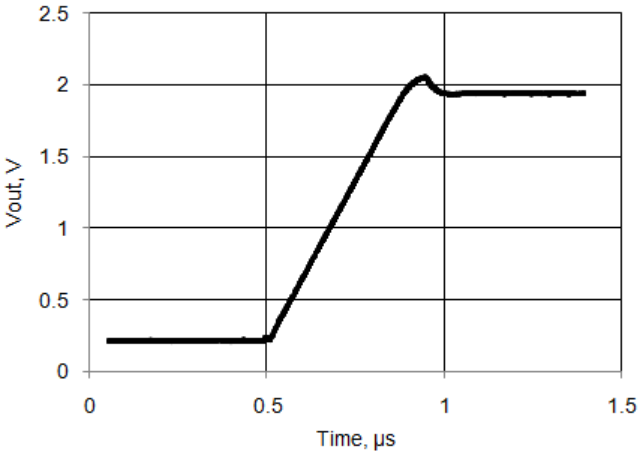


Figure 11-23. Opamp Step Response, Falling

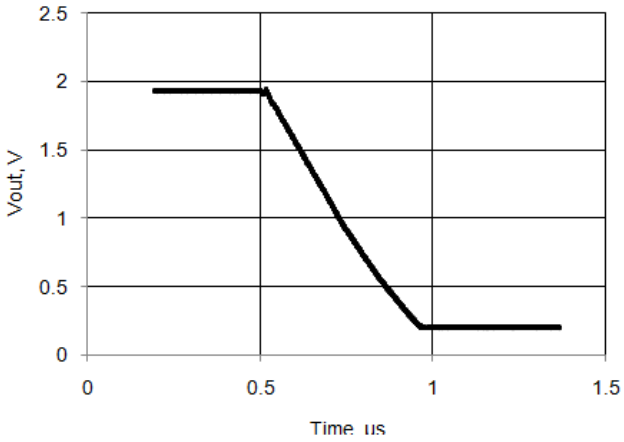
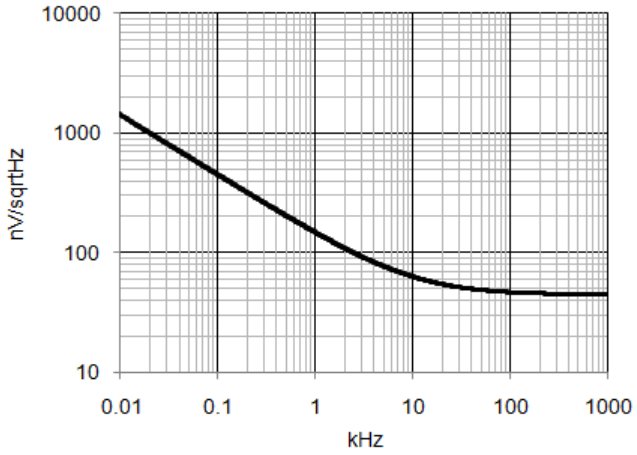


Figure 11-22. Opamp Noise vs Frequency, V_{DDA} = 5V



11.5.2 Voltage Reference

Table 11-17. Voltage Reference Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{REF}	Precision reference voltage	Initial trimming	1.017 (–0.7%)	1.024	1.033 (+0.9%)	V
	Temperature drift[36]		–	–	57	ppm/°C
	Long term drift		–	100	–	ppm/Khr
	Thermal cycling drift (stability)[36]		–	100	–	ppm

Note
36. Based on device characterization (Not production tested).

11.5.5 Comparator

Table 11-21. Comparator DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{OS}	Input offset voltage in fast mode	Factory trim, Vin ≥ 0.5 V	–		15	mV
	Input offset voltage in slow mode	Factory trim, Vin ≥ 0.5 V	–		15	mV
V_{OS}	Input offset voltage in ultra low power mode		–	±12	–	mV
V_{HYST}	Hysteresis	Hysteresis enable mode	–	10	32	mV
V_{ICM}	Input common mode voltage	High current / fast mode	V_{SSA}	–	V_{DDA} – 0.1	V
		Low current / slow mode	V_{SSA}	–	V_{DDA}	V
		Ultra low power mode	V_{SSA}	–	V_{DDA} – 0.9	
CMRR	Common mode rejection ratio		–	50	–	dB
I_{CMP}	High current mode/fast mode[38]		–	–	400	µA
	Low current mode/slow mode[38]		–	–	100	µA
	Ultra low power mode[38]		–	6	–	µA

Table 11-22. Comparator AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
T_{RESP}	Response time, high current mode[38]	50 mV overdrive, measured pin-to-pin	–	75	110	ns
	Response time, low current mode[38]	50 mV overdrive, measured pin-to-pin	–	155	200	ns
	Response time, ultra low power mode[38]	50 mV overdrive, measured pin-to-pin	–	55	–	µs

Note
38. Based on device characterization (Not production tested).

11.5.6 Current Digital-to-analog Converter (IDAC)

All specifications are based on use of the low-resistance IDAC output pins (see Pin Descriptions on page 9 for details). See the IDAC component data sheet in PSoC Creator for full electrical specifications and APIs.

Unless otherwise specified, all charts and graphs show typical values.

Table 11-23. IDAC DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Resolution		–	–	8	bits
I_{OUT}	Output current at code = 255	Range = 2.04 mA, code = 255, Rload = 600 Ω	–	2.04	–	mA
		Range = 255 µA, code = 255, Rload = 600 Ω	–	255	–	µA
		Range = 31.875 µA, code = 255, Rload = 600 Ω	–	31.875	–	µA
	Monotonicity		–	–	Yes	
Ezs	Zero scale error		–	0	±2.5	LSB
Eg	Gain error		–	–	±5	%
TC_Eg	Temperature coefficient of gain error	Range = 2.04 mA	–	–	0.04	%/°C
		Range = 255 µA	–	–	0.04	%/°C
		Range = 31.875 µA	–	–	0.05	%/°C
INL	Integral nonlinearity	Range = 255 µA, Codes 8 – 255, Rload = 600 Ω, Cload = 15 pF	–	–	±3	LSB
DNL	Differential nonlinearity, non-monotonic	Range = 255 µA, Rload = 600 Ω, Cload = 15 pF	–	–	±1.6	LSB
Vcompliance	Dropout voltage, source or sink mode	Voltage headroom at max current, Rload to Vdda or Rload to Vssa, Vdiff from Vdda	1	–	–	V
I_{DD}	Operating current, code = 0	Slow mode, source mode, range = 31.875 µA	–	44	100	µA
		Slow mode, source mode, range = 255 µA,	–	33	100	µA
		Slow mode, source mode, range = 2.04 mA	–	33	100	µA
		Slow mode, sink mode, range = 31.875 µA	–	36	100	µA
		Slow mode, sink mode, range = 255 µA	–	33	100	µA
		Slow mode, sink mode, range = 2.04 mA	–	33	100	µA
		Fast mode, source mode, range = 31.875 µA	–	310	500	µA
		Fast mode, source mode, range = 255 µA	–	305	500	µA
		Fast mode, source mode, range = 2.04 mA	–	305	500	µA
		Fast mode, sink mode, range = 31.875 µA	–	310	500	µA
		Fast mode, sink mode, range = 255 µA	–	300	500	µA
		Fast mode, sink mode, range = 2.04 mA	–	300	500	µA

11.5.10 Programmable Gain Amplifier

The PGA is created using a SC/CT analog block; see the PGA component data sheet in PSoC Creator for full electrical specifications and APIs.

Unless otherwise specified, operating conditions are:

- Operating temperature = 25 °C for typical values
- Unless otherwise specified, all charts and graphs show typical values

Table 11-31. PGA DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
Vin	Input voltage range	Power mode = minimum	Vssa	–	Vdda	V
Vos	Input offset voltage	Power mode = high, gain = 1	–	–	20	mV
TCVos	Input offset voltage drift with temperature	Power mode = high, gain = 1	–	–	±30	µV/°C
Ge1	Gain error, gain = 1		–	–	±2	%
Ge16	Gain error, gain = 16		–	–	±8	%
Ge50	Gain error, gain = 50		–	–	±10	%
Vonl	DC output nonlinearity	Gain = 1	–	–	±0.1	% of FSR
Cin	Input capacitance		–	–	7	pF
Voh	Output voltage swing	Power mode = high, gain = 1, Rload = 100 kΩ to V_{DDA} / 2	V_{DDA} – 0.15	–	–	V
Vol	Output voltage swing	Power mode = high, gain = 1, Rload = 100 kΩ to V_{DDA} / 2	–	–	V_{SSA} + 0.15	V
Vsrc	Output voltage under load	Iload = 250 µA, power mode = high	–	–	300	mV
Idd	Operating current	Power mode = high	–	1.5	1.65	mA
PSRR	Power supply rejection ratio		48	–	–	dB

Table 11-32. PGA AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
BW1	–3 dB bandwidth	Power mode = high, gain = 1,noninverting mode, 300 mV ≤ VIN ≤ V_{DDA} – 1.2 V, CL ≤ 25 pF	6	8	–	MHz
SR1	Slew rate	Power mode = high, gain = 1, 20% to 80%	3	–	–	V/µs
e_n	Input noise density	Power mode = high, Vdda = 5 V, at 100 kHz	–	43	–	nV/sqrtHz

11.6.3 Pulse Width Modulation

The following specifications apply to the Timer/Counter/PWM peripheral, in PWM mode. PWM components can also be implemented in UDBs; for more information, see the PWM component data sheet in PSoC Creator.

Table 11-39. PWM DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	16-bit PWM block current consumption	Input clock frequency – 3 MHz	–	65	–	µA
		Input clock frequency –12 MHz	–	170	–	µA
		Input clock frequency – 48 MHz	–	650	–	µA
		Input clock frequency – 67 MHz	–	900	–	µA

Table 11-40. PWM AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Operating frequency		DC	–	67.01	MHz
	Pulse width		13	–	–	ns
	Pulse width (external)		30	–	–	ns
	Kill pulse width		13	–	–	ns
	Kill pulse width (external)		30	–	–	ns
	Enable pulse width		13	–	–	ns
	Enable pulse width (external)		30	–	–	ns
	Reset pulse width		13	–	–	ns
	Reset pulse width (external)		30	–	–	ns

11.6.4 I^2C

Table 11-41. Fixed I^2C DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Block current consumption	Enabled, configured for 100 kbps	–	90	250	µA
		Enabled, configured for 400 kbps	–	100	250	µA

Table 11-42. Fixed I^2C AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Bit rate		–	–	400	Kbps

11.6.5 Digital Filter Block

Table 11-43. DFB DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	DFB operating current	64-tap FIR at F_{DFB}				
		100 kHz (1.3 ksps)	–	0.03	0.075	mA
		500 kHz (6.7 ksps)	–	0.16	0.3	mA
		1 MHz (13.4 ksps)	–	0.33	0.57	mA
		10 MHz (134 ksps)	–	3.3	5.5	mA
		48 MHz (644 ksps)	–	15.7	26	mA
		67 MHz (900 ksps)	–	21.8	35.6	mA

Table 11-44. DFB AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
F_{DFB}	DFB operating frequency		DC	–	67.01	MHz

11.6.6 USB

Table 11-45. USB DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{USB_5}	Device supply for USB operation	USB configured, USB regulator enabled	4.35	–	5.25	V
$V_{USB\_3.3}$		USB configured, USB regulator bypassed	3.15	–	3.6	V
$I_{USB\_Configured}$	Device supply current in device active mode	V_{DDD} = 5 V, bus clock ≥ 33 MHz	–	55	–	mA
		V_{DDD} = 3.3 V, bus clock ≥ 33 MHz	–	40	–	mA
$I_{USB\_Suspended}$	Device supply current in device sleep mode	V_{DDD} = 5 V, connected to USB host	–	0.5	–	mA
		V_{DDD} = 3.3 V, connected to USB host	–	0.5	–	mA

Notes
40. Refer to ISO 11898 specification for details.
41. Rise/fall time matching (TR) not guaranteed, see USB Driver AC Specifications on page 65.

11.7 Memory

Specifications are valid for –40 °C ≤ T_A ≤ 85 °C and T_J ≤ 100 °C, except where noted. Specifications are valid for 2.7 V to 5.5 V, except where noted.

11.7.1 Flash

Table 11-47. Flash DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Erase and program voltage	V_{DDD} pin	2.7	–	5.5	V

Table 11-48. Flash AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
T_{WRITE}	Row write time (erase + program)		–	8.3	32	ms
T_{BULK}	Bulk erase time (256 KB)	10 °C < average ambient temp. T_A < 40 °C	–	117	440	ms
	Sector erase time (16 KB)	10 °C < average ambient temp. T_A < 40 °C	–	6.3	26	ms
T_{PROG}	Total device programming time	No overhead[42]	–	9	32.5	seconds
	Flash data retention time, retention period measured from last erase cycle	Average ambient temp. T_A ≤ 55 °C, 100 K erase/program cycles	20	–	–	years
		Average ambient temp. T_A ≤ 70 °C, 10 K erase/program cycles	10	–	–	

11.7.2 EEPROM

Table 11-49. EEPROM DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Erase and program voltage		2.7	–	5.5	V

Table 11-50. EEPROM AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
T_{WRITE}	Single row erase/write cycle time		–	8.3	32	ms
	EEPROM data retention time, retention period measured from last erase cycle	Average ambient temp, T_A ≤ 55 °C, 1M erase/program cycles	20	–	–	years

11.7.3 SRAM

Table 11-51. SRAM DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{SRAM}	SRAM retention voltage		1.2	–	–	V

Table 11-52. SRAM AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
F_{SRAM}	SRAM operating frequency		DC	–	67.01	MHz

Note
42. See application note AN64359 for a description of a low-overhead method of programming PSoC 5 flash.

11.9 Clocking

Specifications are valid for –40 °C ≤ T_A ≤ 85 °C and T_J ≤ 100 °C, except where noted. Specifications are valid for 2.7 V to 5.5 V, except where noted. Unless otherwise specified, all charts and graphs show typical values.

11.9.1 kHz External Crystal Oscillator (kHzECO)

For more information on crystal selection for the kHzECO, refer to application note AN54439: PSoC 3 and PSoC 5 External Oscillators.

Table 11-59. kHz ECO DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
I_{DD}	Oscillator operating current	Low power mode; CL = 6 pF	–	0.25	–	µA
C_{IN}	Capacitance at Pins kHz-XTAL:Xi and kHz-XTAL:Xo[49]		–	5	7	pF

Table 11-60. kHz ECO Crystal Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
F	Crystal frequency		–	32.768	–	kHz
C_L	Crystal load capacitance	Recommended values	–	6 or 12.5	–	pF
D_L	Crystal drive level tolerance		1	–	–	µW

11.9.2 Internal Main Oscillator

Table 11-61. IMO DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Supply current					
	48 MHz		–	465	850	µA
	24 MHz		–	195	500	µA
	12 MHz		–	150	450	µA
	6 MHz		–	120	400	µA
	3 MHz		–	105	300	µA

Note
49. Based on device characterization (Not production tested).

Figure 11-60. IMO Current vs. Frequency

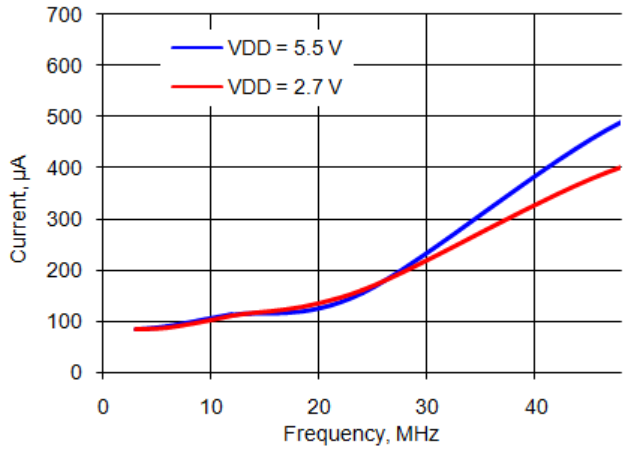


Table 11-62. IMO AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
F_{IMO}	IMO frequency stability (with factory trim)					
	48 MHz		–10	–	10	%
	24 MHz		–8	–	8	%
	12 MHz		–6.25	–	6.25	%
	6 MHz		–5.8	–	5.8	%
	3 MHz		–5	–	5	%
	Startup time[50]	From enable (during normal system operation) or wakeup from low power state	–	–	12	µs
Jp–p	Jitter (peak to peak)[50]					
	F = 24 MHz		–	0.5	–	ns
	F = 3 MHz		–	2.3	–	ns

Figure 11-61. IMO Frequency Variation vs. Temperature

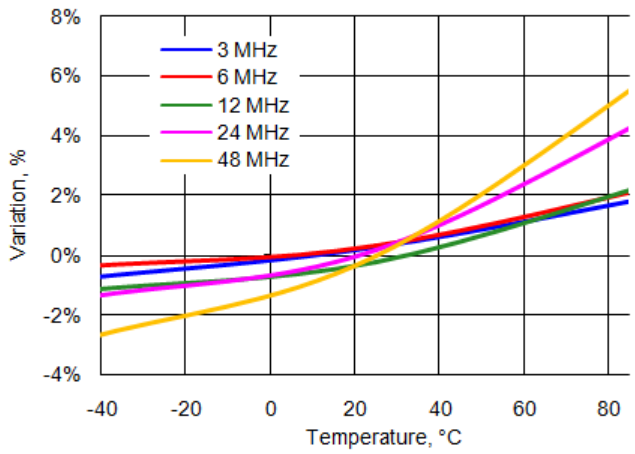
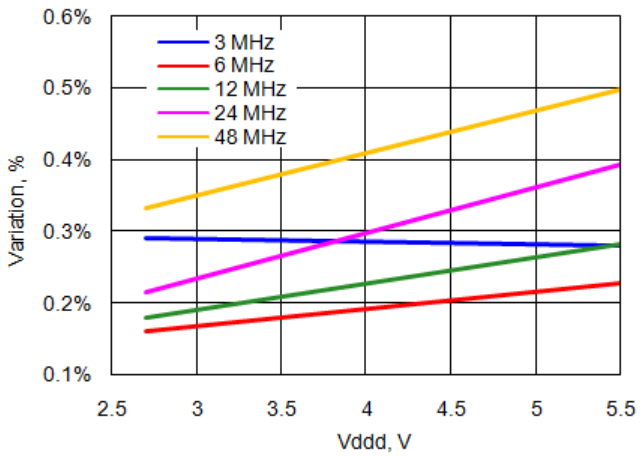


Figure 11-62. IMO Frequency Variation vs. V_{DDD}



Note
50. Based on device characterization (Not production tested).

Table 14-1. Acronyms Used in this Document (continued)

Acronym	Description
PLD	programmable logic device, see also PAL
PLL	phase-locked loop
PMDD	package material declaration data sheet
POR	power-on reset
PRS	pseudo random sequence
PS	port read data register
PSoC®	Programmable System-on-Chip™
PSRR	power supply rejection ratio
PWM	pulse-width modulator
RAM	random-access memory
RISC	reduced-instruction-set computing
RMS	root-mean-square
RSVD	reserved
RTC	real-time clock
RTL	register transfer language
RTR	remote transmission request
RX	receive
SAR	successive approximation register
SC/CT	switched capacitor/continuous time
SCL	I^2C serial clock
SDA	I^2C serial data
S/H	sample and hold
SIO	special input/output, GPIO with advanced features. See GPIO.
SNR	signal-to-noise ratio
SOC	start of conversion
SOF	start of frame

Table 14-1. Acronyms Used in this Document (continued)

Acronym	Description
SPI	Serial Peripheral Interface, a communications protocol
SR	slew rate
SRAM	static random access memory
SRES	software reset
SWD	serial wire debug, a test protocol
SWV	single-wire viewer
TD	transaction descriptor, see also DMA
THD	total harmonic distortion
TIA	transimpedance amplifier
TRM	technical reference manual
TTL	transistor-transistor logic
TX	transmit
UART	Universal Asynchronous Transmitter Receiver, a communications protocol
UDB	universal digital block
USB	Universal Serial Bus
USBIO	USB input/output, PSoC pins used to connect to a USB port
VDAC	voltage DAC, see also DAC, IDAC
WDT	watchdog timer
WOL	write once latch, see also NVL
WRES	watchdog timer reset
XRES	external reset I/O pin
XTAL	crystal

15. Reference Documents

PSoC® 3, PSoC® 5 Architecture TRM

PSoC® 5 Registers TRM