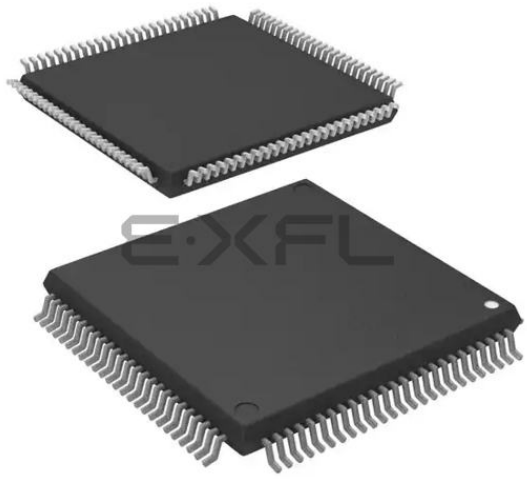
Renesas Electronics America Inc - M306NKFHGP#U3 Datasheet



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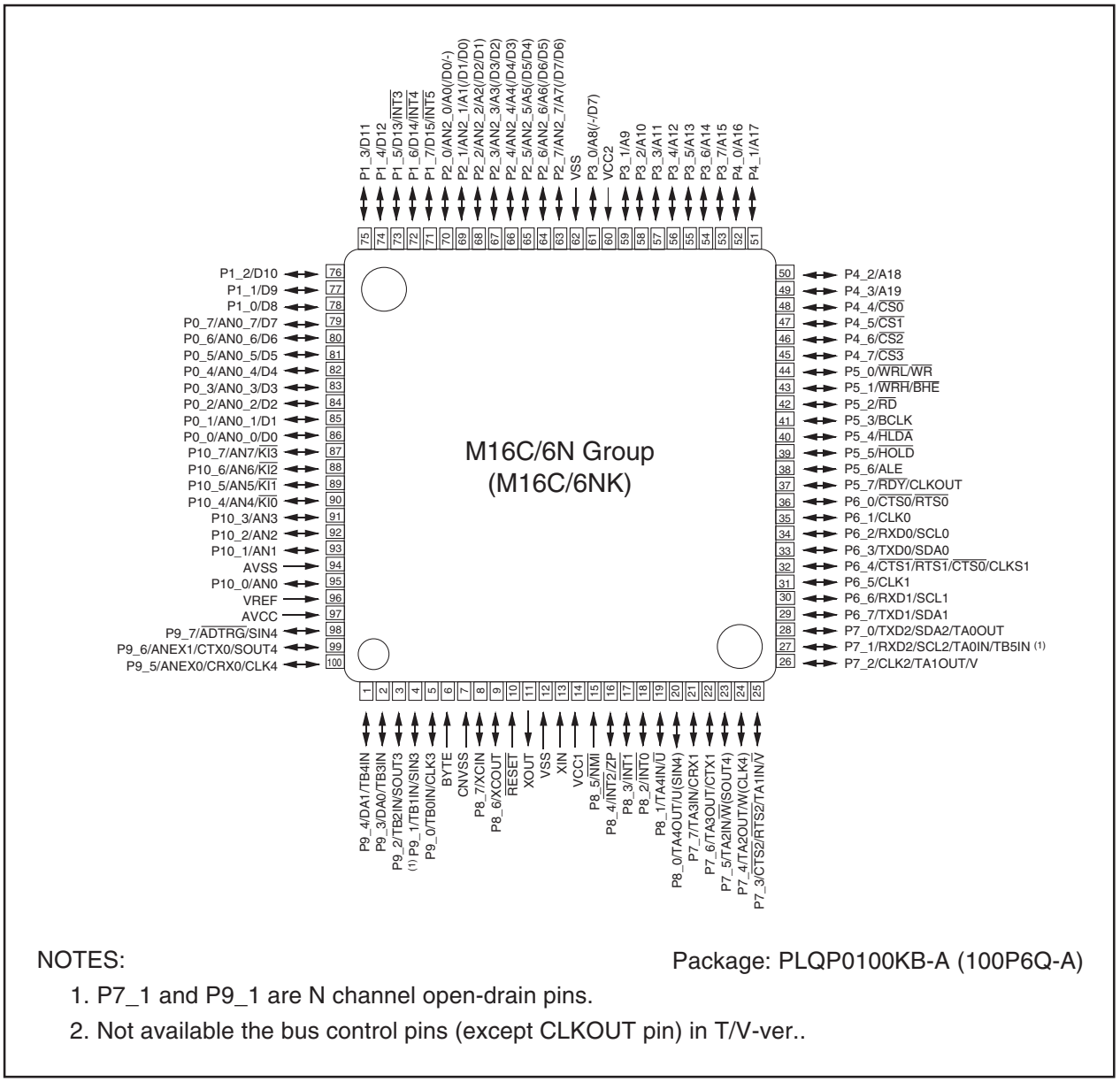
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	M16C/60
Core Size	16-Bit
Speed	24MHz
Connectivity	CANbus, I²C, IEBus, SIO, UART/USART
Peripherals	DMA, WDT
Number of I/O	85
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	31K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 26x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/m306nkfhgp-u3

1.5 Pin Assignments

Figures 1.3 and 1.4 show the Pin Assignment (Top View). Tables 1.4 to 1.8 list the List of Pin Names.



NOTES: Package: PLQP0100KB-A (100P6Q-A)

1. P7_1 and P9_1 are N channel open-drain pins.
2. Not available the bus control pins (except CLKOUT pin) in T/V-ver..

Figure 1.3 Pin Assignments (Top View) (1)

3. Memory

Figure 3.1 shows a Memory Map. The address space extends the 1 Mbyte from address 00000h to FFFFFh. The internal ROM is allocated in a lower address direction beginning with address FFFFFh. For example, a 512-Kbyte internal ROM is allocated to the addresses from 80000h to FFFFFh.

As for the flash memory version, 4-Kbyte space (block A) exists in 0F000h to 0FFFFh. 4-Kbyte space is mainly for storing data. In addition to storing data, 4-Kbyte space also can store programs.

The fixed interrupt vector table is allocated to the addresses from FFFDCh to FFFFFh. Therefore, store the start address of each interrupt routine here.

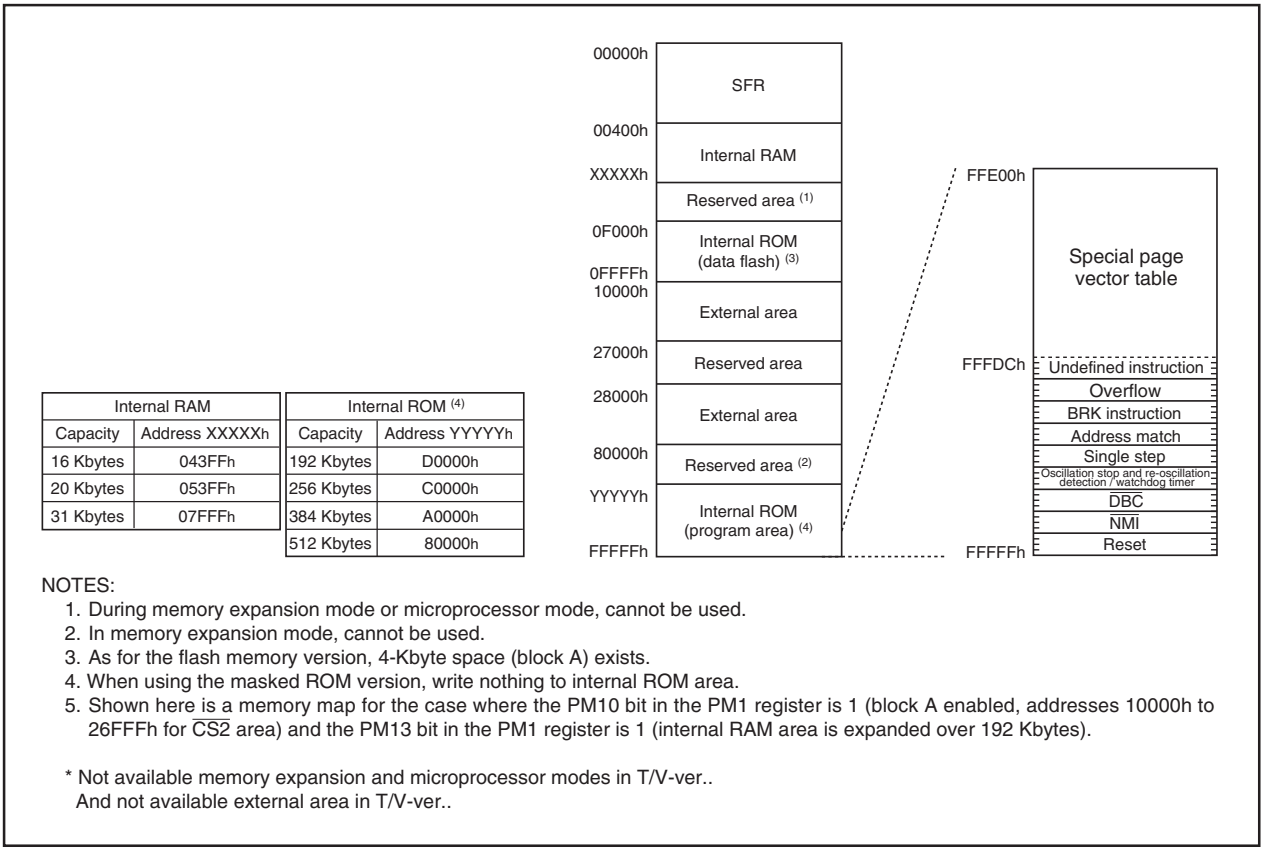
The internal RAM is allocated in an upper address direction beginning with address 00400h. For example, a 31-Kbyte internal RAM is allocated to the addresses from 00400h to 07FFFh. In addition to storing data, the internal RAM also stores the stack used when calling subroutines and when interrupts are generated.

The Special Function Registers (SFRs) are allocated to the addresses from 00000h to 003FFh. Peripheral function control registers are located here. Of the SFR, any area which has no functions allocated is reserved for future use and cannot be accessed by user.

The special page vector table is allocated to the addresses from FFE00h to FFFDBh. This vector is used by the JMPS or JSRS instruction. For details, refer to **M16C/60, M16C/20, M16C/Tiny Series Software Manual**.

In memory expansion and microprocessor modes, some areas are reserved for future use and cannot be used by users.

Use T/V-ver. in single-chip mode. The memory expansion and microprocessor modes cannot be used.



Internal RAM	
Capacity	Address XXXXXh
16 Kbytes	043FFh
20 Kbytes	053FFh
31 Kbytes	07FFFh

Internal ROM (4)	
Capacity	Address YYYYYh
192 Kbytes	D0000h
256 Kbytes	C0000h
384 Kbytes	A0000h
512 Kbytes	80000h

NOTES:
1. During memory expansion mode or microprocessor mode, cannot be used.
2. In memory expansion mode, cannot be used.
3. As for the flash memory version, 4-Kbyte space (block A) exists.
4. When using the masked ROM version, write nothing to internal ROM area.
5. Shown here is a memory map for the case where the PM10 bit in the PM1 register is 1 (block A enabled, addresses 10000h to 26FFFh for $\overline{CS2}$ area) and the PM13 bit in the PM1 register is 1 (internal RAM area is expanded over 192 Kbytes).

* Not available memory expansion and microprocessor modes in T/V-ver..
And not available external area in T/V-ver..

Figure 3.1 Memory Map

Table 4.6 SFR Information (6) [1]

Address	Register	Symbol	After Reset
0140h	CAN0 Message Box 14: Identifier /DLC		XXh
0141h			XXh
0142h			XXh
0143h			XXh
0144h			XXh
0145h			XXh
0146h	CAN0 Message Box 14: Data Field		XXh
0147h			XXh
0148h			XXh
0149h			XXh
014Ah			XXh
014Bh			XXh
014Ch			XXh
014Dh			XXh
014Eh	CAN0 Message Box 14: Time Stamp		XXh
014Fh			XXh
0150h	CAN0 Message Box 15: Identifier /DLC		XXh
0151h			XXh
0152h			XXh
0153h			XXh
0154h			XXh
0155h			XXh
0156h	CAN0 Message Box 15: Data Field		XXh
0157h			XXh
0158h			XXh
0159h			XXh
015Ah			XXh
015Bh			XXh
015Ch			XXh
015Dh			XXh
015Eh	CAN0 Message Box 15: Time Stamp		XXh
015Fh			XXh
0160h	CAN0 Global Mask Register	C0GMR	XXh
0161h			XXh
0162h			XXh
0163h			XXh
0164h			XXh
0165h			XXh
0166h	CAN0 Local Mask A Register	C0LMAR	XXh
0167h			XXh
0168h			XXh
0169h			XXh
016Ah			XXh
016Bh			XXh
016Ch	CAN0 Local Mask B Register	C0LMBR	XXh
016Dh			XXh
016Eh			XXh
016Fh			XXh
0170h			XXh
0171h			XXh
0172h			
0173h			
0174h			
0175h			
0176h			
0177h			
0178h			
0179h			
017Ah			
017Bh			
017Ch			
017Dh			
017Eh			
017Fh			

X: Undefined

NOTE:
1. Blank spaces are reserved. No access is allowed.

Table 4.7 SFR Information (7) [2]

Address	Register	Symbol	After Reset
0180h			
0181h			
0182h			
0183h			
0184h			
0185h			
0186h			
0187h			
0188h			
0189h			
018Ah			
018Bh			
018Ch			
018Dh			
018Eh			
018Fh			
0190h			
0191h			
0192h			
0193h			
0194h			
0195h			
0196h			
0197h			
0198h			
0199h			
019Ah			
019Bh			
019Ch			
019Dh			
019Eh			
019Fh			
01A0h			
01A1h			
01A2h			
01A3h			
01A4h			
01A5h			
01A6h			
01A7h			
01A8h			
01A9h			
01AAh			
01ABh			
01ACh			
01ADh			
01AEh			
01AFh			
01B0h			
01B1h			
01B2h			
01B3h			
01B4h			
01B5h	Flash Memory Control Register 1 [1]	FMR1	0X00XX0Xb
01B6h			
01B7h	Flash Memory Control Register 0 [1]	FMR0	00000001b
01B8h	Address Match Interrupt Register 2	RMAD2	00h
01B9h			00h
01BAh			X0h
01BBh	Address Match Interrupt Enable Register 2	AIER2	XXXXXX00b
01BCh	Address Match Interrupt Register 3	RMAD3	00h
01BDh			00h
01BEh			X0h
01BFh			

X: Undefined

NOTES:
1. These registers are included in the flash memory version. Cannot be accessed by users in the mask ROM version.
2. Blank spaces are reserved. No access is allowed.

Table 4.8 SFR Information (8) (3)

Address	Register	Symbol	After Reset
01C0h	Timer B3, B4, B5 Count Start Flag	TBSR	000XXXXXb
01C1h			
01C2h	Timer A1-1 Register	TA11	XXh
01C3h			XXh
01C4h	Timer A2-1 Register	TA21	XXh
01C5h			XXh
01C6h	Timer A4-1 Register	TA41	XXh
01C7h			XXh
01C8h	Three-Phase PWM Control Register 0	INVC0	00h
01C9h	Three-Phase PWM Control Register 1	INVC1	00h
01CAh	Three-Phase Output Buffer Register 0	IDB0	00111111b
01CBh	Three-Phase Output Buffer Register 1	IDB1	00111111b
01CCh	Dead Time Timer	DTT	XXh
01CDh	Timer B2 Interrupt Generation Frequency Set Counter	ICTB2	XXh
01CEh			
01CFh	Interrupt Source Select Register 2	IFSR2	X0000000b
01D0h	Timer B3 Register	TB3	XXh
01D1h			XXh
01D2h	Timer B4 Register	TB4	XXh
01D3h			XXh
01D4h	Timer B5 Register	TB5	XXh
01D5h			XXh
01D6h	SI/O6 Transmit/Receive Register (1)	S6TRR	XXh
01D7h			
01D8h	SI/O6 Control Register (1)	S6C	01000000b
01D9h	SI/O6 Bit Rate Register (1)	S6BRG	XXh
01DAh	SI/O3, 4, 5, 6 Transmit/Receive Register (2)	S3456TRR	XXXX0000b
01DBh	Timer B3 Mode Register	TB3MR	00XX0000b
01DCh	Timer B4 Mode Register	TB4MR	00XX0000b
01DDh	Timer B5 Mode Register	TB5MR	00XX0000b
01DEh	Interrupt Source Select Register 0	IFSR0	00h
01DFh	Interrupt Source Select Register 1	IFSR1	00h
01E0h	SI/O3 Transmit/Receive Register	S3TRR	XXh
01E1h			
01E2h	SI/O3 Control Register	S3C	01000000b
01E3h	SI/O3 Bit Rate Register	S3BRG	XXh
01E4h	SI/O4 Transmit/Receive Register	S4TRR	XXh
01E5h			
01E6h	SI/O4 Control Register	S4C	01000000b
01E7h	SI/O4 Bit Rate Register	S4BRG	XXh
01E8h	SI/O5 Transmit/Receive Register (1)	S5TRR	XXh
01E9h			
01EAh	SI/O5 Control Register (1)	S5C	01000000b
01EBh	SI/O5 Bit Rate Register (1)	S5BRG	XXh
01ECh	UART0 Special Mode Register 4	U0SMR4	00h
01EDh	UART0 Special Mode Register 3	U0SMR3	000X0X0Xb
01EEh	UART0 Special Mode Register 2	U0SMR2	X0000000b
01EFh	UART0 Special Mode Register	U0SMR	X0000000b
01F0h	UART1 Special Mode Register 4	U1SMR4	00h
01F1h	UART1 Special Mode Register 3	U1SMR3	000X0X0Xb
01F2h	UART1 Special Mode Register 2	U1SMR2	X0000000b
01F3h	UART1 Special Mode Register	U1SMR	X0000000b
01F4h	UART2 Special Mode Register 4	U2SMR4	00h
01F5h	UART2 Special Mode Register 3	U2SMR3	000X0X0Xb
01F6h	UART2 Special Mode Register 2	U2SMR2	X0000000b
01F7h	UART2 Special Mode Register	U2SMR	X0000000b
01F8h	UART2 Transmit/Receive Mode Register	U2MR	00h
01F9h	UART2 Bit Rate Register	U2BRG	XXh
01FAh	UART2 Transmit Buffer Register	U2TB	XXh
01FBh			XXh
01FCh	UART2 Transmit/Receive Control Register 0	U2C0	00001000b
01FDh	UART2 Transmit/Receive Control Register 1	U2C1	00000010b
01FEh	UART2 Receive Buffer Register	U2RB	XXh
01FFh			XXh

X: Undefined

NOTES:
1. These registers exist only in the 128-pin version.
2. Bits S5TRF and S6TRF in the S3456TRR register are used in the 128-pin version.
3. Blank spaces are reserved. No access is allowed.

Table 4.10 SFR Information (10) (1)

Address	Register	Symbol	After Reset
0240h			
0241h			
0242h	CAN0 Acceptance Filter Support Register	C0AFS	XXh
0243h			XXh
0244h	CAN1 Acceptance Filter Support Register	C1AFS	XXh
0245h			XXh
0246h			
0247h			
0248h			
0249h			
024Ah			
024Bh			
024Ch			
024Dh			
024Eh			
024Fh			
0250h			
0251h			
0252h			
0253h			
0254h			
0255h			
0256h			
0257h			
0258h			
0259h			
025Ah			
025Bh			
025Ch			
025Dh			
025Eh	Peripheral Clock Select Register	PCLKR	00h
025Fh	CAN0/1 Clock Select Register	CCLKR	00h
0260h	CAN1 Message Box 0: Identifier / DLC		XXh
0261h			XXh
0262h			XXh
0263h			XXh
0264h			XXh
0265h			XXh
0266h	CAN1 Message Box 0: Data Field		XXh
0267h			XXh
0268h			XXh
0269h			XXh
026Ah			XXh
026Bh			XXh
026Ch			XXh
026Dh			XXh
026Eh	CAN1 Message Box 0:Time Stamp		XXh
026Fh			XXh
0270h	CAN1 Message Box 1: Identifier / DLC		XXh
0271h			XXh
0272h			XXh
0273h			XXh
0274h			XXh
0275h			XXh
0276h	CAN1 Message Box 1: Data Field		XXh
0277h			XXh
0278h			XXh
0279h			XXh
027Ah			XXh
027Bh			XXh
027Ch			XXh
027Dh			XXh
027Eh	CAN1 Message Box 1:Time Stamp		XXh
027Fh			XXh

X: Undefined

NOTE:
1. Blank spaces are reserved. No access is allowed.

Table 4.12 SFR Information (12)

Address	Register	Symbol	After Reset
02C0h	CAN1 Message Box 6: Identifier / DLC		XXh
02C1h			XXh
02C2h			XXh
02C3h			XXh
02C4h			XXh
02C5h			XXh
02C6h	CAN1 Message Box 6: Data Field		XXh
02C7h			XXh
02C8h			XXh
02C9h			XXh
02CAh			XXh
02CBh			XXh
02CCh			XXh
02CDh			XXh
02CEh	CAN1 Message Box 6: Time Stamp		XXh
02CFh			XXh
02D0h	CAN1 Message Box 7: Identifier / DLC		XXh
02D1h			XXh
02D2h			XXh
02D3h			XXh
02D4h			XXh
02D5h			XXh
02D6h	CAN1 Message Box 7: Data Field		XXh
02D7h			XXh
02D8h			XXh
02D9h			XXh
02DAh			XXh
02DBh			XXh
02DCh			XXh
02DDh			XXh
02DEh	CAN1 Message Box 7: Time Stamp		XXh
02DFh			XXh
02E0h	CAN1 Message Box 8: Identifier / DLC		XXh
02E1h			XXh
02E2h			XXh
02E3h			XXh
02E4h			XXh
02E5h			XXh
02E6h	CAN1 Message Box 8: Data Field		XXh
02E7h			XXh
02E8h			XXh
02E9h			XXh
02EAh			XXh
02EBh			XXh
02ECh			XXh
02EDh			XXh
02EEh	CAN1 Message Box 8: Time Stamp		XXh
02EFh			XXh
02F0h	CAN1 Message Box 9: Identifier / DLC		XXh
02F1h			XXh
02F2h			XXh
02F3h			XXh
02F4h			XXh
02F5h			XXh
02F6h	CAN1 Message Box 9: Data Field		XXh
02F7h			XXh
02F8h			XXh
02F9h			XXh
02FAh			XXh
02FBh			XXh
02FCh			XXh
02FDh			XXh
02FEh	CAN1 Message Box 9: Time Stamp		XXh
02FFh			XXh

X: Undefined

Table 4.14 SFR Information (14) [1]

Address	Register	Symbol	After Reset
0340h	CAN1 Message Box 14: Identifier / DLC		XXh
0341h			XXh
0342h			XXh
0343h			XXh
0344h			XXh
0345h			XXh
0346h	CAN1 Message Box 14: Data Field		XXh
0347h			XXh
0348h			XXh
0349h			XXh
034Ah			XXh
034Bh			XXh
034Ch			XXh
034Dh			XXh
034Eh	CAN1 Message Box 14: Time Stamp		XXh
034Fh			XXh
0350h	CAN1 Message Box 15: Identifier / DLC		XXh
0351h			XXh
0352h			XXh
0353h			XXh
0354h			XXh
0355h			XXh
0356h	CAN1 Message Box 15: Data Field		XXh
0357h			XXh
0358h			XXh
0359h			XXh
035Ah			XXh
035Bh			XXh
035Ch			XXh
035Dh			XXh
035Eh	CAN1 Message Box 15: Time Stamp		XXh
035Fh			XXh
0360h	CAN1 Global Mask Register	C1GMR	XXh
0361h			XXh
0362h			XXh
0363h			XXh
0364h			XXh
0365h			XXh
0366h	CAN1 Local Mask A Register	C1LMAR	XXh
0367h			XXh
0368h			XXh
0369h			XXh
036Ah			XXh
036Bh			XXh
036Ch	CAN1 Local Mask B Register	C1LMBR	XXh
036Dh			XXh
036Eh			XXh
036Fh			XXh
0370h			XXh
0371h			XXh
0372h			
0373h			
0374h			
0375h			
0376h			
0377h			
0378h			
0379h			
037Ah			
037Bh			
037Ch			
037Dh			
037Eh			
037Fh			

X: Undefined

NOTE:
1. Blank spaces are reserved. No access is allowed.

5. Electrical Characteristics

5.1 Electrical Characteristics (Normal-ver.)

Table 5.1 Absolute Maximum Ratings

Symbol	Parameter		Condition	Rated Value	Unit
V_{CC}	Supply voltage (VCC1 = VCC2)		VCC = AVCC	–0.3 to 6.5	V
AV_{CC}	Analog supply voltage		VCC = AVCC	–0.3 to 6.5	V
V_I	Input voltage	$\overline{RESET}$, CNVSS, BYTE, P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0, P7_2 to P7_7, P8_0 to P8_7, P9_0, P9_2 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1, VREF, XIN		–0.3 to VCC+0.3	V
		P7_1, P9_1		–0.3 to 6.5	V
V_O	Output voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0, P9_2 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1, XOUT		–0.3 to VCC+0.3	V
		P7_1, P9_1		–0.3 to 6.5	V
P_d	Power dissipation		Topr = 25°C	700	mW
T_{opr}	Operating ambient temperature	During MCU operation		–40 to 85	°C
		During flash memory program and erase operation		0 to 60	
T_{stg}	Storage temperature			–65 to 150	°C

NOTE:
1. Ports P11 to P14 are only in the 128-pin version.

Table 5.2 Recommended Operating Conditions (1) [1]

Symbol	Parameter		Standard			Unit
			Min.	Typ.	Max.	
V_{CC}	Supply voltage (VCC1 = VCC2)		3.0	5.0	5.5	V
AV_{CC}	Analog supply voltage			V_{CC}		V
V_{SS}	Supply voltage			0		V
AV_{SS}	Analog supply voltage			0		V
V_{IH}	HIGH input voltage	P3_1 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0, P7_2 to P7_7, P8_0 to P8_7, P9_0, P9_2 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1, XIN, $\overline{RESET}$, CNVSS, BYTE	0.8 V_{CC}		V_{CC}	V
		P7_1, P9_1	0.8 V_{CC}		6.5	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 (During single-chip mode)	0.8 V_{CC}		V_{CC}	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 (Data input during memory expansion and microprocessor modes)	0.5 V_{CC}		V_{CC}	
V_{IL}	LOW input voltage	P3_1 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1, XIN, $\overline{RESET}$, CNVSS, BYTE	0		0.2 V_{CC}	V V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 (During single-chip mode)	0		0.2 V_{CC}	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 (Data input during memory expansion and microprocessor modes)	0		0.16 V_{CC}	V
$I_{OH(peak)}$	HIGH peak output current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0, P9_2 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1			–10.0	mA
$I_{OH(avg)}$	HIGH average output current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0, P9_2 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1			–5.0	mA
$I_{OL(peak)}$	LOW peak output current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1			10.0	mA
$I_{OL(avg)}$	LOW average output current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1			5.0	mA

NOTES:
1. Referenced to VCC = 3.0 to 5.5 V at Topr = –40 to 85°C unless otherwise specified.
2. Average output current values during 100 ms period.
3. The total $I_{OL(peak)}$ for ports P0, P1, P2, P8_6, P8_7, P9, P10, P11, P14_0, and P14_1 must be 80 mA max.
   The total $I_{OL(peak)}$ for ports P3, P4, P5, P6, P7, P8_0 to P8_4, P12, and P13 must be 80 mA max.
   The total $I_{OH(peak)}$ for ports P0, P1, and P2 must be –40 mA max.
   The total $I_{OH(peak)}$ for ports P3, P4, P5, P12, and P13 must be –40 mA max.
   The total $I_{OH(peak)}$ for ports P6, P7, and P8_0 to P8_4 must be –40 mA max.
   The total $I_{OH(peak)}$ for ports P8_6, P8_7, P9, P10, P11, P14_0, and P14_1 must be –40 mA max.
4. P11 to P14 are only in the 128-pin version.

Table 5.5 Electrical Characteristics (2) [1]

Symbol	Parameter		Measuring Condition		Standard			Unit
					Min.	Typ.	Max.	
I_{CC}	Power supply current (VCC = 3.0 to 5.5 V)	In single-chip mode, the output pins are open and other pins are VSS.	Mask ROM	f(BCLK) = 24 MHz, PLL operation, No division		21	37	mA
				On-chip oscillation, No division		1		mA
			Flash memory	f(BCLK) = 24 MHz, PLL operation, No division		23	39	mA
				On-chip oscillation, No division		1.8		mA
			Flash memory program	f(BCLK) = 10 MHz, VCC = 5 V		15		mA
			Flash memory erase	f(BCLK) = 10 MHz, VCC = 5 V		25		mA
			Mask ROM	f(BCLK) = 32 kHz, Low power dissipation mode, ROM [2]		25		µA
			Flash memory	f(BCLK) = 32 kHz, Low power dissipation mode, RAM [2]		25		µA
				f(BCLK) = 32 kHz, Low power dissipation mode, Flash memory [2]		420		µA
			Mask ROM Flash memory	On-chip oscillation, Wait mode		50		µA
				f(BCLK) = 32 kHz, Wait mode [3], Oscillation capacity High		8.5		µA
				f(BCLK) = 32 kHz, Wait mode [3], Oscillation capacity Low		3.0		µA
				Stop mode, Topr = 25°C		0.8	3.0	µA

NOTES:
1. Referenced to VCC = 3.0 to 5.5 V, VSS = 0 V at Topr = –40 to 85°C, f(BCLK) = 24 MHz unless otherwise specified.
2. This indicates the memory in which the program to be executed exists.
3. With one timer operated using fC32.

Timing Requirements

VCC = 5 V

(Referenced to VCC = 5 V, VSS = 0 V, at Topr = –40 to 85°C unless otherwise specified)

Table 5.11 External Clock Input (XIN Input)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t_C	External clock input cycle time	62.5		ns
$t_{w(H)}$	External clock input HIGH pulse width	25		ns
$t_{w(L)}$	External clock input LOW pulse width	25		ns
t_r	External clock rise time		15	ns
t_f	External clock fall time		15	ns

Table 5.12 Memory Expansion Mode and Microprocessor Mode

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{ac1(RD-DB)}$	Data input access time (for setting with no wait)		(NOTE 1)	ns
$t_{ac2(RD-DB)}$	Data input access time (for setting with wait)		(NOTE 2)	ns
$t_{ac3(RD-DB)}$	Data input access time (when accessing multiplexed bus area)		(NOTE 3)	ns
$t_{su(DB-RD)}$	Data input setup time	40		ns
$t_{su(RDY-BCLK)}$	$\overline{RDY}$ input setup time	30		ns
$t_{su(HOLD-BCLK)}$	$\overline{HOLD}$ input setup time	40		ns
$t_{h(RD-DB)}$	Data input hold time	0		ns
$t_{h(BCLK-RDY)}$	$\overline{RDY}$ input hold time	0		ns
$t_{h(BCLK-HOLD)}$	$\overline{HOLD}$ input hold time	0		ns

NOTES:

1. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(BCLK)} - 45 \text{ [ns]}$$

2. Calculated according to the BCLK frequency as follows:

$$\frac{(n - 0.5) \times 10^9}{f(BCLK)} - 45 \text{ [ns]}$$

n is “2” for 1-wait setting, “3” for 2-wait setting and “4” for 3-wait setting.

3. Calculated according to the BCLK frequency as follows:

$$\frac{(n - 0.5) \times 10^9}{f(BCLK)} - 45 \text{ [ns]}$$

n is “2” for 2-wait setting, “3” for 3-wait setting.

Timing Requirements

VCC = 5 V

(Referenced to VCC = 5 V, VSS = 0 V, at Topr = –40 to 85°C unless otherwise specified)

Table 5.13 Timer A Input (Counter Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	100		ns
$t_{w(TAH)}$	TAiIN input HIGH pulse width	40		ns
$t_{w(TAL)}$	TAiIN input LOW pulse width	40		ns

Table 5.14 Timer A Input (Gating Input in Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	400		ns
$t_{w(TAH)}$	TAiIN input HIGH pulse width	200		ns
$t_{w(TAL)}$	TAiIN input LOW pulse width	200		ns

Table 5.15 Timer A Input (External Trigger Input in One-shot Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	200		ns
$t_{w(TAH)}$	TAiIN input HIGH pulse width	100		ns
$t_{w(TAL)}$	TAiIN input LOW pulse width	100		ns

Table 5.16 Timer A Input (External Trigger Input in Pulse Width Modulation Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(TAH)}$	TAiIN input HIGH pulse width	100		ns
$t_{w(TAL)}$	TAiIN input LOW pulse width	100		ns

Table 5.17 Timer A Input (Counter Increment/decrement Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(UP)}$	TAiOUT input cycle time	2000		ns
$t_{w(UPH)}$	TAiOUT input HIGH pulse width	1000		ns
$t_{w(UPL)}$	TAiOUT input LOW pulse width	1000		ns
$t_{su(UP-TIN)}$	TAiOUT input setup time	400		ns
$t_{h(TIN-UP)}$	TAiOUT input hold time	400		ns

Table 5.18 Timer A Input (Two-phase Pulse Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	800		ns
$t_{su(TAIN-TAOUT)}$	TAiOUT input setup time	200		ns
$t_{su(TAOUT-TAIN)}$	TAiIN input setup time	200		ns

Switching Characteristics

VCC = 5 V

(Referenced to VCC = 5 V, VSS = 0 V, at Topr = –40 to 85 °C unless otherwise specified)

Table 5.26 Memory Expansion Mode and Microprocessor Mode (for 1- to 3-wait setting and external area access)

Symbol	Parameter	Measuring Condition	Standard		Unit
			Min.	Max.	
$t_{d(BCLK-AD)}$	Address output delay time	Figure 5.2		25	ns
$t_{h(BCLK-AD)}$	Address output hold time (in relation to BCLK)		4		ns
$t_{h(RD-AD)}$	Address output hold time (in relation to RD)		0		ns
$t_{h(WR-AD)}$	Address output hold time (in relation to WR)		(NOTE 1)		ns
$t_{d(BCLK-CS)}$	Chip select output delay time			25	ns
$t_{h(BCLK-CS)}$	Chip select output hold time (in relation to BCLK)		4		ns
$t_{d(BCLK-ALE)}$	ALE signal output delay time			15	ns
$t_{h(BCLK-ALE)}$	ALE signal output hold time		–4		ns
$t_{d(BCLK-RD)}$	RD signal output delay time			25	ns
$t_{h(BCLK-RD)}$	RD signal output hold time		0		ns
$t_{d(BCLK-WR)}$	WR signal output delay time			25	ns
$t_{h(BCLK-WR)}$	WR signal output hold time		0		ns
$t_{d(BCLK-DB)}$	Data output delay time (in relation to BCLK)			40	ns
$t_{h(BCLK-DB)}$	Data output hold time (rin relation to BCLK) (3)		4		ns
$t_{d(DB-WR)}$	Data output delay time (in relation to WR)		(NOTE 2)		ns
$t_{h(WR-DB)}$	Data output hold time (in relation to WR) (3)		(NOTE 1)		ns
$t_{d(BCLK-HLDA)}$	$\overline{HLDA}$ output delay time			40	ns

NOTES:

1. Calculated according to the BCLK frequency as follows:

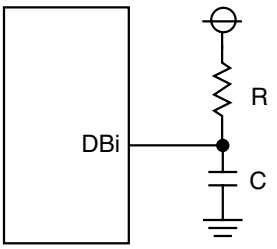
$$\frac{0.5 \times 10^9}{f(BCLK)} - 10 \text{ [ns]}$$

2. Calculated according to the BCLK frequency as follows:

$$\frac{(n - 0.5) \times 10^9}{f(BCLK)} - 40 \text{ [ns]}$$

n is “1” for 1-wait setting, “2” for 2-wait setting and “3” for 3-wait setting. When n = 1, f(BCLK) is 12.5 MHz or less.

3. This standard value shows the timing when the output is off, and does not show hold time of data bus.
Hold time of data bus varies with capacitor volume and pull-up (pull-down) resistance value.
Hold time of data bus is expressed in
$t = -CR \times \ln (1 - V_{OL} / V_{CC})$
by a circuit of the right figure.
For example, when $V_{OL} = 0.2\ V_{CC}$, C = 30 pF, R =1 kΩ, hold time of output “L” level is
$t = -30\text{ pF} \times 1\text{ k}\Omega \times \ln (1 - 0.2\ V_{CC} / V_{CC}) = 6.7$ ns.

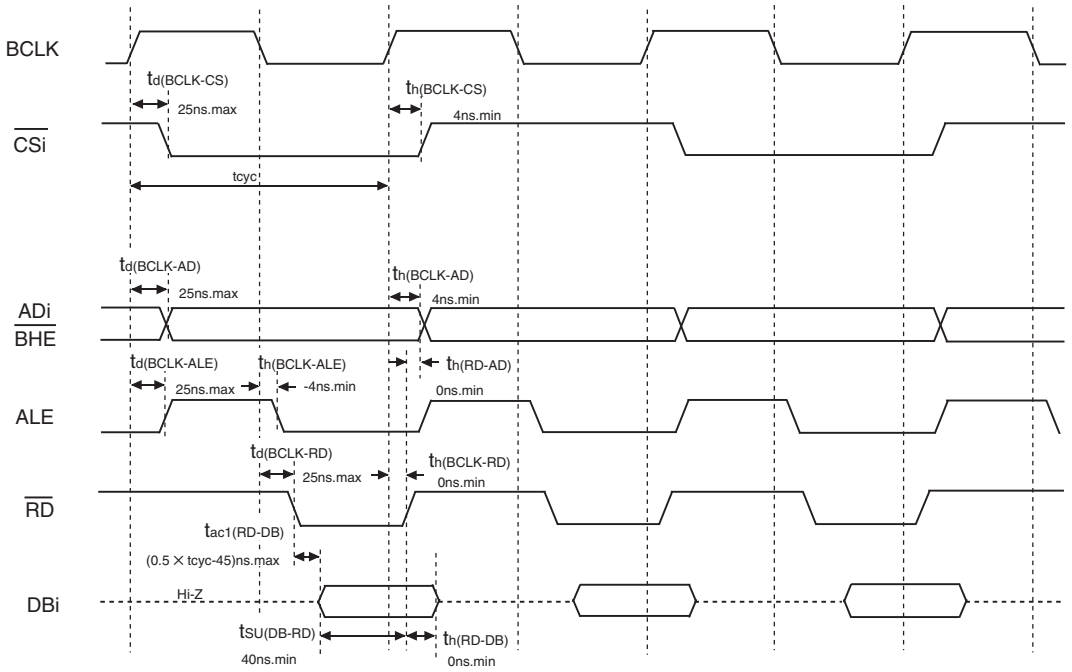


Memory Expansion Mode and Microprocessor Mode

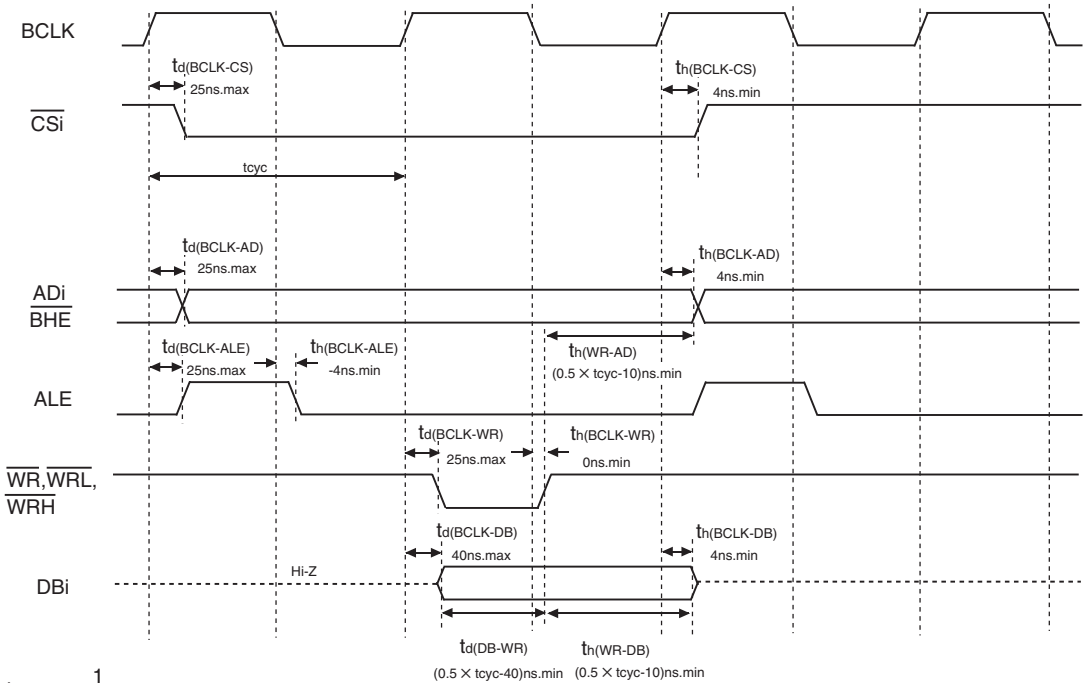
VCC = 5 V

(For setting with no wait)

Read timing



Write timing



$$tcyc = \frac{1}{f(BCLK)}$$

Measuring conditions :

- VCC = 5 V
- Input timing voltage : V_{IL} = 0.8 V, V_{IH} = 2.0 V
- Output timing voltage : V_{OL} = 0.4 V, V_{OH} = 2.4 V

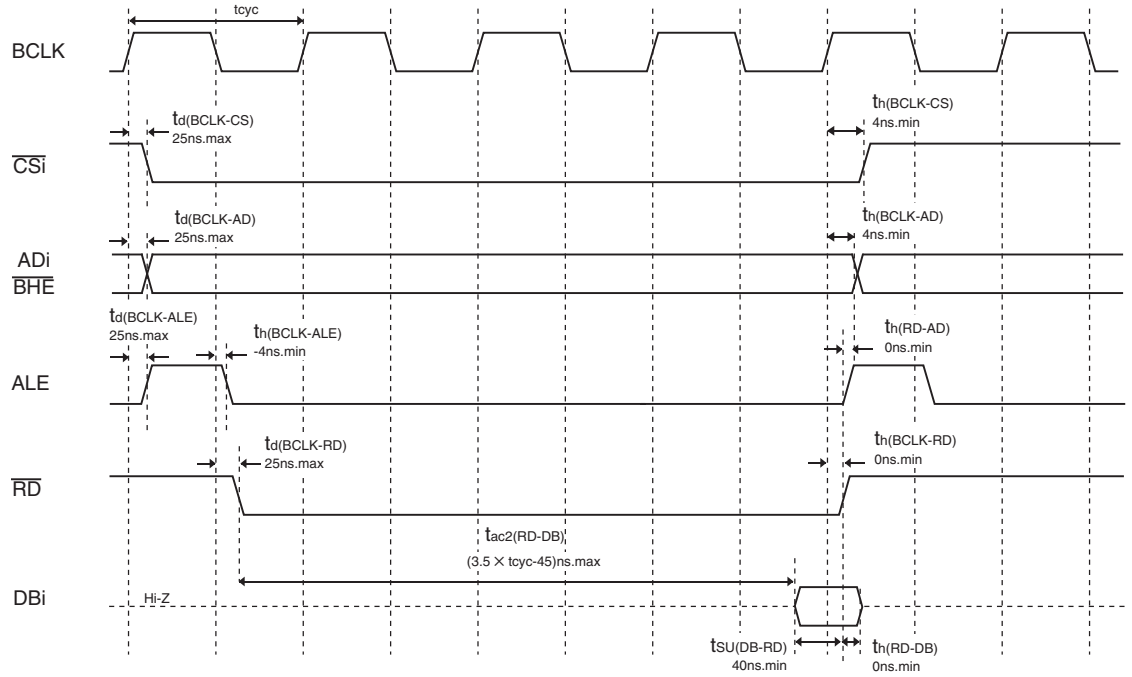
Figure 5.5 Timing Diagram (3)

Memory Expansion Mode and Microprocessor Mode

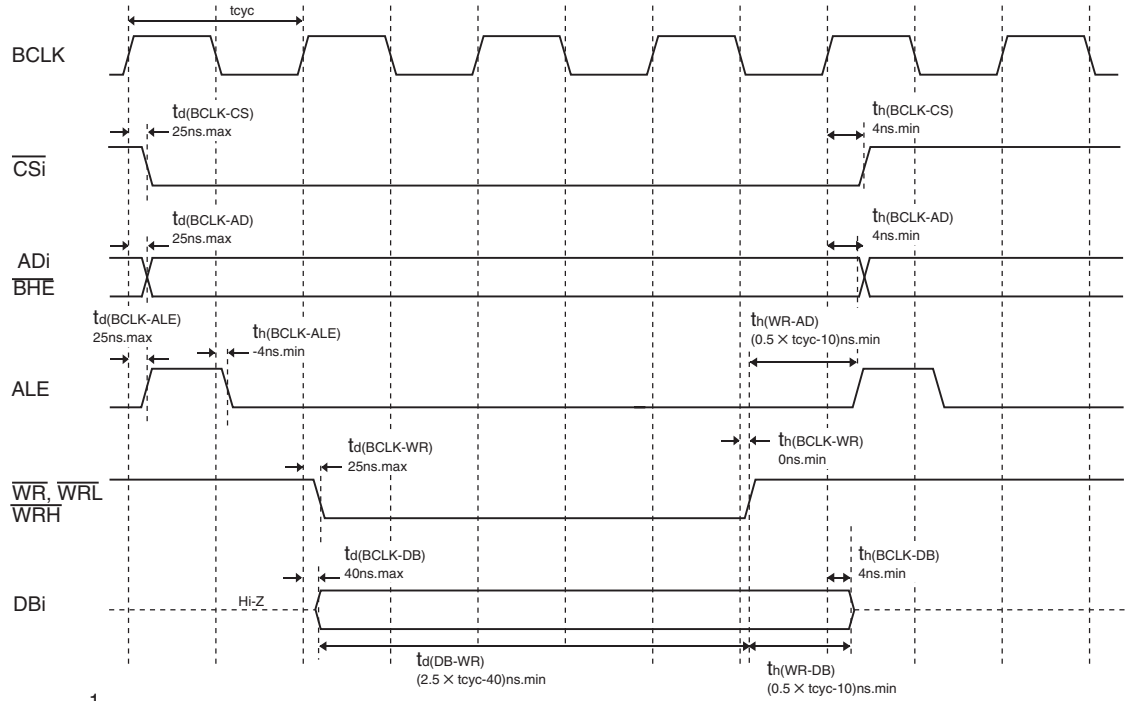
VCC = 5 V

(For 3-wait setting and external area access)

Read timing



Write timing



$$tcyc = \frac{1}{f(BCLK)}$$

Measuring conditions :

- VCC = 5 V
- Input timing voltage : V_{IL} = 0.8 V, V_{IH} = 2.0 V
- Output timing voltage : V_{OL} = 0.4 V, V_{OH} = 2.4 V

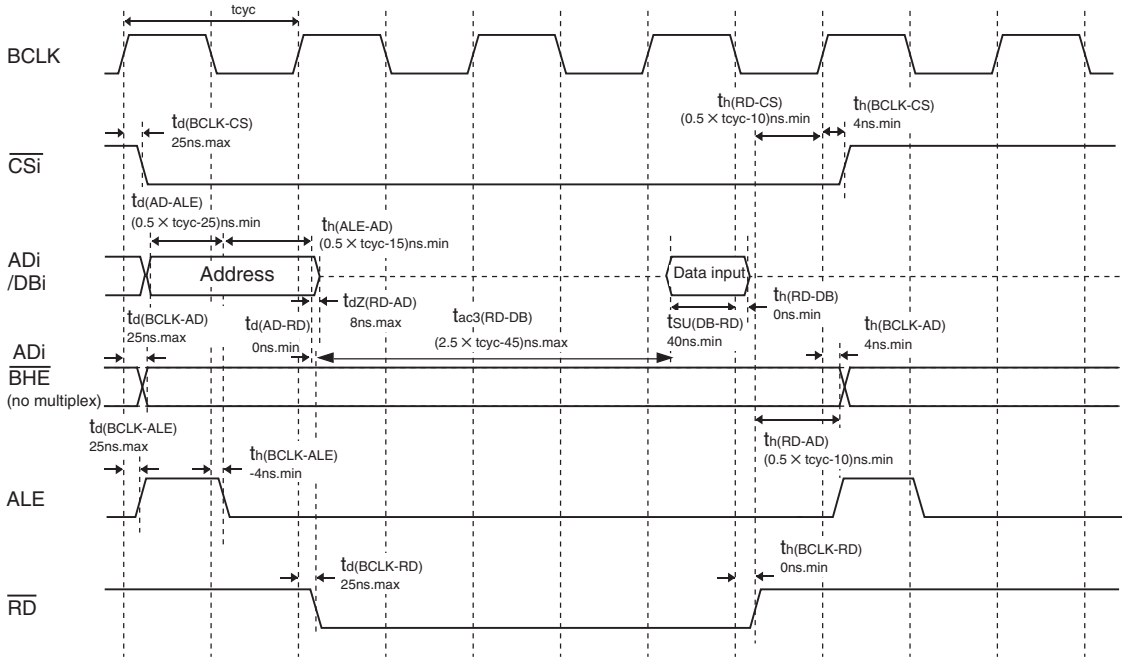
Figure 5.8 Timing Diagram (6)

Memory Expansion Mode and Microprocessor Mode

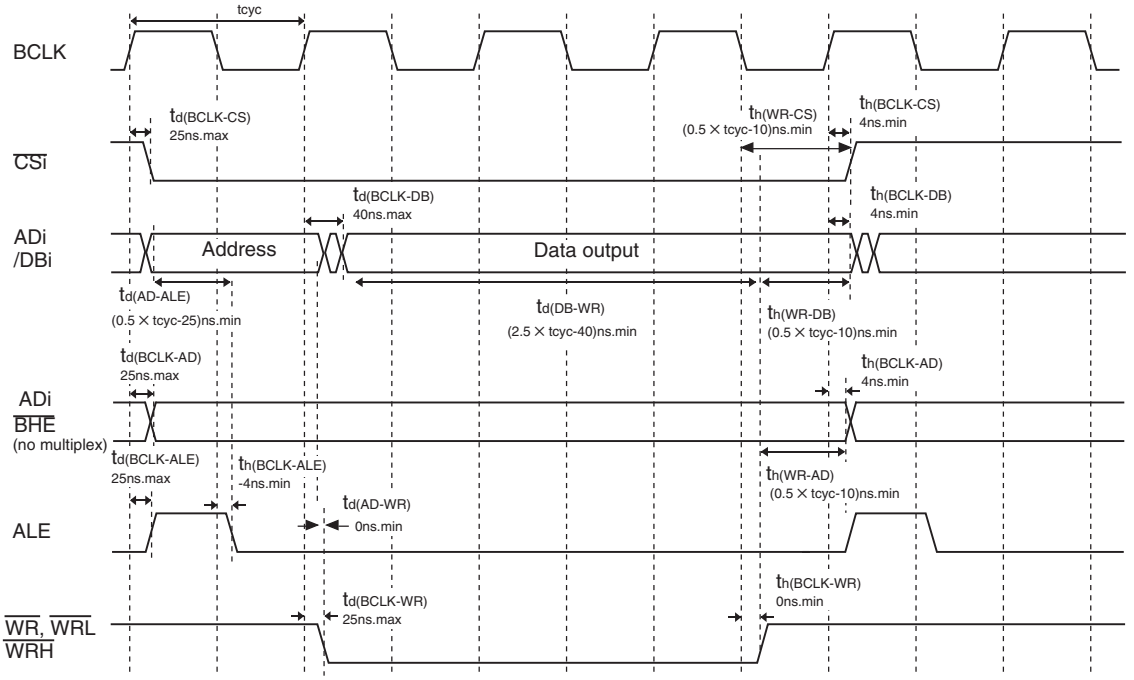
VCC = 5 V

(For 3-wait setting, external area access and multiplexed bus selection)

Read timing



Write timing



$$tcyc = \frac{1}{f(BCLK)}$$

Measuring conditions :

- VCC = 5 V
- Input timing voltage : V_{IL} = 0.8 V, V_{IH} = 2.0 V
- Output timing voltage : V_{OL} = 0.4 V, V_{OH} = 2.4 V

Figure 5.10 Timing Diagram (8)

Table 5.28 Electrical Characteristics (1) **VCC = 3.3 V**

Symbol	Parameter			Measuring Condition	Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	HIGH output voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0, P9_2 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1		I_{OH} = –1 mA	V_{CC}-0.5		V_{CC}	V
V_{OH}	HIGH output voltage	XOUT	HIGHPOWER	I_{OH} = –0.1 mA	V_{CC}-0.5		V_{CC}	V
			LOWPOWER	I_{OH} = –50 µA	V_{CC}-0.5		V_{CC}	
	HIGH output voltage	XCOUT	HIGHPOWER	With no load applied		2.5		V
			LOWPOWER	With no load applied		1.6		
V_{OL}	LOW output voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1		I_{OL} = 1 mA			0.5	V
V_{OL}	LOW output voltage	XOUT	HIGHPOWER	I_{OL} = 0.1 mA			0.5	V
			LOWPOWER	I_{OL} = 50 µA			0.5	
	LOW output voltage	XCOUT	HIGHPOWER	With no load applied		0		V
			LOWPOWER	With no load applied		0		
V_{T+}-V_{T-}	Hysteresis	$\overline{HOLD}$, $\overline{RDY}$, TA0IN to TA4IN, TB0IN to TB5IN, $\overline{INT0}$ to $\overline{INT8}$, NMI, $\overline{ADTRG}$, $\overline{CTS0}$ to $\overline{CTS2}$, SCL0 to SCL2, SDA0 to SDA2, CLK0 to CLK6, TA0OUT to TA4OUT, $\overline{KI0}$ to $\overline{KI3}$, RXD0 to RXD2, SIN3 to SIN6			0.2		0.8	V
V_{T+}-V_{T-}	Hysteresis	$\overline{RESET}$			0.2		1.8	V
I_{IH}	HIGH input current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1, XIN, $\overline{RESET}$, CNVSS, BYTE		V_I = 3.3 V			4.0	µA
I_{IL}	LOW input current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1, XIN, $\overline{RESET}$, CNVSS, BYTE		V_I = 0 V			–4.0	µA
R_{PULLUP}	Pull-up resistance	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0, P9_2 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1		V_I = 0 V	50	100	500	kΩ
R_{fXIN}	Feedback resistance	XIN				3.0		MΩ
R_{fXCIN}	Feedback resistance	XCIN				25		MΩ
V_{RAM}	RAM retention voltage			At stop mode	2.0			V

NOTES:
1. Referenced to VCC = 3.0 to 3.6 V, VSS = 0 V at Topr = –40 to 85°C, f(BCLK) = 24 MHz unless otherwise specified.
2. P11 to P14, $\overline{INT6}$ to $\overline{INT8}$, CLK5, CLK6, SIN5, and SIN6 are only in the 128-pin version.

Switching Characteristics VCC = 3.3 V

(Referenced to VCC = 3.3 V, VSS = 0 V, at Topr = –40 to 85 °C unless otherwise specified)

Table 5.44 Memory Expansion Mode and Microprocessor Mode (for 1- to 3-wait setting and external area access)

Symbol	Parameter	Measuring Condition	Standard		Unit
			Min.	Max.	
$t_{d(BCLK-AD)}$	Address output delay time	Figure 5.11		30	ns
$t_{h(BCLK-AD)}$	Address output hold time (in relation to BCLK)		4		ns
$t_{h(RD-AD)}$	Address output hold time (in relation to RD)		0		ns
$t_{h(WR-AD)}$	Address output hold time (in relation to WR)		(NOTE 1)		ns
$t_{d(BCLK-CS)}$	Chip select output delay time			30	ns
$t_{h(BCLK-CS)}$	Chip select output hold time (in relation to BCLK)		4		ns
$t_{d(BCLK-ALE)}$	ALE signal output delay time			25	ns
$t_{h(BCLK-ALE)}$	ALE signal output hold time		–4		ns
$t_{d(BCLK-RD)}$	RD signal output delay time			30	ns
$t_{h(BCLK-RD)}$	RD signal output hold time		0		ns
$t_{d(BCLK-WR)}$	WR signal output delay time			30	ns
$t_{h(BCLK-WR)}$	WR signal output hold time		0		ns
$t_{d(BCLK-DB)}$	Data output delay time (in relation to BCLK)			40	ns
$t_{h(BCLK-DB)}$	Data output hold time (in relation to BCLK) (3)		4		ns
$t_{d(DB-WR)}$	Data output delay time (in relation to WR)		(NOTE 2)		ns
$t_{h(WR-DB)}$	Data output hold time (in relation to WR) (3)		(NOTE 1)		ns
$t_{d(BCLK-HLDA)}$	$\overline{HLDA}$ output delay time			40	ns

NOTES:

1. Calculated according to the BCLK frequency as follows:

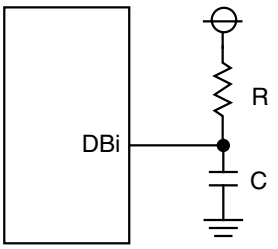
$$\frac{0.5 \times 10^9}{f(BCLK)} - 10 \text{ [ns]}$$

2. Calculated according to the BCLK frequency as follows:

$$\frac{(n - 0.5) \times 10^9}{f(BCLK)} - 40 \text{ [ns]}$$

n is “1” for 1-wait setting, “2” for 2-wait setting and “3” for 3-wait setting. When n = 1, f(BCLK) is 12.5 MHz or less.

3. This standard value shows the timing when the output is off, and does not show hold time of data bus.
Hold time of data bus varies with capacitor volume and pull-up (pull-down) resistance value.
Hold time of data bus is expressed in
$t = -CR \times \ln (1 - V_{OL} / V_{CC})$
by a circuit of the right figure.
For example, when $V_{OL} = 0.2\ V_{CC}$, C = 30 pF, R =1 kΩ, hold time of output “L” level is
$t = -30\ pF \times 1\ k\Omega \times \ln (1 - 0.2\ V_{CC} / V_{CC}) = 6.7$ ns.



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