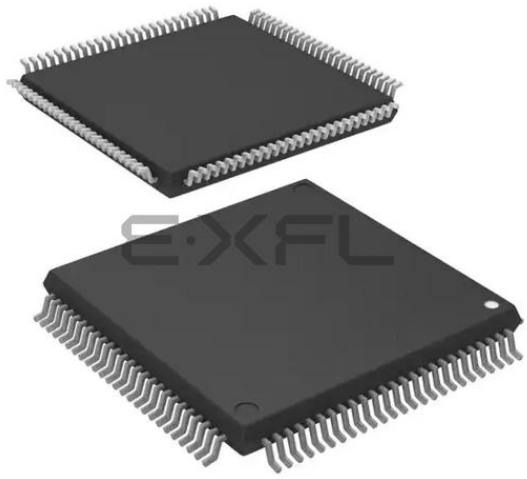
Renesas Electronics America Inc - M306NKFJGP#U3 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	M16C/60
Core Size	16-Bit
Speed	24MHz
Connectivity	CANbus, I²C, IEBus, SIO, UART/USART
Peripherals	DMA, WDT
Number of I/O	85
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	31K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 26x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/m306nkfjgp-u3

Table 1.2 Functions and Specifications for M16C/6N Group (128-pin Version: M16C/6NM)

Item			Specification	
			Normal-ver.	T/V-ver.
CPU	Number of fundamental instructions		91 instructions	
	Minimum instruction execution time		41.7 ns (f(BCLK) = 24 MHz, 1/1 prescaler, without software wait)	50.0 ns (f(BCLK) = 20 MHz, 1/1 prescaler, without software wait)
	Operating mode		Single-chip, memory expansion, and microprocessor modes	Single-chip mode
	Address space		1 Mbyte	
	Memory capacity		Refer to **Table 1.3 Product Information**	
Peripheral Function	Ports		Input/Output: 113 pins, Input: 1 pin	
	Multifunction timers		Timer A: 16 bits × 5 channels Timer B: 16 bits × 6 channels Three-phase motor control circuit	
	Serial interfaces		3 channels Clock synchronous, UART, I²C-bus (1), IEBus (2) 4 channels Clock synchronous	
	A/D converter		10-bit A/D converter: 1 circuit, 26 channels	
	D/A converter		8 bits × 2 channels	
	DMAC		2 channels	
	CRC calculation circuit		CRC-CCITT	
	CAN module		2 channels with 2.0B specification	
	Watchdog timer		15 bits × 1 channel (with prescaler)	
	Interrupts		Internal: 34 sources, External: 12 sources Software: 4 sources, Priority levels: 7 levels	
	Clock generation circuits		4 circuits • Main clock oscillation circuit (*) • Sub clock oscillation circuit (*) • On-chip oscillator • PLL frequency synthesizer (*) Equipped with on-chip feedback resistor	
	Oscillation-stopped detector		Main clock oscillation stop and re-oscillation detection function	
Electrical Characteristics	Supply voltage		VCC = 3.0 to 5.5 V (f(BCLK) = 24 MHz, 1/1 prescaler, without software wait)	VCC = 4.2 to 5.5 V (f(BCLK) = 20 MHz, 1/1 prescaler, without software wait)
	Consumption current	Mask ROM	21 mA (f(BCLK) = 24 MHz, PLL operation, no division)	-
		Flash memory	23 mA (f(BCLK) = 24 MHz, PLL operation, no division)	21 mA (f(BCLK) = 20 MHz, PLL operation, no division)
		Mask ROM	3 µA (f(BCLK) = 32 kHz, Wait mode, Oscillation capacity Low)	
		Flash memory	0.8 µA (Stop mode, Topr = 25°C)	
Flash Memory Version	Programming and erasure voltage		3.0 ± 0.3 V or 5.0 ± 0.5 V	5.0 ± 0.5 V
	Programming and erasure endurance		100 times	
I/O Characteristics	I/O withstand voltage		5.0 V	
	Output current		5 mA	
Operating Ambient Temperature			-40 to 85°C	T version: -40 to 85°C V version: -40 to 125°C (option)
Device Configuration			CMOS high-performance silicon gate	
Package			128-pin molded-plastic LQFP	

NOTES:
1. I²C-bus is a trademark of Koninklijke Philips Electronics N.V.
2. IEBus is a trademark of NEC Electronics Corporation.

option: All options are on request basis.

1.3 Block Diagram

Figure 1.1 shows a Block Diagram.

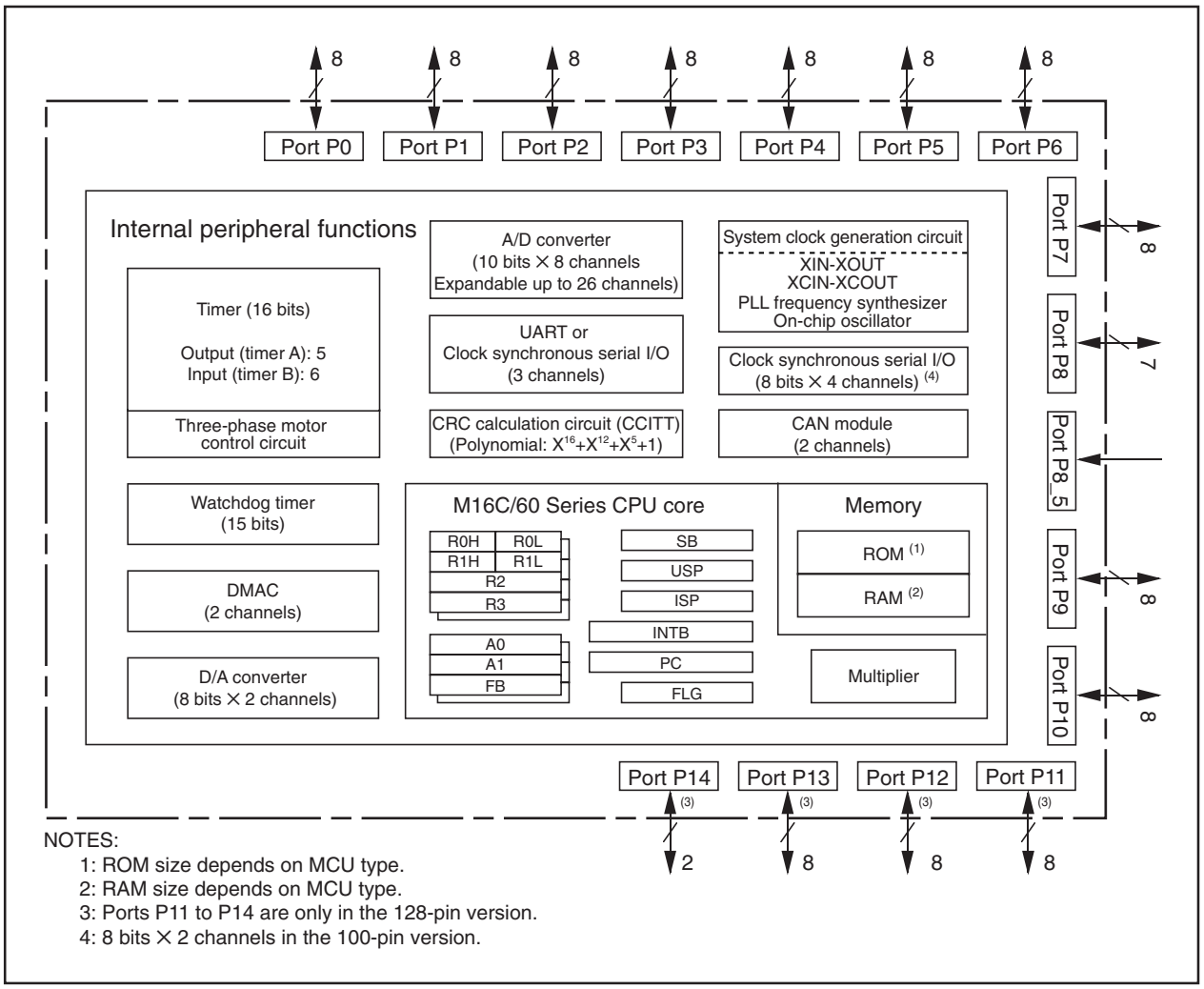


Figure 1.1 Block Diagram

1.4 Product Information

Table 1.3 lists the Product Information and Figure 1.2 shows the Type Number, Memory Size, and Packages.

Table 1.3 Product Information As of Aug. 2006

Type No.	ROM Capacity	RAM Capacity	Package Type (2)	Remarks	
M306NKFHGP	384 K + 4 Kbytes	31 Kbytes	PLQP0100KB-A	Flash memory version (1)	Normal-ver.
M306NMFHGP			PLQP0128KB-A		
M306NKFJGP	512 K + 4 Kbytes	31 Kbytes	PLQP0100KB-A		
M306NMFJGP			PLQP0128KB-A		
M306NKFHTGP (D)	384 K + 4 Kbytes	31 Kbytes	PLQP0100KB-A		T-ver.
M306NMFHTGP (D)			PLQP0128KB-A		
M306NKFJTGP	512 K + 4 Kbytes	31 Kbytes	PLQP0100KB-A		
M306NMFJTGP			PLQP0128KB-A		
M306NKFHVGP (D)	384 K + 4 Kbytes	31 Kbytes	PLQP0100KB-A		V-ver.
M306NMFHVGP (D)			PLQP0128KB-A		
M306NKFJVGP (D)	512 K + 4 Kbytes	31 Kbytes	PLQP0100KB-A		
M306NMFJVGP (D)			PLQP0128KB-A		
M306NKME-XXXGP	192 Kbytes	16 Kbytes	PLQP0100KB-A	Mask ROM version	Normal-ver.
M306NMME-XXXGP			PLQP0128KB-A		
M306NKMG-XXXGP	256 Kbytes	20 Kbytes	PLQP0100KB-A		
M306NMMG-XXXGP			PLQP0128KB-A		

(D): Under development

NOTES:

1. Data flash memory provides an additional 4 Kbytes of ROM capacity (block A).
2. The correspondence between new and old package types is as follows.
   PLQP0100KB-A: 100P6Q-A
   PLQP0128KB-A: 128P6Q-A

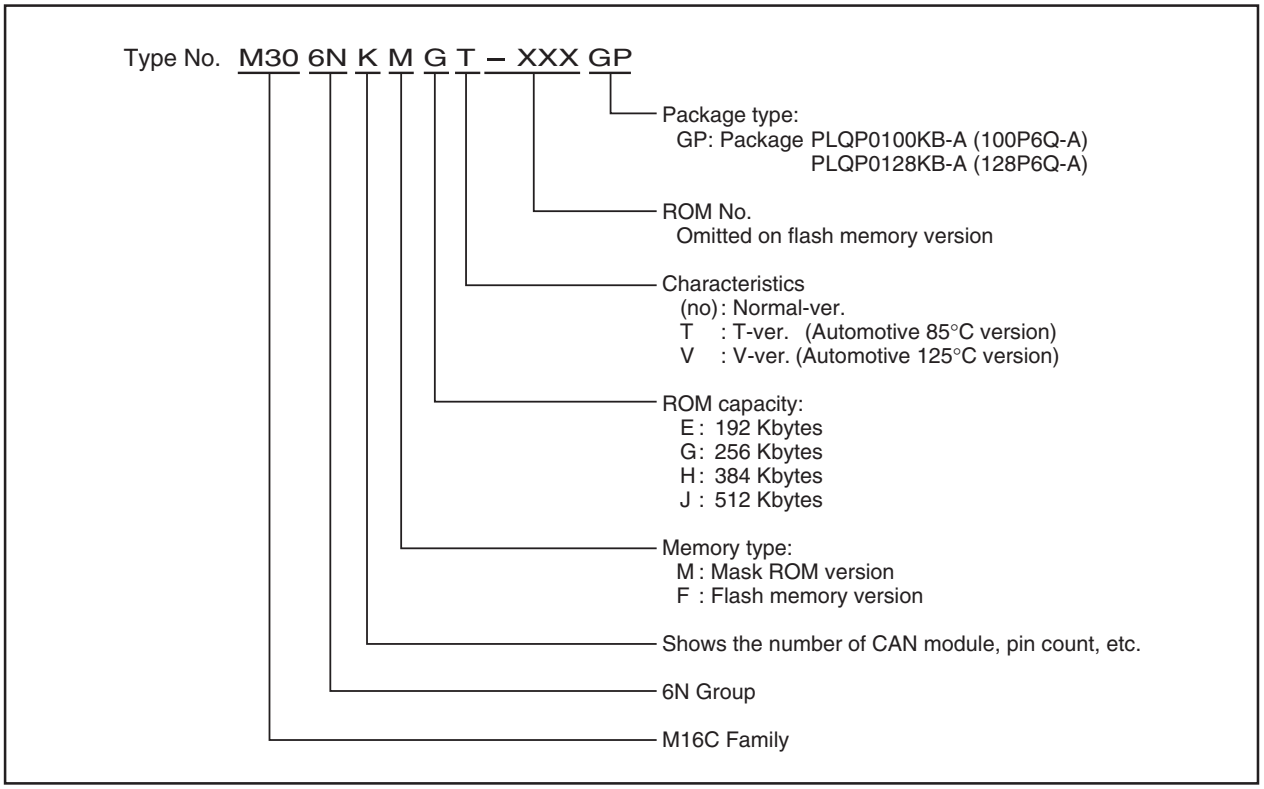


Figure 1.2 Type Number, Memory Size, and Package

3. Memory

Figure 3.1 shows a Memory Map. The address space extends the 1 Mbyte from address 00000h to FFFFFh. The internal ROM is allocated in a lower address direction beginning with address FFFFFh. For example, a 512-Kbyte internal ROM is allocated to the addresses from 80000h to FFFFFh.

As for the flash memory version, 4-Kbyte space (block A) exists in 0F000h to 0FFFFh. 4-Kbyte space is mainly for storing data. In addition to storing data, 4-Kbyte space also can store programs.

The fixed interrupt vector table is allocated to the addresses from FFFDCh to FFFFFh. Therefore, store the start address of each interrupt routine here.

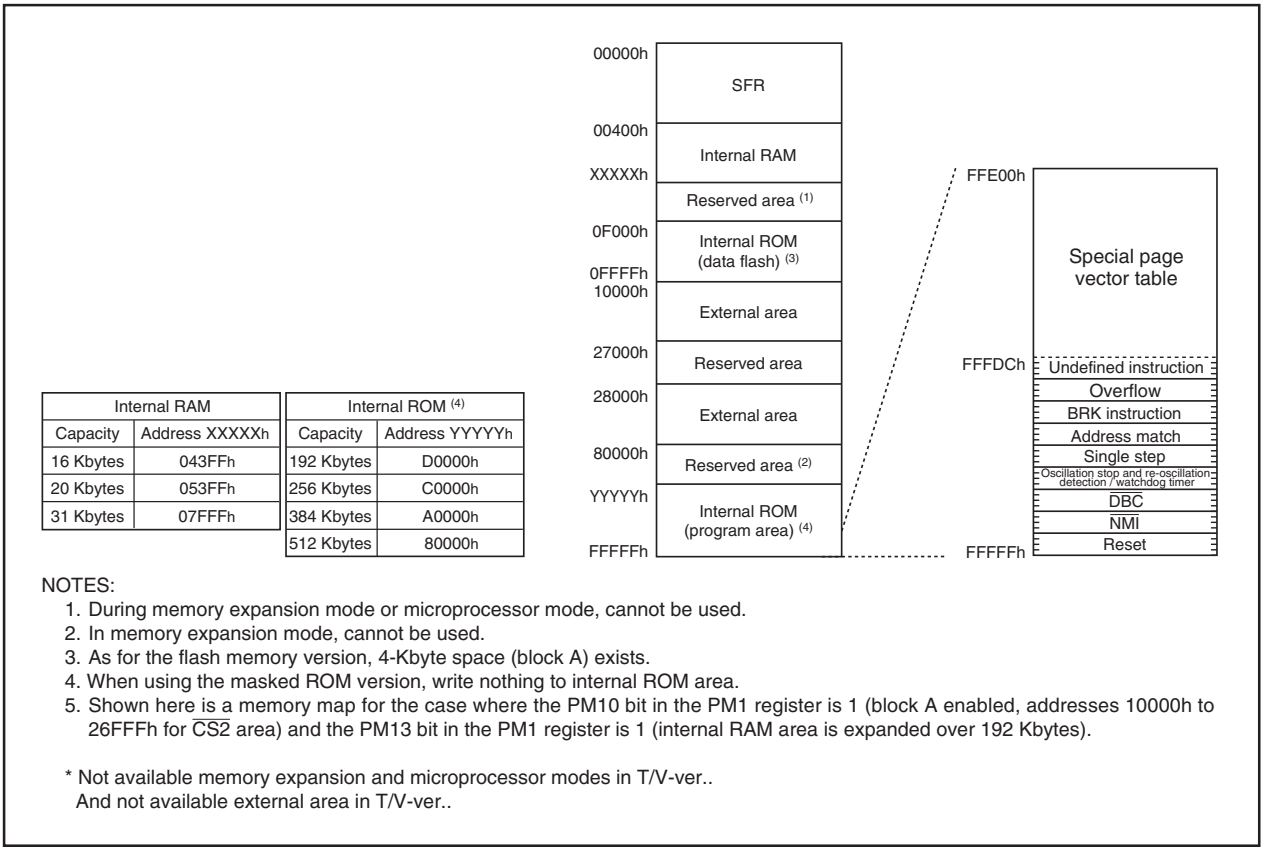
The internal RAM is allocated in an upper address direction beginning with address 00400h. For example, a 31-Kbyte internal RAM is allocated to the addresses from 00400h to 07FFFh. In addition to storing data, the internal RAM also stores the stack used when calling subroutines and when interrupts are generated.

The Special Function Registers (SFRs) are allocated to the addresses from 00000h to 003FFh. Peripheral function control registers are located here. Of the SFR, any area which has no functions allocated is reserved for future use and cannot be accessed by user.

The special page vector table is allocated to the addresses from FFE00h to FFFDBh. This vector is used by the JMPS or JSRS instruction. For details, refer to **M16C/60, M16C/20, M16C/Tiny Series Software Manual**.

In memory expansion and microprocessor modes, some areas are reserved for future use and cannot be used by users.

Use T/V-ver. in single-chip mode. The memory expansion and microprocessor modes cannot be used.



Internal RAM	
Capacity	Address XXXXXh
16 Kbytes	043FFh
20 Kbytes	053FFh
31 Kbytes	07FFFh

Internal ROM (4)	
Capacity	Address YYYYYh
192 Kbytes	D0000h
256 Kbytes	C0000h
384 Kbytes	A0000h
512 Kbytes	80000h

NOTES:
1. During memory expansion mode or microprocessor mode, cannot be used.
2. In memory expansion mode, cannot be used.
3. As for the flash memory version, 4-Kbyte space (block A) exists.
4. When using the masked ROM version, write nothing to internal ROM area.
5. Shown here is a memory map for the case where the PM10 bit in the PM1 register is 1 (block A enabled, addresses 10000h to 26FFFh for $\overline{CS2}$ area) and the PM13 bit in the PM1 register is 1 (internal RAM area is expanded over 192 Kbytes).

* Not available memory expansion and microprocessor modes in T/V-ver..
And not available external area in T/V-ver..

Figure 3.1 Memory Map

Table 4.5 SFR Information (5)

Address	Register	Symbol	After Reset
0100h	CAN0 Message Box 10: Identifier / DLC		XXh
0101h			XXh
0102h			XXh
0103h			XXh
0104h			XXh
0105h			XXh
0106h	CAN0 Message Box 10: Data Field		XXh
0107h			XXh
0108h			XXh
0109h			XXh
010Ah			XXh
010Bh			XXh
010Ch			XXh
010Dh			XXh
010Eh	CAN0 Message Box 10: Time Stamp		XXh
010Fh			XXh
0110h	CAN0 Message Box 11: Identifier / DLC		XXh
0111h			XXh
0112h			XXh
0113h			XXh
0114h			XXh
0115h			XXh
0116h	CAN0 Message Box 11: Data Field		XXh
0117h			XXh
0118h			XXh
0119h			XXh
011Ah			XXh
011Bh			XXh
011Ch			XXh
011Dh			XXh
011Eh	CAN0 Message Box 11: Time Stamp		XXh
011Fh			XXh
0120h	CAN0 Message Box 12: Identifier / DLC		XXh
0121h			XXh
0122h			XXh
0123h			XXh
0124h			XXh
0125h			XXh
0126h	CAN0 Message Box 12: Data Field		XXh
0127h			XXh
0128h			XXh
0129h			XXh
012Ah			XXh
012Bh			XXh
012Ch			XXh
012Dh			XXh
012Eh	CAN0 Message Box 12: Time Stamp		XXh
012Fh			XXh
0130h	CAN0 Message Box 13: Identifier / DLC		XXh
0131h			XXh
0132h			XXh
0133h			XXh
0134h			XXh
0135h			XXh
0136h	CAN0 Message Box 13: Data Field		XXh
0137h			XXh
0138h			XXh
0139h			XXh
013Ah			XXh
013Bh			XXh
013Ch			XXh
013Dh			XXh
013Eh	CAN0 Message Box 13: Time Stamp		XXh
013Fh			XXh

X: Undefined

Table 4.6 SFR Information (6) [1]

Address	Register	Symbol	After Reset
0140h	CAN0 Message Box 14: Identifier /DLC		XXh
0141h			XXh
0142h			XXh
0143h			XXh
0144h			XXh
0145h			XXh
0146h	CAN0 Message Box 14: Data Field		XXh
0147h			XXh
0148h			XXh
0149h			XXh
014Ah			XXh
014Bh			XXh
014Ch			XXh
014Dh			XXh
014Eh	CAN0 Message Box 14: Time Stamp		XXh
014Fh			XXh
0150h	CAN0 Message Box 15: Identifier /DLC		XXh
0151h			XXh
0152h			XXh
0153h			XXh
0154h			XXh
0155h			XXh
0156h	CAN0 Message Box 15: Data Field		XXh
0157h			XXh
0158h			XXh
0159h			XXh
015Ah			XXh
015Bh			XXh
015Ch			XXh
015Dh			XXh
015Eh	CAN0 Message Box 15: Time Stamp		XXh
015Fh			XXh
0160h	CAN0 Global Mask Register	C0GMR	XXh
0161h			XXh
0162h			XXh
0163h			XXh
0164h			XXh
0165h			XXh
0166h	CAN0 Local Mask A Register	C0LMAR	XXh
0167h			XXh
0168h			XXh
0169h			XXh
016Ah			XXh
016Bh			XXh
016Ch	CAN0 Local Mask B Register	C0LMBR	XXh
016Dh			XXh
016Eh			XXh
016Fh			XXh
0170h			XXh
0171h			XXh
0172h			
0173h			
0174h			
0175h			
0176h			
0177h			
0178h			
0179h			
017Ah			
017Bh			
017Ch			
017Dh			
017Eh			
017Fh			

X: Undefined

NOTE:
1. Blank spaces are reserved. No access is allowed.

Table 4.11 SFR Information (11)

Address	Register	Symbol	After Reset
0280h	CAN1 Message Box 2: Identifier / DLC		XXh
0281h			XXh
0282h			XXh
0283h			XXh
0284h			XXh
0285h			XXh
0286h	CAN1 Message Box 2: Data Field		XXh
0287h			XXh
0288h			XXh
0289h			XXh
028Ah			XXh
028Bh			XXh
028Ch			XXh
028Dh			XXh
028Eh	CAN1 Message Box 2: Time Stamp		XXh
028Fh			XXh
0290h	CAN1 Message Box 3: Identifier / DLC		XXh
0291h			XXh
0292h			XXh
0293h			XXh
0294h			XXh
0295h			XXh
0296h	CAN1 Message Box 3: Data Field		XXh
0297h			XXh
0298h			XXh
0299h			XXh
029Ah			XXh
029Bh			XXh
029Ch			XXh
029Dh			XXh
029Eh	CAN1 Message Box 3: Time Stamp		XXh
029Fh			XXh
02A0h	CAN1 Message Box 4: Identifier / DLC		XXh
02A1h			XXh
02A2h			XXh
02A3h			XXh
02A4h			XXh
02A5h			XXh
02A6h	CAN1 Message Box 4: Data Field		XXh
02A7h			XXh
02A8h			XXh
02A9h			XXh
02AAh			XXh
02ABh			XXh
02ACh			XXh
02ADh			XXh
02AEh	CAN1 Message Box 4: Time Stamp		XXh
02AFh			XXh
02B0h	CAN1 Message Box 5: Identifier / DLC		XXh
02B1h			XXh
02B2h			XXh
02B3h			XXh
02B4h			XXh
02B5h			XXh
02B6h	CAN1 Message Box 5: Data Field		XXh
02B7h			XXh
02B8h			XXh
02B9h			XXh
02BAh			XXh
02BBh			XXh
02BCh			XXh
02BDh			XXh
02BEh	CAN1 Message Box 5: Time Stamp		XXh
02BFh			XXh

X: Undefined

Table 5.2 Recommended Operating Conditions (1) [1]

Symbol	Parameter		Standard			Unit
			Min.	Typ.	Max.	
V_{CC}	Supply voltage (VCC1 = VCC2)		3.0	5.0	5.5	V
AV_{CC}	Analog supply voltage			V_{CC}		V
V_{SS}	Supply voltage			0		V
AV_{SS}	Analog supply voltage			0		V
V_{IH}	HIGH input voltage	P3_1 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0, P7_2 to P7_7, P8_0 to P8_7, P9_0, P9_2 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1, XIN, $\overline{RESET}$, CNVSS, BYTE	0.8 V_{CC}		V_{CC}	V
		P7_1, P9_1	0.8 V_{CC}		6.5	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 (During single-chip mode)	0.8 V_{CC}		V_{CC}	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 (Data input during memory expansion and microprocessor modes)	0.5 V_{CC}		V_{CC}	
V_{IL}	LOW input voltage	P3_1 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1, XIN, $\overline{RESET}$, CNVSS, BYTE	0		0.2 V_{CC}	V V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 (During single-chip mode)	0		0.2 V_{CC}	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 (Data input during memory expansion and microprocessor modes)	0		0.16 V_{CC}	V
$I_{OH(peak)}$	HIGH peak output current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0, P9_2 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1			–10.0	mA
$I_{OH(avg)}$	HIGH average output current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0, P9_2 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1			–5.0	mA
$I_{OL(peak)}$	LOW peak output current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1			10.0	mA
$I_{OL(avg)}$	LOW average output current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1			5.0	mA

NOTES:
1. Referenced to VCC = 3.0 to 5.5 V at Topr = –40 to 85°C unless otherwise specified.
2. Average output current values during 100 ms period.
3. The total $I_{OL(peak)}$ for ports P0, P1, P2, P8_6, P8_7, P9, P10, P11, P14_0, and P14_1 must be 80 mA max.
   The total $I_{OL(peak)}$ for ports P3, P4, P5, P6, P7, P8_0 to P8_4, P12, and P13 must be 80 mA max.
   The total $I_{OH(peak)}$ for ports P0, P1, and P2 must be –40 mA max.
   The total $I_{OH(peak)}$ for ports P3, P4, P5, P12, and P13 must be –40 mA max.
   The total $I_{OH(peak)}$ for ports P6, P7, and P8_0 to P8_4 must be –40 mA max.
   The total $I_{OH(peak)}$ for ports P8_6, P8_7, P9, P10, P11, P14_0, and P14_1 must be –40 mA max.
4. P11 to P14 are only in the 128-pin version.

Table 5.3 Recommended Operating Conditions (2) (1)

Symbol	Parameter				Standard			Unit
					Min.	Typ.	Max.	
f(XIN)	Main clock input oscillation frequency (2) (3) (4)	No wait	Mask ROM version Flash memory version	VCC = 3.0 to 5.5 V	0		16	MHz
f(XCIN)	Sub clock oscillation frequency					32.768	50	kHz
f(Ring)	On-chip oscillation frequency					1		MHz
f(PLL)	PLL clock oscillation frequency				16		24	MHz
f(BCLK)	CPU operation clock			VCC = 3.0 to 5.5 V	0		24	MHz
$t_{su(PLL)}$	PLL frequency synthesizer stabilization wait time						20	ms

NOTES:

1. Referenced to VCC = 3.0 to 5.5 V at Topr = –40 to 85°C unless otherwise specified.
2. Relationship between main clock oscillation frequency and supply voltage is shown right.
3. Execute program/erase of flash memory by VCC = 3.3 ± 0.3 V or VCC = 5.0 ± 0.5 V.
4. When using 16 MHz and over, use PLL clock. PLL clock oscillation frequency which can be used is 16 MHz, 20 MHz or 24 MHz.

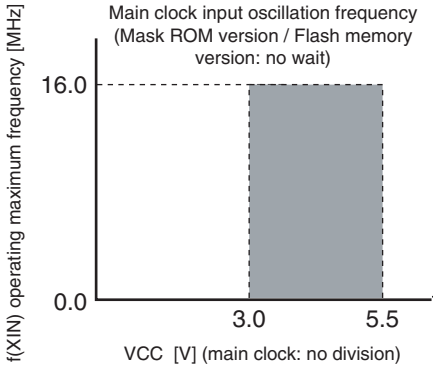


Table 5.5 Electrical Characteristics (2) [1]

Symbol	Parameter		Measuring Condition		Standard			Unit
					Min.	Typ.	Max.	
I_{CC}	Power supply current (VCC = 3.0 to 5.5 V)	In single-chip mode, the output pins are open and other pins are VSS.	Mask ROM	f(BCLK) = 24 MHz, PLL operation, No division		21	37	mA
				On-chip oscillation, No division		1		mA
			Flash memory	f(BCLK) = 24 MHz, PLL operation, No division		23	39	mA
				On-chip oscillation, No division		1.8		mA
			Flash memory program	f(BCLK) = 10 MHz, VCC = 5 V		15		mA
			Flash memory erase	f(BCLK) = 10 MHz, VCC = 5 V		25		mA
			Mask ROM	f(BCLK) = 32 kHz, Low power dissipation mode, ROM [2]		25		µA
			Flash memory	f(BCLK) = 32 kHz, Low power dissipation mode, RAM [2]		25		µA
				f(BCLK) = 32 kHz, Low power dissipation mode, Flash memory [2]		420		µA
			Mask ROM Flash memory	On-chip oscillation, Wait mode		50		µA
				f(BCLK) = 32 kHz, Wait mode [3], Oscillation capacity High		8.5		µA
				f(BCLK) = 32 kHz, Wait mode [3], Oscillation capacity Low		3.0		µA
				Stop mode, Topr = 25°C		0.8	3.0	µA

NOTES:
1. Referenced to VCC = 3.0 to 5.5 V, VSS = 0 V at Topr = –40 to 85°C, f(BCLK) = 24 MHz unless otherwise specified.
2. This indicates the memory in which the program to be executed exists.
3. With one timer operated using fC32.

Timing Requirements

VCC = 5 V

(Referenced to VCC = 5 V, VSS = 0 V, at Topr = –40 to 85°C unless otherwise specified)

Table 5.19 Timer B Input (Counter Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time (counted on one edge)	100		ns
$t_{w(TBH)}$	TBiIN input HIGH pulse width (counted on one edge)	40		ns
$t_{w(TBL)}$	TBiIN input LOW pulse width (counted on one edge)	40		ns
$t_{c(TB)}$	TBiIN input cycle time (counted on both edges)	200		ns
$t_{w(TBH)}$	TBiIN input HIGH pulse width (counted on both edges)	80		ns
$t_{w(TBL)}$	TBiIN input LOW pulse width (counted on both edges)	80		ns

Table 5.20 Timer B Input (Pulse Period Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time	400		ns
$t_{w(TBH)}$	TBiIN input HIGH pulse width	200		ns
$t_{w(TBL)}$	TBiIN input LOW pulse width	200		ns

Table 5.21 Timer B Input (Pulse Width Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time	400		ns
$t_{w(TBH)}$	TBiIN input HIGH pulse width	200		ns
$t_{w(TBL)}$	TBiIN input LOW pulse width	200		ns

Table 5.22 A/D Trigger Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{C(AD)}$	$\overline{\text{ADTRG}}$ input cycle time (trigger able minimum)	1000		ns
$t_{w(ADL)}$	$\overline{\text{ADTRG}}$ input LOW pulse width	125		ns

Table 5.23 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	200		ns
$t_{w(CKH)}$	CLKi input HIGH pulse width	100		ns
$t_{w(CKL)}$	CLKi input LOW pulse width	100		ns
$t_{d(C-Q)}$	TXDi output delay time		80	ns
$t_{h(C-Q)}$	TXDi hold time	0		ns
$t_{su(D-C)}$	RXDi input setup time	70		ns
$t_{h(C-D)}$	RXDi input hold time	90		ns

Table 5.24 External Interrupt $\overline{\text{INTi}}$ Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{\text{INTi}}$ input HIGH pulse width	250		ns
$t_{w(INL)}$	$\overline{\text{INTi}}$ input LOW pulse width	250		ns

Switching Characteristics

VCC = 5 V

(Referenced to VCC = 5 V, VSS = 0 V, at Topr = –40 to 85 °C unless otherwise specified)

Table 5.26 Memory Expansion Mode and Microprocessor Mode (for 1- to 3-wait setting and external area access)

Symbol	Parameter	Measuring Condition	Standard		Unit
			Min.	Max.	
$t_{d(BCLK-AD)}$	Address output delay time	Figure 5.2		25	ns
$t_{h(BCLK-AD)}$	Address output hold time (in relation to BCLK)		4		ns
$t_{h(RD-AD)}$	Address output hold time (in relation to RD)		0		ns
$t_{h(WR-AD)}$	Address output hold time (in relation to WR)		(NOTE 1)		ns
$t_{d(BCLK-CS)}$	Chip select output delay time			25	ns
$t_{h(BCLK-CS)}$	Chip select output hold time (in relation to BCLK)		4		ns
$t_{d(BCLK-ALE)}$	ALE signal output delay time			15	ns
$t_{h(BCLK-ALE)}$	ALE signal output hold time		–4		ns
$t_{d(BCLK-RD)}$	RD signal output delay time			25	ns
$t_{h(BCLK-RD)}$	RD signal output hold time		0		ns
$t_{d(BCLK-WR)}$	WR signal output delay time			25	ns
$t_{h(BCLK-WR)}$	WR signal output hold time		0		ns
$t_{d(BCLK-DB)}$	Data output delay time (in relation to BCLK)			40	ns
$t_{h(BCLK-DB)}$	Data output hold time (rin relation to BCLK) (3)		4		ns
$t_{d(DB-WR)}$	Data output delay time (in relation to WR)		(NOTE 2)		ns
$t_{h(WR-DB)}$	Data output hold time (in relation to WR) (3)		(NOTE 1)		ns
$t_{d(BCLK-HLDA)}$	$\overline{HLDA}$ output delay time			40	ns

NOTES:

1. Calculated according to the BCLK frequency as follows:

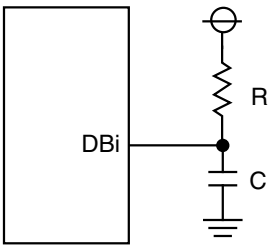
$$\frac{0.5 \times 10^9}{f(BCLK)} - 10 \text{ [ns]}$$

2. Calculated according to the BCLK frequency as follows:

$$\frac{(n - 0.5) \times 10^9}{f(BCLK)} - 40 \text{ [ns]}$$

n is “1” for 1-wait setting, “2” for 2-wait setting and “3” for 3-wait setting. When n = 1, f(BCLK) is 12.5 MHz or less.

3. This standard value shows the timing when the output is off, and does not show hold time of data bus.
Hold time of data bus varies with capacitor volume and pull-up (pull-down) resistance value.
Hold time of data bus is expressed in
$t = -CR \times \ln (1 - V_{OL} / V_{CC})$
by a circuit of the right figure.
For example, when $V_{OL} = 0.2\ V_{CC}$, C = 30 pF, R =1 kΩ, hold time of output “L” level is
$t = -30\text{ pF} \times 1\text{ k}\Omega \times \ln (1 - 0.2\ V_{CC} / V_{CC}) = 6.7$ ns.

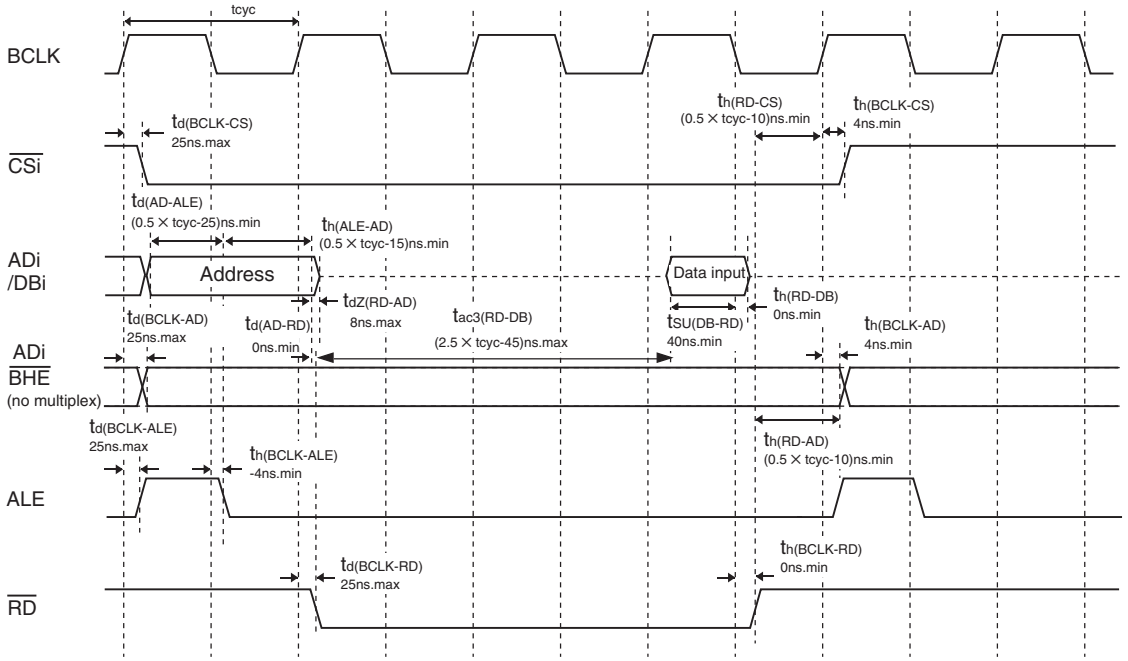


Memory Expansion Mode and Microprocessor Mode

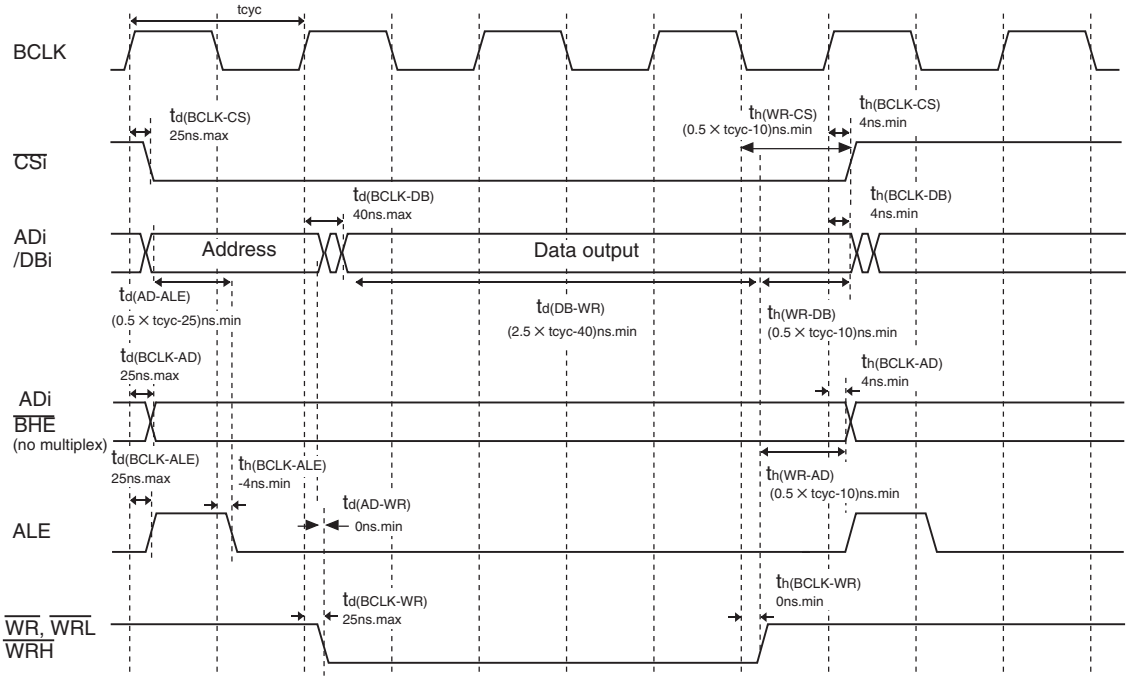
VCC = 5 V

(For 3-wait setting, external area access and multiplexed bus selection)

Read timing



Write timing



$$tcyc = \frac{1}{f(BCLK)}$$

Measuring conditions :

- VCC = 5 V
- Input timing voltage : V_{IL} = 0.8 V, V_{IH} = 2.0 V
- Output timing voltage : V_{OL} = 0.4 V, V_{OH} = 2.4 V

Figure 5.10 Timing Diagram (8)

Timing Requirements

VCC = 3.3 V

(Referenced to VCC = 3.3 V, VSS = 0 V, at Topr = –40 to 85°C unless otherwise specified)

Table 5.37 Timer B Input (Counter Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time (counted on one edge)	150		ns
$t_{w(TBH)}$	TBiIN input HIGH pulse width (counted on one edge)	60		ns
$t_{w(TBL)}$	TBiIN input LOW pulse width (counted on one edge)	60		ns
$t_{c(TB)}$	TBiIN input cycle time (counted on both edges)	300		ns
$t_{w(TBH)}$	TBiIN input HIGH pulse width (counted on both edges)	120		ns
$t_{w(TBL)}$	TBiIN input LOW pulse width (counted on both edges)	120		ns

Table 5.38 Timer B Input (Pulse Period Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time	600		ns
$t_{w(TBH)}$	TBiIN input HIGH pulse width	300		ns
$t_{w(TBL)}$	TBiIN input LOW pulse width	300		ns

Table 5.39 Timer B Input (Pulse Width Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time	600		ns
$t_{w(TBH)}$	TBiIN input HIGH pulse width	300		ns
$t_{w(TBL)}$	TBiIN input LOW pulse width	300		ns

Table 5.40 A/D Trigger Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{C(AD)}$	$\overline{\text{ADTRG}}$ input cycle time (trigger able minimum)	1500		ns
$t_{w(ADL)}$	$\overline{\text{ADTRG}}$ input LOW pulse width	200		ns

Table 5.41 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	300		ns
$t_{w(CKH)}$	CLKi input HIGH pulse width	150		ns
$t_{w(CKL)}$	CLKi input LOW pulse width	150		ns
$t_{d(C-Q)}$	TXDi output delay time		160	ns
$t_{h(C-Q)}$	TXDi hold time	0		ns
$t_{su(D-C)}$	RXDi input setup time	100		ns
$t_{h(C-D)}$	RXDi input hold time	90		ns

Table 5.42 External Interrupt $\overline{\text{INTi}}$ Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{\text{INTi}}$ input HIGH pulse width	380		ns
$t_{w(INL)}$	$\overline{\text{INTi}}$ input LOW pulse width	380		ns

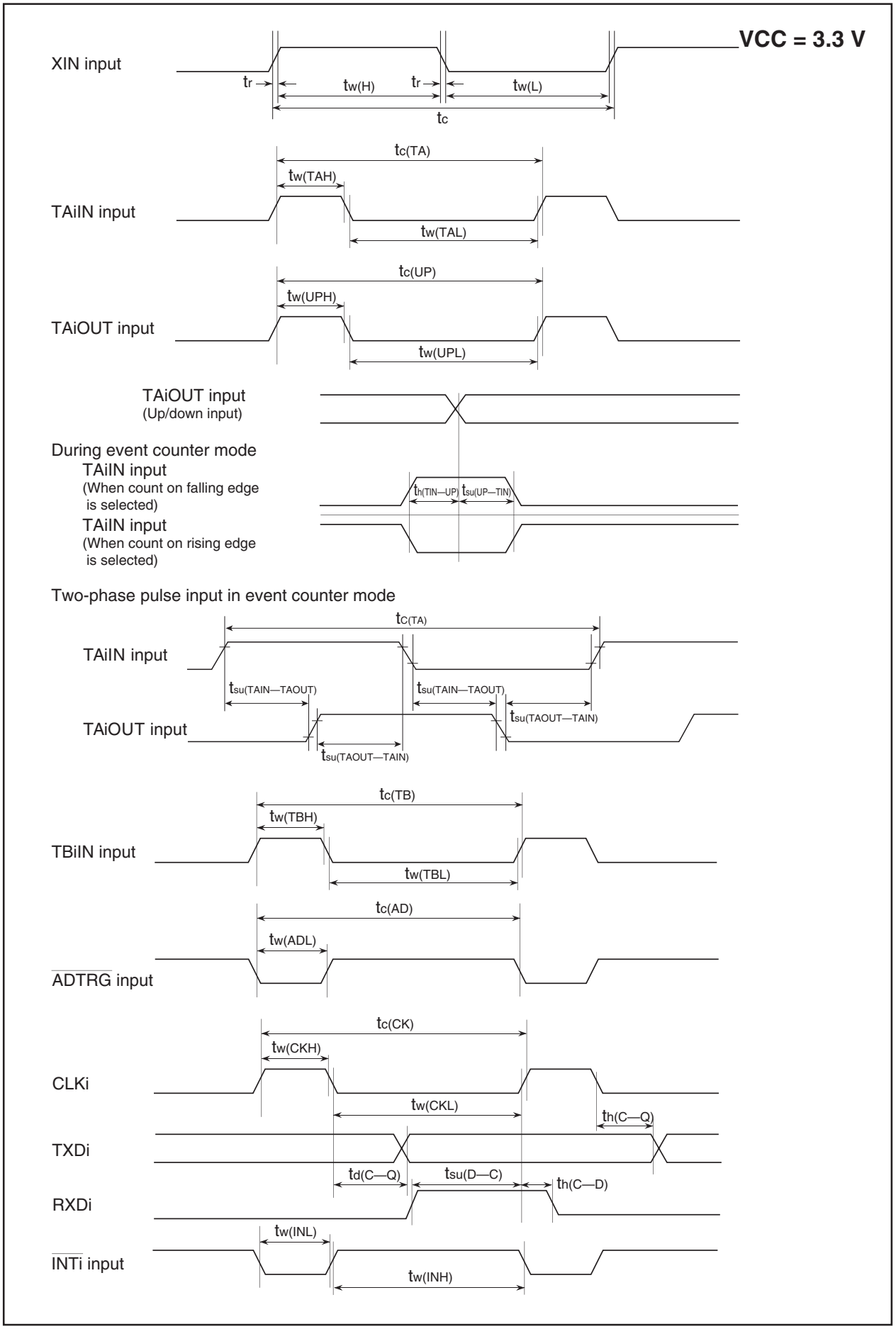


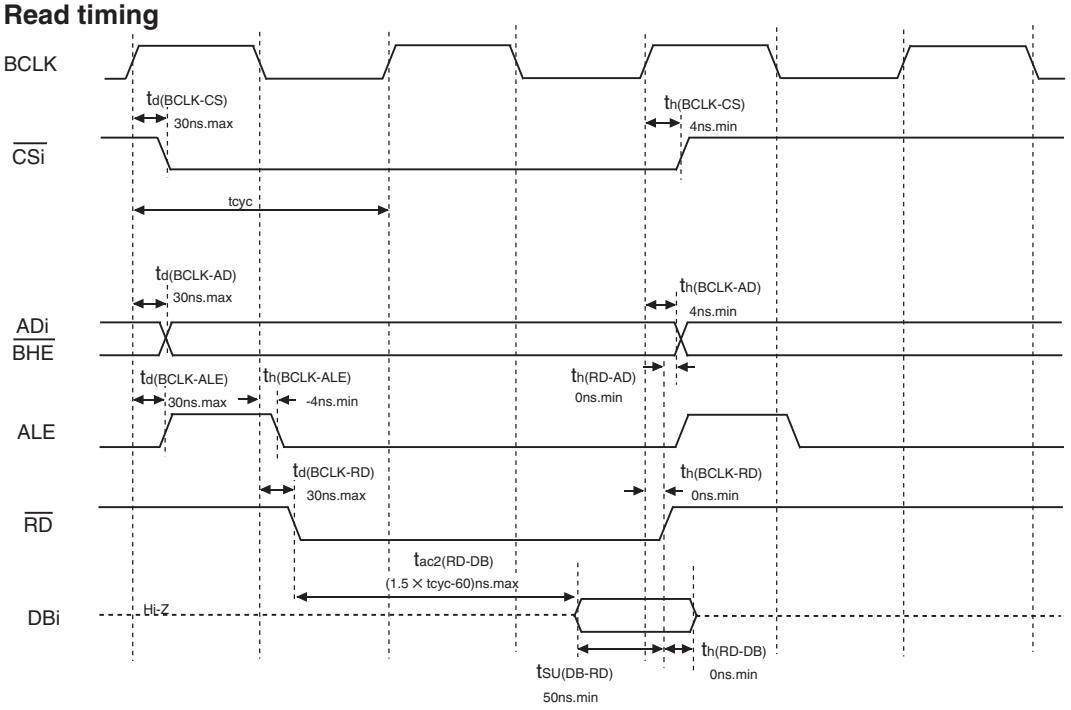
Figure 5.12 Timing Diagram (1)

Memory Expansion Mode and Microprocessor Mode

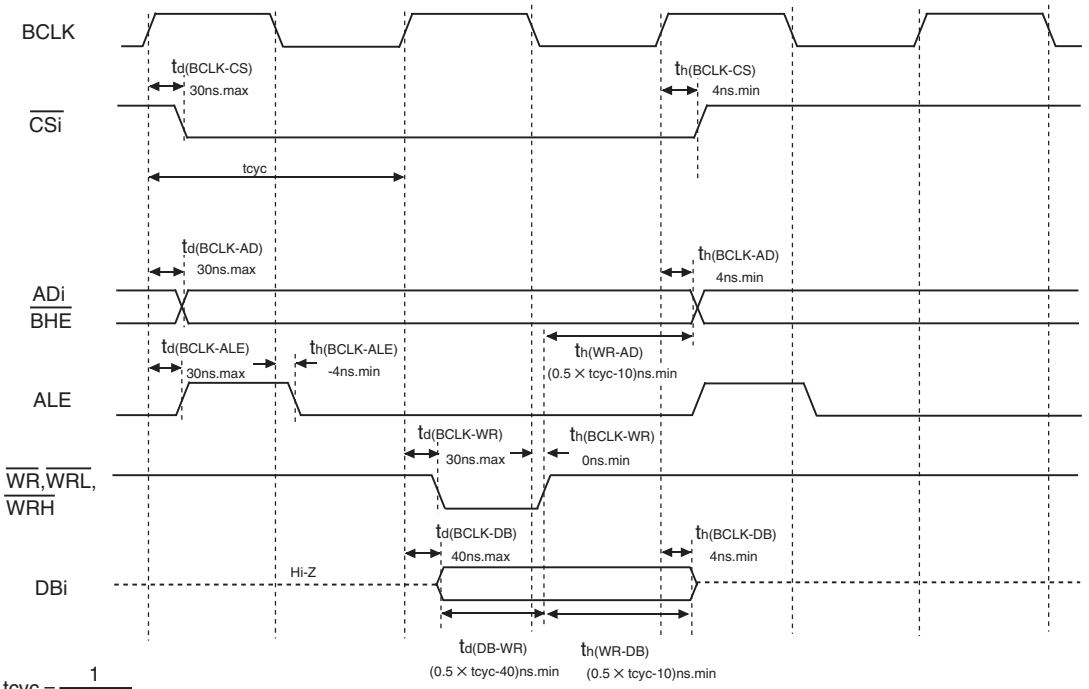
VCC = 3.3 V

(For 1-wait setting and external area access)

Read timing



Write timing



$$tcyc = \frac{1}{f(BCLK)}$$

Measuring conditions :

- VCC = 3.3 V
- Input timing voltage : V_{IL} = 0.6 V, V_{IH} = 2.7 V
- Output timing voltage : V_{OL} = 1.65 V, V_{OH} = 1.65 V

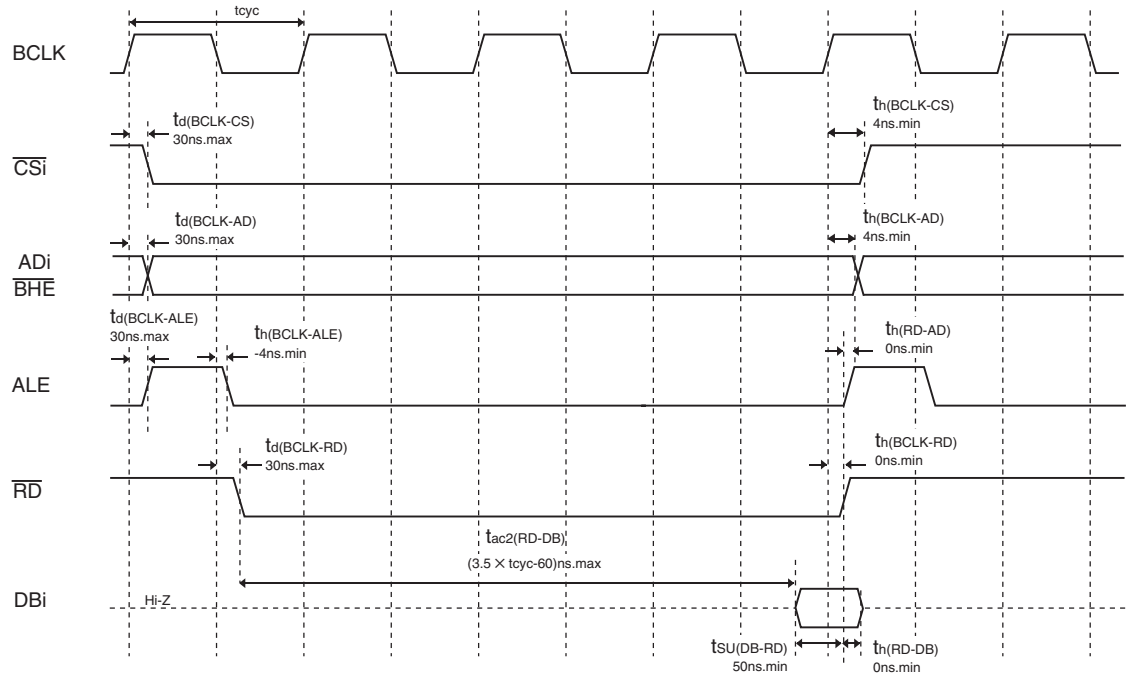
Figure 5.15 Timing Diagram (4)

Memory Expansion Mode and Microprocessor Mode

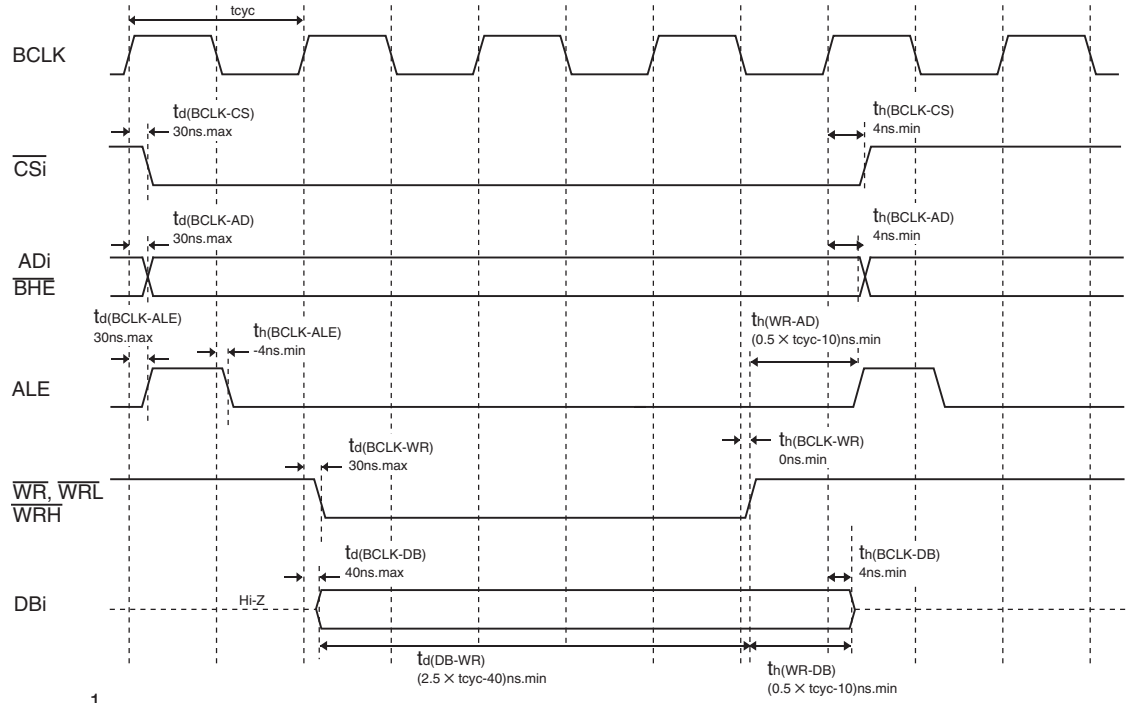
VCC = 3.3 V

(For 3-wait setting and external area access)

Read timing



Write timing



$$tcyc = \frac{1}{f(BCLK)}$$

Measuring conditions :

- VCC = 3.3 V
- Input timing voltage : V_{IL} = 0.6 V, V_{IH} = 2.7 V
- Output timing voltage : V_{OL} = 1.65 V, V_{OH} = 1.65 V

Figure 5.17 Timing Diagram (6)

Table 5.47 Recommended Operating Conditions (1) [1]

Symbol	Parameter		Standard			Unit
			Min.	Typ.	Max.	
V_{CC}	Supply voltage (VCC1 = VCC2)		4.2	5.0	5.5	V
AV_{CC}	Analog supply voltage			V_{CC}		V
V_{SS}	Supply voltage			0		V
AV_{SS}	Analog supply voltage			0		V
V_{IH}	HIGH input voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0, P7_2 to P7_7, P8_0 to P8_7, P9_0, P9_2 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1, XIN, $\overline{\text{RESET}}$, CNVSS, BYTE	0.8 V_{CC}		V_{CC}	V
		P7_1, P9_1	0.8 V_{CC}		6.5	V
V_{IL}	LOW input voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1, XIN, $\overline{\text{RESET}}$, CNVSS, BYTE	0		0.2 V_{CC}	V
$I_{OH(peak)}$	HIGH peak output current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0, P9_2 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1			–10.0	mA
$I_{OH(avg)}$	HIGH average output current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0, P9_2 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1			–5.0	mA
$I_{OL(peak)}$	LOW peak output current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1			10.0	mA
$I_{OL(avg)}$	LOW average output current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1			5.0	mA

NOTES:

1. Referenced to VCC = 4.2 to 5.5 V at Topr = –40 to 85°C unless otherwise specified.
2. Average output current values during 100 ms period.
3. The total $I_{OL(peak)}$ for ports P0, P1, P2, P8_6, P8_7, P9, P10, P11, P14_0, and P14_1 must be 80 mA max.
   The total $I_{OL(peak)}$ for ports P3, P4, P5, P6, P7, P8_0 to P8_4, P12, and P13 must be 80 mA max.
   The total $I_{OH(peak)}$ for ports P0, P1, and P2 must be –40 mA max.
   The total $I_{OH(peak)}$ for ports P3, P4, P5, P12, and P13 must be –40 mA max.
   The total $I_{OH(peak)}$ for ports P6, P7, and P8_0 to P8_4 must be –40 mA max.
   The total $I_{OH(peak)}$ for ports P8_6, P8_7, P9, P10, P11, P14_0, and P14_1 must be –40 mA max.
4. P11 to P14 are only in the 128-pin version.

Table 5.51 A/D Conversion Characteristics (1)

Symbol	Parameter		Measuring Condition		Standard			Unit
					Min.	Typ.	Max.	
–	Resolution		VREF = VCC				10	Bit
INL	integral nonlinearity erro	10 bits	VREF = VCC = 5 V	ANEX0, ANEX1 input, AN0 to AN7 input, AN0_0 to AN0_7 input, AN2_0 to AN2_7 input			±3	LSB
				External operation amp connection mode			±7	LSB
		8 bits	VREF = AVCC = VCC = 5 V				±2	LSB
–	Absolute accuracy	10 bits	VREF = VCC = 5 V	ANEX0, ANEX1 input, AN0 to AN7 input, AN0_0 to AN0_7 input, AN2_0 to AN2_7 input			±3	LSB
				External operation amp connection mode			±7	LSB
		8 bits	VREF = AVCC = VCC = 5 V				±2	LSB
DNL	Differential nonlinearity error						±1	LSB
–	Offset error						±3	LSB
–	Gain error						±3	LSB
R_{LADDER}	Resistor ladder		VREF = VCC		10		40	kΩ
t_{CONV}	10-bit conversion time, sample & hold available		VREF = VCC = 5 V, ϕAD = 10 MHz		3.3			µs
	8-bit conversion time, sample & hold available		VREF = VCC = 5 V, ϕAD = 10 MHz		2.8			µs
t_{SAMP}	Sampling time				0.3			µs
V_{REF}	Reference voltage				2.0		V_{CC}	V
V_{IA}	Analog input voltage				0		V_{REF}	V

NOTES:
1. Referenced to VCC = AVCC = VREF = 4.2 to 5.5 V, VSS = AVSS = 0 V, –40 to 85°C unless otherwise specified.
2. ϕAD frequency must be 10 MHz or less.
3. When sample & hold is disabled, ϕAD frequency must be 250 kHz or more in addition to a limit of NOTE 2.
   When sample & hold is enabled, ϕAD frequency must be 1 MHz or more in addition to a limit of NOTE 2.

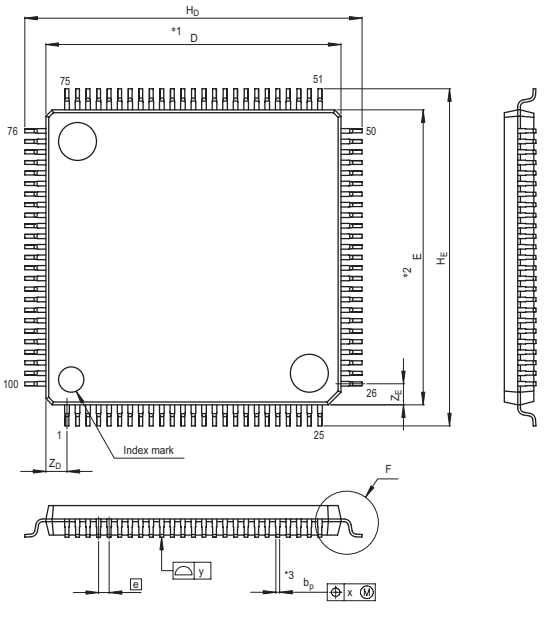
Table 5.52 D/A conversion Characteristics (1)

Symbol	Parameter	Measuring Condition	Standard			Unit
			Min.	Typ.	Max.	
–	Resolution				8	Bits
–	Absolute accuracy				1.0	%
t_{su}	Setup time				3	µs
R_O	Output tesistance		4	10	20	kΩ
I_{VREF}	Reference power supply input current	(NOTE 2)			1.5	mA

NOTES:
1. Referenced to VCC = AVCC = VREF = 4.2 to 5.5 V, VSS = AVSS = 0 V, –40 to 85°C unless otherwise specified.
2. This applies when using one D/A converter, with the DAi register (i = 0, 1) for the unused D/A converter set to 00h.
   The resistor ladder of the A/D converter is not included. Also, the I_{VREF} will flow even if VREF is disconnected by the ADCON1 register.

Appendix 1. Package Dimensions

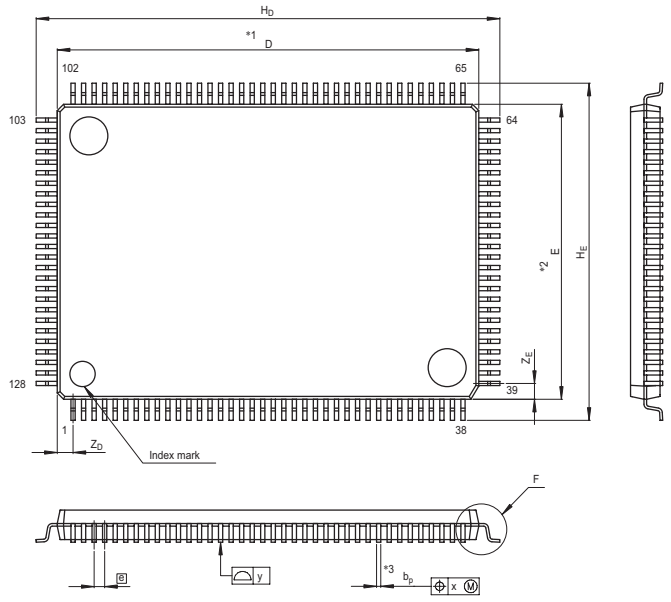
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP100-14x14-0.50	PLQP0100KB-A	100P6Q-A / FP-100U / FP-100UV	0.6g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.0	—
Z_E	—	1.0	—
L	0.35	0.5	0.65
L_1	—	1.0	—

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP128-14x20-0.50	PLQP0128KB-A	128P6Q-A	0.9g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	19.9	20.0	20.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	21.8	22.0	22.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0.05	0.125	0.2
b_p	0.17	0.22	0.27
b_1	—	0.20	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.10
y	—	—	0.10
Z_D	—	0.75	—
Z_E	—	0.75	—
L	0.35	0.5	0.65
L_1	—	1.0	—