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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

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Product Status	Active
Core Processor	M16C/60
Core Size	16-Bit
Speed	24MHz
Connectivity	CANbus, I ² C, IEBus, SIO, UART/USART
Peripherals	DMA, WDT
Number of I/O	111
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	31K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 26x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	128-LQFP
Supplier Device Package	128-LFQFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/m306nmfjgp-u3

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RENESAS

M16C/6N Group (M16C/6NK, M16C/6NM)

Renesas MCU

REJ03B0058-0210 Rev.2.10 Aug 25, 2006

1. Overview

The M16C/6N Group (M16C/6NK, M16C/6NM) of MCUs are built using the high-performance silicon gate CMOS process using the M16C/60 Series CPU core and are packaged in 100-pin and 128-pin plastic molded LQFP. These MCUs operate using sophisticated instructions featuring a high level of instruction efficiency. With 1 Mbyte of address space, they are capable of executing instructions at high speed. Being equipped with two CAN (Controller Area Network) modules in the M16C/6N Group (M16C/6NK, M16C/6NM), the MCU is suited to drive automotive and industrial control systems. The CAN modules comply with the 2.0B specification. In addition, this MCU contains a multiplier and DMAC which combined with fast instruction processing capability, makes it suitable for control of various OA, communication equipment which requires high-speed arithmetic/logic operations.

1.1 Applications

- Car audio and industrial control systems, other (Normal-ver. product)
- Automotive, industrial control systems and other automobile, other (T/V-ver. product)

Specifications written in this manual are believed to be accurate, but are not guaranteed to be entirely free of error. Specifications in this manual may be changed for functional or performance improvements. Please make sure your manual is the latest edition.



Table 1.4 List of Pin Names for 100-Pin Package (1)

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	UART Pin	Analog Pin	CAN Module Pin	Bus Control Pin ⁽¹⁾
1		P9_4		TB4IN		DA1		
2		P9_3		TB3IN		DA0		
3		P9_2		TB2IN	SOUT3			
4		P9_1		TB1IN	SIN3			
5		P9_0		TB0IN	CLK3			
6	BYTE							
7	CNVSS							
8	XCIN	P8_7						
9	XCOUT	P8_6						
10	RESET							
11	XOUT							
12	VSS							
13	XIN							
14	VCC1							
15		P8_5	NMI					
16		P8_4	INT2	ZP				
17		P8_3	INT1					
18		P8_2	INT0					
19		P8_1		TA4IN/U				
20		P8_0		TA4OUT/U	(SIN4)			
21		P7_7		TA3IN			CRX1	
22		P7_6		TA3OUT			CTX1	
23		P7_5		TA2IN/W	(SOUT4)			
24		P7_4		TA2OUT/W	(CLK4)			
25		P7_3		TA1IN/V	CTS2/RTS2			
26		P7_2		TA1OUT/V	CLK2			
27		P7_1		TA0IN/TB5IN	RXD2/SCL2			
28		P7_0		TA0OUT	TXD2/SDA2			
29		P6_7			TXD1/SDA1			
30		P6_6			RXD1/SCL1			
31		 P6_5			CLK1			
32		P6_4			CTS1/RTS1/CTS0/CLKS1			
33		 P6_3			TXD0/SDA0			
34		P6_2			RXD0/SCL0			
35		P6_1			CLK0			
36		 P6_0			CTS0/RTS0			
37		P5_7						RDY/CLKOU
38		P5_6						ALE
39		P5_5						HOLD
40		P5_4						HLDA
41		P5_3						BCLK
42		P5_2						RD
43		P5_1						WRH/BHE
44		P5_0						WRL/WR
45		P4_7						CS3
46		P4_6						CS2
47		P4_5		<u> </u>				CS1
48		P4_4						CSO
40		P4_4						A19
49 50		P4_3						A19 A18

NOTE:

1. Not available the bus control pins (except CLKOUT pin; Pin No.37) in T/V-ver..

	1					-	
125		P10_2				AN2	
126		P10_1				AN1	
127	AVSS						
128		P10_0				AN0	
OTE:							
OTE:							
UIE.							
1. No	t availabl	e the bus	s control i	oins in T/V-ve	r		
		5 Duc			• • •		

Port

P1_2

P1_1

P1_0

P0_7

P0_6

P0_5

P0_4

P0_3

P0_2

P0_1

P0_0

P11_7

P11_6

P11_5

P11_4

P11_3

P11_2

P11_1

P11_0

P10_7

P10_6

P10_5

P10_4

P10_3

KI3

KI2

KI1

KI0

Control

Pin

Pin No.

101

102

103

104

105

106

107

108

109

110

111

112

113

114

115

116

117

118

119

120

121

122

123

124

Bus Control

Pin⁽¹⁾

D10

D9

D8

D7

D6

D5

D4

D3

D2

D1

D0

CAN Module

Pin

Analog

Pin

AN0_7

AN0_6

AN0_5

AN0_4

AN0_3

AN0_2

AN0_1

AN0_0

AN7

AN6

AN5

AN4

AN3

UART Pin

SIN6

CLK6

SOUT6

SOUT5

SIN5

CLK5

Table 1.8 List of Pin Names for 128-Pin Package (3)

Interrupt

Pin

Timer Pin



1.6 Pin Functions

Tables 1.9 to 1.11 list the Pin Functions.

Signal Name	Pin Name	I/O Type	Description
Power supply	VCC1, VCC2,		Apply 3.0 to 5.5 V to the VCC1 and VCC2 pins and 0 V to the VSS
input	VSS		pin. The VCC apply condition is that VCC2 = VCC1 $^{(1)}$.
Analog power	AVCC, AVSS		Applies the power supply for the A/D converter. Connect the AVCC
supply input			pin to VCC1. Connect the AVSS pin to VSS.
Reset input	RESET		The MCU is in a reset state when applying "L" to the this pin.
CNVSS (2)	CNVSS		Switches processor mode. Connect this pin to VSS to when after
			a reset to start up in single-chip mode. Connect this pin to VCC1
			to start up in microprocessor mode.
External data	BYTE		Switches the data bus in external memory space. The data bus
bus width			is 16-bit long when the this pin is held "L" and 8-bit long when
select input ⁽²⁾			the this pin is held "H". Set it to either one. Connect this pin to
ooloot input			VSS when single-chip mode.
Bus control	D0 to D7	I/O	Inputs and outputs data (D0 to D7) when these pins are set as
pins ⁽³⁾	001007	1/0	the separate bus.
pino	D8 to D15	I/O	Inputs and outputs data (D8 to D15) when external 16-bit data
	0010013	1/0	bus is set as the separate bus.
	A0 to A19	0	Output address bits (A0 to A19).
	A0/D0 to A7/D7	I/O	Input and output data (D0 to D7) and output address bits (A0 to
	AU/DU 10 A7/D7	1/0	A7) by time-sharing when external 8-bit data bus are set as the
			multiplexed bus.
		1/0	Input and output data (D0 to D7) and output address bits (A1 to
	A1/D0 to A8/D7	I/O	
			A8) by time-sharing when external 16-bit data bus are set as the
		0	multiplexed bus.
	CS0 to CS3	0	Output CS0 to CS3 signals. CS0 to CS3 are chip-select signals
		0	to specify an external space.
	WRL/WR	0	Output WRL, WRH, (WR, BHE), RD signals. WRL and WRH or
	WRH/BHE		BHE, and WR can be switched by program.
	RD		• WRL, WRH, and RD are selected
			The WRL signal becomes "L" by writing data to an even address
			in an external memory space.
			The WRH signal becomes "L" by writing data to an odd address
			in an external memory space.
			The RD pin signal becomes "L" by reading data in an external
			memory space.
			• WR, BHE, and RD are selected
			The WR signal becomes "L" by writing data in an external
			memory space.
			The RD signal becomes "L" by reading data in an external
			memory space.
			The BHE signal becomes "L" by accessing an odd address.
			Select WR, BHE, and RD for an external 8-bit data bus.
	ALE	0	ALE is a signal to latch the address.
	HOLD	I	While the HOLD pin is held "L", the MCU is placed in a hold
			state.
	HLDA	0	In a hold state, HLDA outputs a "L" signal.
	RDY	I	While applying a "L" signal to the RDY pin, the MCU is placed in
	1	1	a wait state.

Table 1.9 Pin Functions (100-pin and 128-pin Versions) (1)

I: Input O: Output I/O: Input/Output

NOTES:

- 1. In this manual, hereafter, VCC refers to VCC1 unless otherwise noted.
- 2. Connect to VSS in T/V-ver..
- 3. Not available the bus control pins in T/V-ver..

3. Memory

Figure 3.1 shows a Memory Map. The address space extends the 1 Mbyte from address 00000h to FFFFFh. The internal ROM is allocated in a lower address direction beginning with address FFFFh. For example, a 512-Kbyte internal ROM is allocated to the addresses from 80000h to FFFFh.

As for the flash memory version, 4-Kbyte space (block A) exists in 0F000h to 0FFFFh. 4-Kbyte space is mainly for storing data. In addition to storing data, 4-Kbyte space also can store programs.

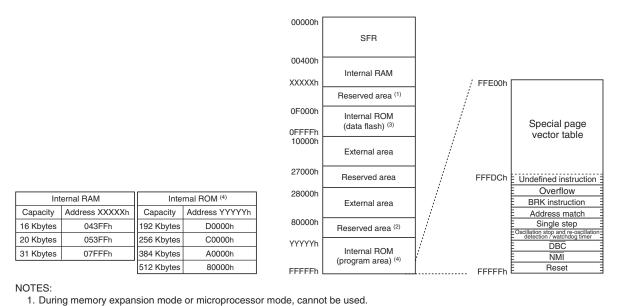
The fixed interrupt vector table is allocated to the addresses from FFFDCh to FFFFFh. Therefore, store the start address of each interrupt routine here.

The internal RAM is allocated in an upper address direction beginning with address 00400h. For example, a 31-Kbyte internal RAM is allocated to the addresses from 00400h to 07FFFh. In addition to storing data, the internal RAM also stores the stack used when calling subroutines and when interrupts are generated.

The Special Function Registers (SFRs) are allocated to the addresses from 00000h to 003FFh. Peripheral function control registers are located here. Of the SFR, any area which has no functions allocated is reserved for future use and cannot be accessed by user.

The special page vector table is allocated to the addresses from FFE00h to FFFDBh. This vector is used by the JMPS or JSRS instruction. For details, refer to M16C/60, M16C/20, M16C/Tiny Series Software Manual. In memory expansion and microprocessor modes, some areas are reserved for future use and cannot be used by users.

Use T/V-ver. in single-chip mode. The memory expansion and microprocessor modes cannot be used.



2. In memory expansion mode, cannot be used.

3. As for the flash memory version, 4-Kbyte space (block A) exists.

4. When using the masked ROM version, write nothing to internal ROM area. 5. Shown here is a memory map for the case where the PM10 bit in the PM1 register is 1 (block A enabled, addresses 10000h to 26FFFh for CS2 area) and the PM13 bit in the PM1 register is 1 (internal RAM area is expanded over 192 Kbytes).

* Not available memory expansion and microprocessor modes in T/V-ver.. And not available external area in T/V-ver..

Figure 3.1 Memory Map



M16C/6N Group (M16C/6NK, M16C/6NM)

Table 4.6 SFR Information (6) (1)

Address	Register	Symbol	After Reset
0140h	~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~	, í	XXh
0141h			XXh
0142h	CAN0 Message Box 14: Identifier /DLC		XXh
0143h			XXh
0144h			XXh
0145h 0146h			XXh XXh
0146h 0147h			XXh
0147h			XXh
0149h	OANO Marriero Bried A. Bala Field		XXh
014Ah	CAN0 Message Box 14: Data Field		XXh
014Bh			XXh
014Ch			XXh
014Dh			XXh
014Eh	CAN0 Message Box 14: Time Stamp		XXh XXh
014Fh 0150h			XXh
0151h			XXh
0152h			XXh
0153h	CAN0 Message Box 15: Identifier /DLC		XXh
0154h			XXh
0155h			XXh
0156h			XXh
0157h			XXh
0158h			XXh XXh
0159h 015Ah	CAN0 Message Box 15: Data Field		XXh
015Bh			XXh
015Ch			XXh
015Dh			XXh
015Eh	CAN0 Message Box 15: Time Stamp		XXh
015Fh			XXh
0160h			XXh
0161h			XXh XXh
0162h 0163h	CAN0 Global Mask Register	C0GMR	XXh
0164h			XXh
0165h			XXh
0166h			XXh
0167h			XXh
0168h	CAN0 Local Mask A Register	COLMAR	XXh
0169h			XXh
016Ah			XXh XXh
016Bh 016Ch			XXn XXh
016Dh			XXh
016Eh			XXh
016Fh	CAN0 Local Mask B Register	COLMBR	XXh
0170h			XXh
0171h			XXh
0172h			
0173h			
0174h 0175h			
0175h 0176h			
0177h			
0178h			
0179h			
017Ah			
017Bh			
017Ch			
017Dh			
017Eh 017Fh			
017Fn			

X: Undefined

NOTE:

1. Blank spaces are reserved. No access is allowed.

Table 4.8 SFR Information (8)⁽³⁾

Address	Register	Symbol	After Reset
01C0h	Timer B3, B4, B5 Count Start Flag	TBSR	000XXXXb
01C0h		TBSN	000//////0
01C2h			XXh
01C2h	Timer A1-1 Register	TA11	XXh
01C3h			XXh
01C4n	Timer A2-1 Register	TA21	XXh
	-		XXh
01C6h	Timer A4-1 Register	TA41	XXh
01C7h	Three Dhees DMM Control Desister 0	1010/00	
01C8h	Three-Phase PWM Control Register 0	INVC0	00h 00h
01C9h	Three-Phase PWM Control Register 1		
01CAh	Three-Phase Output Buffer Register 0	IDB0	0011111b
01CBh	Three-Phase Output Buffer Register 1	IDB1	00111111b
01CCh	Dead Time Timer	DTT	XXh
01CDh	Timer B2 Interrupt Generation Frequency Set Counter	ICTB2	XXh
01CEh			
01CFh	Interrupt Source Select Register 2	IFSR2	X000000b
01D0h	Timer B3 Register	твз —	XXh
01D1h		150	XXh
01D2h	Timer B4 Register	ТВ4	XXh
01D3h		1 04	XXh
01D4h	Timer B5 Register	тв5	XXh
01D5h		185	XXh
01D6h	SI/O6 Transmit/Receive Register (1)	S6TRR	XXh
01D7h			
01D8h	SI/O6 Control Register (1)	S6C	0100000b
01D9h	SI/O6 Bit Rate Register (1)	S6BRG	XXh
01DAh	SI/O3, 4, 5, 6 Transmit/Receive Register (2)	S3456TRR	XXXX0000b
01DBh	Timer B3 Mode Register	TB3MR	00XX0000b
01DCh	Timer B4 Mode Register	TB4MR	00XX0000b
01DDh	Timer B5 Mode Register	TB5MR	00XX0000b
01DEh	Interrupt Source Select Register 0	IFSR0	00h
01DFh	Interrupt Source Select Register 1	IFSR1	00h
01E0h	SI/O3 Transmit/Receive Register	S3TRR	XXh
01E1h			
01E2h	SI/O3 Control Register	S3C	0100000b
01E3h	SI/O3 Bit Rate Register	S3BRG	XXh
01E4h	SI/O4 Transmit/Receive Register	S4TRR	XXh
01E5h		011111	700
01E6h	SI/O4 Control Register	S4C	0100000b
01E7h	SI/O4 Bit Rate Register	S4BRG	XXh
01E8h	SI/O5 Transmit/Receive Register ⁽¹⁾	S5TRR	XXh
01E9h		551NN	
01EAh	SI/O5 Control Register ⁽¹⁾	S5C	0100000b
01EAn 01EBh	SI/OS Bit Rate Register ⁽¹⁾	S5BRG	XXh
	UARTO Special Mode Register 4	U0SMR4	XXn 00h
01ECh	UARTO Special Mode Register 3	U0SMR4	000X0X0Xb
01EDh		U0SMR3	X000000b
01EEh	UARTO Special Mode Register 2		
01EFh	UARTO Special Mode Register	UOSMR	X000000b
01F0h	UART1 Special Mode Register 4	U1SMR4	00h
01F1h	UART1 Special Mode Register 3	U1SMR3	000X0X0Xb
01F2h	UART1 Special Mode Register 2	U1SMR2	X000000b
01F3h	UART1 Special Mode Register	U1SMR	X000000b
01F4h	UART2 Special Mode Register 4	U2SMR4	00h
01F5h	UART2 Special Mode Register 3	U2SMR3	000X0X0Xb
01F6h	UART2 Special Mode Register 2	U2SMR2	X000000b
01F7h	UART2 Special Mode Register	U2SMR	X000000b
01F8h	UART2 Transmit/Receive Mode Register	U2MR	00h
01F9h	UART2 Bit Rate Register	U2BRG	XXh
01FAh	LIAPT2 Transmit Buffor Pogistor	U2TB	XXh
01FBh	UART2 Transmit Buffer Register	UZIB	XXh
01FCh	UART2 Transmit/Receive Control Register 0	U2C0	00001000b
01FDh	UART2 Transmit/Receive Control Register 1	U2C1	00000010b
01FEh			XXh
01FFh	UART2 Receive Buffer Register	U2RB	XXh
X. Undefin	· · · · · · · · · · · · · · · · · · ·	· · ·	

X: Undefined

NOTES:

These registers exist only in the 128-pin version.
 Bits S5TRF and S6TRF in the S3456TRR register are used in the 128-pin version.
 Blank spaces are reserved. No access is allowed.



M16C/6N Group (M16C/6NK, M16C/6NM)

Table 4.9 SFR Information (9)

Address	Register	Symbol	After Reset
0200h	CAN0 Message Control Register 0	COMCTLO	00h
0200h	CANO Message Control Register 1	COMCTL1	00h
0202h	CANO Message Control Register 2	C0MCTL2	00h
0203h	CANO Message Control Register 3	COMCTL3	00h
0203h	CANO Message Control Register 4	COMCTL4	00h
020411 0205h	CANO Message Control Register 5	COMCTL5	00h
0205h	CANO Message Control Register 6	COMCTL6	00h
020011 0207h	CANO Message Control Register 7	COMCTL7	00h
0207h 0208h	CANO Message Control Register 8	COMCTL8	00h
0208h	CANO Message Control Register 9	COMCTL9	00h
	CANO Message Control Register 10	COMCTL10	00h
020Ah	CANO Message Control Register 10	COMCTL10	00h
020Bh	CANO Message Control Register 12		
020Ch		COMCTL12	00h
020Dh	CANO Message Control Register 13	COMCTL13	00h
020Eh	CANO Message Control Register 14	COMCTL14	00h
020Fh	CAN0 Message Control Register 15	C0MCTL15	00h
0210h	CAN0 Control Register	C0CTLR -	X000001b
0211h		0001211	XX0X0000b
0212h	CAN0 Status Register	COSTR -	00h
0213h		00011	X000001b
0214h	CAN0 Slot Status Register	COSSTR -	00h
0215h	CANO SIOL STATUS REGISTER	CUSSIN	00h
0216h	CANG Interrupt Constant Desciptor	00105	00h
0217h	CAN0 Interrupt Control Register	COICR -	00h
0218h			00h
0219h	CAN0 Extended ID Register	C0IDR -	00h
021Ah			XXh
021An	CAN0 Configuration Register	C0CONR -	XXh
021Dh	CAN0 Receive Error Count Register	CORECR	00h
0210h	CANO Transmit Error Count Register	COTECR	00h
021Dh	OANO Hanshin Enor Oount Hegister	OULON	00h
021En	CAN0 Time Stamp Register	COTSR -	00h
	CAN1 Message Control Register 0		00h
0220h		C1MCTL0	
0221h	CAN1 Message Control Register 1	C1MCTL1	00h
0222h	CAN1 Message Control Register 2	C1MCTL2	00h
0223h	CAN1 Message Control Register 3	C1MCTL3	00h
0224h	CAN1 Message Control Register 4	C1MCTL4	00h
0225h	CAN1 Message Control Register 5	C1MCTL5	00h
0226h	CAN1 Message Control Register 6	C1MCTL6	00h
0227h	CAN1 Message Control Register 7	C1MCTL7	00h
0228h	CAN1 Message Control Register 8	C1MCTL8	00h
0229h	CAN1 Message Control Register 9	C1MCTL9	00h
022Ah	CAN1 Message Control Register 10	C1MCTL10	00h
022Bh	CAN1 Message Control Register 11	C1MCTL11	00h
022Ch	CAN1 Message Control Register 12	C1MCTL12	00h
022Dh	CAN1 Message Control Register 13	C1MCTL13	00h
022Eh	CAN1 Message Control Register 14	C1MCTL14	00h
022Fh	CAN1 Message Control Register 15	C1MCTL15	00h
0230h			X000001b
0231h	CAN1 Control Register	C1CTLR -	XX0X0000b
0232h	OANH Older Desider	01070	00h
0233h	CAN1 Status Register	C1STR -	X000001b
0234h			00h
0235h	CAN1 Slot Status Register	C1SSTR -	00h
0236h			00h
0230h	CAN1 Interrupt Control Register	C1ICR	00h
0238h			00h
0238h	CAN1 Extended ID Register	C1IDR	00h
			XXh
023Ah	CAN1 Configuration Register	C1CONR	
023Bh		010500	XXh
023Ch	CAN1 Receive Error Count Register	C1RECR	00h
023Dh	CAN1 Transmit Error Count Register	C1TECR	00h
023Eh	CAN1 Time Stamp Register	C1TSR -	<u>00h</u>
023Fh	r - U		00h

X: Undefined



Table 4.10 SFR Information (10) (1)

0240h	Address	Register	Symbol	After Reset
0241h CANA Acceptance Filer Support Register COAFS XXh 0244h CANA Acceptance Filer Support Register CIAFS XXh 0244h CANA Acceptance Filer Support Register CIAF XXh 0244h CANA Acceptance Filer Support Register CIAF XXh 0255h CANA Cace Acceptance Filer Support Register CIAF XXh 0255h CANA Cace Acceptance Filer Support Register CIAF XXh 0255h CANA C		. Togotol	- Cyllizer	
CANA Acceptance Filter Support Register CAFS XOR 0244h CANI Acceptance Filter Support Register CIAFS XXh 0245h CANI Acceptance Filter Support Register CIAFS XXh 0255h CANI Acceptance Filter				
Own Acceptance Filter Support Register CHAPS XXh 0244h CAN1 Acceptance Filter Support Register C1APS XXh 0245h C Xh Xh 0246h Image: Construction of the support Register Image: Construction of the support Register Xh 0246h Image: Construction of the support Register Image: Construction of the support Register Image: Construction of the support Register 0244h Image: Construction of the support Register Image: Construction of the support Register Image: Construction of the support Register 0244h Image: Construction of the support Register Image: Construction of the support Register Image: Construction of the support Register 0245h Image: Construction of the support Register Image: Construction of the support Register Image: Construction of the support Register 025h Image: Construction of the support Register Image: Construction of the support Register Image: Construction of the support Register 025h Image: Construction of the support Register Image: Construction of the support Register Image: Construction of the support Register 025h Image: Construction of the support Register Image: Construction of the support Register </td <td></td> <td></td> <td>00450</td> <td>XXh</td>			00450	XXh
02446 04456 CHAFS XKh 02456 CAFS XKh 02467 Image: Comparison of the second		CANO Acceptance Filter Support Register	COAFS	XXh
1244bn 1 XAII 644bn 1 1 645bn 1 1 625bn 1 1		CANIT Accontones Filter Support Desister	01450	
0248h	0245h	CANT Acceptance Filter Support Register	CIAFS	XXh
0248h0248h0248h0248h0248h0248h0248h0248h0248h0248h0248h0248h0248h0248h0248h0258h0258h0285h <t< td=""><td>0246h</td><td></td><td></td><td></td></t<>	0246h			
0244n(meta(meta)0244n(meta)(meta)0244n(meta)(meta)0244n(meta)(meta)0244n(meta)(meta)0244n(meta)(meta)0244n(meta)(meta)0244n(meta)(meta)0244n(meta)(meta)0251n(meta)(meta)0252n(meta)(meta)0253n(me	0247h			
0244h024b024b024b024b024b024b024b024b024b024b024b025h026h026h </td <td>0248h</td> <td></td> <td></td> <td></td>	0248h			
024ch Image: Constraint of the state of				
024Ch 024Ch 024Ch 025Ch 025Ch <td></td> <td></td> <td></td> <td></td>				
024Eh Image: Constraint of the stamp of				
024Eh				
0245h				
0250h				
ddddddddddddddddddddddddddddddddddd				
10252h				
0253h0254h0255h0257h0258h <t< td=""><td></td><td></td><td></td><td></td></t<>				
0254h				
1225h				
0225h0257h0258h0258h0258h0258h0258h0258h0258h0258h0258h0258h0258h0258h0258h0258h0258h0258h0258h0268h0278h0278h <t< td=""><td></td><td></td><td></td><td></td></t<>				
0257h0258h0258h0258h0258h0257hCAN/1 Clock Select RegisterPCLKR0257hCAN/1 Clock Select RegisterCCLKR0267hCAN/1 Message Box 0: Identifier / DLC0267hCAN/1 Message Box 0: Identifier / DLC0267hCAN/1 Message Box 0: Data FieldXXh0267hCAN/1 Message Box 0: Data FieldXXh0267hCAN/1 Message Box 0: Time StampXXh0267hCAN/1 Message Box 1: Identifier / DLCXXh0267hCAN/1 Message Box 0: Time StampXXh0267hCAN/1 Message Box 1: Identifier / DLCXXh027hCAN/1 Message Box 1: Data FieldXXh027hCAN/1 Message Box 1: Data FieldXXh027hCAN/1 Message Box 1:				
10258h				
0259h				
1025AhImage: constraint of the state of the s				
10250hImage: constraint of the state of the s				
1025ChImage: constraint of the state of the s				
025Dhcmcm025EhPeripheral Clock Select RegisterPCLKR00h026hhCAN0/1 Clock Select RegisterCLKR00h026hhXXhXXh026ahXXhXXh026ahXXhXXh026bhXXhXXh026bhXXhXXh026bhXXhXXh026bhXXhXXh026bhXXhXXh026bhXXhXXh026bhXXhXXh026bhXXhXXh026bhXXhXXh026bhXXhXXh026bhXXhXXh026bhXXhXXh026bhXXhXXh026bhXXhXXh026bhXXhXXh027bhXXh <t< td=""><td></td><td></td><td></td><td></td></t<>				
0225hPeripheral Clock Select RegisterPCLKR00h0260hCCLKR00h0260hCCLKR00h0260hXXhXXh0263hXXhXXh0263hXXhXXh0266hXXhXXh0266hXXhXXh0266hXXhXXh0266hXXhXXh0266hXXhXXh0266hXXhXXh0266hXXhXXh0266hXXhXXh0266hXXhXXh0266hXXhXXh0266hXXhXXh0266hXXhXXh0266hXXhXXh0266hXXhXXh0266hXXhXXh0267hXXhXXh0270hXXhXXh0271hXXhXXh0273hXXhXXh0273hXXhXXh0277hXXhXXh0277hXXhXXh0277hXXhXXh0277hXXhXXh0277hXXhXXh0277hXXhXXh0277hXXhXXh0277hXXhXXh0277hXXhXXh0277hXXhXXh0277hXXhXXh0277hXXhXXh0277hXXhXXh0277hXXhXXh0277hXXhXXh0277hXXhXXh0277h <td></td> <td></td> <td></td> <td></td>				
025Fh CAN0/1 Clock Select Register CCLKR 00h 0260h 0261h XXh XXh 0262h CAN1 Message Box 0: Identifier / DLC XXh XXh 0263h XXh XXh XXh 0264h XXh XXh XXh 0266h XXh XXh XXh 0270h XXh XXh XXh 0270h XXh XXh XXh 0278h XXh XXh XXh <td></td> <td>Perinheral Clock Salect Begister</td> <td>PCLKB</td> <td>00h</td>		Perinheral Clock Salect Begister	PCLKB	00h
0260h 0261h 0262h 0263h Xh Xh 0264h 0266h Xh Xh 0266h 0266h Xh Xh 0266h Xh Xh 0266h Xh Xh 0267h Xh Xh 0268h Xh Xh 0260h Xh Xh 0260h Xh Xh 0260h Xh Xh 0270h Xh Xh 0271h Xh Xh 0274h Xh Xh 0274h Xh Xh 0274h Xh Xh 0278h Xh Xh 0278h Xh Xh 0278h <td></td> <td>CANO/1 Clock Select Register</td> <td></td> <td></td>		CANO/1 Clock Select Register		
0261h 0263h 0263h 0266h 0266h Xh Xh 0266h 0266h Xh Xh 0266h 0268h 0266h Xh Xh 0266h 0268h Xh Xh 0268h 0268h Xh Xh 0268h 0268h Xh Xh 0268h Xh Xh 0260h Xh Xh 0270h Xh Xh <td></td> <td></td> <td>OOLINI</td> <td></td>			OOLINI	
0262h 0263h CAN1 Message Box 0: Identifier / DLC XXh 0264h XXh 0264h XXh 0265h XXh 0267h XXh 0267h XXh 0268h XXh 0267h XXh 0268h XXh 0268h XXh 0268h XXh 0266h XXh 0267h XXh 0271h XXh 02721h XXh 0273h XXh 0274h XXh 0274h XXh 0274h XXh 0274h XXh 0274h XXh 0274h XXh 0276h <td></td> <td></td> <td></td> <td></td>				
0263h 0265hXxh0266h 0266hXXh0266h 0266hXXh0266h 0268hXXh0268h 0268hXXh0268h 0268hXXh0268h 0268hXXh0268h 0268hXXh0268h 0268hXXh0266h 0268hXXh0266h 0268hXXh0266h 0266hXXh0266h 0266hXXh0266h 0266hXXh0266h 0266hXXh0266h 0267hXXh0267h 0270hXXh0270h 0271h 0273hXXh0271h 0273hXXh0273h 0274hXXh0276h 0276hXXh0276h 0277h 0276hXXh0278h 0277h 0278hXXh0279h 0270hXXh0279h 0270hXXh0279h 0270hXXh0279h 0270hXXh0270h 0270hXXh0270h 0270hXXh0270h 0270hXXh0270h 0270hXXh0270h 0270hXXh0270h 0270hXXh0270h 0270hXXh0270h 0270hXXh0270h 0270hXXh0270h 0270hXXh0270h 0270hXXh0270h 0270hXXh0270h 0270hXXh0270h 0270hXXh0270h 0270hXXh0270h 0270hXXh0270h 0270hXXh0270h 0270h		CANIT Massage Boy & Identifier / DLC		
0264h 0266hXXh0266h 0267hXXh0267h 0268hXXh0268h 0268hXXh0268h 0268hXXh0268h 0260hXXh0268h 0260hXXh0268h 0260hXXh0268h 0260hXXh0268h 0260hXXh0268h 0260hXXh0260h 0260hXXh0260h 0260hXXh0260h 0260hXXh0260h 0260hXXh0260h 0260hXXh0260h 0260hXXh0260h 0260hXXh0260h 0270hXXh0270h 0273hXXh0273h		CAN1 Message Box 0: Identifier / DLC		
0265hXXh0267hXXh0268hXXh0278hXXh				
0266h XXh 0269h XXh 0269h XXh 0269h XXh 0269h XXh 0260h XXh 0270h XXh 0270h XXh 0271h XXh 0272h XXh 0274h XXh 0275h XXh 0276h XXh 0271h <td></td> <td></td> <td></td> <td></td>				
0267h 0269h 0268h 0269h 0268h 0269h 0268h 0269h 0268h 0269h 0268h 0269h 0260h 0260h 0260h 0260h 0260h 0260h 0260h 0260h 0260h 0270h 0270h 0270h 0270h 0270h 0270h 0270h 0270h 0274h 0274h 0270h 0274h 0274h 0274h 0270h 0274h 027h 027h 027h<				
0268h 0268h 0268h 0268hXxh0268h 0268hXxh0268h 0268hXxh0268h 0268hXxh0268h 0268hXxh0268h 0268hXxh0268h 0268hXxh0268h 0268hXxh0268h 0268hXxh0269h 0268hXxh0270h 0270hXXh0270h 0271hXXh0271h 0274hXXh0273h 0274hXXh0274h 0278hXXh0278h 0278hXXh0278h 0278hXXh0278h 0278hXXh0278h 0278hXXh0278h 0278hXXh0278h 0278hXXh0278h 0278hXXh0278h 0278hXXh0278h 0278hXXh0278h 0278hXXh0278h 0278hXXh0278h 0279hXXh0278h 0279hXNh0278h 0279hXNh0278h 0279hXNh0278h 0279hXNh0278h 0279hXNh0278h 0279hXNh0278h 0279hXNh0278h 0279hXNh0278h 0279hXNh0278h 0279hXNh0278h 0279hXNh0278h 0279hXNh0278h 0279hXNh0278h 0279hXNh0278h 0279hXNh0278h 0279hXNh0278h 0279hXNh0279h 0279hXNh <td></td> <td></td> <td></td> <td></td>				
0269h 0268h 0268h 0260hCAN1 Message Box 0: Data FieldXXh0260hXXh0260hXXh0260hXXh0260hXXh0260hXXh0260hXXh0260hXXh0260hXXh0260hXXh0260hXXh0260hXXh0270hXXh0270hXXh0271hXXh0270hXXh0				XXh
026Ah 026Bh 026ChXxh026ChXXh026DhXXh026ChXXh026Eh 0270h 0270hCAN1 Message Box 0:Time StampXXh0270h 0271hXXh0270h 0273hXXh0274hXXh0274hXXh0274hXXh0274hXXh0276h 0277hXXh0276h 0277hXXh0277h 0278hXXh0278h 0277hXXh0278h 0277hXXh0278h 0277hXXh0278h 0277hXXh0278h 0277hXXh0278h 0277hXXh0278h 0277hXXh0278h 0277hXXh0278h 0277hXXh0278h 0277hXXh0278h 0272h </td <td></td> <td>CAN1 Message Box 0: Data Field</td> <td></td> <td></td>		CAN1 Message Box 0: Data Field		
026ChXXh026DhXXh026EhCAN1 Message Box 0:Time StampXXh026FhXXhXXh0270hXXhXXh0270hXXhXXh0271hXXhXXh0273h </td <td>026Ah</td> <td>or in the souge box of bala here</td> <td></td> <td></td>	026Ah	or in the souge box of bala here		
026DhXXh026EhCAN1 Message Box 0:Time StampXXh026EhCAN1 Message Box 0:Time StampXXh0270hXXhXXh0271hXXhXXh0273hXXhXXh0274hXXhXXh0274hXXhXXh0275hXXhXXh0276hXXhXXh0277hXXhXXh0278hXXhXXh0278hXXhXXh0278hXXhXXh0278hXXhXXh0278hXXhXXh0278hXXhXXh0278hXXhXXh0278hXXhXXh0278hXXhXXh0278hXXhXXh0270hXXhXXh0272hXXhXXh0272hXXhXXh027bhXXhXXh027FhCAN1 Message Box 1: Time StampXXh027FhXXhXXh	026Bh			
026Eh 026FhCAN1 Message Box 0:Time StampXXh0270h 0270h 0271h 0272h 0273h 0273hXXhXXh0274h 0273h 0273hCAN1 Message Box 1: Identifier / DLCXXh0273h 0273hXXhXXh<				
026FhCANT Message Box 0: Time StampXXh0270hXXhXXh0271hXXhXXh0272hXXhXXh0273hXXhXXh0274hXXhXXh0275hXXhXXh0276hXXhXXh0277hXXhXXh0278hXXhXXh0278hXXhXXh0278hXXhXXh0278hXXhXXh0278hXXhXXh0278hXXhXXh0278hXXhXXh0278hXXhXXh0270hXXhXXh0270hXXhXXh0270hXXhXXh0270hXXhXXh0270hXXhXXh0270hXXhXXh027FhCAN1 Message Box 1:Time StampXXh027FhXXhXXh				
026Fn 027h 0270h 027h 0271h 027h 0273h 027h 0274h 027h 0275h 027h 0276h 027h 0277h 027h 0278h 027h 0270h 027h 0270h 027h 027Ch 027h 027Ch 027h 027Ch 027h 027Ch 027h 027Fh 027h 027Fh 027h		CAN1 Message Box 0. Time Stamp		
0271h XXh 0272h XXh 0273h XXh 0274h XXh 0274h XXh 0274h XXh 0275h XXh 0276h XXh 0277h XXh 0278h XXh 0270h XXh XXh				
0272h AN1 Message Box 1: Identifier / DLC XXh 0273h XXh 0274h XXh 0274h XXh 0275h XXh 0276h XXh 0277h XXh 0278h XXh 0278h XXh 0278h XXh 0278h XXh 0278h XXh 0270h				
0273h 0274h XXh 0274h XXh 0275h XXh 0276h XXh 0277h XXh 0278h XXh 0278h XXh 0278h XXh 0278h XXh 0270h XXh 027Fh XXh				XXh
0273h 0274h 0274h XXh 0275h XXh 0276h XXh 0277h XXh 0278h XXh 0279h XXh 0270h XXh 027Fh XXh		CAN1 Message Box 1: Identifier / DLC		
0275h XXh 0276h XXh 0277h XXh 0278h XXh 0279h XXh 0279h XXh 0272h XXh 0278h XXh 0278h XXh 0278h XXh 0270h XXh		-		
0276h XXh 0277h XXh 0278h XXh 0279h XXh 0279h XXh 0279h XXh 0279h XXh 0279h XXh 0270h XXh 027Fh XXh				
0277h XXh 0278h XXh 0279h XXh 027Ah XXh 027Ah XXh 027Ah XXh 027Bh XXh 027Ch XXh 027Dh XXh 027Dh XXh 027Eh XNh Message Box 1: Time Stamp 027Fh XXh				
0278h XXh 0279h XXh 027Ah XXh 027Ah XXh 027Bh XXh 027Ch XXh 027Dh XXh 027Dh XXh 027Eh XXh 027Fh XXh				XXh
0279h CAN1 Message Box 1: Data Field XXh 027Ah XXh XXh 027Bh XXh XXh 027Ch XXh XXh 027Dh XXh XXh 027Dh XXh XXh 027Eh CAN1 Message Box 1: Time Stamp XXh 027Fh XXh XXh	02//h			
027Ah CANT Message Box 1: Data Field XXh 027Bh XXh XXh 027Ch XXh XXh 027Dh XXh XXh 027Eh CAN1 Message Box 1: Time Stamp XXh 027Fh XXh XXh				
027Bh XXh 027Ch XXh 027Dh XXh 027Dh XXh 027Eh XXh 027Fh XXh	0279h	CAN1 Message Box 1: Data Field		
027Ch XXh 027Dh XXh 027Eh XXh 027Fh XXh 027Fh XXh				
027Dh XXh 027Eh CAN1 Message Box 1:Time Stamp 027Fh XXh				
027Eh 027Fh CAN1 Message Box 1:Time Stamp XXh XXh				
027Fh XXh				
		CAN1 Message Box 1:Time Stamp		
	X: Undefine	1	1	

X: Undefined

NOTE:

1. Blank spaces are reserved. No access is allowed.



Table 4.13 SFR Information (13)

Address	Register	Symbol	After Reset
0300h	· · · · · · · · · · · · · · · · · · ·		XXh
0301h			XXh
0302h	CANIT Managere Day 10. Identifier / DLO		XXh
0303h	CAN1 Message Box 10: Identifier / DLC		XXh
0304h			XXh
0305h			XXh
0306h			XXh
0307h			XXh
0308h			XXh
0309h	CAN1 Message Box 10: Data Field		XXh
030Ah	CANT MESSage Dox TO. Data Field		XXh
030Bh			XXh
030Ch			XXh
030Dh			XXh
030Eh	CAN1 Message Box 10: Time Stamp		XXh
030Fh			XXh
0310h			XXh
0311h			XXh
0312h	CAN1 Message Box 11: Identifier / DLC		XXh
0313h			XXh
0314h			XXh
0315h			XXh
0316h			XXh
0317h			XXh
0318h			XXh
0319h	CAN1 Message Box 11: Data Field		XXh
031Ah	0		XXh
031Bh			XXh
031Ch			XXh
031Dh			XXh
031Eh 031Fh	CAN1 Message Box 11: Time Stamp		XXh XXh
0320h			XXh
0320h			XXh
0322h			XXh
0323h	CAN1 Message Box 12: Identifier / DLC		XXh
0324h			XXh
0325h			XXh
0326h			XXh
0327h			XXh
0328h			XXh
0329h	ONH Marrie Bridd Bale Field		XXh
032Ah	CAN1 Message Box 12: Data Field		XXh
032Bh			XXh
032Ch			XXh
032Dh			XXh
032Eh	CAN1 Message Box 12: Time Stamp		XXh
032Fh			XXh
0330h			XXh
0331h			XXh
0332h	CAN1 Message Box 13: Identifier / DLC		XXh
0333h			XXh
0334h			XXh
0335h			XXh
0336h			XXh
0337h			XXh
0338h			XXh
0339h	CAN1 Message Box 13: Data Field		XXh
033Ah			XXh XXh
033Bh 033Ch			XXh
033Ch 033Dh			XXh
033Eh			XXh
033Fh	CAN1 Message Box 13: Time Stamp		XXh
V: Undofin		I	77711

X: Undefined



Table 4.15 SFR Information (15) (2)

0393h Court Start Flag OP 00 0393h Cock Prescieler Reset Plag CPSRF 00XXXXXXxXx 0383b. Tridger Placet Register TRGSR 00h 0383b. Tridger Select Register TRGSR 00h 0383b. Tridger Select Register TRGSR 00h 0383b. Tridger Select Register TRGSR 00h 0383b. Timer AD Register TA0 XXh 0383b. Timer AA Register TA1 XXh 0383b. Timer AA Register TA2 XXh 0383b. Timer AA Register TA3 XXh 0383b. Timer AA Register TB0 XXh 0383b. Timer AB Register TB1 XXh 0383b. Timer AD Register TB2 XXh 0383b. Timer AD Register TA0HR OOh 0393b. Timer AD Register TA0HR OOh 0393b. Timer AD Register TA0HR OOh 0393b. Timer AD Register	Address	Register	Symbol	After Reset
0381n Circk Prescaler Reset Plag ONSF 00h 0382n One-Shot Start Flag 00h 00h 0384h UpDer 74 X0h 0384h Umer A Register 74 X0h 0384h Imer A Register 740M 00h 0384h Imer A Rode Register <td></td> <td></td> <td></td> <td></td>				
One-Shot Start Flag ONF ODR 0383h Tinger Select Register TAGS R 00h 0384h UpDown Flag UDF 00h1(1) 0385h Tiner AD Register TA0 XXh 0385h Tiner AD Register TA1 XXh 0386h Tiner AT Register TA2 XXh 0386h Tiner AZ Register TA3 XXh 0386h Tiner AZ Register TA3 XXh 0386h Tiner AZ Register TA4 XXh 0386h Tiner AZ Register TA4 XXh 0386h Tiner BD Register TA4 XXh 0387h Tiner BD Register TB6 XXh 0387h Tiner BD Register TB1 XXh 0387h Tiner BD Register TA1H XXh 0387h Tiner BD Register TA1H XXh 0387h Tiner AD Mode Register TA1HA XXh 0388h Tiner AD Mode Register TA1HA XXh <td< td=""><td></td><td></td><td></td><td></td></td<>				
Togger Select RegisterTRGSRODh0388hUDF00h'100388hImer AD RegisterTAO00h'100388hTimer AD RegisterTAOXXh0388hTimer AT RegisterTAIXXh0388hTimer AZ RegisterTA2XXh0388hTimer AZ RegisterTA2XXh0388hTimer AZ RegisterTA3XXh0388hTimer AZ RegisterTA4XXh0388hTimer AZ RegisterTA4XXh0388hTimer AZ RegisterTA4XXh0388hTimer A RegisterTB1XXh0388hTimer B RegisterTB1XXh0388hTimer A Mode RegisterTA4XXh0388hTimer A Mode RegisterTA4MOOh0388hTimer				
OB38.h Up/Down Flag ODh (1) 0385h Timer A0 Register TA0 XXh 0387h Timer A0 Register TA0 XXh 0388h Timer A1 Register TA1 XXh 0388h Timer A2 Register TA2 XXh 0388h Timer A3 Register TA3 XXh 0388h Timer A3 Register TA4 XXh 0389h Timer A3 Register TA4 XXh 0389h Timer B0 Register TA4 XXh 0389h Timer B0 Register TB0 XXh 0389h Timer B1 Register TA4 XXh 0389h Timer A0 Mode Register TA0MR Odh 0389h Timer A0 Mode Register TA0MR Odh 0389h Timer A1 Mode Register TA0MR Odh 0389h Timer A2 Mode Register TA0MR Odh 0389h Timer A2 Mode Register TA0MR Odh 0389h Timer A1 Mode Register TA0MR Odh				
10385h Timer A0 Register TA0 XXh 0385h Timer A1 Register TA1 XXh 0385h Timer A1 Register TA1 XXh 0385h Timer A2 Register TA1 XXh 0385h Timer A3 Register TA2 XXh 0385h Timer A3 Register TA3 XXh 0385h Timer A4 Register TA4 XXh 0385h Timer A4 Register TB0 XXh 0385h Timer A3 Register TB0 XXh 0385h Timer A4 Register TB1 XXh 0385h Timer B0 Register TB1 XXh 0393bh Timer B1 Register TB2 Xxh 0393bh Timer A1 Mode Register TAMR 00h 0393bh Timer A1 Mode Register TAMR 00h 0393bh Timer A2 Mode Register TAMR 00h 0393bh Timer A2 Mode Register TAMR 00h 0393bh Timer A2 Mode Register TBMR 00X0000h 0393bh Timer A2 Mode Register TBMR 00A 0393bh Timer A2 Mode Register TBMR 00X0000h 0393bh Timer A2 Mode Register TBMR 00X0000h				
10988h 10987hTmar AD RegisterTAOXXh0388h 0388h 0388hTimer A1 RegisterTA1XXh0388h 0388hTimer A2 RegisterTA2XXh0388h 0388hTimer A2 RegisterTA2XXh0388h 0388hTimer A2 RegisterTA3XXh0388h 0388hTimer A3 RegisterTA3XXh0388h 0388hTimer A4 RegisterTA4XXh0388h 0388hTimer B0 RegisterTB0XXh0388h 0388hTimer B0 RegisterTB1XXh0388hTimer B1 RegisterTB1XXh0388hTimer B2 RegisterTAMROOh0388hTimer A1 Mode RegisterTAMROOh0388hTimer A2 Mode RegisterTBMRO0XX0000b0398hTimer A2 Mode RegisterTBMRO0XX000b0398hTimer B1 Mode RegisterTBMRO0XX000b0398hTimer B2 Model RegisterTBMRO0XX000b0398hTimer B2 Model RegisterTBMRO0XX000b0398hTimer B2 Model RegisterTBMRO0XX000b0398hTimer B2 Model RegisterTBMRO0XX000b0398hTimer B2 Mode RegisterTBMR				
Inter AJ HegisterIA0XXh0388hTimer A1 RegisterTA1XXh0388hTimer A2 RegisterTA2XXh0386hTimer A2 RegisterTA3XXh0386hTimer A3 RegisterTA3XXh0386hTimer A3 RegisterTA3XXh0386hTimer A4 RegisterTA4XXh0387hTimer B0 RegisterTA4XXh0387hTimer B0 RegisterTB1XXh0392hTimer B1 RegisterTB1XXh0392hTimer B2 RegisterTAM00h0393hTimer B2 RegisterTAMR00h0393hTimer A0 Mode RegisterTAMR00h0393hTimer A0 Mode RegisterTAMR00h0393hTimer A1 Mode RegisterTAMR00h0393hTimer A1 Mode RegisterTAMR00h0393hTimer A1 Mode RegisterTAMR00h0393hTimer A2 Mode RegisterTBMR00XX000h0393hTimer A2 Mode RegisterTBMR00XX000h0393hTimer B3 Mode RegisterTBMR00XX000h0393hTimer B4 Mode RegisterTBMR00XX000h0393hTimer B5 Mode RegisterTBMR00XX000h0393hTi				XXh
J0388 0388h 0388hTimer A1 RegisterTA1XXh0388h 0388h 0388hTimer A2 RegisterTA2XXh0388h 0388hTimer A3 RegisterTA3XXh0388h 0389hTimer A3 RegisterTA3XXh0389h 0398hTimer A4 RegisterTA4XXh0389h 0398hTimer A4 RegisterTB0XXh0398h 0398hTimer B0 RegisterTB1XXh0398hTimer B1 RegisterTB1XXh0398hTimer B1 RegisterTB2X0h0398hTimer B2 RegisterTAMR00h0398hTimer A1 Mode RegisterTBMR00Xx0000h0398hTimer A1 Mode RegisterTBMR00Xx000h0398hTimer B1 Mode RegisterTBMR00Xx000h0398hTimer B2 Mode RegisterTBMR <td></td> <td>Timer A0 Register</td> <td>TAO</td> <td>XXh</td>		Timer A0 Register	TAO	XXh
Inter A PagisterIAIXXh0388h 0382h 0383h 0382h 0383h 03				
Imer A2 Register TA2 XXh 038Bh Timer A3 Register TA3 XXh 038Bh Timer A4 Register TA3 XXh 038Bh Timer A4 Register TA4 XXh 038Bh Timer B0 Register TB0 XXh 039Bh Timer B1 Register TB1 XXh 039Bh Timer B1 Register TB1 XXh 039Bh Timer B2 Register TB1 XXh 039Bh Timer A0 Mode Register TA0MR 00h 039Bh Timer A1 Mode Register TA0MR 00h 039Bh Timer A2 Mode Register TA0MR 00h 039Bh Timer A3 Mode Register TA0MR 0		Timer A1 Register	TA1	
Time A Register TA2 XXh 038Ch Timer A3 Register TA3 XXh 038Ch Timer A3 Register TA4 XXh 038Ch Timer A4 Register TA4 XXh 038Ch Timer B0 Register TB0 XXh 039Ch Timer B0 Register TB1 XXh 039Ch Timer B1 Register TB2 XXh 039Ch Timer A0 Mode Register TA0MR 000h 039Ch Timer A1 Mode Register TA0MR 00h 039Ch Timer A2 Mode Register TA0MR 00h 039Ch Timer A3 Mode Register TA0MR 00h 039Ch Timer A3 Mode Register TA0MR 00h 039Ch Timer B1 Mode Register TB0MR 00xX0000b 039Ch Timer B2 Special Mode Register TB2KR 00XX0000b 039Ch Timer B2 Mode Register TB2KR 00XX0000b 039Ch Timer B2 Mode Register TB2KR 00XX0000b 039Ch Timer B2 Mode Register <td></td> <td></td> <td></td> <td></td>				
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03B0hUART Transmit/Receive Control Register 2UCONX000000b03B1h		UART1 Receive Buffer Register	U1RB —	
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03B3hImage: constraint of the sector of the sec				
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03B5hImage: constraint of the sector of the sec				
03B6h Image: constraint of the section of the secti				
03B7h				
0388h DMA0 Request Source Select Register DM0SL 00h 03B9h 00 00h 03BAh DMA1 Request Source Select Register DM1SL 00h 03BBh 00 00h 00h 03BCh CRC Data Register CRCD XXh 03BCh CRC Input Register CRCIN XXh 03BFh CRC Input Register CRCIN XXh			<u> </u>	
03B9h DMA1 Request Source Select Register DM1SL 00h 03BAh DMA1 Request Source Select Register DM1SL 00h 03BBh CRC Data Register XXh 03BDh CRC Input Register XXh 03BFh CRC Input Register CRCIN		DMA0 Bequest Source Select Begister	DMOSI	00h
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03BDh CRC Input Register CRCIN XXh 03BFh CRC Input Register CRCIN XXh		CRC Data Register	CRCD	
03BFh		CBC Input Begister		
				AA11

X: Undefined

NOTES:

Bits TA2P to TA4P in the UDF register are set to 0 after reset. However, the contents in these bits are undefined when read.
 Blank spaces are reserved. No access is allowed.

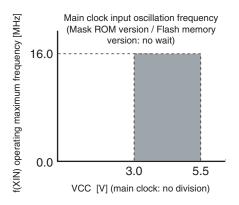


Table 5.3 Recommended Operating Conditions (2) (1)

Symbol	Parameter			Standard			Unit	
Symbol		Fal	ameter		Min.	Тур.	Max.	Unit
f(XIN)	fain clock input oscillation No wait Mask ROM version VCC = 3.0 to 5.5 V				0		16	MHz
	frequency (2) (3) (4)		Flash memory version					
f(XCIN)	Sub clock oscillation fre	ub clock oscillation frequency					50	kHz
f(Ring)	On-chip oscillation frequ	uency				1		MHz
f(PLL)	PLL clock oscillation fre	quency			16		24	MHz
f(BCLK)	CPU operation clock	CPU operation clock VCC = 3.0 to 5.5 \			0		24	MHz
tsu(PLL)	PLL frequency synthesi	zer stab	ilization wait time				20	ms

NOTES:

- 1. Referenced to VCC = 3.0 to 5.5 V at Topr = -40 to 85°C unless otherwise specified.
- 2. Relationship between main clock oscillation frequency and supply voltage is shown right.
- 3. Execute program/erase of flash memory by VCC = 3.3 \pm 0.3 V or VCC = 5.0 \pm 0.5 V.
- 4. When using 16 MHz and over, use PLL clock. PLL clock oscillation frequency which can be used is 16 MHz, 20 MHz or 24 MHz.





Symbol	Parameter			Measuring Condition	5	Standa	rd	Unit
Symbol				Measuring Condition	Min.	Тур.	Max.	Unit
_	Resolution		VREF =	= VCC			10	Bit
INL	Integral	10 bits	VREF	ANEX0, ANEX1 input, AN0 to AN7 input,			±3	LSB
	nonlinearity		= VCC	AN0_0 to AN0_7 input, AN2_0 to AN2_7 input				
	error		= 5 V	External operation amp connection mode			±7	LSB
			VREF	ANEX0, ANEX1 input, AN0 to AN7 input,			±5	LSB
			= VCC	AN0_0 to AN0_7 input, AN2_0 to AN2_7 input				
			= 3.3 V	External operation amp connection mode			±7	LSB
		8 bits	VREF =	= AVCC = VCC = 3.3 V			±2	LSB
_	Absolute	10 bits	VREF	ANEX0, ANEX1 input, AN0 to AN7 input,			±3	LSB
	accuracy		= VCC	AN0_0 to AN0_7 input, AN2_0 to AN2_7 input				
			= 5 V	External operation amp connection mode			±7	LSB
			VREF	ANEX0, ANEX1 input, AN0 to AN7 input,			±5	LSB
			= VCC	AN0_0 to AN0_7 input, AN2_0 to AN2_7 input				
			= 3.3 V	External operation amp connection mode			±7	LSB
		8 bits	VREF =	= AVCC = VCC = 3.3 V			±2	LSB
DNL	Differential non	linearity error					±1	LSB
_	Offset error						±3	LSB
_	Gain error						±3	LSB
RLADDER	Resistor ladde	r	VREF =	= VCC	10		40	kΩ
tconv	10-bit conversi	ion time,	VREF =	= VCC = 5 V, φAD = 10 MHz	3.3			μs
	sample & hold	available						
	8-bit conversion	on time,	VREF =	= VCC = 5 V, φAD = 10 MHz	2.8			μs
	sample & hold available							
t samp	Sampling time				0.3			μs
VREF	Reference volt	age			2.0		Vcc	V
VIA	Analog input v	oltage			0		VREF	V

Table 5.6 A	/D Conversion	Characteristics	(1)
-------------	---------------	-----------------	-----

NOTES:

1. Referenced to VCC = AVCC = VREF = 3.3 to 5.5 V, VSS = AVSS = 0 V, -40 to 85°C unless otherwise specified.

2. ϕ AD frequency must be 10 MHz or less.

When sample & hold is disabled, φAD frequency must be 250 kHz or more in addition to a limit of NOTE 2.
 When sample & hold is enabled, φAD frequency must be 1 MHz or more in addition to a limit of NOTE 2.

Table 5.7 D/A conversion Characteristics (1)

Symbol	Parameter	Measuring Condition	S	Unit		
		Measuring Condition	Min.	Тур.	Max.	
-	Resolution				8	Bits
-	Absolute accuracy				1.0	%
tsu	Setup time				3	μs
Ro	Output resistance		4	10	20	kΩ
IVREF	Reference power supply input current	(NOTE 2)			1.5	mA

NOTES:

1. Referenced to VCC = AVCC = VREF = 3.3 to 5.5 V, VSS = AVSS = 0 V, -40 to 85°C unless otherwise specified.

2. This applies when using one D/A converter, with the DAi register (i = 0, 1) for the unused D/A converter set to 00h. The resistor ladder of the A/D converter is not included. Also, the IVREF will flow even if VREF is disconnected by the ADCON1 register.

Switching Characteristics

VCC = 5 V

(Referenced to VCC = 5 V, VSS = 0 V, at Topr = -40 to 85 °C unless otherwise specified)

		-	-		
Symbol	Parameter	Measuring	Stan	Unit	
Symbol	Falameter	Condition	Min.	Max.	
$t_{d(BCLK-AD)}$	Address output delay time	Figure 5.2		25	ns
th(BCLK-AD)	Address output hold time (in relation to BCLK)		4		ns
th(RD-AD)	Address output hold time (in relation to RD)		0		ns
th(WR-AD)	Address output hold time (in relation to WR)		(NOTE 1)		ns
td(BCLK-CS)	Chip select output delay time			25	ns
th(BCLK-CS)	Chip select output hold time (rin relation to BCLK)		4		ns
$t_{d(BCLK-ALE)}$	ALE signal output delay time			15	ns
$\mathbf{t}_{h(BCLK-ALE)}$	ALE signal output hold time		-4		ns
td(BCLK-RD)	RD signal output delay time			25	ns
th(BCLK-RD)	RD signal output hold time		0		ns
$t_{d(BCLK-WR)}$	WR signal output delay time			25	ns
$t_{h(BCLK-WR)}$	WR signal output hold time		0		ns
td(BCLK-DB)	Data output delay time (in relation to BCLK)			40	ns
th(BCLK-DB)	Data output hold time (in relation to BCLK) (3)		4		ns
$t_{d(DB-WR)}$	Data output delay time (in relation to WR)		(NOTE 2)		ns
th(WR-DB)	Data output hold time (rin relation to WR) (3)		(NOTE 1)		ns
$t_{d(BCLK-HLDA)}$	HLDA output delay time			40	ns

Table 5.25 Memory Expansion Mode and Microprocessor Mode (for setting with no wait)

NOTES:

1. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(BCLK)}$$
 – 10 [ns]

2. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(BCLK)} - 40 \text{ [ns]} \qquad f(BCLK) \text{ is } 12.5 \text{ MHz or less.}$$

3. This standard value shows the timing when the output is off, and does not show hold time of data bus.

Hold time of data bus varies with capacitor volume and pull-up (pull-down) resistance value.

Hold time of data bus is expressed in

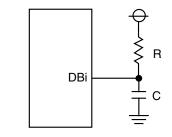
 $t = - CR \times ln (1 - V_{OL} / V_{CC})$

by a circuit of the right figure.

For example, when $V_{OL} = 0.2 V_{CC}$, C = 30 pF,

R =1 k Ω , hold time of output "L" level is

t = $-30 \text{ pF} \times 1 \text{ k}\Omega \times \text{ln} (1 - 0.2 \text{ Vcc} / \text{Vcc}) = 6.7 \text{ ns.}$



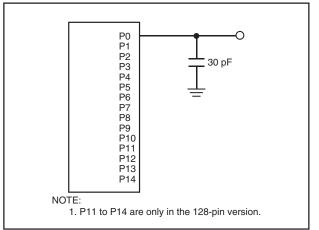


Figure 5.2 Port P0 to P14 Measurement Circuit



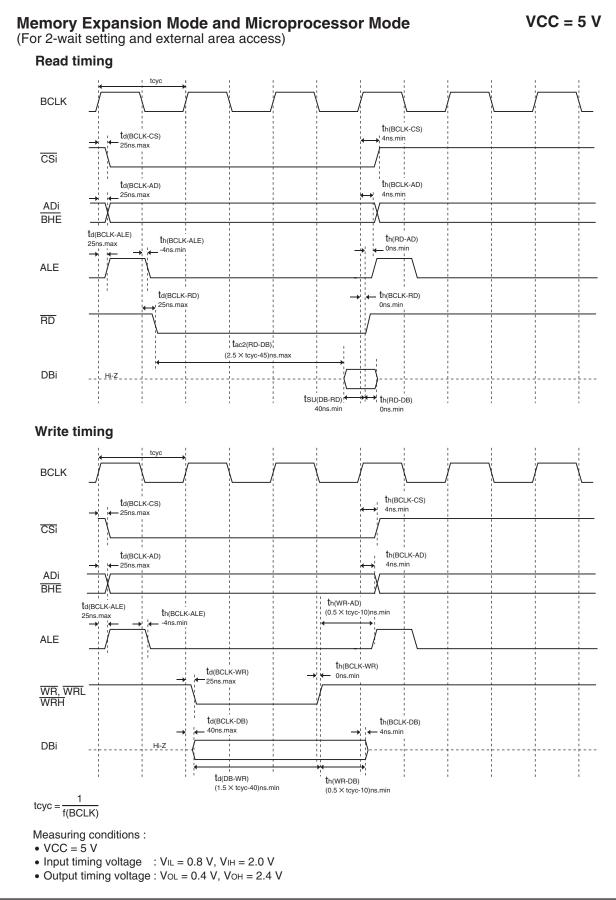


Figure 5.7 Timing Diagram (5)

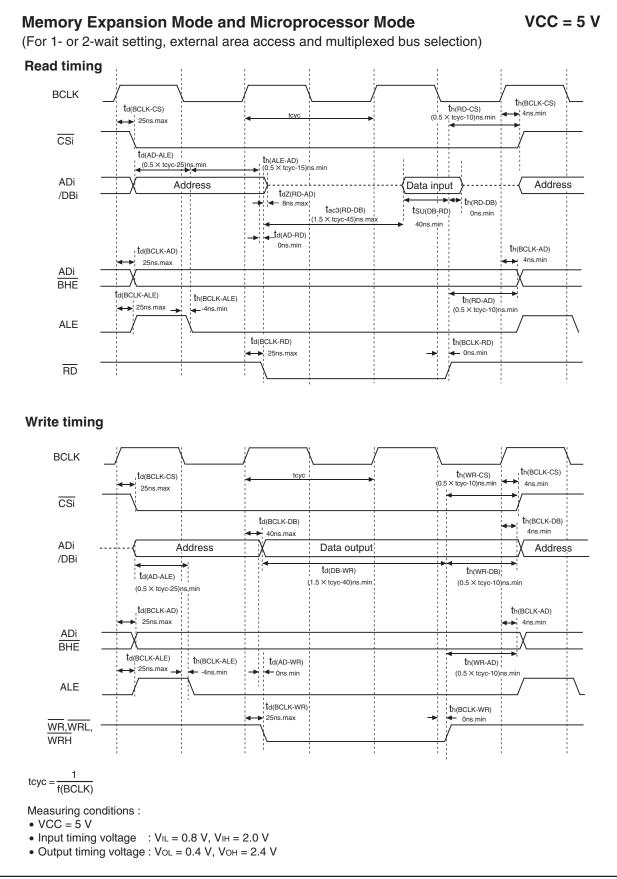


Figure 5.9 Timing Diagram (7)

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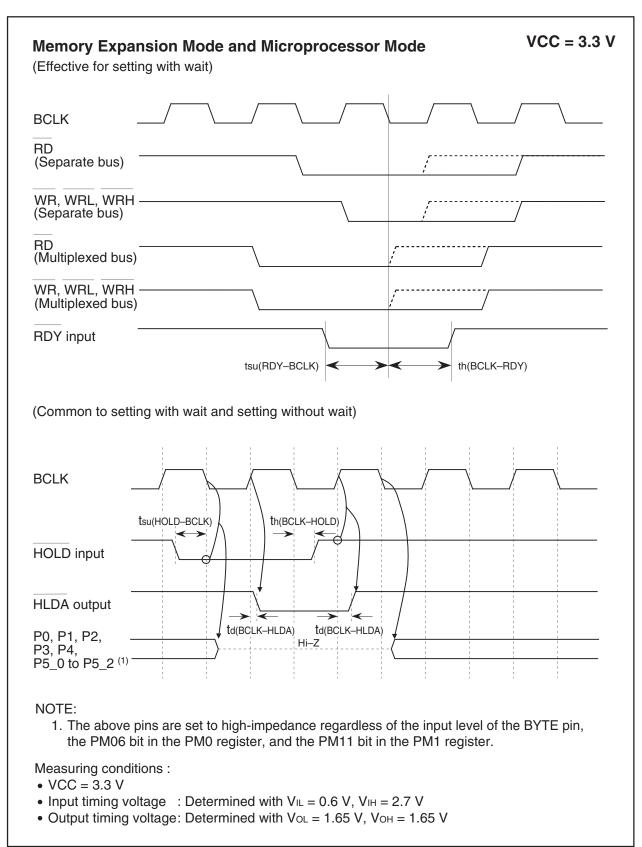


Figure 5.13 Timing Diagram (2)

5.2 Electrical Characteristics (T/V-ver.)

Symbol			Parameter	Condition	Rated Value	Unit
Vcc	Supply vo	oltage (VC	C1 = VCC2)	VCC = AVCC	-0.3 to 6.5	V
AVcc	Analog si	upply volta	age	VCC = AVCC	-0.3 to 6.5	V
Vı	Input voltage	P0_0 to P3_0 to P6_0 to F P9_0, P P11_0 to	CNVSS, BYTE, P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_7, P7_0, P7_2 to P7_7, P8_0 to P8_7, 9_2 to P9_7, P10_0 to P10_7, P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_1, VREF, XIN		-0.3 to VCC+0.3	V
		P7_1, P			-0.3 to 6.5	V
Vo	Output voltage	P3_0 to P6_0 to P8_0 to I P10_0 to	P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_7, P7_0, P7_2 to P7_7, P8_4, P8_6, P8_7, P9_0, P9_2 to P9_7, P10_7, P11_0 to P11_7, P12_0 to P12_7, p P13_7, P14_0, P14_1, XOUT		-0.3 to VCC+0.3	V
		P7_1, P	9_1		-0.3 to 6.5	V
Pd	Power dis	ssipation		Topr = 25°C	700	mW
Topr	Operating ambient temperature		During MCU operation During flash memory program and		T version: -40 to 85 V version: -40 to 125 (option) 0 to 60	°C
			erase operation			
Tstg	Storage t	emperatu	re		-65 to 150	°C

Table 5.46 Absolute Maximum Ratings

option: All options are on request basis. NOTE:

1. Ports P11 to P14 are only in the 128-pin version.



Timing Requirements VCC = 5 V (Referenced to VCC = 5 V, VSS = 0 V, at Topr = -40 to 85°C unless otherwise specified)

Table 5.63 Timer B Input (Counter Input in Event Counter Mode)

Symbol	Parameter	Stan	Unit	
	Falameter	Min.	Max.	Unit
tc(TB)	TBiIN input cycle time (counted on one edge)	100		ns
t _{w(TBH)}	TBiIN input HIGH pulse width (counted on one edge)	40		ns
tw(TBL)	TBiIN input LOW pulse width (counted on one edge)	40		ns
tc(TB)	TBiIN input cycle time (counted on both edges)	200		ns
t _{w(TBH)}	TBiIN input HIGH pulse width (counted on both edges)	80		ns
tw(TBL)	TBiIN input LOW pulse width (counted on both edges)	80		ns

Table 5.64 Timer B Input (Pulse Period Measurement Mode)

Symbol	Devemater	Stan	Unit	
Symbol	Parameter	Min.	Max.	Unit
t _{c(TB)}	TBiIN input cycle time	400		ns
tw(TBH)	TBiIN input HIGH pulse width	200		ns
tw(TBL)	TBiIN input LOW pulse width	200		ns

Table 5.65 Timer B Input (Pulse Width Measurement Mode)

Symbol	Determeter	Stan	Unit	
Symbol	Symbol Parameter -		Max.	Unit
t _{c(TB)}	TBiIN input cycle time	400		ns
tw(TBH)	TBiIN input HIGH pulse width	200		ns
tw(TBL)	TBiIN input LOW pulse width	200		ns

Table 5.66 A/D Trigger Input

Symbol	Parameter	Stan	Linit	
		Min.	Max.	Unit
tc(AD)	ADTRG input cycle time (trigger able minimum)	1000		ns
tw(ADL)	ADTRG input LOW pulse width	125		ns

Table 5.67 Serial Interface

Symbol	Deremeter	Stan	Unit	
	Parameter			Max.
tc(CK)	CLKi Input cycle time	200		ns
t _{w(CKH)}	CLKi Input HIGH pulse width	100		ns
tw(CKL)	CLKi Input LOW pulse width	100		ns
td(C-Q)	TXDi output delay time		80	ns
th(C-Q)	TXDi hold time	0		ns
tsu(D-C)	RXDi input setup time	70		ns
th(C-D)	RXDi input hold time	90		ns

Table 5.68 External Interrupt INTi Input

Symbol	Parameter		Standard		
	Parameter	Min.	Max.	Unit	
tw(INH)	INTi input HIGH pulse width	250		ns	
t _{w(INL)}	INTi input LOW pulse width	250		ns	

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