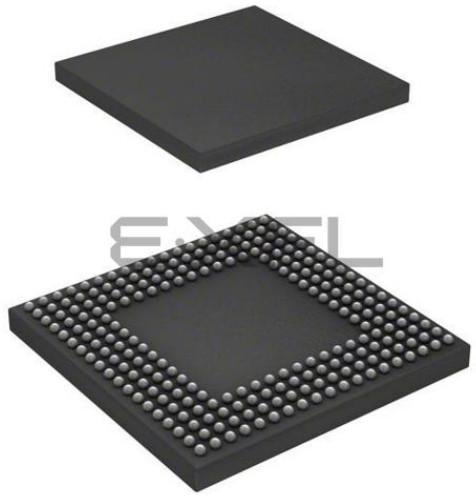


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	SH-3
Core Size	32-Bit Single-Core
Speed	133MHz
Connectivity	EBI/EMI, FIFO, IrDA, SCI, SmartCard
Peripherals	DMA, POR, WDT
Number of I/O	96
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 2.05V
Data Converters	A/D 8x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	240-LFBGA
Supplier Device Package	240-LFBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/d6417709sbp133bv

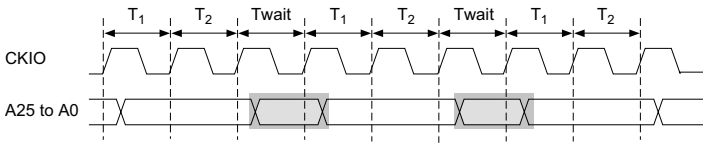
Renesas 32-Bit RISC Microcomputer
SuperH™ RISC engine Family/SH7700 Series

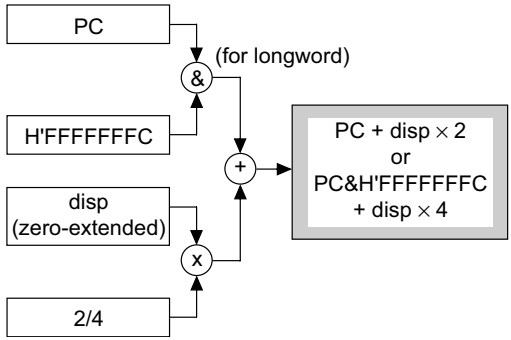
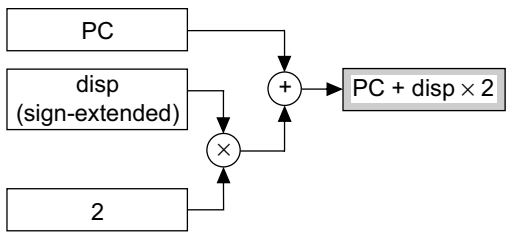
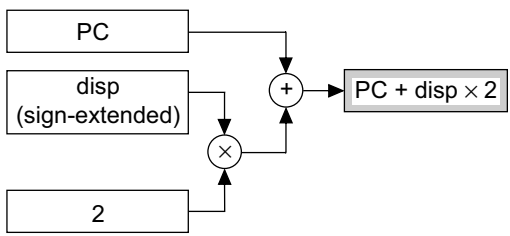
SH7709S Group

Hardware Manual

RENESAS

REJ09B0081-0500O

Section	Page	Description
10.2.13 MCS0 Control Register (MCSCR0)	258	Description added Bit 6—CS2/CS0 Select (CS2/0) Only 0 should be used for the CS2/0 bit in MCSCR0. Either 0 or 1 may be used for MCSCR1 to MCSCR7.
10.3.4 Synchronous DRAM Interface	290	Bank Active description added … .In bank active mode, too, all banks become inactive after a refresh cycle or after the bus is released as the result of bus arbitration. The bank active mode should not be used unless the bus width for all areas is 32 bits.
10.3.6 PCMCIA Interface Figure 10.32 Basic Timing for PCMCIA Memory Card Interface	310	Figure amended D15 to D0 (Write)
10.3.7 Waits between Access Cycles Figure 10.40 Waits between Access Cycles	320	Figure amended 
10.3.10 $\overline{\text{MCS[0]}}$ to $\overline{\text{MCS[7]}}$ Pin Control	323	Description amended This enables 32-, 64-, 128-, or 256-Mbit memory to be connected to area 0 or area 2. However, only CS2/0 = 0 (area 0) should be used for MCSCR0. Table 10.15 shows MCSCR0–MCSCR7 settings and $\overline{\text{MCS[0]}}$–$\overline{\text{MCS[7]}}$ assertion conditions.
11.6 Usage Notes	387	Description added 13. DMAC transfers should not be performed in the sleep mode under conditions other than when the clock ratio of Iϕ (on-chip clock) to Bϕ (bus clock) is 1:1. 14. When the following three conditions are all met, the frequency control register (FRQCR) should not be changed while a DMAC transfer is in progress. • Bits IFC2 to IFC0 are changed. • STC2 to STC0 in FRQCR are not changed. • The clock ratio of Iϕ (on-chip clock) to Bϕ (bus clock) after the change is other than 1:1.
13.4.3 Precautions when Using RTC Module Standby	426	Newly added

Addressing Mode	Instruction Format	Effective Address Calculation Method	Calculation Formula
PC-relative with displacement	@(disp:8, PC)	Effective address is register PC contents with 8-bit displacement disp added. After disp is zero-extended, it is multiplied by 2 (word), or 4 (longword), according to the operand size. With a longword operand, the lower 2 bits of PC are masked. 	Word: PC + disp × 2 Longword: PC & H'FFFF FFFC + disp × 4
PC-relative	disp:8	Effective address is register PC contents with 8-bit displacement disp added after being sign-extended and multiplied by 2. 	PC + disp × 2
	disp:12	Effective address is register PC contents with 12-bit displacement disp added after being sign-extended and multiplied by 2. 	PC + disp × 2

2.4 Instruction Set

2.4.1 Instruction Set Classified by Function

The SH7709S instruction set includes 68 basic instruction types, as listed in table 2.4.

Table 2.4 Classification of Instructions

Classification	Types	Operation Code	Function	No. of Instructions
Data transfer	5	MOV	Data transfer	39
		MOVA	Effective address transfer	
		MOVT	T bit transfer	
		SWAP	Swap of upper and lower bytes	
		XTRCT	Extraction of middle of linked registers	
Arithmetic operations	21	ADD	Binary addition	33
		ADDC	Binary addition with carry	
		ADDV	Binary addition with overflow check	
		CMP/cond	Comparison	
		DIV1	Division	
		DIV0S	Initialization of signed division	
		DIV0U	Initialization of unsigned division	
		DMULS	Signed double-precision multiplication	
		DMULU	Unsigned double-precision multiplication	
		DT	Decrement and test	
		EXTS	Sign extension	
		EXTU	Zero extension	
		MAC	Multiply-and-accumulate operation, double-precision multiply-and-accumulate operation	

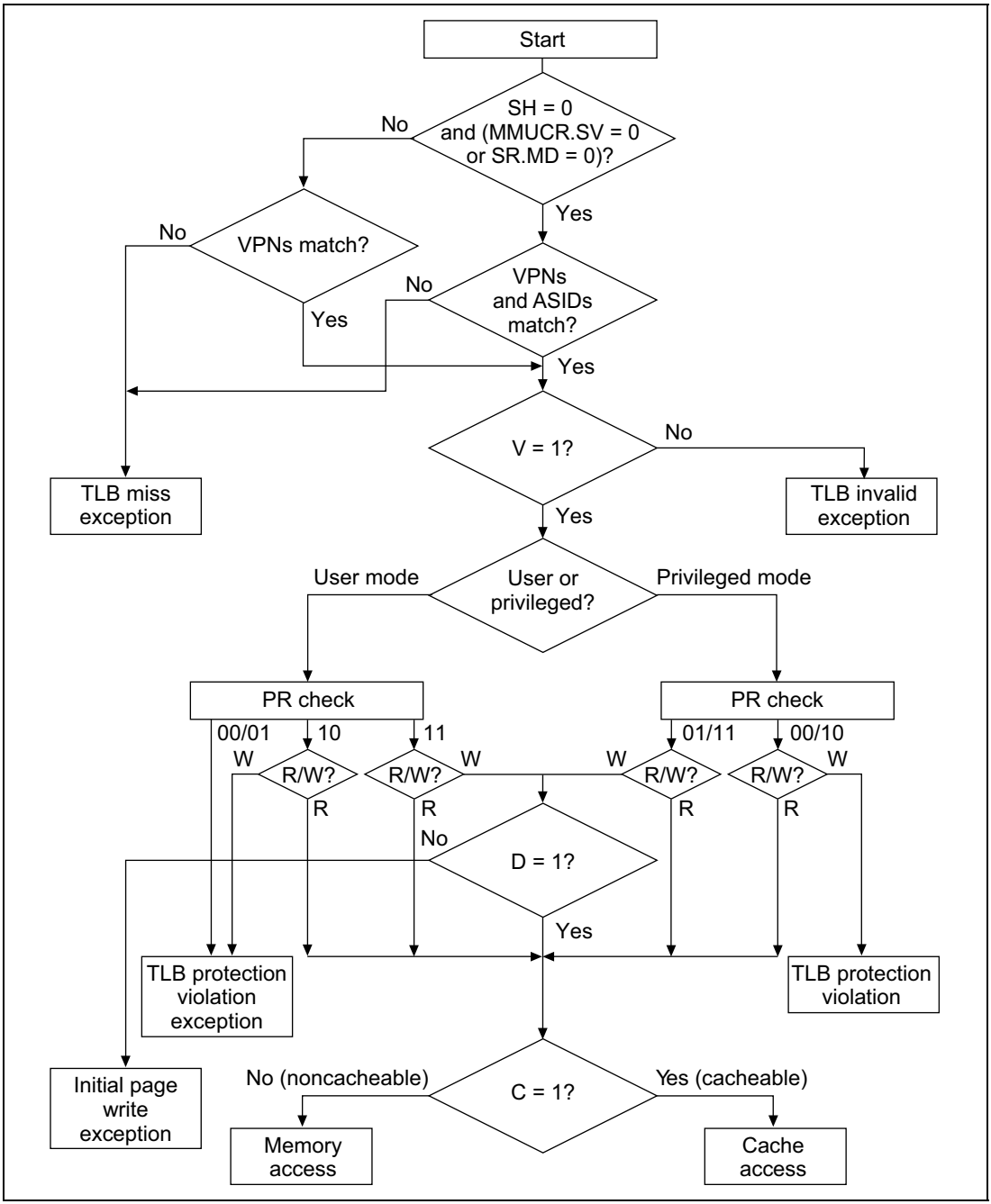


Figure 3.11 MMU Exception Generation Flowchart

10.3 BSC Operation

10.3.1 Endian/Access Size and Data Alignment

The SH7709S supports both big endian, in which the 0 address is the most significant byte in the byte data, and little endian, in which the 0 address is the least significant byte. Switching between the two is designated by an external pin (MD5 pin) at the time of a power-on reset. After a power-on reset, big endian is engaged when MD5 is low; little endian is engaged when MD5 is high.

Three data bus widths are available for ordinary memory (byte, word, longword) and two data bus widths (word and longword) for synchronous DRAM. For the PCMCIA interface, choose from byte and word. This means data alignment is done by matching the device's data width and endian. The access unit must also be matched to the device's bus width. This also means that when longword data is read from a byte-width device, four read operations must be performed. In the SH7709S, data alignment and conversion of data length is performed automatically between the respective interfaces.

Tables 10.7 to 10.12 show the relationship between endian, device data width, and access unit.

Table 10.7 32-Bit External Device/Big-Endian Access and Data Alignment

	Data Bus				Strobe Signals			
Operation	**D31–D24**	**D23–D16**	**D15–D8**	**D7–D0**	**$\overline{WE3}$, DQMUU**	**$\overline{WE2}$, DQMUL**	**$\overline{WE1}$, DQMLU**	**$\overline{WE0}$, DQMLL**
Byte access at 0	Data 7–0	—	—	—	Asserted			
Byte access at 1	—	Data 7–0	—	—		Asserted		
Byte access at 2	—	—	Data 7–0	—			Asserted	
Byte access at 3	—	—	—	Data 7–0				Asserted
Word access at 0	Data 15–8	Data 7–0	—	—	Asserted	Asserted		
Word access at 2	—	—	Data 15–8	Data 7–0			Asserted	Asserted
Longword access at 0	Data 31–24	Data 23–16	Data 15–8	Data 7–0	Asserted	Asserted	Asserted	Asserted

Table 10.14 Example of Correspondence between SH7709S and Synchronous DRAM Address Pins (AMX [3:0] = 0100 (32-Bit Bus Width))

SH7709S Address Pin			Synchronous DRAM Address Pin	
	RAS Cycle	CAS Cycle		Function
A15	A23	A23	A13(BA1)	BANK select bank address
A14	A22	A22	A12(BA0)	
A13	A21	A13	A11	Address
A12	A20	L/H	A10	Address precharge setting
A11	A19	A11	A9	Address
A10	A18	A10	A8	
A9	A17	A9	A7	
A8	A16	A8	A6	
A7	A15	A7	A5	
A6	A14	A6	A4	
A5	A13	A5	A3	
A4	A12	A4	A2	
A3	A11	A3	A1	
A2	A10	A2	A0	
A1	A9	A1	Not used	
A0	A0	A0	Not used	

Burst Read: In the example in figure 10.15 it is assumed that four 2M × 8-bit synchronous DRAMs are connected and a 32-bit data width is used, and the burst length is 1. Following the Tr cycle in which ACTV command output is performed, a READ command is issued in the Tc1, Tc2, and Tc3 cycles, and a READA command in the Tc4 cycle, and the read data is accepted at the rising edge of the external command clock (CKIO) from cycle Td1 to cycle Td4. The Tpc cycle is used to wait for completion of auto-precharge based on the READA command inside the synchronous DRAM; no new access command can be issued to the same bank during this cycle, but access to synchronous DRAM for another area is possible. In the SH7709S, the number of Tpc cycles is determined by the TPC bit specification in MCR, and commands cannot be issued for the same synchronous DRAM during this interval.

The example in figure 10.14 shows the basic cycle. To connect low-speed synchronous DRAM, the cycle can be extended by setting WCR2 and MCR bits. The number of cycles from the ACTV command output cycle, Tr, to the READ command output cycle, Tc1, can be specified by the RCD bits in MCR, with values of 0 to 3 specifying 1 to 4 cycles, respectively. In case of 2 or more cycles, a Trw cycle, in which an NOP command is issued for the synchronous DRAM, is inserted between the Tr cycle and the Tc cycle. The number of cycles from READ and READA command output cycles Tc1-Tc4 to the first read data latch cycle, Td1, can be specified as 1 to 3 cycles

Power-On Sequence: In order to use synchronous DRAM, mode setting must first be performed after powering on. To perform synchronous DRAM initialization correctly, the bus state controller registers must first be set, followed by a write to the synchronous DRAM mode register. In synchronous DRAM mode register setting, the address signal value at that time is latched by a combination of the $\overline{RAS}$, $\overline{CAS}$, and RD/$\overline{WR}$ signals. If the value to be set is X, the bus state controller provides for value X to be written to the synchronous DRAM mode register by performing a write to address H'FFFFD000 + X for area 2 synchronous DRAM, and to address H'FFFFE000 + X for area 3 synchronous DRAM. In this operation the data is ignored, but the mode write is performed as a byte-size access. To set burst read/single write, CAS latency 1 to 3, wrap type = sequential, and burst length 1 supported by the SH7709S, arbitrary data is written in a byte-size access to the following addresses.

With 32-bit bus width:

	Area 2	Area 3
CAS latency 1	FFFFD840	FFFFE840
CAS latency 2	FFFFD880	FFFFE880
CAS latency 3	FFFFD8C0	FFFFE8C0

With 16-bit bus width:

	Area 2	Area 3
CAS latency 1	FFFFD420	FFFFE420
CAS latency 2	FFFFD440	FFFFE440
CAS latency 3	FFFFD460	FFFFE460

Mode register setting timing is shown in figure 10.28.

As a result of the write to address H'FFFFD000 + X or H'FFFFE000 + X, a precharge all banks (PALL) command is first issued in the TRp1 cycle, then a mode register write command is issued in the TMw1 cycle.

Address signals, when the mode-register write command is issued, are as follows:

32-bit bus width:
- A15–A9 = 0000100 (burst read and single write)
- A8–A6 = CAS latency
- A5 = 0 (burst type = sequential)
- A4–A2 = 000 (burst length 1)

16-bit bus width:
- A14–A8 = 0000100 (burst read and single write)
- A7–A5 = CAS latency
- A4 = 0 (burst type = sequential)
- A3–A1 = 000 (burst length 1)

10.3.5 Burst ROM Interface

Setting bits A0BST1–0, A5BST1–0, and A6BST1–0 in BCR1 to a non-zero value allows burst ROM to be connected to areas 0, 5, and 6. The burst ROM interface provides high-speed access to ROM that has a nibble access function. The timing for nibble access to burst ROM is shown in figure 10.29. Two wait cycles are set. Basically, access is performed in the same way as for normal space, but when the first cycle ends the $\overline{CS0}$ signal is not negated, and only the address is changed before the next access is executed. When 8-bit ROM is connected, the number of consecutive accesses can be set as 4, 8, or 16 by bits A0BST1–0, A5BST1–0, or A6BST1–0. When 16-bit ROM is connected, 4 or 8 can be set in the same way. When 32-bit ROM is connected, only 4 can be set.

$\overline{WAIT}$ pin sampling is performed in the first access if one or more wait states are set, and is always performed in the second and subsequent accesses.

The second and subsequent access cycles also comprise two cycles when a burst ROM setting is made and the wait specification is 0. The timing in this case is shown in figure 10.30.

However, the $\overline{WAIT}$ signal is ignored in the following three cases:

- A write to external address space in dual address mode with 16-byte DMA transfer
- Transfer from an external device with DACK to external address space in single address mode with 16-byte DMA transfer
- Cache write-back access

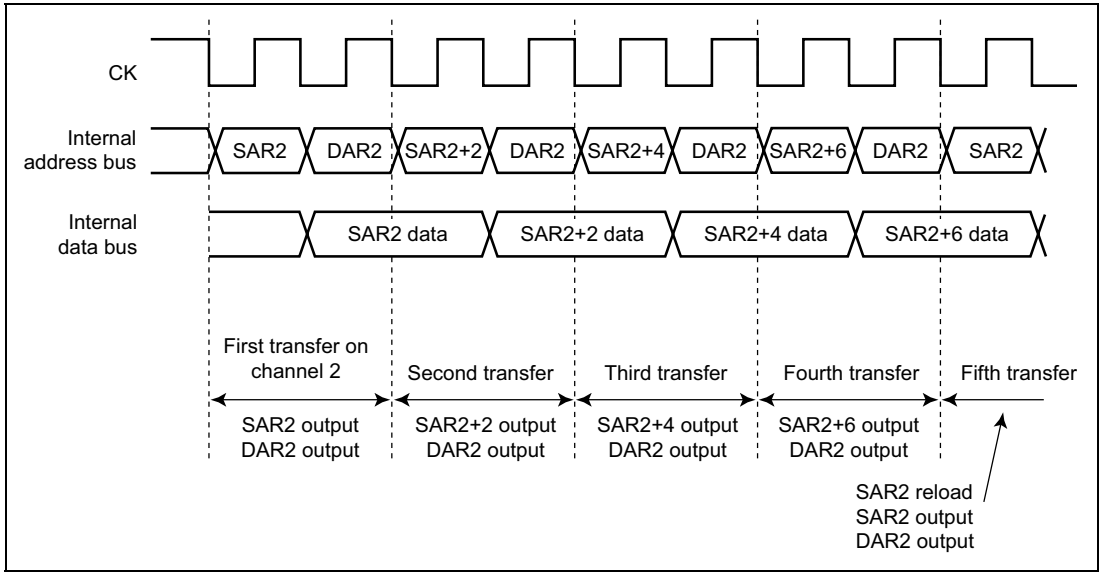


Figure 11.23 Timing Chart of Source Address Reload Function

The reload function can be executed with a transfer data size of 8, 16, or 32 bits.

DMATCR2, which specifies the transfer count, decrements 1 each time a transfer ends regardless of whether the reload function is on or off. Consequently, a multiple of four must be specified in DMATCR2 when the reload function is on. Operation is not guaranteed if other values are specified.

The counter that counts the execution of four transfers for the address reload function is reset by clearing the DME bit in DMAOR or the DE bit in CHCR2, by setting the transfer end flag (TE bit in CHCR2), by DMAC address error, and by NMI input, as well as by a reset, but the SAR2, DAR2, and DMATCR2 registers are not reset. Therefore, if these sources are generated, there will be a mix of an initialized counter and uninitialized registers in the DMAC, and a malfunction will be caused by restarting the DMAC in that state. Consequently, if one of these sources other than setting of the TE bit occurs during use of the address reload function, set SAR2, DAR2, and DMATCR2 again.

11.4 Compare Match Timer (CMT)

11.4.1 Overview

The DMAC has an on-chip compare match timer (CMT) to generate DMA transfer requests. The CMT has a 16-bit counter.

Features

The CMT has the following features:

- Four types of counter input clock can be selected
  — One of four internal clocks (Pϕ/4, Pϕ/8, Pϕ/16, Pϕ/64) can be selected.
- Generates a DMA transfer request when compare match occurs.

Block Diagram

Figure 11.24 shows a block diagram of the CMT.

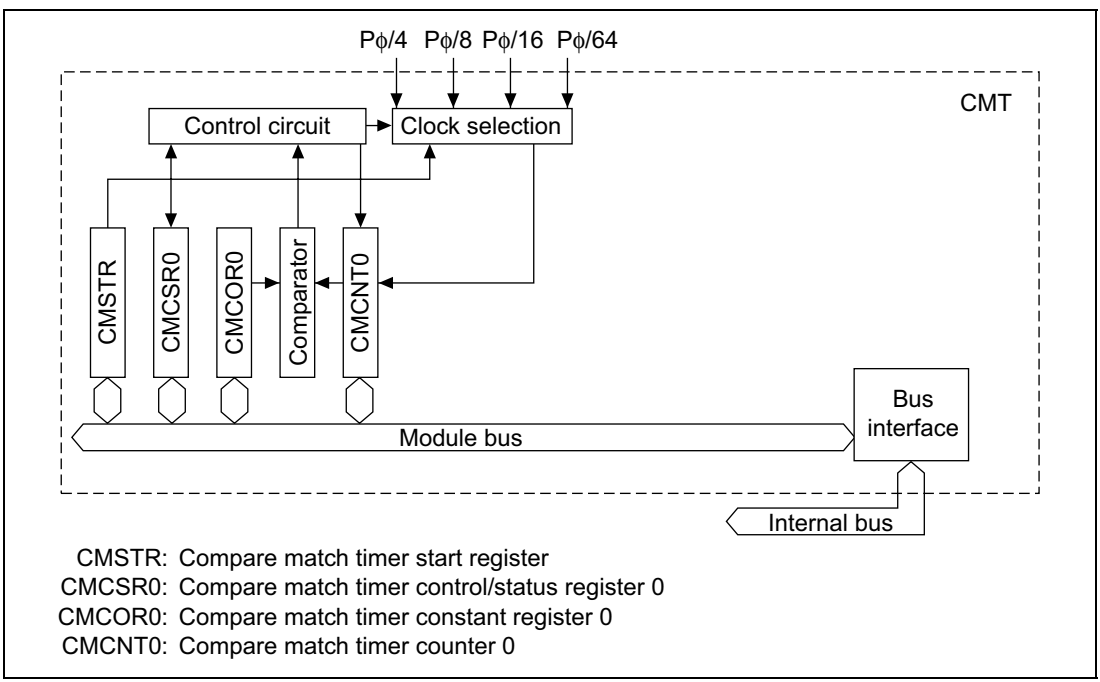


Figure 11.24 Block Diagram of CMT

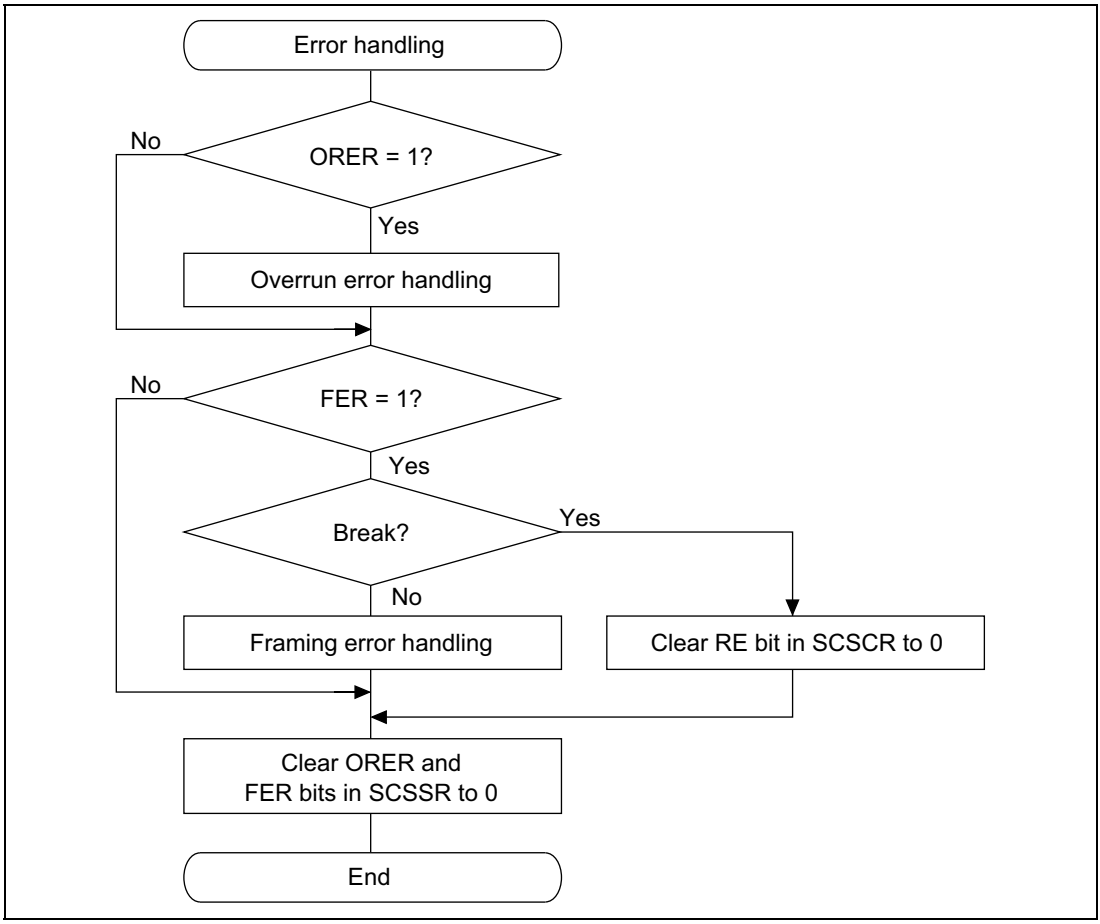


Figure 14.15 Sample Flowchart for Receiving Multiprocessor Serial Data (cont)

Bit 3—Framing Error (FER): Indicates a framing error in the data read from the receive FIFO data register (SCFRDR).

Bit 3: FER	Description
0	No receive framing error occurred in the data read from SCFRDR (Initial value) [Clearing conditions] (1) When the chip undergoes a power-on reset or enters standby mode (2) When no framing error is present in the data read from SCFRDR
1	A receive framing error occurred in the data read from SCFRDR [Setting condition] When a framing error is present in the data read from SCFRDR

Bit 2—Parity Error (PER): Indicates a parity error in the data read from the receive FIFO data register (SCFRDR).

Bit 2: PER	Description
0	No receive parity error occurred in the data read from SCFRDR (Initial value) [Clearing conditions] (1) When the chip undergoes a power-on reset or enters standby mode (2) When no parity error is present in the data read from SCFRDR
1	A receive framing error occurred in the data read from SCFRDR [Setting condition] When a parity error is present in the data read from SCFRDR

Table 19.24 Read/Write Operation of the SC Port Data Register (SCPDR)

SCPnMD1	SCPnMD0	Pin State	Read	Write
0	0	Other function (see table 18.1)	SCPDR value	Value is written to SCPDR, but does not affect pin state
	1	Output	SCPDR value	Write value is output from pin
1	0	Input (Pull-up MOS on)	Pin state	Value is written to SCPDR, but does not affect pin state
	1	Input (Pull-up MOS off)	Pin state	Value is written to SCPDR, but does not affect pin state

(n = 0 to 6)

SCPnMD1	SCPnMD0	Pin State	Read	Write
0	0	Other function (see table 18.1)	Low level	Ignored (no effect on pin state)
	1	Output	Low level	Ignored (no effect on pin state)
1	0	Input (Pull-up MOS on)	Pin state	Ignored (no effect on pin state)
	1	Input (Pull-up MOS off)	Pin state	Ignored (no effect on pin state)

(n = 7)

23.3.2 Control Signal Timing

Table 23.6 Control Signal Timing

Vcc = 3.3 ± 0.3 V, Vcc = 1.55 to 2.15 V, AVcc = 3.3 ± 0.3 V, Ta = –20 to 75°C

Item	Symbol	Min	Max	Unit	Figure
$\overline{\text{RESETP}}$ pulse width	t_{RESPW}	20 *2	—	tcyc	23.11,
$\overline{\text{RESETP}}$ setup time*1	t_{RESPS}	20	—	ns	23.12
$\overline{\text{RESETP}}$ hold time	t_{RESPH}	4	—	ns	
$\overline{\text{RESETM}}$ pulse width	t_{RESMW}	20 *3	—	tcyc	
$\overline{\text{RESETM}}$ setup time	t_{RESMS}	6	—	ns	
$\overline{\text{RESETM}}$ hold time	t_{RESMH}	34	—	ns	
$\overline{\text{BREQ}}$ setup time	t_{BREQS}	6	—	ns	23.14
$\overline{\text{BREQ}}$ hold time	t_{BREQH}	4	—	ns	
NMI setup time *1	t_{NMIS}	10	—	ns	23.12
NMI hold time	t_{NMIH}	4	—	ns	
IRQ5–IRQ0 setup time *1	t_{IRQS}	10	—	ns	
IRQ5–IRQ0 hold time	t_{IRQH}	4	—	ns	
$\overline{\text{IRQOUT}}$ delay time	t_{IRQOD}	—	10	ns	23.13
$\overline{\text{BACK}}$ delay time	t_{BACKD}	—	10	ns	23.14,
STATUS1, STATUS0 delay time	t_{STD}	—	10	ns	23.15
Bus tri-state delay time 1	t_{BOFF1}	0	15	ns	
Bus tri-state delay time 2	t_{BOFF2}	0	15	ns	
Bus buffer-on time 1	t_{BON1}	0	15	ns	
Bus buffer-on time 2	t_{BON2}	0	15	ns	

Notes: 1. $\overline{\text{RESETP}}$, NMI, and IRQ5 to IRQ0 are asynchronous. Changes are detected at the clock fall when the setup shown is used. When the setup cannot be used, detection can be delayed until the next clock falls.

2. In the standby mode, $t_{RESPW} = t_{OSC1}$ (100 µs) when XTAL oscillation is continued and $t_{RESPW} = t_{OSC2}$ (10 ms) when XTAL oscillation is off. In the sleep mode, $t_{RESPW} = t_{PLL1}$ (100 µs).
When the clock multiplication ratio is changed, $t_{RESPW} = t_{PLL1}$ (100 µs).

3. In the standby mode, $t_{RESMW} = t_{OSC2}$ (10 ms). In the sleep mode, $\overline{\text{RESETM}}$ must be kept low until STATUS (0-1) changes to reset (HH). When the clock multiplication ratio is changed, $\overline{\text{RESETM}}$ must be kept low until STATUS (0-1) changes to reset (HH).

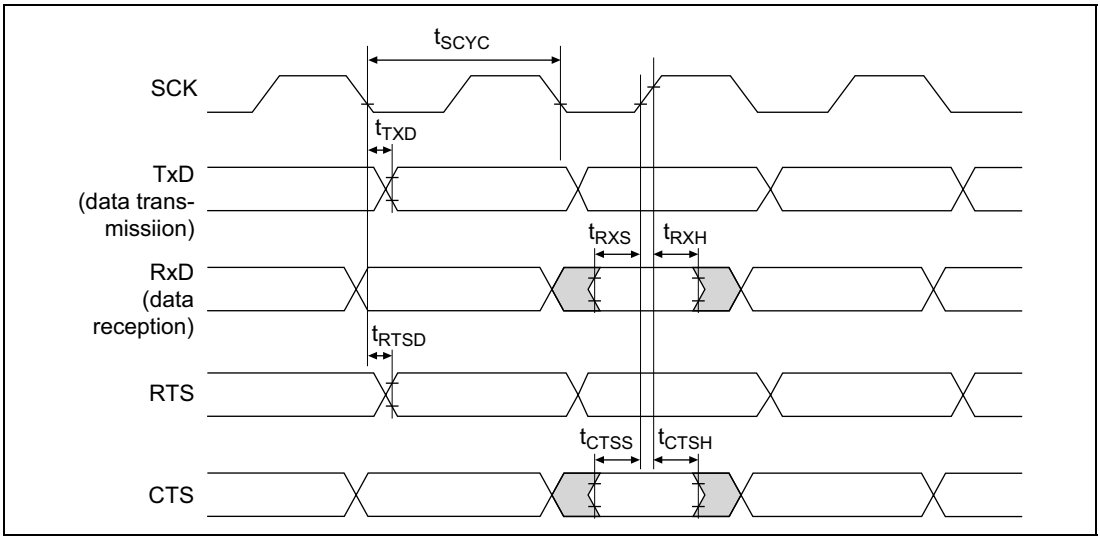


Figure 23.51 SCI I/O Timing in Clock Synchronous Mode

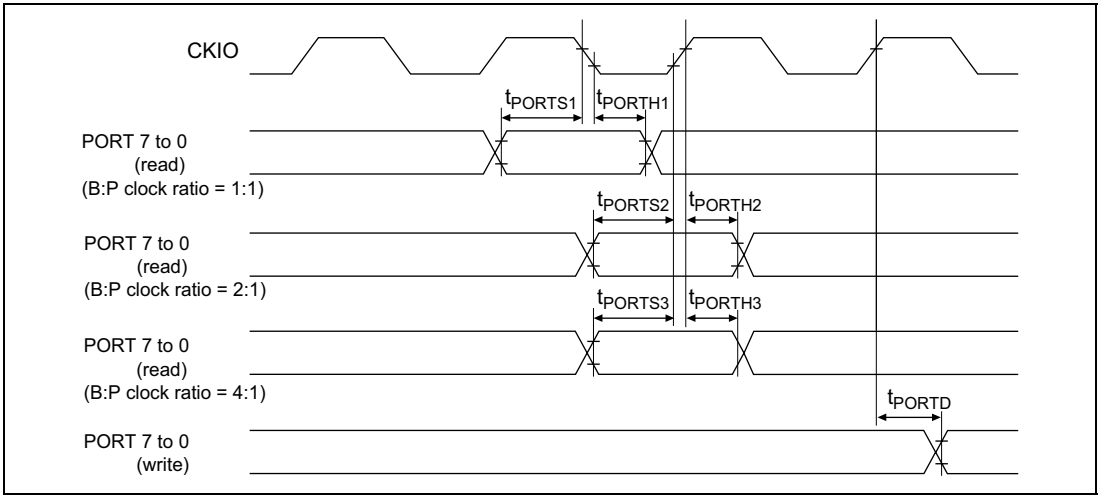


Figure 23.52 I/O Port Timing

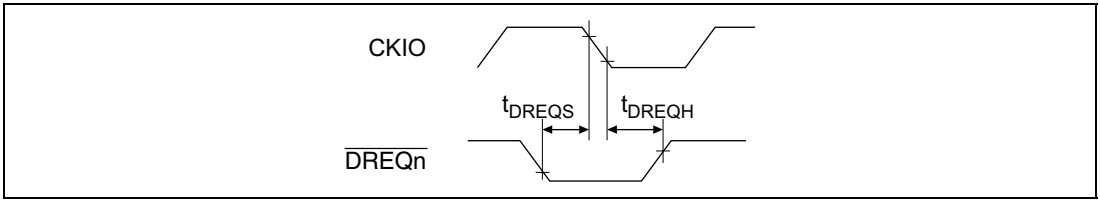
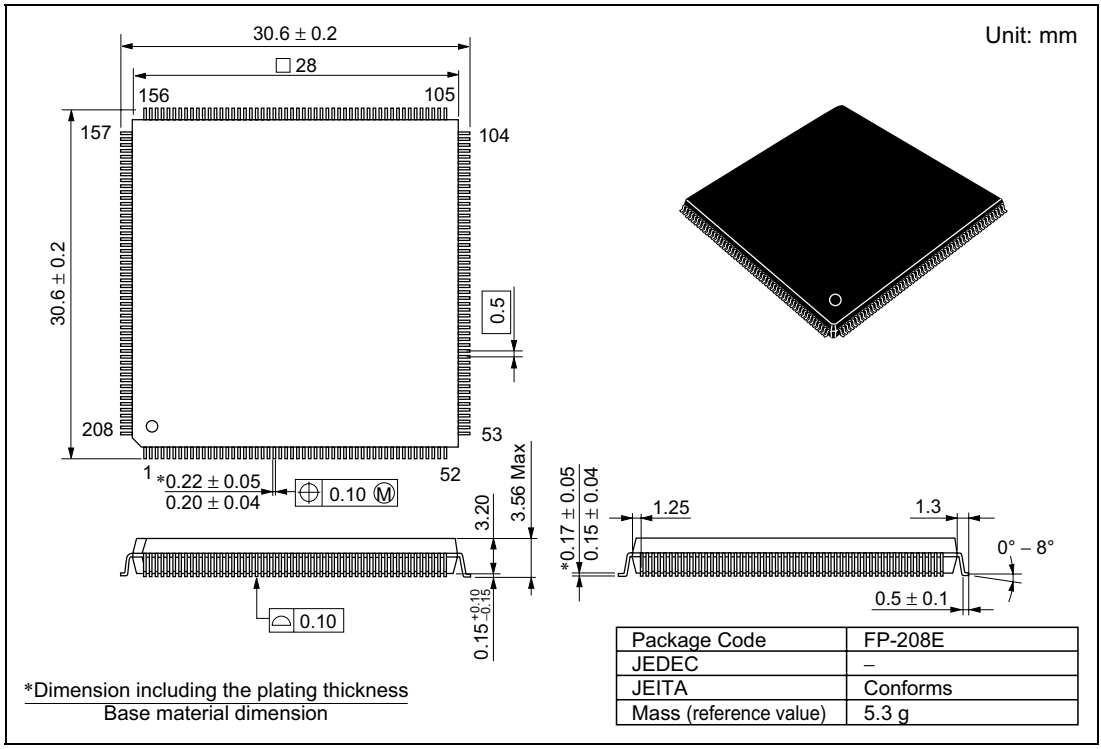


Figure 23.53 $\overline{\text{DREQ}}$ Input Timing



Package Code	FP-208E
JEDEC	–
JEITA	Conforms
Mass (reference value)	5.3 g

Figure D.2 Package Dimensions (FP-208E)