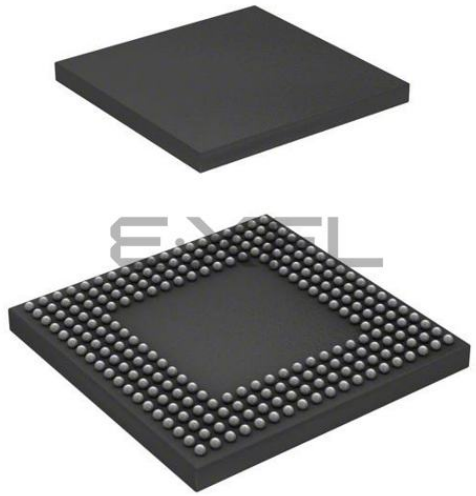

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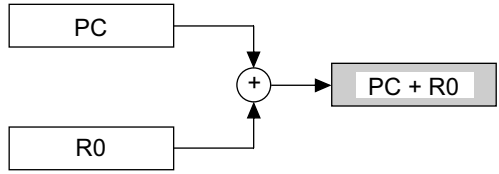
Details	
Product Status	Active
Core Processor	SH-3
Core Size	32-Bit Single-Core
Speed	167MHz
Connectivity	EBI/EMI, FIFO, IrDA, SCI, SmartCard
Peripherals	DMA, POR, WDT
Number of I/O	96
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.75V ~ 2.05V
Data Converters	A/D 8x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	240-LFBGA
Supplier Device Package	240-LFBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/d6417709sbp167bv

Addressing Mode	Instruction Format	Effective Address Calculation Method	Calculation Formula
PC-relative	Rn	Effective address is sum of register PC and Rn contents.  	PC + Rn
Immediate	#imm:8	8-bit immediate data imm of TST, AND, OR, or XOR instruction is zero-extended.	—
	#imm:8	8-bit immediate data imm of MOV, ADD, or CMP/EQ instruction is sign-extended.	—
	#imm:8	8-bit immediate data imm of TRAPA instruction is zero-extended and multiplied by 4.	—

Note: For the addressing modes below that use a displacement (disp), the assembler descriptions in this manual show the value before scaling (×1, ×2, or ×4) is performed according to the operand size. This is done to clarify the operation of the IC. Refer to the relevant assembler notation rules for the actual assembler descriptions.

@ (disp:4, Rn) ; Register indirect with displacement

@ (disp:8, Rn) ; GBR indirect with displacement

@ (disp:8, PC) ; PC-relative with displacement

disp:8, disp:12; PC-relative

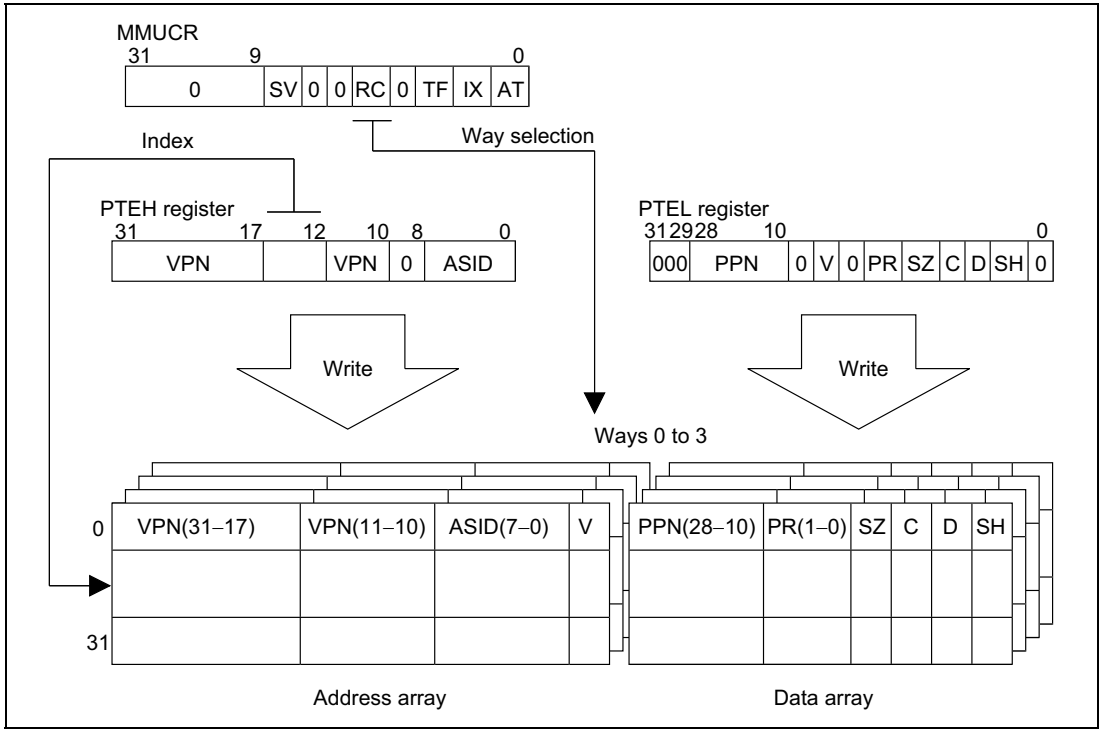


Figure 3.9 Operation of LDTLB Instruction

Bit 21—Break ASID Mask A (BASMA): Specifies whether the bits of the channel A break ASID7-ASID0 (BASA7 to BASA0) set in BASRA are masked or not.

Bit 21: BASMA	Description	
0	All BASRA bits are included in break condition, ASID is checked	(Initial value)
1	No BASRA bits are included in break condition, ASID is not checked	

Bit 20—Break ASID Mask B (BASMB): Specifies whether the bits of channel B break ASID7-ASID0 (BASB7 to BASB0) set in BASRB are masked or not.

Bit 20: BASMB	Description	
0	All BASRB bits are included in break condition, ASID is checked	(Initial value)
1	No BASRB bits are included in break condition, ASID is not checked	

Bits 19 to 16—Reserved: These bits are always read as 0. The write value should always be 0.

Bit 15—CPU Condition Match Flag A (SCMFCA): When the CPU bus cycle condition in the break conditions set for channel A is satisfied, this flag is set to 1 (not cleared to 0). In order to clear this flag, write 0 into this bit.

Bit 15: SCMFCA	Description	
0	The CPU cycle condition for channel A does not match	(Initial value)
1	The CPU cycle condition for channel A matches	

Bit 14—CPU Condition Match Flag B (SCMFCB): When the CPU bus cycle condition in the break conditions set for channel B is satisfied, this flag is set to 1 (not cleared to 0). In order to clear this flag, write 0 into this bit.

Bit 14: SCMFCB	Description	
0	The CPU cycle condition for channel B does not match	(Initial value)
1	The CPU cycle condition for channel B matches	

Bit 6—Timer Mode Select (WT/$\overline{IT}$): Selects whether to use the WDT as a watchdog timer or an interval timer.

Bit 6: WT/$\overline{IT}$	Description	
0	Used as interval timer	(Initial value)
1	Used as watchdog timer	

Note: If WT/$\overline{IT}$ is modified when the WDT is running, the up-count may not be performed correctly.

Bit 5—Reset Select (RSTS): Selects the type of reset when WTCNT overflows in watchdog timer mode. In interval timer mode, this setting is ignored.

Bit 5: RSTS	Description	
0	Power-on reset	(Initial value)
1	Manual reset	

Note: $\overline{RESETOUT}$ is output.

Bit 4—Watchdog Timer Overflow (WOVF): Indicates that the WTCNT has overflowed in watchdog timer mode. This bit is not set in interval timer mode.

Bit 4: WOVF	Description	
0	No overflow	(Initial value)
1	WTCNT has overflowed in watchdog timer mode	

Bit 3—Interval Timer Overflow (IOVF): Indicates that WTCNT has overflowed in interval timer mode. This bit is not set in watchdog timer mode.

Bit 3: IOVF	Description	
0	No overflow	(Initial value)
1	WTCNT has overflowed in interval timer mode	

Bits 2 to 0—Clock Select 2 to 0 (CKS2 to CKS0): These bits select the clock to be used for the WTCNT count from the eight types obtainable by dividing the peripheral clock. The overflow period in the table is the value when the peripheral clock (Pϕ) is 15 MHz.

Bits 5 to 3—Clock Select Bits (CKS2 to CKS0): Select the clock input to RTCNT. The source clock is the external bus clock (CKIO). The RTCNT count clock is CKIO divided by the specified ratio. RTCOR must be set before setting CKS2-CKS0.

			Description
Bit 5: CKS2	**Bit 4: CKS1**	**Bit 3: CKS0**	**Normal external bus clock**
0	0	0	Clock input disabled
		1	Bus clock (CKIO)/4
	1	0	CKIO/16
		1	CKIO/64
1	0	0	CKIO/256
		1	CKIO/1024
	1	0	CKIO/2048
		1	CKIO/4096

Bit 2—Refresh Count Overflow Flag (OVF): Indicates when the number of refresh requests indicated in the refresh count register (RFCR) exceeds the limit set in the LMTS bit in RTCSR.

Bit 2: OVF	**Description**
0	RFCR has not exceeded the count limit value set in LMTS (Initial value) Clearing condition: When 0 is written to OVF
1	RFCR has exceeded the count limit value set in LMTS Setting condition: When the RFCR value has exceeded the count limit value set in LMTS*

Note: * Contents do not change when 1 is written to OVF.

Bit 1—Refresh Count Overflow Interrupt Enable (OVIE): Selects whether to suppress generation of interrupt requests by the OVF bit in RTCSR when OVF is set to 1.

Bit 1: OVIE	**Description**
0	Interrupt request by OVF is disabled (Initial value)
1	Interrupt request by OVF is enabled

11.1.2 Block Diagram

Figure 11.1 shows a block diagram of the DMAC.

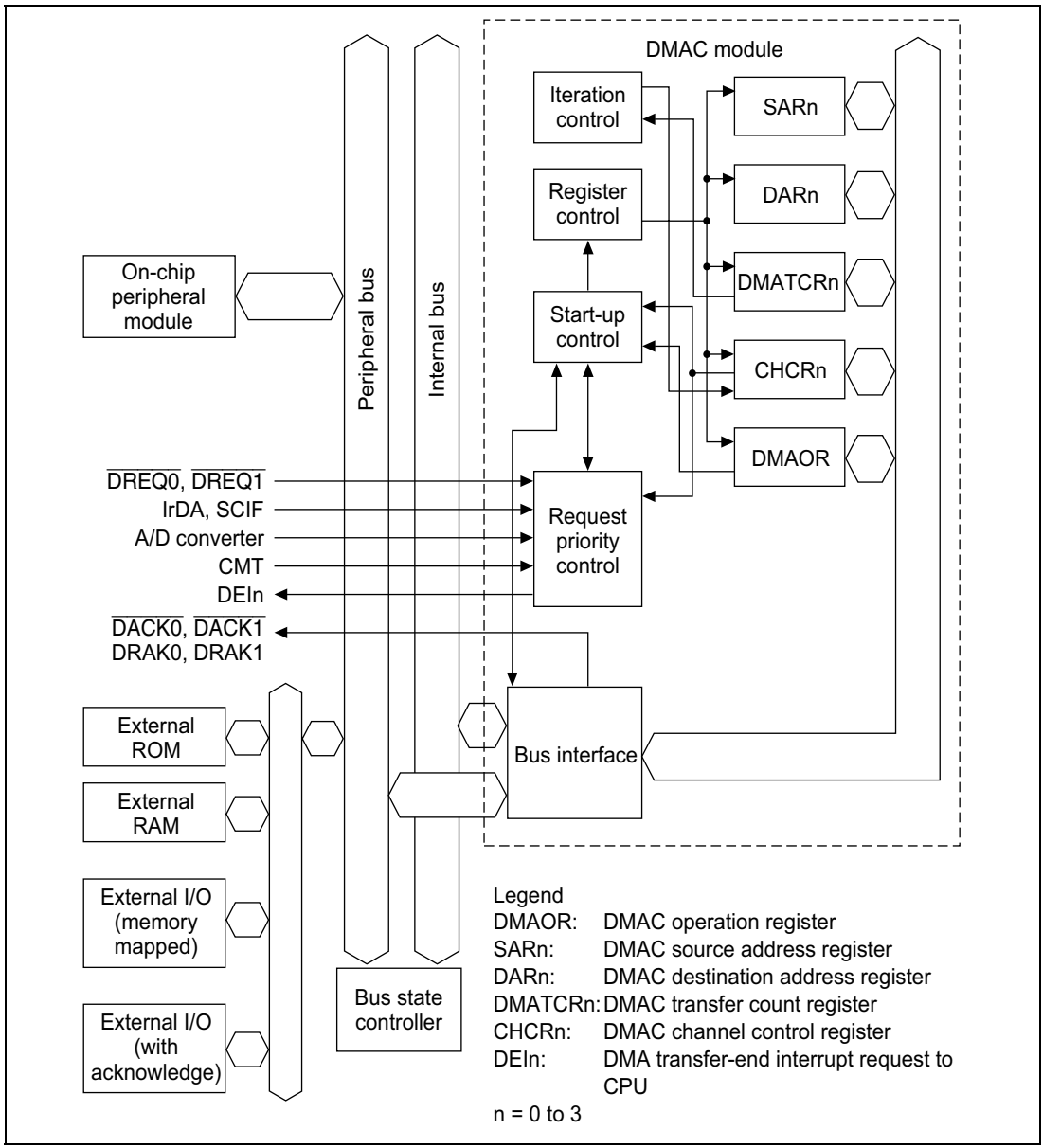


Figure 11.1 Block Diagram of DMAC

12.1.3 Pin Configuration

Table 12.1 shows the pin configuration of the TMU.

Table 12.1 TMU Pin

Channel	Pin	I/O	Description
Clock input/clock output	TCLK	I/O	External clock input pin/input capture control input pin/realtime clock (RTC) output pin

12.1.4 Register Configuration

Table 12.2 shows the TMU register configuration.

Table 12.2 TMU Registers

Channel	Register	Abbre-viation	R/W	Initial Value*	Address	Access Size
Common	Timer output control register	TOCR	R/W	H'00	H'FFFFFE90	8
	Timer start register	TSTR	R/W	H'00	H'FFFFFE92	8
0	Timer constant register 0	TCOR0	R/W	H'FFFFFFFF	H'FFFFFE94	32
	Timer counter 0	TCNT0	R/W	H'FFFFFFFF	H'FFFFFE98	32
	Timer control register 0	TCR0	R/W	H'0000	H'FFFFFE9C	16
1	Timer constant register 1	TCOR1	R/W	H'FFFFFFFF	H'FFFFFEA0	32
	Timer counter 1	TCNT1	R/W	H'FFFFFFFF	H'FFFFFEA4	32
	Timer control register 1	TCR1	R/W	H'0000	H'FFFFFEA8	16
2	Timer constant register 2	TCOR2	R/W	H'FFFFFFFF	H'FFFFFEAC	32
	Timer counter 2	TCNT2	R/W	H'FFFFFFFF	H'FFFFFEB0	32
	Timer control register 2	TCR2	R/W	H'0000	H'FFFFFEB4	16
	Input capture register 2	TCPR2	R	Undefined	H'FFFFFEB8	32

Note: * Initialized by power-on resets or manual resets.

Bits 4 and 3—Clock Edge 1 and 0 (CKEG1, CKEG0): Select the external clock edge when the external clock is selected, or when the input capture function is used.

Bit 4: CKEG1	Bit 3: CKEG0	Description	
0	0	Count/capture register set on rising edge	(Initial value)
	1	Count/capture register set on falling edge	
1	X	Count/capture register set on both rising and falling edge	

Note: X means 0, 1, or 'Don't care'.

Bits 2 to 0—Timer Prescaler 2 to 0 (TPSC2 to TPSC0): Select the TCNT count clock.

Bit 2: TPSC2	Bit 1: TPSC1	Bit 0: TPSC0	Description	
0	0	0	Internal clock: count on Pϕ/4	(Initial value)
		1	Internal clock: count on Pϕ/16	
	1	0	Internal clock: count on Pϕ/64	
		1	Internal clock: count on Pϕ/256	
1	0	0	Internal clock: count on clock output of on-chip RTC (RTC CLK)	
		1	Count on TCLK pin input	
	1	0	Reserved (Setting prohibited)	
		1	Reserved (Setting prohibited)	

Section 13 Realtime Clock (RTC)

13.1 Overview

The SH7709S has a realtime clock (RTC) with its own 32.768-kHz crystal oscillator.

13.1.1 Features

- Clock and calendar functions (BCD display): Seconds, minutes, hours, date, day of the week, month, and year
- 1-Hz to 64-Hz timer (binary display)
- Start/stop function
- 30-second adjust function
- Alarm interrupt: Frame comparison of seconds, minutes, hours, date, day of the week, and month can be used as conditions for the alarm interrupt
- Cyclic interrupts: The interrupt cycle may be 1/256 second, 1/64 second, 1/16 second, 1/4 second, 1/2 second, 1 second, or 2 seconds
- Carry interrupt: A carry interrupt indicates when a carry occurs during a counter read
- Automatic leap year correction

14.2.2 Receive Data Register (SCRDR)

The receive data register (SCRDR) stores serial receive data. The SCI completes the reception of one byte of serial data by moving the received data from the receive shift register (SCRSR) into SCRDR for storage. SCRSR is then ready to receive the next data. This double buffering allows the SCI to receive data continuously.

The CPU can read but not write to SCRDR. SCRDR is initialized to H'00 by a reset and in standby or module standby mode.

Bit:	7	6	5	4	3	2	1	0
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R

14.2.3 Transmit Shift Register (SCTSR)

The transmit shift register (SCTSR) transmits serial data. The SCI loads transmit data from the transmit data register (SCTDR) into SCTSR, then transmits the data serially from the TxD pin, LSB (bit 0) first. After transmitting one-byte data, the SCI automatically loads the next transmit data from SCTDR into SCTSR and starts transmitting again. If the TDRE bit in SCSSR is 1, however, the SCI does not load the SCTDR contents into SCTSR. The CPU cannot read or write to SCTSR directly.

Bit:	7	6	5	4	3	2	1	0
R/W:	—	—	—	—	—	—	—	—

In serial transmission, the SCIF operates as described below.

1. When data is written into the transmit FIFO data register (SCFTDR), the SCIF transfers the data from SCFTDR to the transmit shift register (SCTSR) and starts transmitting. Confirm that the TDFE flag in the serial status register (SCSSR) is set to 1 before writing transmit data to SCFTDR. The number of data bytes that can be written is (16 – transmit trigger setting).

2. When data is transferred from SCFTDR to SCTSR and transmission is started, consecutive transmit operations are performed until there is no transmit data left in SCFTDR. When the number of transmit data bytes in SCFTDR falls below the transmit trigger number set in the FIFO control register (SCFCR), the TDFE flag is set. If the TIE bit in the serial control register (SCSR) is set to 1 at this time, a transmit-FIFO-data-empty interrupt (TXI) request is generated.

   The serial transmit data is sent from the TxD pin in the following order.

   a. Start bit: One-bit 0 is output.
   b. Transmit data: 8-bit or 7-bit data is output in LSB-first order.
   c. Parity bit: One parity bit (even or odd parity) is output. (A format in which a parity bit is not output can also be selected.)
   d. Stop bit(s): One or two 1-bits (stop bits) are output.
   e. Mark state: 1 is output continuously until the start bit that starts the next transmission is sent.

3. The SCIF checks the SCFTDR transmit data at the timing for sending the stop bit. If data is present, the data is transferred from SCFTDR to SCTSR, the stop bit is sent, and then serial transmission of the next frame is started.

   If there is no transmit data, the TEND flag in SCSSR is set to 1, the stop bit is sent, and then the line goes to the mark state in which 1 is output continuously.

Port	Port Function (Related Module)	Other Function (Related Module)
C	PTC0 input/output (port)/PINT0 input (INTC)	$\overline{\text{MCS0}}$ output (BSC)
D	PTD7 input/output (port)	DACK1 output (DMAC)
D	PTD6 input (port)	$\overline{\text{DREQ1}}$ input (DMAC)
D	PTD5 input/output (port)	DACK0 output (DMAC)
D	PTD4 input (port)	$\overline{\text{DREQ0}}$ input (DMAC)
D	PTD3 input/output (port)	$\overline{\text{WAKEUP}}$ output (WTC)
D	PTD2 input/output (port)	$\overline{\text{RESETOUT}}$ output
D	PTD1 input/output (port)	DRAK0 output (DMAC)
D	PTD0 input/output (port)	DRAK1 output (DMAC)
E	PTE7 input/output (port)	$\overline{\text{AUDSYNC}}$ output (AUD)
E	PTE6 input/output (port)	—
E	PTE5 input/output (port)	$\overline{\text{CE2B}}$ output (PCMCIA)
E	PTE4 input/output (port)	$\overline{\text{CE2A}}$ output (PCMCIA)
E	PTE3 input/output (port)	—
E	PTE2 input/output (port)	$\overline{\text{RAS3U}}$ output (BSC)
E	PTE1 input/output (port)	—
E	PTE0 input/output (port)	TDO output (UDI)
F	PTF7 input (port)/PINT15 input (INTC)	$\overline{\text{TRST}}$ input (AUD, UDI)
F	PTF6 input (port)/PINT14 input (INTC)	TMS input (UDI)
F	PTF5 input (port)/PINT13 input (INTC)	TD1 input (UDI)
F	PTF4 input (port)/PINT12 input (INTC)	TCK input (UDI)
F	PTF3 input (port)/PINT11 input (INTC)	$\overline{\text{IRLS3}}$ input (INTC)
F	PTF2 input (port)/PINT10 input (INTC)	$\overline{\text{IRLS2}}$ input (INTC)
F	PTF1 input (port)/PINT9 input (INTC)	$\overline{\text{IRLS1}}$ input (INTC)
F	PTF0 input (port)/PINT8 input (INTC)	$\overline{\text{IRLS0}}$ input (INTC)
G	PTG7 input (port)	$\overline{\text{IOIS16}}$ input (PCMCIA)
G	PTG6 input (port)	$\overline{\text{ASEMD0}}$ input (AUD, UDI)
G	PTG5 input (port)	$\overline{\text{ASEBRKAK}}$ output (AUD)
G	PTG4 input (port)	CKIO2 output (CPG)
G	PTG3 input (port)	AUDATA3 output (AUD)
G	PTG2 input (port)	AUDATA2 output (AUD)

18.3.2 Port B Control Register (PBCR)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PB7 MD1	PB7 MD0	PB6 MD1	PB6 MD0	PB5 MD1	PB5 MD0	PB4 MD1	PB4 MD0	PB3 MD1	PB3 MD0	PB2 MD1	PB2 MD0	PB1 MD1	PB1 MD0	PB0 MD1	PB0 MD0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The port B control register (PBCR) is a 16-bit readable/writable register that selects the pin functions. PBCR is initialized to H'0000 by a power-on reset, but is not initialized by a manual reset, in standby mode, or in sleep mode.

Bits 15 and 14—PB7 Mode 1 and 0 (PB7MD1, PB7MD0)
Bits 13 and 12—PB6 Mode 1 and 0 (PB6MD1, PB6MD0)
Bits 11 and 10—PB5 Mode 1 and 0 (PB5MD1, PB5MD0)
Bits 9 and 8—PB4 Mode 1 and 0 (PB4MD1, PB4MD0)
Bits 7 and 6—PB3 Mode 1 and 0 (PB3MD1, PB3MD0)
Bits 5 and 4—PB2 Mode 1 and 0 (PB2MD1, PB2MD0)
Bits 3 and 2—PB1 Mode 1 and 0 (PB1MD1, PB1MD0)
Bits 1 and 0—PB0 Mode 1 and 0 (PB0MD1, PB0MD0)
These bits select the pin functions and perform input pull-up MOS control.

Bit (2n + 1)	Bit 2n		
PBnMD1	**PBnMD0**	**Pin Function**	
0	0	Other function (see table 18.1)	(Initial value)
0	1	Port output	
1	0	Port input (Pull-up MOS: on)	
1	1	Port input (Pull-up MOS: off)	

(n = 0 to 7)

19.1 Overview

The SH7709S has twelve 8-bit ports (ports A to L and SC). All port pins are multiplexed with other pin functions (the pin function controller (PFC) handles the selection of pin functions and pull-up MOS control). Each port has a data register which stores data for the pins.

19.2 Port A

Port A is an 8-bit input/output port with the pin configuration shown in figure 19.1. Each pin has an input pull-up MOS, which is controlled by the port A control register (PACR) in the PFC.

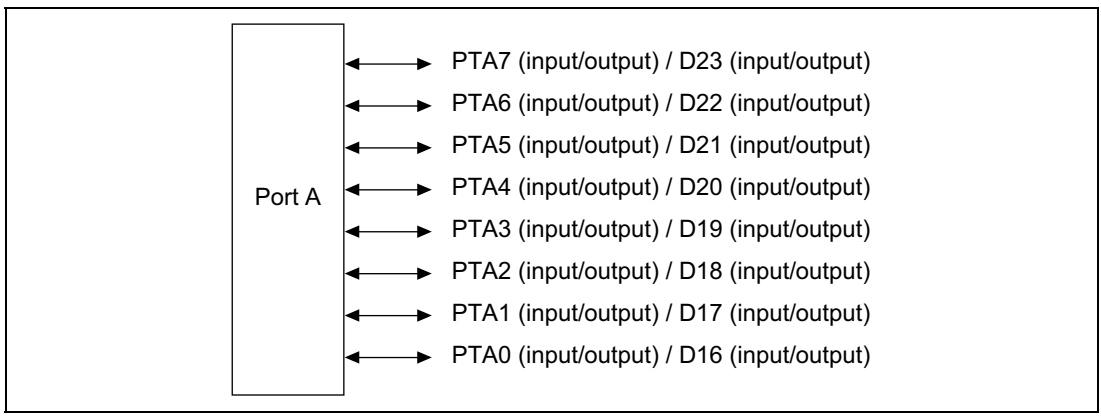


Figure 19.1 Port A

19.2.1 Register Description

Table 19.1 summarizes the port A register.

Table 19.1 Port A Register

Name	Abbreviation	R/W	Initial Value	Address	Access Size
Port A data register	PADR	R/W	H'00	H'04000120 (H'A4000120)*	8

Notes: This register is located in area 1 of physical space. Therefore, when the cache is on, either access this register from the P2 area of logical space or else make an appropriate setting using the MMU so that this register is not cached.

* When address translation by the MMU does not apply, the address in parentheses should be used.

Bit	Pin Name	I/O	Bit	Pin Name	I/O
277	D10	OUT	247	D12	Control
276	D9	OUT	246	D11	Control
275	D8	OUT	245	D10	Control
274	D7	OUT	244	D9	Control
273	D6	OUT	243	D8	Control
272	D5	OUT	242	D7	Control
271	D4	OUT	241	D6	Control
270	D3	OUT	240	D5	Control
269	D2	OUT	239	D4	Control
268	D1	OUT	238	D3	Control
267	D0	OUT	237	D2	Control
266	D31/PTB7	Control	236	D1	Control
265	D30/PTB6	Control	235	D0	Control
264	D29/PTB5	Control	234	$\overline{BS}$/PTK4	IN
263	D28/PTB4	Control	233	$\overline{WE2}$/DQMUL/$\overline{ICIORD}$/PTK6	IN
262	D27/PTB3	Control	232	$\overline{WE3}$/DQMUU/$\overline{ICIORD}$/PTK7	IN
261	D26/PTB2	Control	231	$\overline{AUDSYNC}$/PTE7	IN
260	D25/PTB1	Control	230	$\overline{CS2}$/PTK0	IN
259	D24/PTB0	Control	229	$\overline{CS3}$/PTK1	IN
258	D23/PTA7	Control	228	$\overline{CS4}$/PTK2	IN
257	D22/PTA6	Control	227	$\overline{CS5}$/$\overline{CE1A}$/PTK3	IN
256	D21/PTA5	Control	226	$\overline{CE2A}$/PTE4	IN
255	D20/PTA4	Control	225	$\overline{CE2B}$/PTE5	IN
254	D19/PTA3	Control	224	A0	OUT
253	D18/PTA2	Control	223	A1	OUT
252	D17/PTA1	Control	222	A2	OUT
251	D16/PTA0	Control	221	A3	OUT
250	D15	Control	220	A4	OUT
249	D14	Control	219	A5	OUT
248	D13	Control	218	A6	OUT

Bit	Pin Name	I/O	Bit	Pin Name	I/O
217	A7	OUT	187	$\overline{CS4}$/PTK2	OUT
216	A8	OUT	186	$\overline{CS5}$/$\overline{CE1A}$/PTK3	OUT
215	A9	OUT	185	$\overline{CS6}$/$\overline{CE1B}$	OUT
214	A10	OUT	184	$\overline{CE2A}$/PTE4	OUT
213	A11	OUT	183	$\overline{CE2B}$/PTE5	OUT
212	A12	OUT	182	A0	Control
211	A13	OUT	181	A1	Control
210	A14	OUT	180	A2	Control
209	A15	OUT	179	A3	Control
208	A16	OUT	178	A4	Control
207	A17	OUT	177	A5	Control
206	A18	OUT	176	A6	Control
205	A19	OUT	175	A7	Control
204	A20	OUT	174	A8	Control
203	A21	OUT	173	A9	Control
202	A22	OUT	172	A10	Control
201	A23	OUT	171	A11	Control
200	A24	OUT	170	A12	Control
199	A25	OUT	169	A13	Control
198	$\overline{BS}$/PTK4	OUT	168	A14	Control
197	$\overline{RD}$	OUT	167	A15	Control
196	$\overline{WE0}$/DQMLL	OUT	166	A16	Control
195	$\overline{WE1}$/DQMLU/$\overline{WE}$	OUT	165	A17	Control
194	$\overline{WE2}$/DQMUL/$\overline{ICIORD}$/ PTK6	OUT	164	A18	Control
193	$\overline{WE3}$/DQMUU/$\overline{ICIOWR}$/ PTK7	OUT	163	A19	Control
192	RD/$\overline{WR}$	OUT	162	A20	Control
191	$\overline{AUDSYNC}$/PTE7	OUT	161	A21	Control
190	$\overline{CS0}$/MCS0	OUT	160	A22	Control
189	$\overline{CS2}$/PTK0	OUT	159	A23	Control
188	$\overline{CS3}$/PTK1	OUT	158	A24	Control

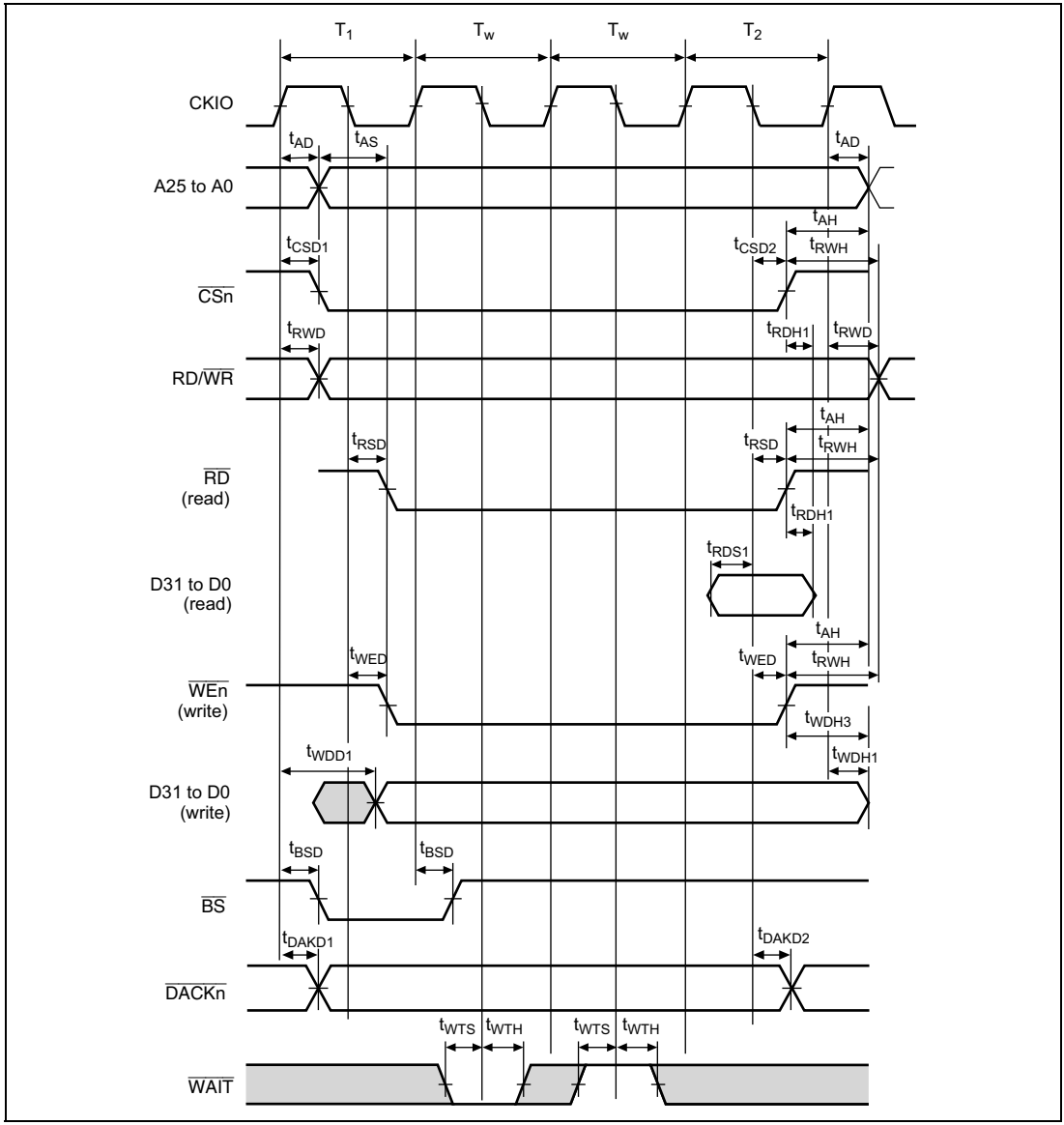
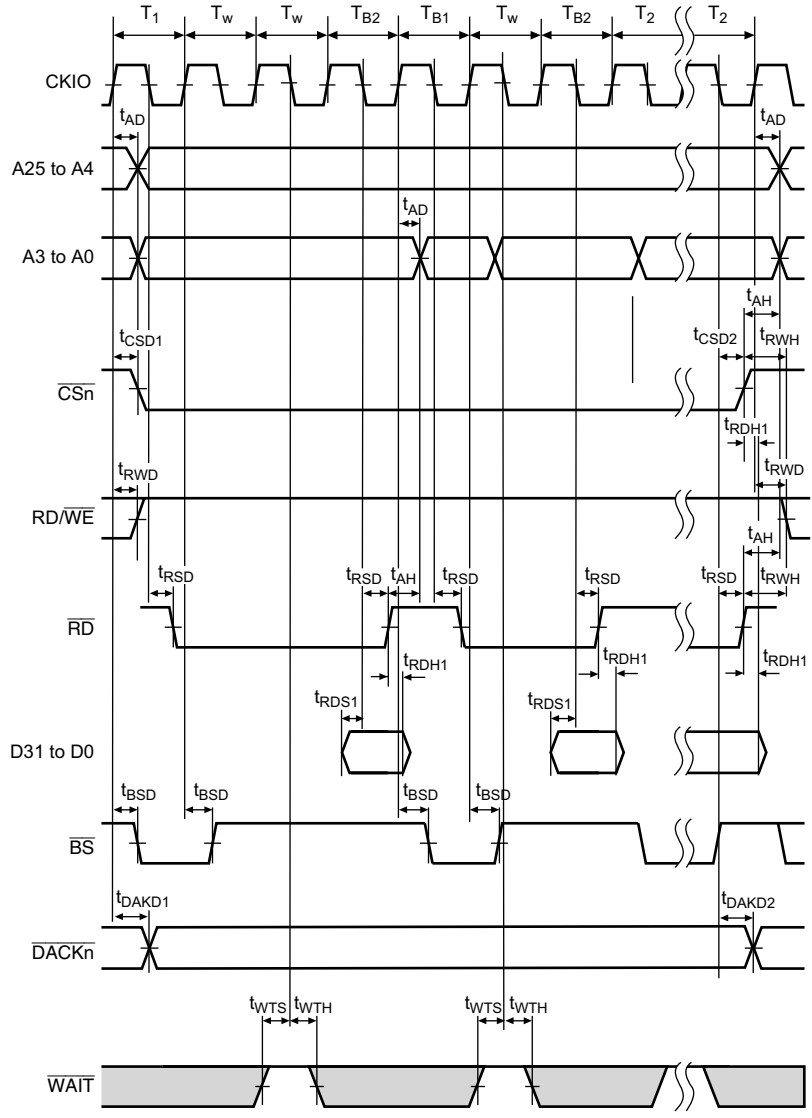


Figure 23.18 Basic Bus Cycle (External Wait, WAITSEL = 1)



Note: In the write cycle, the basic bus cycle is performed.

Figure 23.20 Burst ROM Bus Cycle (Two Waits)

23.3.11 Delay Time Variation Due to Load Capacitance

A graph (reference data) of the variation in delay time when a load capacitance greater than that stipulated (30 or 50 pF) is connected to this LSI's pins is shown below. The graph shown in figure 23.60 should be taken into consideration in the design process if the stipulated capacitance is exceeded in connecting an external device.

If the connected load capacitance exceeds the range shown in figure 23.60, the graph will not be a straight line.

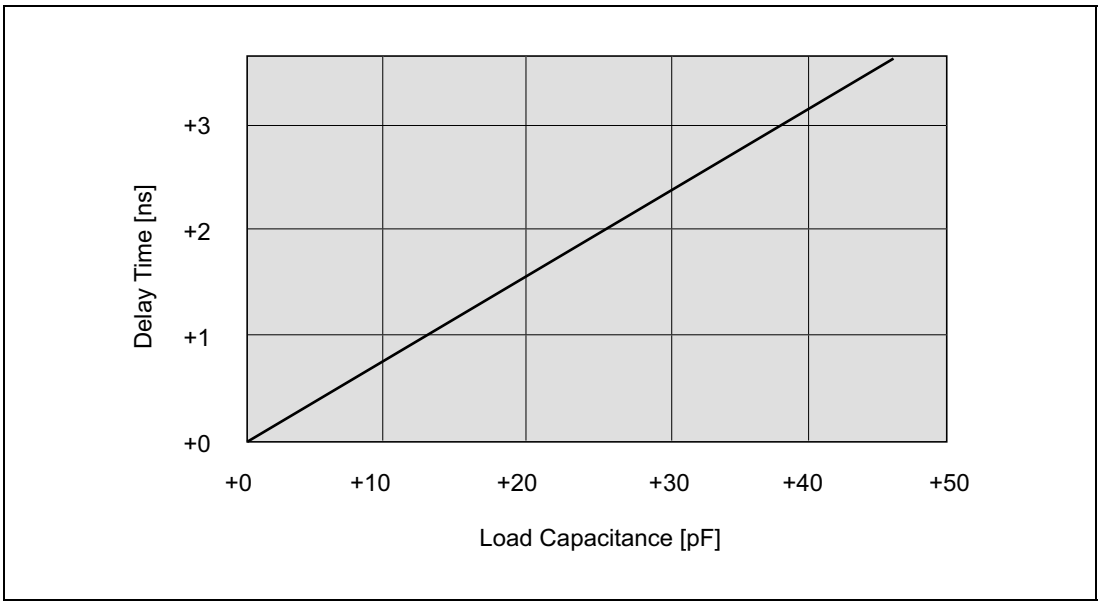


Figure 23.60 Load Capacitance vs. Delay Time