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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	SH-3
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	EBI/EMI, FIFO, IrDA, SCI, SmartCard
Peripherals	DMA, POR, WDT
Number of I/O	96
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.55V ~ 1.95V
Data Converters	A/D 8x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	208-LQFP
Supplier Device Package	208-LQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/d6417709sf100bv

Exception Type	Exception Event	Exception Code
General interrupt requests (cont)	External hardware interrupts (cont):	
	IRL3–IRL0 = 0010	H'240
	IRL3–IRL0 = 0011	H'260
	IRL3–IRL0 = 0100	H'280
	IRL3–IRL0 = 0101	H'2A0
	IRL3–IRL0 = 0110	H'2C0
	IRL3–IRL0 = 0111	H'2E0
	IRL3–IRL0 = 1000	H'300
	IRL3–IRL0 = 1001	H'320
	IRL3–IRL0 = 1010	H'340
	IRL3–IRL0 = 1011	H'360
	IRL3–IRL0 = 1100	H'380
	IRL3–IRL0 = 1101	H'3A0
	IRL3–IRL0 = 1110	H'3C0

4.2.5 Exception Request Masks

When the BL bit in SR is 0, exceptions and interrupts are accepted.

If a general exception event occurs when the BL bit in SR is 1, the CPU's internal registers are set to their post-reset state, other module registers retain their contents prior to the general exception, and a branch is made to the same address (H'A0000000) as for a reset.

If a general interrupt occurs when BL = 1, the request is masked (held pending) and not accepted until the BL bit is cleared to 0 by software. For reentrant exception handling, SPC and SSR must be saved and the BL bit in SR cleared to 0.

4.2.6 Returning from Exception Handling

The RTE instruction is used to return from exception handling. When RTE is executed, the SPC value is set in PC, and the SSR value in SR, and the return from exception handling is performed by branching to the SPC address.

If SPC and SSR have been saved in external memory, set the BL bit in SR to 1, then restore SPC and SSR, and issue an RTE instruction.

Bits 5 and 4—IRQ2 Sense Select (IRQ21S, IRQ20S): Select whether the interrupt signal to the IRQ2 pin is detected at the rising edge, at the falling edge, or at the low level.

Bit 5: IRQ21S	Bit 4: IRQ20S	Description
0	0	An interrupt request is detected at IRQ2 input falling edge (Initial value)
	1	An interrupt request is detected at IRQ2 input rising edge
1	0	An interrupt request is detected at IRQ2 input low level
	1	Reserved

Bits 3 and 2—IRQ1 Sense Select (IRQ11S, IRQ10S): Select whether the interrupt signal to the IRQ1 pin is detected at the rising edge, at the falling edge, or at the low level.

Bit 3: IRQ11S	Bit 2: IRQ10S	Description
0	0	An interrupt request is detected at IRQ1 input falling edge (Initial value)
	1	An interrupt request is detected at IRQ1 input rising edge
1	0	An interrupt request is detected at IRQ1 input low level
	1	Reserved

Bits 1 and 0—IRQ0 Sense Select (IRQ01S, IRQ00S): Select whether the interrupt signal to the IRQ0 pin is detected at the rising edge, at the falling edge, or at the low level.

Bit 1: IRQ01S	Bit 0: IRQ00S	Description
0	0	An interrupt request is detected at IRQ0 input falling edge (Initial value)
	1	An interrupt request is detected at IRQ0 input rising edge
1	0	An interrupt request is detected at IRQ0 input low level
	1	Reserved

7.2.2 Break Address Mask Register A (BAMRA)

BAMRA is a 32-bit read/write register. BAMRA specifies bits masked in the break address specified by BARA. A power-on reset initializes BAMRA to H'00000000.

Bit:	31	30	29	28	27	26	25	24
	BAMA31	BAMA30	BAMA29	BAMA28	BAMA27	BAMA26	BAMA25	BAMA24
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	23	22	21	20	19	18	17	16
	BAMA23	BAMA22	BAMA21	BAMA20	BAMA19	BAMA18	BAMA17	BAMA16
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8
	BAMA15	BAMA14	BAMA13	BAMA12	BAMA11	BAMA10	BAMA9	BAMA8
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	7	6	5	4	3	2	1	0
	BAMA7	BAMA6	BAMA5	BAMA4	BAMA3	BAMA2	BAMA1	BAMA0
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 31 to 0—Break Address Mask Register A31 to A0 (BAMA31 to BAMA0): Specifies bits masked in the channel A break address bits specified by BARA (BAA31–BAA0).

Bits 31 to 0: BAMAn	**Description**
0	Break address bit BAAn of channel A is included in the break condition (Initial value)
1	Break address bit BAAn of channel A is masked and is not included in the break condition

n = 31 to 0

7.2.11 Branch Source Register (BRSR)

BRSR is a 32-bit read register. BRSR stores the last fetched address before branch and the pointer (3 bits) which indicates the number of cycles from fetch to execution for the last executed instruction. BRSR has the flag bit that is set to 1 when branch occurs. This flag bit is cleared to 0, when BRSR is read and also initialized by power-on resets or manual resets. Other bits are not initialized by reset. Eight BRSR registers have queue structure and a stored register is shifted every branch.

Bit:	31	30	29	28	27	26	25	24
	SVF	PID2	PID1	PID0	BSA27	BSA26	BSA25	BSA24
Initial value:	0	*	*	*	*	*	*	*
R/W:	R	R	R	R	R	R	R	R

Bit:	23	22	21	20	19	18	17	16
	BSA23	BSA22	BSA21	BSA20	BSA19	BSA18	BSA17	BSA16
Initial value:	*	*	*	*	*	*	*	*
R/W:	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8
	BSA15	BSA14	BSA13	BSA12	BSA11	BSA10	BSA9	BSA8
Initial value:	*	*	*	*	*	*	*	*
R/W:	R	R	R	R	R	R	R	R

Bit:	7	6	5	4	3	2	1	0
	BSA7	BSA6	BSA5	BSA4	BSA3	BSA2	BSA1	BSA0
Initial value:	*	*	*	*	*	*	*	*
R/W:	R	R	R	R	R	R	R	R

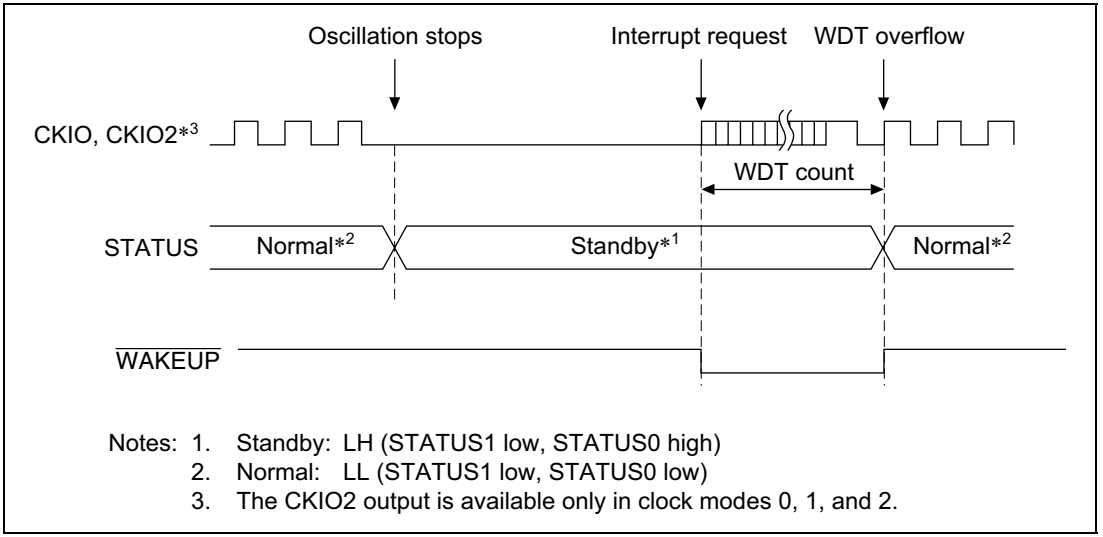
Note: * Undefined value

Bit 31—BRSR Valid Flag (SVF): Indicates whether the address and the pointer by which the branch source address can be calculated. When a branch source address is fetched, this flag is set to 1. This flag is cleared to 0 in reading BRSR.

Bit 31: SVF	Description
0	The value of BRSR register is invalid
1	The value of BRSR register is valid

8.6.2 Timing for Canceling Standby

Standby to Interrupt



Notes: 1. Standby: LH (STATUS1 low, STATUS0 high)
2. Normal: LL (STATUS1 low, STATUS0 low)
3. The CKIO2 output is available only in clock modes 0, 1, and 2.

Figure 8.4 Standby to Interrupt STATUS Output

9.5 Changing the Frequency

The frequency of the internal clock and peripheral clock can be changed either by changing the multiplication ratio of PLL circuit 1 or by changing the division ratios of dividers 1 and 2. All of these are controlled by software through the frequency control register. The methods are described below. To the FRQCR register, do not set values other than those given in table 9.4.

9.5.1 Changing the Multiplication Rate

A PLL settling time is required when the multiplication rate of PLL circuit 1 is changed. The on-chip WDT counts the settling time.

1. In the initial state, the multiplication rate of PLL circuit 1 is 1.
2. Set a value that will become the specified oscillation settling time in the WDT and stop the WDT. The following must be set:
   WTCSR register TME bit = 0: WDT stops
   WTCSR register CKS2–CKS0 bits: Division ratio of WDT count clock
   WTCNT counter: Initial counter value
3. Set the desired value in the STC2 to STC0 bits. The division ratio can also be set in the IFC2–IFC0 bits and PFC2–PFC0 bits.
4. The processor pauses internally and the WDT starts incrementing. In clock modes 0–2 and 7, the internal and peripheral clocks both stop. (except for the peripheral clock supplied to the WDT)
5. Supply of the clock that has been set begins at WDT count overflow, and the processor begins operating again. The WDT stops after it overflows.

When the following three conditions are all met, FRQCR should not be changed while a DMAC transfer is in progress.

- Bits IFC2 to IFC0 are changed.
- STC2 to STC0 are not changed.
- The clock ratio of Iϕ (on-chip clock) to Bϕ (bus clock) after the change is other than 1:1.

9.5.2 Changing the Division Ratio

The WDT will not count unless the multiplication ratio is changed simultaneously.

1. In the initial state, IFC2–IFC0 = 000 and PFC2–PFC0 = 010.
2. Set the IFC2, IFC1, IFC0, PFC2, PFC1, and PFC0 bits to the new division ratio. The values that can be set are limited by the clock mode and the multiplication ratio of PLL circuit 1. Note that if the wrong value is set, the processor will malfunction.
3. The clock is immediately supplied at the new division ratio.

9.7 WDT Registers

9.7.1 Watchdog Timer Counter (WTCNT)

The watchdog timer counter (WTCNT) is an 8-bit readable/writable counter that increments on the selected clock. WTCNT differs from other registers in that it is more difficult to write to. See section 9.7.3, Notes on Register Access, for details. When an overflow occurs, it generates a reset in watchdog timer mode and an interrupt in interval time mode. Its address is H'FFFFFF84. The WTCNT counter is initialized to H'00 only by a power-on reset through the $\overline{\text{RESETP}}$ pin. Use word access to write to the WTCNT counter, with H'5A in the upper byte. Use byte access to read WTCNT.

Bit:	7	6	5	4	3	2	1	0
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

9.7.2 Watchdog Timer Control/Status Register (WTCSR)

The watchdog timer control/status register (WTCSR) is an 8-bit readable/writable register composed of bits to select the clock used for the count, bits to select the timer mode, and overflow flags. WTCSR differs from other registers in that it is more difficult to write to. See section 9.7.3, Notes on Register Access, for details. Its address is H'FFFFFF86. The WTCSR register is initialized to H'00 only by a power-on reset through the $\overline{\text{RESETP}}$ pin. When a WDT overflow causes an internal reset, WTCSR retains its value. When used to count the clock settling time for canceling a standby, it retains its value after counter overflow. Use word access to write to the WTCSR counter, with H'A5 in the upper byte. Use byte access to read WTCSR.

Bit:	7	6	5	4	3	2	1	0
	TME	WT/$\overline{\text{IT}}$	RSTS	WOVF	IOVF	CKS2	CKS1	CKS0
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7—Timer Enable (TME): Starts and stops timer operation. Clear this bit to 0 when using the WDT in standby mode or when changing the clock frequency.

Bit 7: TME	Description
0	Timer disabled: Count-up stops and WTCNT value is retained (Initial value)
1	Timer enabled

Bits 11, 7, and 6—Area 5 Address $\overline{OE}$/$\overline{WE}$ Assert Delay (A5TED2, A5TED1, A5TED0): Specify the delay time from address output to $\overline{OE}$/$\overline{WE}$ assertion for the PCMCIA interface connected to area 5.

Bit 11: A5TED2	Bit 7: A5TED1	Bit 6: A5TED0	Description	
0	0	0	0.5-cycle delay	(Initial value)
		1	1.5-cycle delay	
	1	0	2.5-cycle delay	
		1	3.5-cycle delay	
1	0	0	4.5-cycle delay	
		1	5.5-cycle delay	
	1	0	6.5-cycle delay	
		1	7.5-cycle delay	

Bits 10, 5, and 4—Area 6 Address $\overline{OE}$/$\overline{WE}$ Assert Delay (A6TED2, A6TED1, A6TED0): The A6TED bits specify the delay time from address output to $\overline{OE}$/$\overline{WE}$ assertion for the PCMCIA interface connected to area 6.

Bit 10: A6TED2	Bit 5: A6TED1	Bit 4: A6TED0	Description	
0	0	0	0.5-cycle delay	(Initial value)
		1	1.5-cycle delay	
	1	0	2.5-cycle delay	
		1	3.5-cycle delay	
1	0	0	4.5-cycle delay	
		1	5.5-cycle delay	
	1	0	6.5-cycle delay	
		1	7.5-cycle delay	

Bus Width	Memory Type	Setting AMX 3	AMX 2	AMX 1	AMX 0	Output Timing	External Address Pins A1 to A8	A9	A10	A11	A12	A13	A14	A15	A16
	2M × 16bits × 4banks[*2]	0	1	0	1	Column address	A1 to A8	A9	A10	L/H[*3]	A12	A22[*4]	A23[*4]	A24	
						Row address	A10 to A17	A18	A19	A20	A21	A22[*4]	A23[*4]	A24	
	1M × 16bits × 4banks[*2]	0	1	0	0	Column address	A1 to A8	A9	A10	L/H[*3]	A12	A21[*4]	A22[*4]	A15	
						Row address	A 9 to A16	A17	A18	A19	A20	A21[*4]	A22[*4]	A23	
	2M × 8bits × 4banks[*2]	0	1	0	1	Column address	A1 to A8	A9	A10	L/H[*3]	A12	A22[*4]	A23[*4]	A24	
						Row address	A10 to A17	A18	A19	A20	A21	A22[*4]	A23[*4]	A24	

Notes: 1. Only RAL3L or CASL is output.

2. When addresses are upper 32 Mbytes, $\overline{\text{RAS3U}}$ or $\overline{\text{CASU}}$ is output.
   When addresses are lower 32 Mbytes, $\overline{\text{RAS3L}}$ or $\overline{\text{CASL}}$ is output.
3. L/H is a bit used in the command specification; it is fixed at L or H according to the access mode.
4. Bank address specification

independently for areas 2 and 3 by means of bits A2W1 and A2W0 or A3W1 and A3W0 in WCR2. This number of cycles corresponds to the number of synchronous DRAM CAS latency cycles.

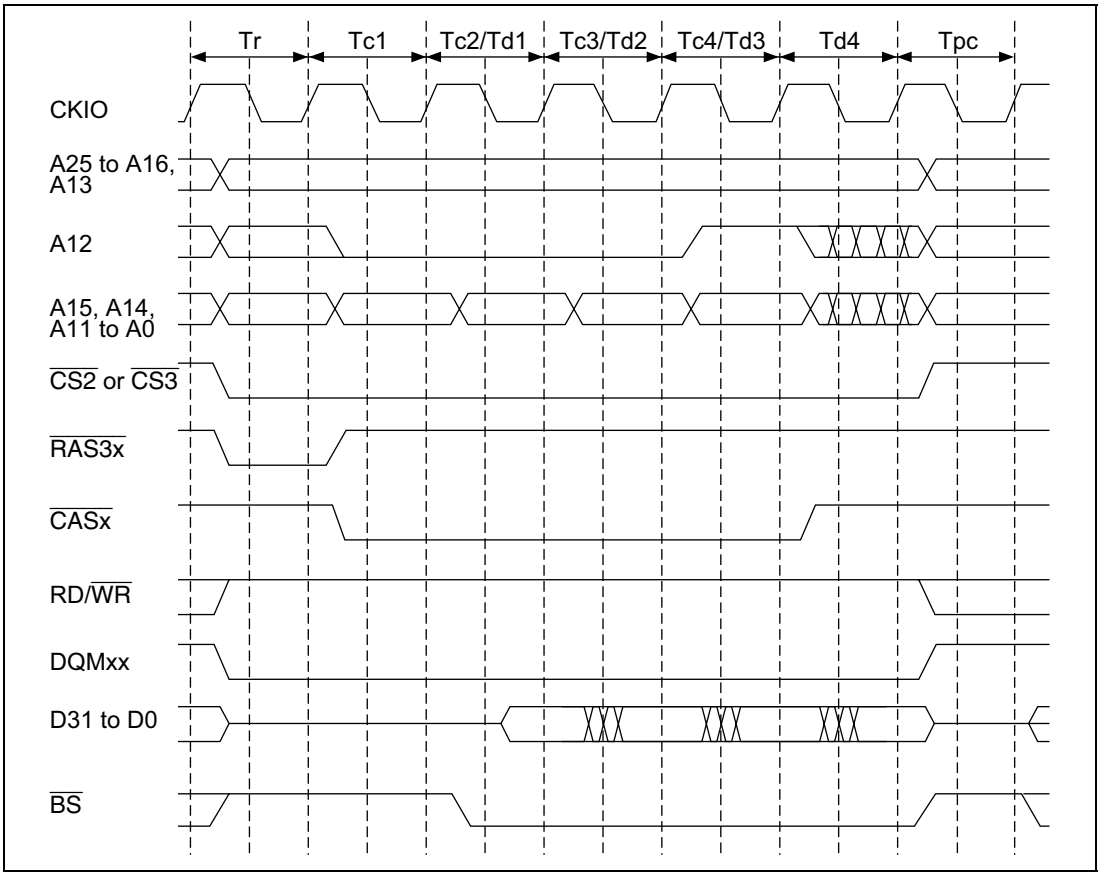


Figure 10.14 Basic Timing for Synchronous DRAM Burst Read

10.3.10 $\overline{\text{MCS[0]}}$ to $\overline{\text{MCS[7]}}$ Pin Control

The SH7709S is provided with pins $\overline{\text{MCS[0]}}$–$\overline{\text{MCS[7]}}$ as dedicated $\overline{\text{CS}}$ pins for the ROM connected to area 0 or 2. Assertion of $\overline{\text{MCS[0]}}$–$\overline{\text{MCS[7]}}$ is controlled by settings in MCSCR0–MCSCR7. This enables 32-, 64-, 128-, or 256-Mbit memory to be connected to area 0 or area 2. However, only CS2/0 = 0 (area 0) should be used for MCSCR0. Table 10.15 shows MCSCR0–MCSCR7 settings and $\overline{\text{MCS[0]}}$–$\overline{\text{MCS[7]}}$ assertion conditions.

As the $\overline{\text{MCS[0]}}$–$\overline{\text{MCS[7]}}$ pins are multiplexed as the PTC0–PTC7 pins, when using these pins as $\overline{\text{MCS[0]}}$–$\overline{\text{MCS[7]}}$, the corresponding bits in the PCCR register should be set to “other function.”

When CS2/0 = 0 in the MCSCR0 and when the PTC0 pin is switched to $\overline{\text{MCS[0]}}$ (when PCOMD1–PCOMD0 are set to “other function”), the $\overline{\text{CS0}}$ pin is also switched to $\overline{\text{MCS[0]}}$.

As port register writes operate on the peripheral clock, they take time compared with instruction execution by the CPU operating on the high-speed internal clock. Therefore, if an instruction that accesses $\overline{\text{MCS[1]}}$ to $\overline{\text{MCS[7]}}$ is located several instructions after an instruction that switches port C to $\overline{\text{MCS}}$, the switch from PTC[n] to $\overline{\text{MCSn}}$ and from $\overline{\text{CS0}}$ to $\overline{\text{MCS[0]}}$ may not be performed correctly.

To prevent this problem, the following switching procedure should be used.

- When the program runs with cache on

(1) To switch port C to $\overline{\text{MCS}}$, set the corresponding bits in the PCCR register to 00 ("other function").

(2) Read the PCCR register and check whether the set value is read. Repeat until the set value is read.

(3) Perform a dummy read from non-cacheable CS0 space (e.g. address H'A0000000). This will result in an access to the CS0 space, and immediately afterward, CS0 will be switched to $\overline{\text{MCS[0]}}$, and port C[n] will be switched to $\overline{\text{MCS[n]}}$.

(4) Access can now be made to the $\overline{\text{MCS[1]}}$ to $\overline{\text{MCS[7]}}$ spaces.

- When the program runs in $\overline{\text{MCS[0]}}$ space with cache off

(1) Set the PCCR register as in (1) above.

(2) Place at least three NOP instructions after the instruction in (1). As a result, when the PCCR register is rewritten, an access to the CS0 space will be generated, and immediately afterward, CS0 will be switched to $\overline{\text{MCS[0]}}$, and port C[n] will be switched to $\overline{\text{MCS[n]}}$.

(3) Access can now be made to the $\overline{\text{MCS[1]}}$ to $\overline{\text{MCS[7]}}$ spaces.

Table 10.15 MCSCRx Settings and $\overline{\text{MCS[x]}}$ Assertion Conditions (x: 0–7)

MCSCRx Settings							$\overline{\text{MCS[x]}}$ Assertion Conditions			
CS2/0	CAP1	CAP0	A25	A24	A23	A22	$\overline{\text{CS0}}$	$\overline{\text{CS2}}$	Address Bus A [25:0]	Notes
0	1	1	0	—	—	—	L	H	H'0000000 to H'1FFFFFF	256-Mbit ROM
			1	—	—	—	L	H	H'2000000 to H'3FFFFFF	
	1	0	0	0	—	—	L	H	H'0000000 to H'0FFFFFF	128-Mbit ROM
			0	1	—	—	L	H	H'1000000 to H'1FFFFFF	
			1	0	—	—	L	H	H'2000000 to H'2FFFFFF	
			1	1	—	—	L	H	H'3000000 to H'3FFFFFF	
	0	1	0	0	0	—	L	H	H'0000000 to H'07FFFFF	64-Mbit ROM
			0	0	1	—	L	H	H'0800000 to H'0FFFFFF	
			0	1	0	—	L	H	H'1000000 to H'17FFFFF	
			0	1	1	—	L	H	H'1800000 to H'1FFFFFF	
			1	0	0	—	L	H	H'2000000 to H'27FFFFF	
			1	0	1	—	L	H	H'2800000 to H'2FFFFFF	
			1	1	0	—	L	H	H'3000000 to H'37FFFFF	
			1	1	1	—	L	H	H'3800000 to H'3FFFFFF	
	0	0	0	0	0	0	L	H	H'0000000 to H'03FFFFF	32-Mbit ROM
			0	0	0	1	L	H	H'0400000 to H'07FFFFF	
			0	0	1	0	L	H	H'0800000 to H'0BFFFFF	
			0	0	1	1	L	H	H'0C00000 to H'0FFFFFF	
			0	1	0	0	L	H	H'1000000 to H'13FFFFF	
			0	1	0	1	L	H	H'1400000 to H'17FFFFF	
			0	1	1	0	L	H	H'1800000 to H'1BFFFFF	
			0	1	1	1	L	H	H'1C00000 to H'1FFFFFF	
			1	0	0	0	L	H	H'2000000 to H'23FFFFF	
			1	0	0	1	L	H	H'2400000 to H'27FFFFF	
			1	0	1	0	L	H	H'2800000 to H'2BFFFFF	
			1	0	1	1	L	H	H'2C00000 to H'2FFFFFF	
			1	1	0	0	L	H	H'3000000 to H'33FFFFF	
			1	1	0	1	L	H	H'3400000 to H'37FFFFF	
			1	1	1	0	L	H	H'3800000 to H'3BFFFFF	
			1	1	1	1	L	H	H'3C00000 to H'3FFFFFF	

14.2.8 SC Port Control Register (SCPCR)/SC Port Data Register (SCPDR)

The SC port control register (SCPCR) and SC port data register (SCPDR) control I/O and data for the port pins multiplexed with the serial communication interface (SCI) pins.

SCPCR settings are used to perform I/O control, to enable data written in SCPDR to be output to the TxD pin, and input data to be read from the RxD pin, and to control serial transmission/reception breaks.

It is also possible to read data on the SCK pin, and write output data.

SCPCR

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SCP7 MD1	SCP7 MD0	SCP6 MD1	SCP6 MD0	SCP5 MD1	SCP5 MD0	SCP4 MD1	SCP4 MD0	SCP3 MD1	SCP3 MD0	SCP2 MD1	SCP2 MD0	SCP1 MD1	SCP1 MD0	SCP0 MD1	SCP0 MD0
Initial value:	1	0	1	0	1	0	0	0	1	0	0	0	1	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

SCPDR

Bit:	7	6	5	4	3	2	1	0
	SCP7DT	SCP6DT	SCP5DT	SCP4DT	SCP3DT	SCP2DT	SCP1DT	SCP0DT
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

SCI pin I/O and data control are performed by bits 3–0 of SCPCR and bits 1 and 0 of SCPDR.

SCPCR Bits 3 and 2—Serial Clock Port I/O (SCP1MD1, SCP1MD0): Specify serial port SCK pin I/O. When the SCK pin is actually used as a port I/O pin, clear the C/$\overline{A}$ bit in SCSMR and bits CKE1 and CKE0 in SCSCR to 0.

Bit 3: SCP1MD1	Bit 2: SCP1MD0	Description
0	0	SCP1DT bit value is not output to SCK pin
0	1	SCP1DT bit value is output to SCK pin
1	0	SCK pin value is read from SCP1DT bit
1	1	(Initial values: 1 and 0)

	Pϕ (MHz)											
	14.7456			16			19.6608			20		
Bit Rate (bits/s)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
110	3	64	0.70	3	70	0.03	3	86	0.31	3	88	–0.25
150	2	191	0.00	2	207	0.16	2	255	0.00	3	64	0.16
300	2	95	0.00	2	103	0.16	2	127	0.00	2	129	0.16
600	1	191	0.00	1	207	0.16	1	255	0.00	2	64	0.16
1200	1	95	0.00	1	103	0.16	1	127	0.00	1	129	0.16
2400	0	191	0.00	0	207	0.16	0	255	0.00	1	64	0.16
4800	0	95	0.00	0	103	0.16	0	127	0.00	0	129	0.16
9600	0	47	0.00	0	51	0.16	0	63	0.00	0	64	0.16
19200	0	23	0.00	0	25	0.16	0	31	0.00	0	32	–1.36
31250	0	14	–1.70	0	15	0.00	0	19	–1.70	0	19	0.00
38400	0	11	0.00	0	12	0.16	0	15	0.00	0	15	1.73

	Pϕ (MHz)											
	24			24.576			28.7			30		
Bit Rate (bits/s)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
110	3	106	–0.44	3	108	0.08	3	126	0.31	3	132	0.13
150	3	77	0.16	3	79	0.00	3	92	0.46	3	97	–0.35
300	2	155	0.16	2	159	0.00	2	186	–0.08	2	194	0.16
600	2	77	0.16	2	79	0.00	2	92	0.46	2	97	–0.35
1200	1	155	0.16	1	159	0.00	1	186	–0.08	1	194	0.16
2400	1	77	0.16	1	79	0.00	1	92	0.46	1	97	–0.35
4800	0	155	0.16	0	159	0.00	0	186	–0.08	0	194	–1.36
9600	0	77	0.16	0	79	0.00	0	92	0.46	0	97	–0.35
19200	0	38	0.16	0	39	0.00	0	46	–0.61	0	48	–0.35
31250	0	23	0.00	0	24	–1.70	0	28	–1.03	0	29	0.00
38400	0	19	–2.34	0	19	0.00	0	22	1.55	0	23	1.73

14.3.2 Operation in Asynchronous Mode

In asynchronous mode, each transmitted or received character begins with a start bit and ends with a stop bit. Serial communication is synchronized one character at a time.

The transmitting and receiving sections of the SCI are independent, so full duplex communication is possible. The transmitter and receiver are both double buffered, so data can be written and read while transmitting and receiving are in progress, enabling continuous transmitting and receiving.

Figure 14.5 shows the general format of asynchronous serial communication. In asynchronous serial communication, the communication line is normally held in the mark (high) state. The SCI monitors the line and starts serial communication when the line goes to the space (low) state, indicating a start bit. One serial character consists of a start bit (low), data (LSB first; starting from the lowerest bit), parity bit (high or low), and stop bit (high), in that order.

When receiving in asynchronous mode, the SCI synchronizes at the falling edge of the start bit. The SCI samples each data bit on the eighth pulse of a clock with a frequency 16 times the bit rate. Receive data is latched at the center of each bit.

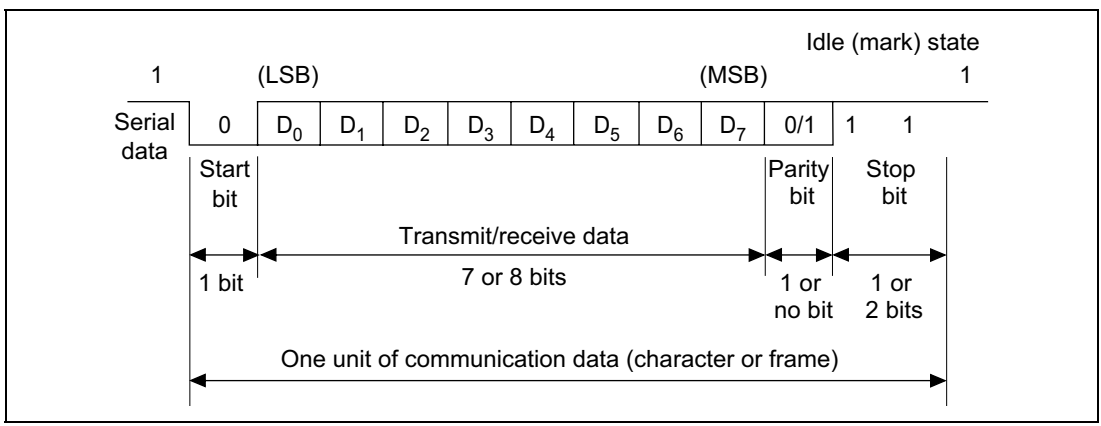
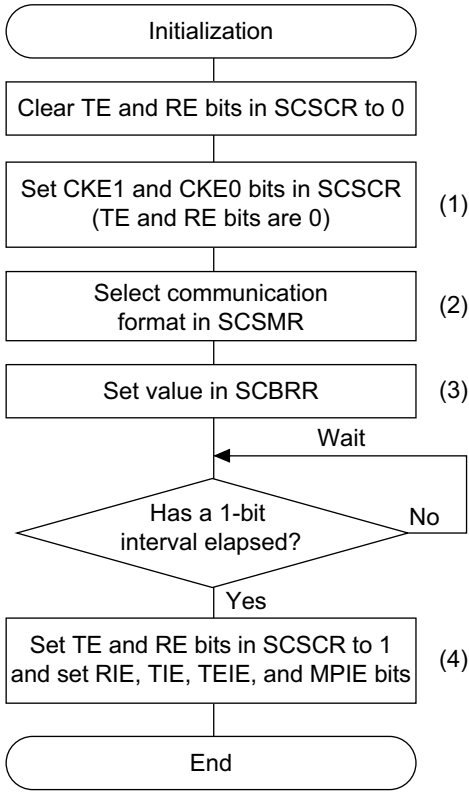


Figure 14.5 Example of Data Format in Asynchronous Communication (8-Bit Data with Parity and Two Stop Bits)



Note: Numbers in parentheses refer to steps in the preceding procedure description.

Figure 14.7 Sample Flowchart for SCI Initialization

Transmitting Serial Data (Asynchronous Mode): Figure 14.8 shows a sample flowchart for transmitting serial data. The procedure for transmitting serial data is:

1. SCI status check and transmit data write: Read the serial status register (SCSSR), check that the TDRE bit is 1, then write transmit data in the transmit data register (SCTDR) and clear TDRE to 0.
2. To continue transmitting serial data: Read the TDRE bit to check whether it is safe to write (if it reads 1); if so, write data in SCTDR, then clear TDRE to 0.
3. To output a break at the end of serial transmission: Set the port SC data register (SCPDR) and port SC control register (SCPCR), then clear the TE bit to 0 in the serial control register (SCSCR). For SCPCR and SCPDR settings, see section 14.2.8, SC Port Control Register (SCPCR)/SC Port Data Register (SCPDR).

17.3.3 Receiving

Received 3/16 IR frame bit-width pulses are demodulated and converted to a UART frame, as shown in figure 17.5.

Demodulation to 0 is performed for pulse output, and demodulation to 1 is performed for no pulse output.

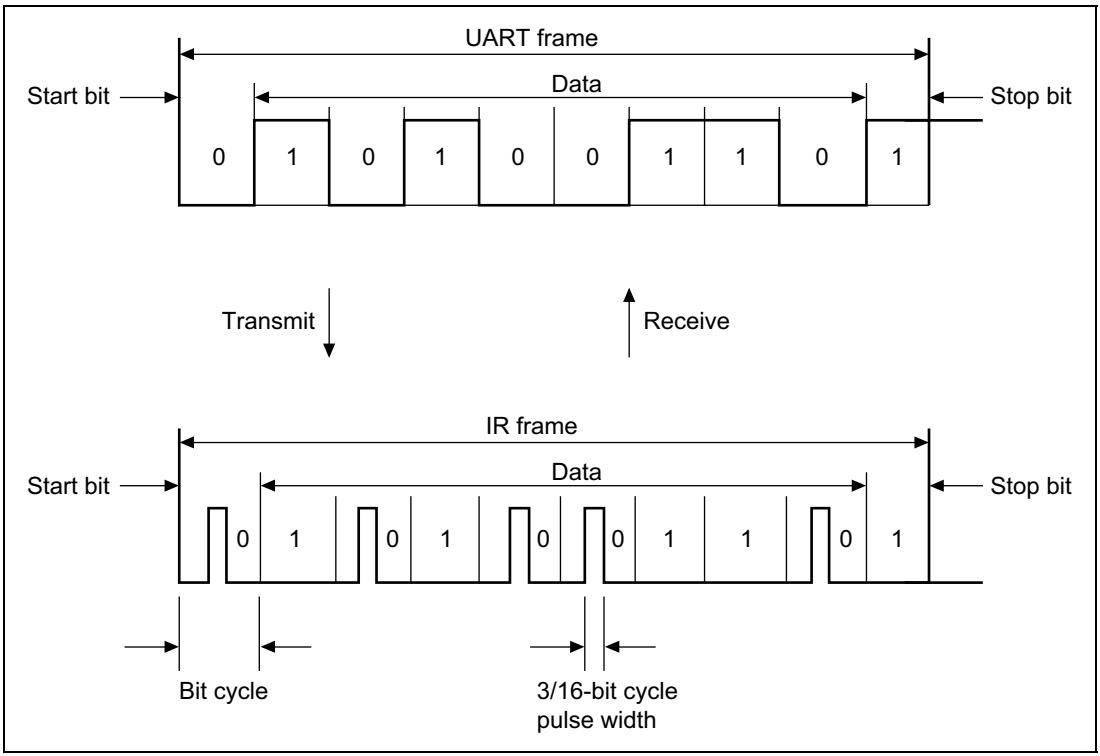


Figure 17.5 Transmit/Receive Operation

20.4.2 Multi Mode (MULTI = 1, SCN = 0)

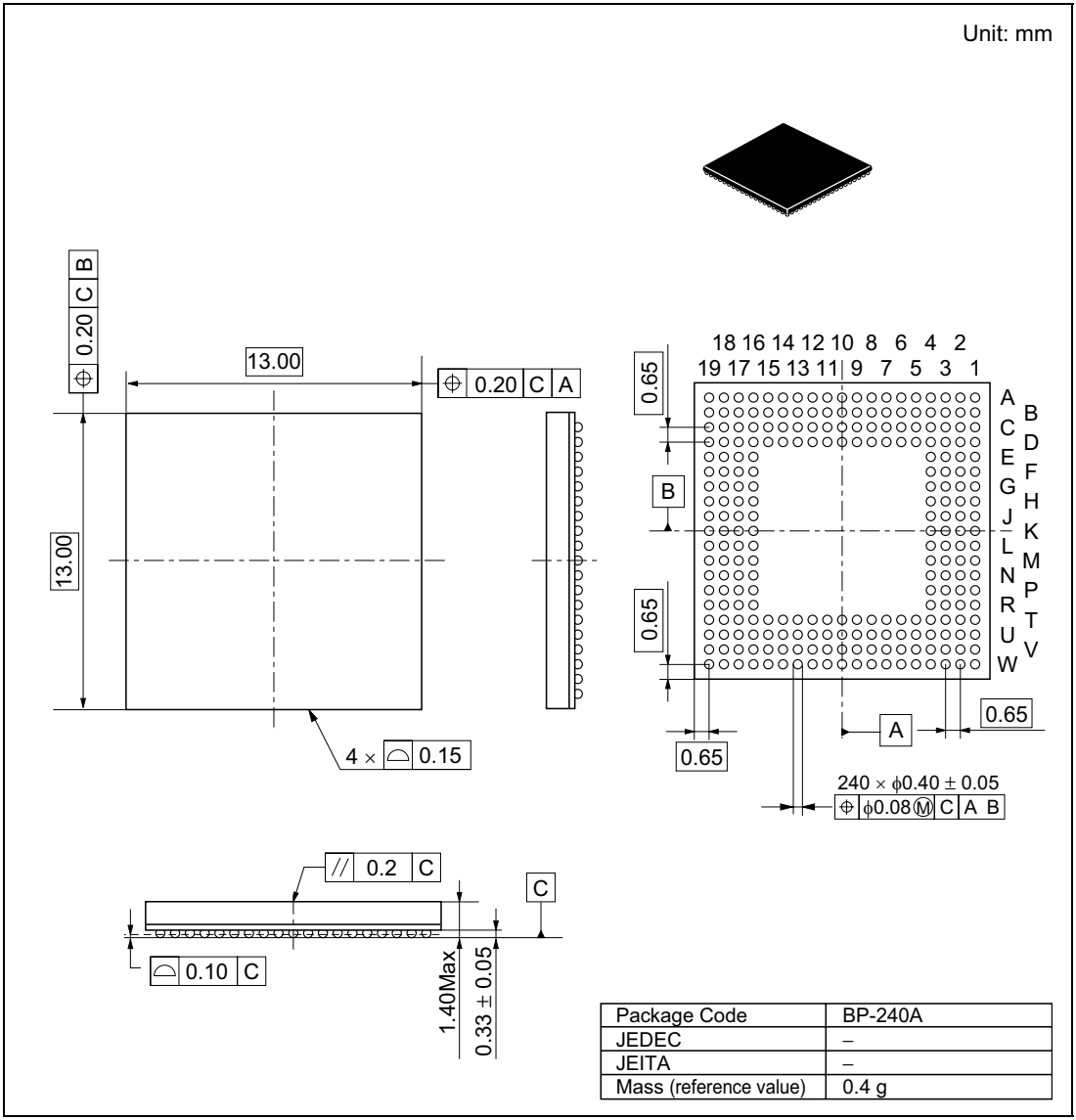
Multi mode should be selected when performing A/D conversions on one or more channels. When the ADST bit is set to 1 by software or external trigger input, A/D conversion starts on the first channel in the group (AN0 when CH2 = 0, AN4 when CH2 = 1). When two or more channels are selected, after conversion of the first channel ends, conversion of the second channel (AN1 or AN5) starts immediately. When A/D conversions end on the selected channels, the ADST bit is cleared to 0. The conversion results are transferred for storage into the A/D data registers corresponding to the channels.

When the mode or analog input channel selection must be changed during A/D conversion, to prevent incorrect operation, first clear the ADST bit to 0 in ADCSR to halt A/D conversion. After making the necessary changes, set the ADST bit to 1. A/D conversion will start again from the first channel in the group. The ADST bit can be set at the same time as the mode or channel selection is changed.

Typical operations when three channels in group 0 (AN0 to AN2) are selected in scan mode are described next. Figure 20.4 shows a timing diagram for this example.

1. Multi mode is selected (MULTI = 1, SCN = 0), channel group 0 is selected (CH2 = 0), analog input channels AN0 to AN2 are selected (CH1 = 1, CH0 = 0), and A/D conversion is started (ADST = 1).
2. When A/D conversion of the first channel (AN0) is completed, the result is transferred into ADDRA. Next, conversion of the second channel (AN1) starts automatically.
3. Conversion proceeds in the same way through the third channel (AN2).
4. When conversion of all selected channels (AN0 to AN2) is completed, the ADF flag is set to 1 and ADST bit is cleared to 0. If the ADIE bit is set to 1, an ADI interrupt is requested at this time.

Pin	Pin No. (FP-208C, FP-208E)	Pin No. (BP-240A)	I/O	Function
A25 to A0	86, 84, 82, 80, 78 to 72, 70, 68 to 60, 58, 56 to 53	V12, T12, V11, W10, V10, U9, T9, V9, W9, T8, U8, W8, U7, V7, W7, T6, U6, V6, W6, T5, U5, W5, W4, V5, V3, V4	O	Address bus
D31 to D24/ PTB[7] to PTB[0]	13 to 18, 20, 22	F4, G1, G2, G3, G4, H1, H3, J1	I/O	Data bus / I/O port
D23 to D16/ PTA[7] to PTA[0]	23 to 26, 28, 30 to 32	J2, J4, J3, K2, K1, L2, L1, M4	I/O	Data bus / I/O port
D15 to D0	34, 36 to 44, 46, 48 to 52	M2, N4, N3, N2, N1, P4, P3, P2, P1, R4, T4, T3, T1, R2, U2,T2	I/O	Data bus
$\overline{\text{MCS}}$[7:0]/ PTC[7:0]/ PINT[7:0]	177 to 180,185 to 188	B11, D11, C11, B10, D9, B9, A9, D8	I/O	Mask ROM chip select / I/O port / port interrupt request
$\overline{\text{WAKEUP}}$/PTD[3]	182	D10	I/O	Wakeup / I/O port
$\overline{\text{RESETOUT}}$/ PTD[2]	184	C9	I/O	Reset output / I/O port
DRAK0/PTD[1]	189	C8	I/O	DMA control pin / I/O port
DRAK1/PTD[0]	190	B8	I/O	DMA control pin / I/O port
$\overline{\text{DREQ0}}$/PTD[4]	191	A8	I	DMA transfer request 0 / input port
$\overline{\text{DREQ1}}$/PTD[6]	192	D7	I	DMA transfer request 1 / input port
AN[5:0]/PTL[5:0]	204 to 199	C4, A5, D4, C5, D5, A6	I	Analog input pin / input port
AN[7:6]/DA[1:0]/ PTL[7:6]	207, 206	B3, B5	I/O	Analog I/O pin / input port
$\overline{\text{CS6}}$/$\overline{\text{CE1B}}$	102	V15	O	Chip select 6 / PCMCIA CE1B
$\overline{\text{CS5}}$/$\overline{\text{CE1A}}$/ PTK[3]	101	W16	I/O	Chip select 5 / PCMCIA CE2B / I/O port
$\overline{\text{CS4}}$/PTK[2]	100	U16	I/O	Chip select 4 / I/O port
$\overline{\text{CS3}}$/PTK[1]	99	W15	I/O	Chip select 3 / I/O port



Package Code	BP-240A
JEDEC	–
JEITA	–
Mass (reference value)	0.4 g

Figure D.3 Package Dimensions (BP-240A)