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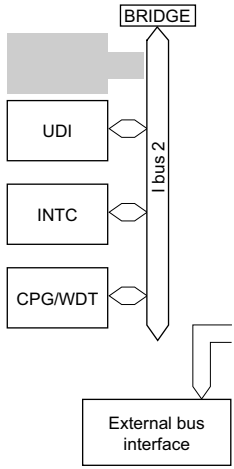
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

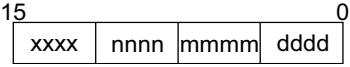
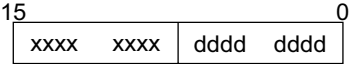
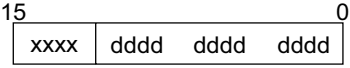
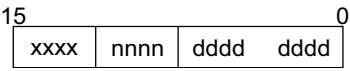
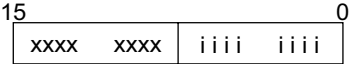
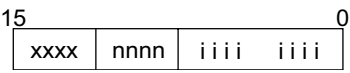
Details	
Product Status	Obsolete
Core Processor	SH-3
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	EBI/EMI, FIFO, IrDA, SCI, SmartCard
Peripherals	DMA, POR, WDT
Number of I/O	96
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.85V ~ 2.15V
Data Converters	A/D 8x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	208-BFQFP Exposed Pad
Supplier Device Package	208-HQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/d6417709shf200bv

List of Items Revised or Added for This Version

Section	Page	Description
1.2 Block Diagram Figure 1.1 Block Diagram	6	ASERAM deleted from figure  ASERAM deleted from legend
2.5.1 Processor States	53	Description amended In the power-on reset state, the internal states of the CPU and the on-chip supporting module registers are initialized. In the manual reset state, the internal states of the CPU and registers of on-chip supporting modules other than the bus state controller (BSC) are initialized. Refer to the register configurations in the relevant sections for further details.
5.4 Memory-Mapped Cache 5.4.1 Address Array	113	Description amended This operation is used to invalidate the address specification for a cache. Write back will take place when the U bit of the entry that received a hit is 1. Note that, when a 0 is written to the V bit, a 0 should always be written to the U bit of the same entry, too.

Item	Features
Cache memory	• 16-kbyte cache, mixed instruction/data • 256 entries, 4-way set associative, 16-byte block length • Write-back, write-through, LRU replacement algorithm • 1-stage write-back buffer • Maximum 2 ways of the cache can be locked
Interrupt controller (INTC)	• 23 external interrupt pins (NMI, IRQ5–IRQ0, PINT15 to PINT0) • On-chip peripheral interrupts: set priority levels for each module
User break controller (UBC)	• 2 break channels • Addresses, data values, type of access, and data size can all be set as break conditions • Supports a sequential break function
Bus state controller (BSC)	• Physical address space divided into six areas (area 0, areas 2 to 6), each a maximum of 64 Mbytes, with the following features settable for each area: — Bus size (8, 16, or 32 bits) — Number of wait cycles (also supports a hardware wait function) — Setting the type of space enables direct connection to SRAM, Synchronous DRAM, and burst ROM — Supports PCMCIA interface (2 channels) — Outputs chip select signal (CS0, CS2–CS6) for corresponding area • Synchronous DRAM refresh function — Programmable refresh interval — Support self-refresh mode • Synchronous DRAM burst access function • Usable as either big or little endian machine
User-debugging Interface (UDI)	• E10A emulator support • JTAG-compliant • Realtime branch address trace • 1-kB on-chip RAM for fast emulation program execution
Timer (TMU)	• 3-channel auto-reload-type 32-bit timer • Input capture function • 6 types of counter input clocks can be selected • Maximum resolution: 2 MHz
Realtime clock (RTC)	• Built-in clock, calendar functions, and alarm functions • On-chip 32-kHz crystal oscillator circuit with a maximum resolution (interrupt cycle) of 1/256 second

Number of Pins				
FP-208C FP-208E	BP-240A	Pin Name	I/O	Description
176	A11	$\overline{\text{CTS2}}$/IRQ5/SCPT[7]	I	Transmit clear 2 / external interrupt request / SCI input port
177	B11	$\overline{\text{MCS}}$[7]/PTC[7]/PINT[7]	O / I/O / I	Mask ROM chip select / input/output port C / port interrupt
178	D11	$\overline{\text{MCS}}$[6]/PTC[6]/PINT[6]	O / I/O / I	Mask ROM chip select / input/output port C / port interrupt
179	C11	$\overline{\text{MCS}}$[5]/PTC[5]/PINT[5]	O / I/O / I	Mask ROM chip select / input/output port C / port interrupt
180	B10	$\overline{\text{MCS}}$[4]/PTC[4]/PINT[4]	O / I/O / I	Mask ROM chip select / input/output port C / port interrupt
181	C10	VssQ	—	Input/output power supply (0 V)
182	D10	$\overline{\text{WAKEUP}}$/PTD[3]	O / I/O	Standby mode interrupt request notification / input/output port D
183	A10	VccQ	—	Input/output power supply (3.3 V)
184	C9	$\overline{\text{RESETOUT}}$/PTD[2]	O / I/O	Reset output / input/output port D
185	D9	$\overline{\text{MCS}}$[3]/PTC[3]/PINT[3]	O / I/O / I	Mask ROM chip select / input/output port C / port interrupt
186	B9	$\overline{\text{MCS}}$[2]/PTC[2]/PINT[2]	O / I/O / I	Mask ROM chip select / input/output port C / port interrupt
187	A9	$\overline{\text{MCS}}$[1]/PTC[1]/PINT[1]	O / I/O / I	Mask ROM chip select / input/output port C / port interrupt
188	D8	$\overline{\text{MCS}}$[0]/PTC[0]/PINT[0]	O / I/O / I	Mask ROM chip select / input/output port C / port interrupt
189	C8	DRAK0/PTD[1]	O / I/O	DMA request acknowledge / input/output port D
190	B8	DRAK1/PTD[0]	O / I/O	DMA request acknowledge / input/output port D
191	A8	$\overline{\text{DREQ0}}$/PTD[4]	I	DMA request / input port D
192	D7	$\overline{\text{DREQ1}}$/PTD[6]	I	DMA request / input port D
193	C7	$\overline{\text{RESETP}}$	I	Power-on reset request
194	B7	CA	I	Chip activate (hardware standby request signal)
195	A7	MD3	I	Area 0 bus width setting
196	D6	MD4	I	Area 0 bus width setting
197	C6	MD5	I	Endian setting

Instruction Format		Source Operand	Destination Operand	Instruction Example
nmd format		mmmm: register direct	nnnndddd: register indirect with displacement	MOV.L Rm,@(disp,Rn)
		mmmmdddd: register indirect with displacement	nnnn: register direct	MOV.L @(disp,Rm),Rn
d format		dddddddd: GBR indirect with displacement	R0 (register direct)	MOV.L @(disp,GBR),R0
		R0 (register direct)	dddddddd: GBR indirect with displacement	MOV.L R0,@(disp,GBR)
		dddddddd: PC-relative with displacement	R0 (register direct)	MOVA @(disp,PC),R0
		dddddddd: PC-relative	—	BF label
d12 format		ddddddddddddd: PC-relative	—	BRA label (label = disp + PC)
nd8 format		dddddddd: PC-relative with displacement	nnnn: register direct	MOV.L @(disp,PC),Rn
i format		iiiiiiii: immediate	Indexed GBR indirect	AND.B #imm, @(R0,GBR)
		iiiiiiii: immediate	R0 (register direct)	AND #imm,R0
		iiiiiiii: immediate	—	TRAPA #imm
ni format		iiiiiiii: immediate	nnnn: register direct	ADD #imm,Rn

Note: * In a multiply-and-accumulate instruction, nnnn is the source register.

Table 2.6 lists the SH7709S data transfer instructions

Table 2.6 Data Transfer Instructions

Instruction		Operation	Code	Privileged Mode	Cycles	T Bit
MOV	#imm,Rn	imm → Sign extension → Rn	1110nnnniiiiiiii	—	1	—
MOV.W	@(disp,PC),Rn	(disp × 2 + PC) → Sign extension → Rn	1001nnnndddddddd	—	1	—
MOV.L	@(disp,PC),Rn	(disp × 4 + PC) → Rn	1101nnnndddddddd	—	1	—
MOV	Rm,Rn	Rm → Rn	0110nnnnmmmm0011	—	1	—
MOV.B	Rm,@Rn	Rm → (Rn)	0010nnnnmmmm0000	—	1	—
MOV.W	Rm,@Rn	Rm → (Rn)	0010nnnnmmmm0001	—	1	—
MOV.L	Rm,@Rn	Rm → (Rn)	0010nnnnmmmm0010	—	1	—
MOV.B	@Rm,Rn	(Rm) → Sign extension → Rn	0110nnnnmmmm0000	—	1	—
MOV.W	@Rm,Rn	(Rm) → Sign extension → Rn	0110nnnnmmmm0001	—	1	—
MOV.L	@Rm,Rn	(Rm) → Rn	0110nnnnmmmm0010	—	1	—
MOV.B	Rm,@–Rn	Rn–1 → Rn, Rm → (Rn)	0010nnnnmmmm0100	—	1	—
MOV.W	Rm,@–Rn	Rn–2 → Rn, Rm → (Rn)	0010nnnnmmmm0101	—	1	—
MOV.L	Rm,@–Rn	Rn–4 → Rn, Rm → (Rn)	0010nnnnmmmm0110	—	1	—
MOV.B	@Rm+,Rn	(Rm) → Sign extension → Rn, Rm + 1 → Rm	0110nnnnmmmm0100	—	1	—
MOV.W	@Rm+,Rn	(Rm) → Sign extension → Rn, Rm + 2 → Rm	0110nnnnmmmm0101	—	1	—
MOV.L	@Rm+,Rn	(Rm) → Rn,Rm + 4 → Rm	0110nnnnmmmm0110	—	1	—
MOV.B	R0,@(disp,Rn)	R0 → (disp + Rn)	10000000nnnndddd	—	1	—
MOV.W	R0,@(disp,Rn)	R0 → (disp × 2 + Rn)	10000001nnnndddd	—	1	—
MOV.L	Rm,@(disp,Rn)	Rm → (disp × 4 + Rn)	0001nnnnmmmmdddd	—	1	—
MOV.B	@(disp,Rm),R0	(disp + Rm) → Sign extension → R0	10000100mmmmdddd	—	1	—
MOV.W	@(disp,Rm),R0	(disp × 2 + Rm) → Sign extension → R0	10000101mmmmdddd	—	1	—
MOV.L	@(disp,Rm),Rn	(disp × 4 + Rm) → Rn	0101nnnnmmmmdddd	—	1	—
MOV.B	Rm,@(R0,Rn)	Rm → (R0 + Rn)	0000nnnnmmmm0100	—	1	—

3.3.4 Page Management Information

In addition to the SH and SZ bits, the page management information of TLB entries also includes D, C, and PR bits.

The D bit of a TLB entry indicates whether the page is dirty (i.e., has been written to). If the D bit is 0, an attempt to write to the page results in an initial page write exception. For physical page swapping between secondary memory and main memory, for example, pages are controlled so that a dirty page is paged out of main memory only after that page is written back to secondary memory.

The C bit in the entry indicates whether the referenced page resides in a cacheable or non-cacheable area of memory. When the control register in area 1 is mapped, set the C bit to 0. The PR field specifies the access rights for the page in privileged and user modes and is used to protect memory. Attempts at nonpermitted accesses result in TLB protection violation exceptions.

Access states designated by the D, C, and PR bits are shown in table 3.2.

Table 3.2 Access States Designated by D, C, and PR Bits

		Privileged Mode		User Mode	
		Reading	**Writing**	**Reading**	**Writing**
D bit	0	Permitted	Initial page write exception	Permitted	Initial page write exception
	1	Permitted	Permitted	Permitted	Permitted
C bit	0	Permitted (no caching)	Permitted (no caching)	Permitted (no caching)	Permitted (no caching)
	1	Permitted (with caching)	Permitted (with caching)	Permitted (with caching)	Permitted (with caching)
PR bit	00	Permitted	TLB protection violation exception	TLB protection violation exception	TLB protection violation exception
	01	Permitted	Permitted	TLB protection violation exception	TLB protection violation exception
	10	Permitted	TLB protection violation exception	Permitted	TLB protection violation exception
	11	Permitted	Permitted	Permitted	Permitted

6.3 INTC Registers

6.3.1 Interrupt Priority Registers A to E (IPRA–IPRE)

Interrupt priority registers A to E (IPRA to IPRE) are 16-bit readable/writable registers in which priority levels from 0 to 15 are set for on-chip peripheral module, IRQ, and PINT interrupts. These registers are initialized to H'0000 by a power-on reset or manual reset, but are not initialized in standby mode.

Bit:	15	14	13	12	11	10	9	8
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	7	6	5	4	3	2	1	0
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 6.7 lists the relationship between the interrupt sources and the IPRA—IPRE bits.

Table 6.7 Interrupt Request Sources and IPRA–IPRE

Register	Bits 15 to 12	Bits 11 to 8	Bits 7 to 4	Bits 3 to 0
IPRA	TMU0	TMU1	TMU2	RTC
IPRB	WDT	REF	SCI0	Reserved*
IPRC	IRQ3	IRQ2	IRQ1	IRQ0
IPRD	PINT0 to PINT7	PINT8 to PINT15	IRQ5	IRQ4
IPRE	DMAC	IrDA	SCIF	ADC

Note: * Always read as 0. Only 0 should be written.

As shown in table 6.7, on-chip peripheral module, IRQ, or PINT interrupts are assigned to four 4-bit groups in each register. These 4-bit groups (bits 15 to 12, bits 11 to 8, bits 7 to 4, and bits 3 to 0) are set with values from H'0 (0000) to H'F (1111). Setting H'0 means priority level 0 (masking is requested); H'F is priority level 15 (the highest level). A reset initializes IPRA–IPRE to H'0000.

6.3.2 Interrupt Control Register 0 (ICR0)

ICR0 is a register that sets the input signal detection mode of external interrupt input pin NMI, and indicates the input signal level at the NMI pin. This register is initialized to H'0000 or H'8000 by a power-on reset or manual reset, but is not initialized in standby mode.

Bit:	15	14	13	12	11	10	9	8
	NMIL	—	—	—	—	—	—	NMIE
Initial value:	0/1*	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W

Bit:	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R

Note: * 1 when NMI input is high, 0 when NMI input is low.

Bit 15—NMI Input Level (NMIL): Sets the level of the signal input at the NMI pin. This bit can be read to determine the NMI pin level. This bit cannot be modified.

Bit 15: NMIL	Description
0	NMI input level is low
1	NMI input level is high

Bit 8—NMI Edge Select (NMIE): Selects whether the falling or rising edge of the interrupt request signal at the NMI pin is detected.

Bit 8: NMIE	Description
0	Interrupt request is detected on falling edge of NMI input
1	Interrupt request is detected on rising edge of NMI input

Bits 14 to 9 and 7 to 0—Reserved: These bits are always read as 0. The write value should always be 0.

Item		Number of States				Notes
		NMI	IRQ	PINT	Peripheral Modules	
Response time	Total	(5.5 + X) × Icyc + 0.5 × Bcyc + 0.5 × Pcyc	(5.5 + X) × Icyc + 1 × Bcyc + 4.5 × Pcyc[*4]	(5.5 + X) × Icyc + 3.5 × Pcyc[*5]	(5.5 + X) × Icyc + 1.5 × Pcyc[*5] (5.5 + X) × Icyc + 3 × Pcyc[*6]	
	Minimum case[*2]	7.5	16.5	12.5	8.5[*5]/11.5[*6]	At 60-MHz (CKIO = 30) operation: 0.13–0.28 µs
	Maximum case[*3]	8.5 + S	26.5 + S	18.5 + S	10.5 + S[*5] 16.5 + S[*6]	At 60-MHz (CKIO = 15) operation: 0.26–0.56 µs (in case of operand cache-hit) At 60-MHz (CKIO = 15) operation: 0.29–0.59 µs (when external memory access is performed with wait = 0)

Icyc: Duration of one cycle of internal clock supplied to CPU.
Bcyc: Duration of one CKIO cycle.
Pcyc: Duration of one cycle of peripheral clock supplied to peripheral modules.

Notes: 1. S also includes the memory access wait time.
The processing requiring the maximum execution time is LDC.L @Rm+, SR. When the memory access is a cache-hit, this requires seven instruction execution cycles. When the external access is performed, the corresponding number of cycles must be added. There are also instructions that perform two external memory accesses; if the external memory access is slow, the number of instruction execution cycles will increase accordingly.
2. The internal clock:CKIO:peripheral clock ratio is 2:1:1.
3. The internal clock:CKIO:peripheral clock ratio is 4:1:1.
4. IRQ mode
5. Modules: TMU, RTC, SCI, WDT, REFC
6. Modules: DMAC, ADC, IrDA, SCIF

7.2.5 Break Address Mask Register B (BAMRB)

BAMRB is a 32-bit read/write register. BAMRB specifies bits masked in the break address specified by BARB. A power-on reset initializes BAMRB to H'00000000.

Bit:	31	30	29	28	27	26	25	24
	BAMB31	BAMB30	BAMB29	BAMB28	BAMB27	BAMB26	BAMB25	BAMB24
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	23	22	21	20	19	18	17	16
	BAMB23	BAMB22	BAMB21	BAMB20	BAMB19	BAMB18	BAMB17	BAMB16
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8
	BAMB15	BAMB14	BAMB13	BAMB12	BAMB11	BAMB10	BAMB9	BAMB8
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	7	6	5	4	3	2	1	0
	BAMB7	BAMB6	BAMB5	BAMB4	BAMB3	BAMB2	BAMB1	BAMB0
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 31 to 0—Break Address Mask Register B31 to B0 (BAMB31 to BAMB0): Specifies bits masked in the channel B break address bits specified by BARB (BAB31—BAB0).

Bits 31 to 0: BAMBn	**Description**
0	Break address BABn of channel B is included in the break condition (Initial value)
1	Break address BABn of channel B is masked and is not included in the break condition

n = 31 to 0

Figure 11.4 shows how the priority order changes when channel 0 and channel 3 transfers are requested simultaneously and a channel 1 transfer is requested during the channel 0 transfer. The DMAC operates as follows:

1. Transfer requests are generated simultaneously for channels 0 and 3.
2. Channel 0 has a higher priority than channel 3, so the channel 0 transfer begins first (channel 3 waits for transfer).
3. A channel 1 transfer request occurs during the channel 0 transfer (channels 1 and 3 are both waiting)
4. When the channel 0 transfer ends, channel 0 becomes lowest-priority.
5. At this point, channel 1 has a higher priority than channel 3, so the channel 1 transfer begins (channel 3 waits for transfer).
6. When the channel 1 transfer ends, channel 1 becomes lowest-priority.
7. The channel 3 transfer begins.
8. When the channel 3 transfer ends, channels 3 and 2 shift downward in priority so that channel 3 becomes the lowest-priority.

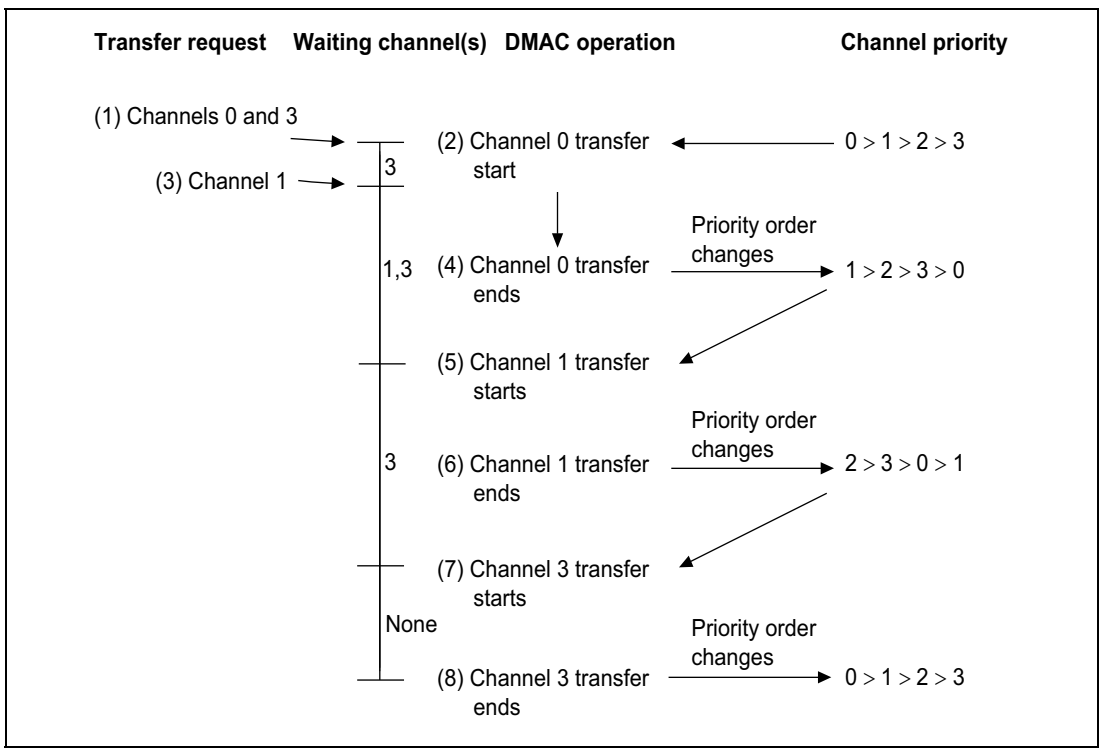


Figure 11.4 Changes in Channel Priority in Round-Robin Mode

11.3.7 DMA Transfer Ending Conditions

The DMA transfer ending conditions are different for ending on an individual channel and ending on all channels together. At the end of transfer, the following conditions are applied except in the case where the value set in the DMA transfer count register (DMATCR) reaches 0.

(a) Cycle-steal mode (external request, internal request, and auto-request)

When the transfer ending conditions are satisfied, DMAC transfer request acceptance is suspended. The DMAC stops operating after completing the number of transfers that it has accepted until the ending conditions are satisfied.

In cycle-steal mode, the operation is the same regardless of whether the transfer request is detected by level or edge.

(b) Burst mode, edge detection (external request, internal request, and auto-request)

The timing from the point where the ending conditions are satisfied to the point where the DMAC stops operating is the same as in cycle-steal mode. With edge detection in burst mode, though only one transfer request is generated to start the DMAC, stop request sampling is performed at the same timing as transfer request sampling in cycle-steal mode. As a result, the period when a stop request is not sampled is regarded as the period when a transfer request is generated, and after performing the DMA transfer for this period, the DMAC stops operating.

(c) Burst mode, level detection (external request)

Same as in (a).

(d) Bus timing when transfer is suspended

Transfer is suspended when one transfer ends. Even if transfer ending conditions are satisfied during a read in direct address transfer in dual address mode, the subsequent write process is executed, and after the transfer in (a) to (c) above has been executed, DMAC operation is suspended.

Individual Channel Ending Conditions: There are two ending conditions. A transfer ends when the value of the channel's DMA transfer count register (DMATCR) is 0, or when the DE bit in the channel's CHCR register is cleared to 0.

- When DMATCR is 0: When the DMATCR value becomes 0 and the corresponding channel's DMA transfer ends, the transfer end flag bit (TE) is set in CHCR. If the IE (interrupt enable) bit has been set, a DMAC interrupt (DEI) request is sent to the CPU. This transfer ending does not apply to (a) to (d) described above.
- When DE in CHCR is 0: Software can halt a DMA transfer by clearing the DE bit in the channel's CHCR register. The TE bit is not set when this happens. This transfer ending applies to (a) to (d) described above.

Register Configuration

Table 11.7 summarizes the CMT register configuration.

Table 11.7 Register Configuration

Name	Abbreviation	R/W	Initial Value	Address	Access Size (Bits)
Compare match timer start register	CMSTR	R/(W)	H'0000	H'04000070 (H'A4000070)*2	8, 16, 32
Compare match timer control/status register 0	CMCSR0	R/(W)*1	H'0000	H'04000072 (H'A4000072)*2	8, 16, 32
Compare match counter 0	CMCNT0	R/W	H'0000	H'04000074 (H'A4000074)*2	8, 16, 32
Compare match constant register 0	CMCOR0	R/W	H'FFFF	H'04000076 (H'A4000076)*2	8, 16, 32

Notes: 1. The only value that can be written to the CMF bit in CMCSR0 is 0 to clear the flag.
2. When address translation by the MMU does not apply, the address in parentheses should be used.

11.4.2 Register Descriptions

Compare Match Timer Start Register (CMSTR)

The compare match timer start register (CMSTR) is a 16-bit register that selects whether compare match counter 0 (CMCNT0) is operated or halted. It is initialized to H'0000 by a reset, but retains its previous value in standby mode.

Bit:	15	14	13	12	11	10	9	8
	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R

Bit:	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	STR0
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/W	R/W

Bits 15 to 2—Reserved: These bits are always read as 0. The write value should alway be 0.

Bit 1—Reserved: This bit can be read or written. The write value should always be 0.

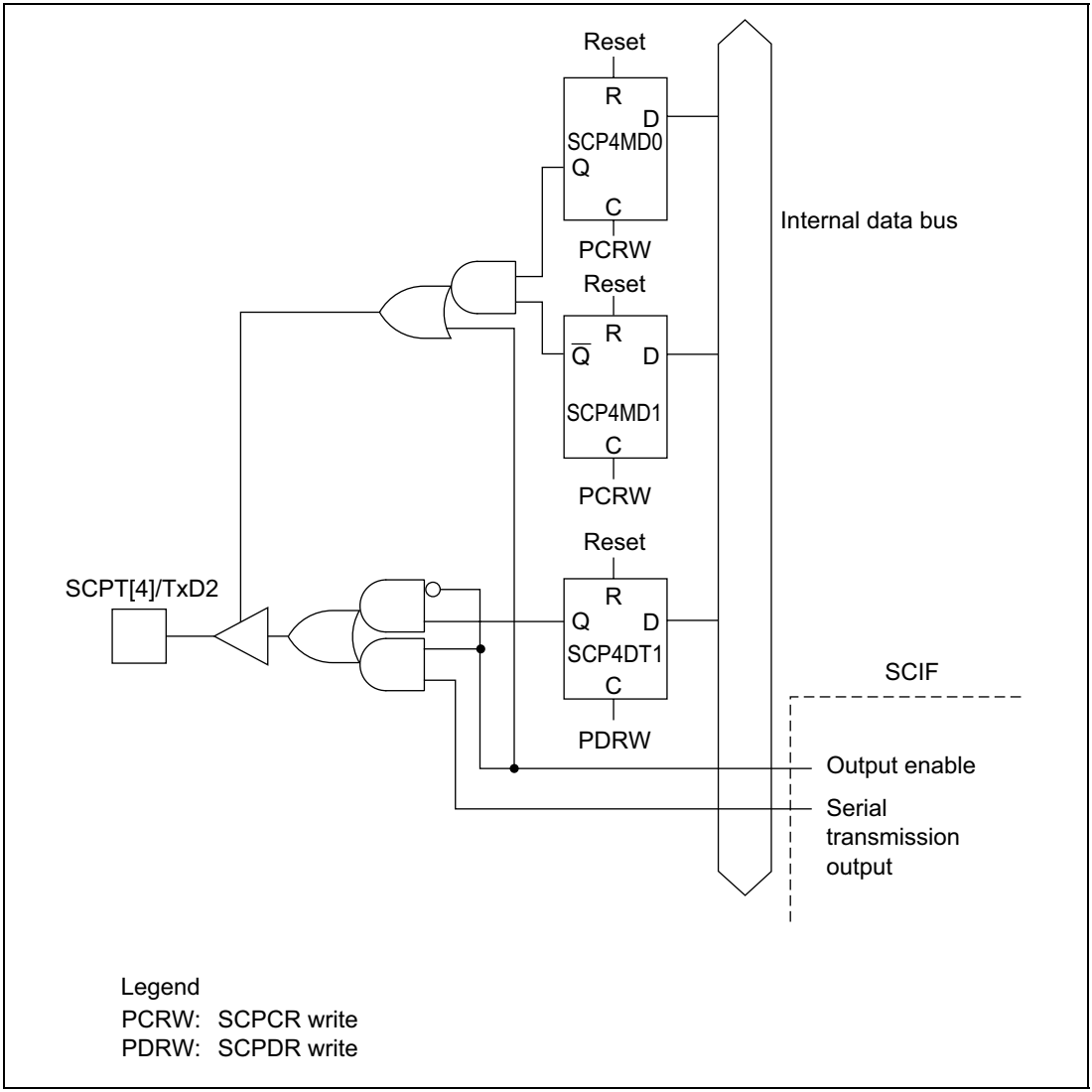


Figure 16.3 SCPT[4]/TxD2 Pin

19.1 Overview

The SH7709S has twelve 8-bit ports (ports A to L and SC). All port pins are multiplexed with other pin functions (the pin function controller (PFC) handles the selection of pin functions and pull-up MOS control). Each port has a data register which stores data for the pins.

19.2 Port A

Port A is an 8-bit input/output port with the pin configuration shown in figure 19.1. Each pin has an input pull-up MOS, which is controlled by the port A control register (PACR) in the PFC.

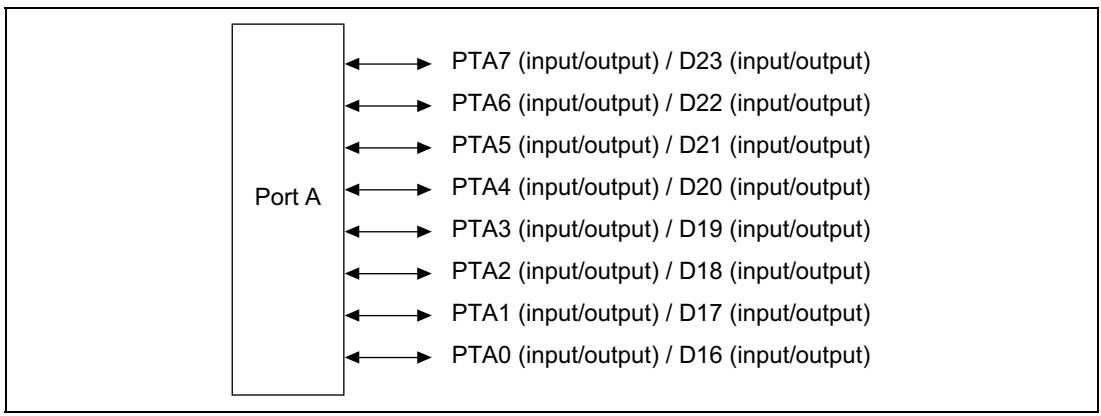


Figure 19.1 Port A

19.2.1 Register Description

Table 19.1 summarizes the port A register.

Table 19.1 Port A Register

Name	Abbreviation	R/W	Initial Value	Address	Access Size
Port A data register	PADR	R/W	H'00	H'04000120 (H'A4000120)*	8

Notes: This register is located in area 1 of physical space. Therefore, when the cache is on, either access this register from the P2 area of logical space or else make an appropriate setting using the MMU so that this register is not cached.

* When address translation by the MMU does not apply, the address in parentheses should be used.

19.10.2 Port J Data Register (PJDR)

Bit:	7	6	5	4	3	2	1	0
	PJ7DT	PJ6DT	PJ5DT	PJ4DT	PJ3DT	PJ2DT	PJ1DT	PJ0DT
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The port J data register (PJDR) is an 8-bit readable/writable register that stores data for pins PTJ7 to PTJ0. Bits PJ7DT to PJ0DT correspond to pins PTJ7 to PTJ0. When the pin function is general output port, if the port is read the value of the corresponding PJDR bit is returned directly. When the function is general input port, if the port is read, the corresponding pin level is read. Table 19.18 shows the function of PJDR.

PJDR is initialized to H'00 by a power-on reset. It retains its previous value in software standby mode and sleep mode, and in a manual reset.

Table 19.18 Port J Data Register (PJDR) Read/Write Operations

PJnMD1	PJnMD0	Pin State	Read	Write
0	0	Other function (see table 18.1)	PJDR value	Value is written to PJDR, but does not affect pin state
	1	Output	PJDR value	Write value is output from pin
1	0	Input (Pull-up MOS on)	Pin state	Value is written to PJDR, but does not affect pin state
	1	Input (Pull-up MOS off)	Pin state	Value is written to PJDR, but does not affect pin state

(n = 0 to 7)

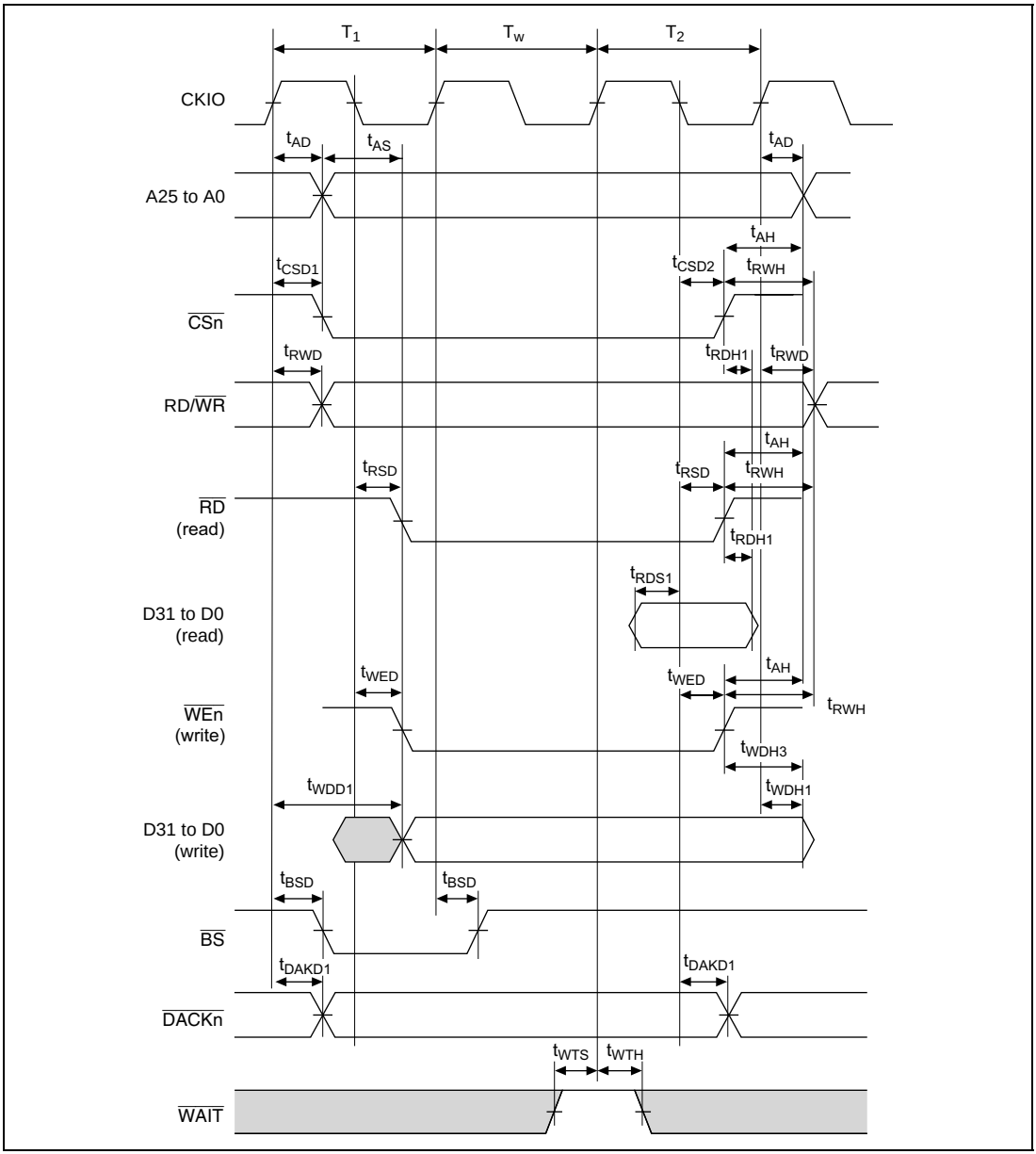


Figure 23.17 Basic Bus Cycle (One Wait)

Category	Pin	Reset		Power-Down		Bus Released
		Power-On Reset	Manual Reset	Standby	Sleep	
Analog	AN[5:0]/PTL[5:0]	Z	ZI*6	Z	I	I
	AN[6:7]/DA[1:0]/PTL[6:7]	Z	ZI*6	OZ*11	IO*8	IO*8

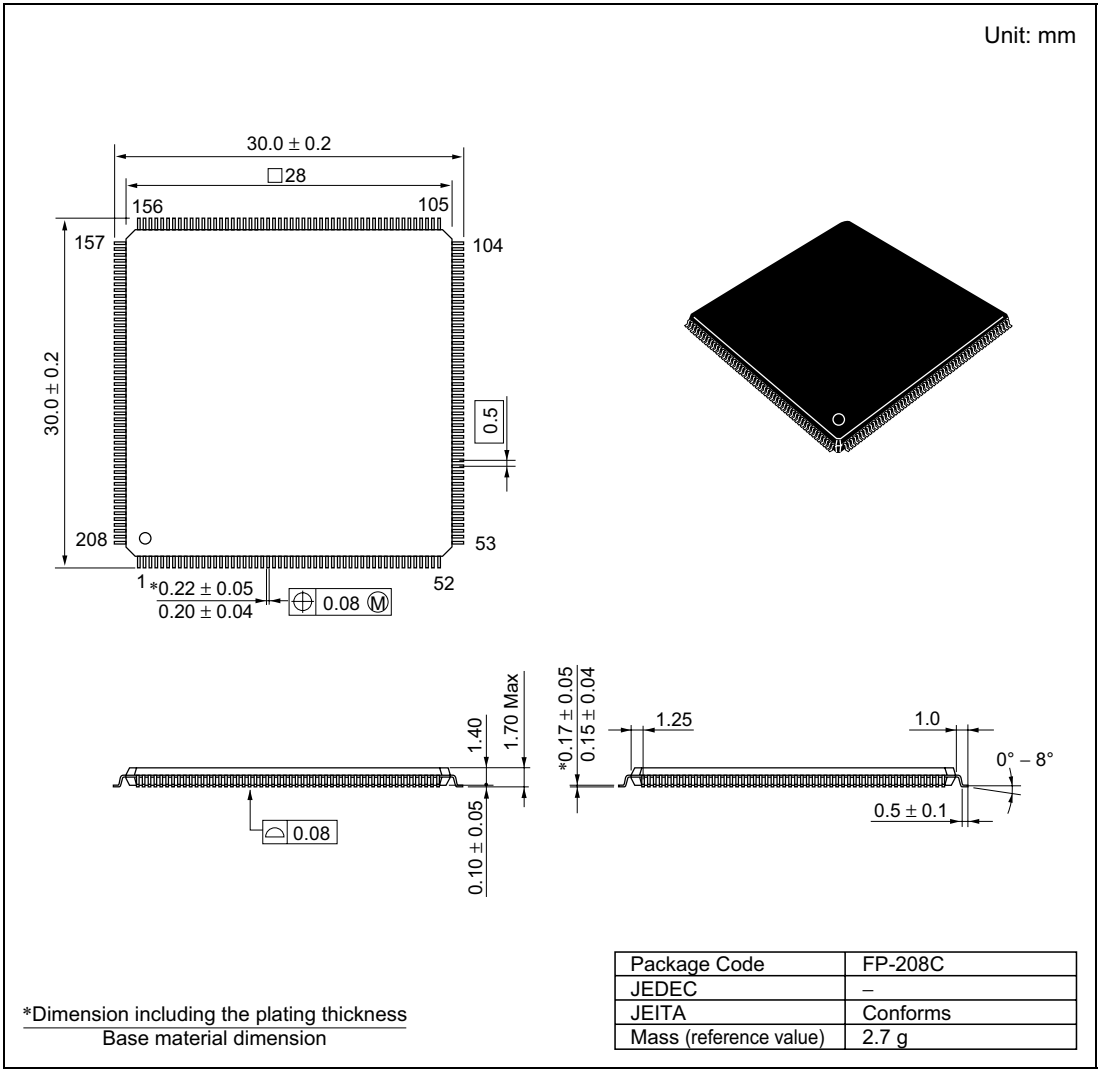
I: Input
O: Output
H: High-level output
L: Low-level output
Z: High impedance
P: Input or output depending on register setting
K: Input pin is high impedance, output pin holds its state
V: I/O buffer off, pull-up MOS on

Notes:
1. Depending on the clock mode (MD2–MD0 setting).
2. K or P when the port function is used.
3. K or P when the port function is used. Z or O when the port function is not used depending on register setting.
4. K or P when the port function is used. I or O when the port function is not used depending on register setting.
5. Depending on register setting.
6. I or O when the port function is used.
7. Input Schmitt buffers of IRQ[5.0] and ADTRG on; other input buffers off.
8. O when DA output is enabled; otherwise I depending on register setting.
9. In standby mode, Z or L depending on register setting.
10. In standby mode, Z or H depending on register setting.
11. O when DA output is enabled; Z otherwise.

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Module
CHCR0	—	—	—	—	—	—	—	—	DMAC
	—	—	—	—	—	RL	AM	AL	
	DM1	DM0	SM1	SM0	RS3	RS2	RS1	RS0	
	—	DS	TM	TS1	TS0	IE	TE	DE	
SAR1									DMAC
DAR1									DMAC
DMATCR1	—	—	—	—	—	—	—	—	DMAC
CHCR1	—	—	—	—	—	—	—	—	DMAC
	—	—	—	—	—	RL	AM	AL	
	DM1	DM0	SM1	SM0	RS3	RS2	RS1	RS0	
	—	DS	TM	TS1	TS0	IE	TE	DE	
SAR2									DMAC
DAR2									DMAC
DMATCR2	—	—	—	—	—	—	—	—	DMAC

Appendix D Package Dimensions

Figures D.1 to D.3 show the SH7709S package dimensions.



Package Code	FP-208C
JEDEC	–
JEITA	Conforms
Mass (reference value)	2.7 g

Figure D.1 Package Dimensions (FP-208C)