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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I ² C, LINbus, SIO, SSU, UART/USART
Peripherals	POR, PWM, Voltage Detect, WDT
Number of I/O	47
Program Memory Size	24KB (24K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 12x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	52-LQFP
Supplier Device Package	52-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f21355cnfp-30

Table 1.2 Specifications for R8C/35C Group (2)

Item	Function	Specification
Serial Interface	UART0, UART1	Clock synchronous serial I/O/UART × 2 channel
	UART2	Clock synchronous serial I/O/UART, I ² C mode (I ² C-bus), multiprocessor communication function
Synchronous Serial Communication Unit (SSU)		1 (shared with I ² C-bus)
I ² C bus		1 (shared with SSU)
LIN Module		Hardware LIN: 1 (timer RA, UART0)
A/D Converter		10-bit resolution × 12 channels, includes sample and hold function, with sweep mode
D/A Converter		8-bit resolution × 2 circuits
Comparator B		2 circuits
Flash Memory		<ul style="list-style-type: none"> • Programming and erasure voltage: VCC = 2.7 to 5.5 V • Programming and erasure endurance: 10,000 times (data flash) 1,000 times (program ROM) • Program security: ROM code protect, ID code check • Debug functions: On-chip debug, on-board flash rewrite function • Background operation (BGO) function
Operating Frequency/Supply Voltage		f(XIN) = 20 MHz (VCC = 2.7 to 5.5 V) f(XIN) = 5 MHz (VCC = 1.8 to 5.5 V)
Current consumption		Typ. 6.5 mA (VCC = 5.0 V, f(XIN) = 20 MHz) Typ. 3.5 mA (VCC = 3.0 V, f(XIN) = 10 MHz) Typ. 3.5 μA (VCC = 3.0 V, wait mode (f(XCIN) = 32 kHz)) Typ. 2.0 μA (VCC = 3.0 V, stop mode)
Operating Ambient Temperature		-20 to 85°C (N version) -40 to 85°C (D version) ⁽¹⁾
Package		52-pin LQFP Package code: PLQP0052JA-A (previous code: 52P6A-A)

Note:

1. Specify the D version if D version functions are to be used.

Table 1.5 Pin Name Information by Pin Number (2)

Pin Number	Control Pin	Port	I/O Pin Functions for Peripheral Modules					
			Interrupt	Timer	Serial Interface	SSU	I ² C bus	A/D Converter, D/A Converter, Comparator B
36		P1_2	$\overline{KI2}$	(TRCIOB)				AN10
37		P1_1	$\overline{KI1}$	(TRCIOA/TRCTRG)				AN9
38		P1_0	$\overline{KI0}$	(TRCIOD)				AN8
39		P0_7		(TRCIOA)				AN0/DA1
40		P0_6		(TRCIOD)				AN1/DA0
41		P0_5		(TRCIOB)				AN2
42		P0_4		TREO (/TRCIOB)				AN3
43		P0_3		(TRCIOB)	(CLK1)			AN4
44		P0_2		(TRCIOA/TRCTRG)	(RXD1)			AN5
45		P0_1		(TRCIOA/TRCTRG)	(TXD1)			AN6
46		P0_0		(TRCIOA/TRCTRG)				AN7
47		P6_4			(RXD1)			
48		P6_3			(TXD1)			
49		P6_2			(CLK1)			
50		P6_1						
51		P6_0		(TREO)				
52		P5_7						

Note:

1. Can be assigned to the pin in parentheses by a program.

Table 1.7 Pin Functions (2)

Item	Pin Name	I/O Type	Description
Reference voltage input	VREF	I	Reference voltage input pin to A/D converter and D/A converter
A/D converter	AN0 to AN11	I	Analog input pins to A/D converter
	ADTRG	I	A/D external trigger input pin
D/A converter	DA0, DA1	O	D/A converter output pins
Comparator B	IVCMP1, IVCMP3	I	Comparator B analog voltage input pins
	IVREF1, IVREF3	I	Comparator B reference voltage input pins
I/O port	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_3 to P4_7, P5_6, P5_7, P6_0 to P6_7	I/O	CMOS I/O ports. Each port has an I/O select direction register, allowing each pin in the port to be directed for input or output individually. Any port set to input can be set to use a pull-up resistor or not by a program. All ports can be used as LED drive ports.
Input port	P4_2	I	Input-only port

I: Input O: Output I/O: Input and output

2.1 Data Registers (R0, R1, R2, and R3)

R0 is a 16-bit register for transfer, arithmetic, and logic operations. The same applies to R1 to R3. R0 can be split into high-order bits (R0H) and low-order bits (R0L) to be used separately as 8-bit data registers. R1H and R1L are analogous to R0H and R0L. R2 can be combined with R0 and used as a 32-bit data register (R2R0). R3R1 is analogous to R2R0.

2.2 Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. It is also used for transfer, arithmetic, and logic operations. A1 is analogous to A0. A1 can be combined with A0 and as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is a 16-bit register for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register that indicates the starting address of an interrupt vector table.

2.5 Program Counter (PC)

PC is 20 bits wide and indicates the address of the next instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointers (SP), USP and ISP, are each 16 bits wide. The U flag of FLG is used to switch between USP and ISP.

2.7 Static Base Register (SB)

SB is a 16-bit register for SB relative addressing.

2.8 Flag Register (FLG)

FLG is an 11-bit register indicating the CPU state.

2.8.1 Carry Flag (C)

The C flag retains carry, borrow, or shift-out bits that have been generated by the arithmetic and logic unit.

2.8.2 Debug Flag (D)

The D flag is for debugging only. Set it to 0.

2.8.3 Zero Flag (Z)

The Z flag is set to 1 when an arithmetic operation results in 0; otherwise to 0.

2.8.4 Sign Flag (S)

The S flag is set to 1 when an arithmetic operation results in a negative value; otherwise to 0.

2.8.5 Register Bank Select Flag (B)

Register bank 0 is selected when the B flag is 0. Register bank 1 is selected when this flag is set to 1.

2.8.6 Overflow Flag (O)

The O flag is set to 1 when an operation results in an overflow; otherwise to 0.

3. Memory

3.1 R8C/35C Group

Figure 3.1 is a Memory Map of R8C/35C Group. The R8C/35C Group has a 1-Mbyte address space from addresses 00000h to FFFFFh. The internal ROM (program ROM) is allocated lower addresses, beginning with address 00000h. For example, a 32-Kbyte internal ROM area is allocated addresses 08000h to 0FFFFh.

The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. The starting address of each interrupt routine is stored here.

The internal ROM (data flash) is allocated addresses 03000h to 03FFFh.

The internal RAM is allocated higher addresses, beginning with address 00400h. For example, a 2.5-Kbyte internal RAM area is allocated addresses 00400h to 00DFFh. The internal RAM is used not only for data storage but also as a stack area when a subroutine is called or when an interrupt request is acknowledged.

Special function registers (SFRs) are allocated addresses 00000h to 002FFh and 02C00h to 02FFFh. Peripheral function control registers are allocated here. All unallocated spaces within the SFRs are reserved and cannot be accessed by users.

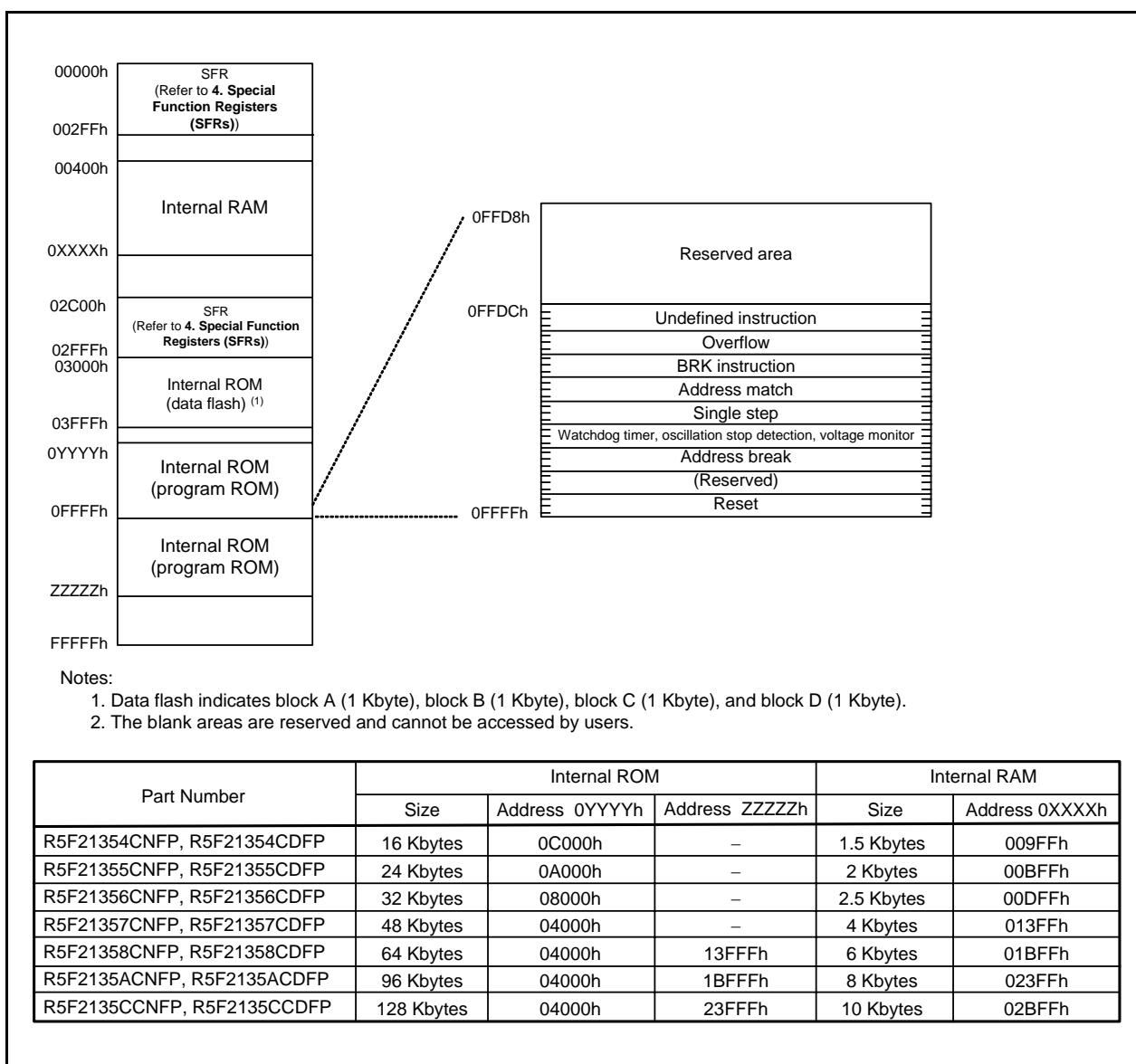


Figure 3.1 Memory Map of R8C/35C Group

Table 4.3 SFR Information (3) (1)

Address	Register	Symbol	After Reset
0080h	DTC Activation Control Register	DTCTL	00h
0081h			
0082h			
0083h			
0084h			
0085h			
0086h			
0087h			
0088h	DTC Activation Enable Register 0	DTCEN0	00h
0089h	DTC Activation Enable Register 1	DTCEN1	00h
008Ah	DTC Activation Enable Register 2	DTCEN2	00h
008Bh	DTC Activation Enable Register 3	DTCEN3	00h
008Ch	DTC Activation Enable Register 4	DTCEN4	00h
008Dh	DTC Activation Enable Register 5	DTCEN5	00h
008Eh	DTC Activation Enable Register 6	DTCEN6	00h
008Fh			
0090h			
0091h			
0092h			
0093h			
0094h			
0095h			
0096h			
0097h			
0098h			
0099h			
009Ah			
009Bh			
009Ch			
009Dh			
009Eh			
009Fh			
00A0h	UART0 Transmit/Receive Mode Register	U0MR	00h
00A1h	UART0 Bit Rate Register	U0BRG	XXh
00A2h	UART0 Transmit Buffer Register	U0TB	XXh
00A3h			XXh
00A4h	UART0 Transmit/Receive Control Register 0	U0C0	00001000b
00A5h	UART0 Transmit/Receive Control Register 1	U0C1	00000010b
00A6h	UART0 Receive Buffer Register	U0RB	XXh
00A7h			XXh
00A8h	UART2 Transmit/Receive Mode Register	U2MR	00h
00A9h	UART2 Bit Rate Register	U2BRG	XXh
00AAh	UART2 Transmit Buffer Register	U2TB	XXh
00ABh			XXh
00ACh	UART2 Transmit/Receive Control Register 0	U2C0	00001000b
00ADh	UART2 Transmit/Receive Control Register 1	U2C1	00000010b
00AEh	UART2 Receive Buffer Register	U2RB	XXh
00AFh			XXh
00B0h	UART2 Digital Filter Function Select Register	URXDF	00h
00B1h			
00B2h			
00B3h			
00B4h			
00B5h			
00B6h			
00B7h			
00B8h			
00B9h			
00BAh			
00BBh	UART2 Special Mode Register 5	U2SMR5	00h
00BCh	UART2 Special Mode Register 4	U2SMR4	00h
00BDh	UART2 Special Mode Register 3	U2SMR3	000X0X0Xb
00BEh	UART2 Special Mode Register 2	U2SMR2	X0000000b
00BFh	UART2 Special Mode Register	U2SMR	X0000000b

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.4 SFR Information (4) (1)

Address	Register	Symbol	After Reset
00C0h	A/D Register 0	AD0	XXh
00C1h			000000XXb
00C2h	A/D Register 1	AD1	XXh
00C3h			000000XXb
00C4h	A/D Register 2	AD2	XXh
00C5h			000000XXb
00C6h	A/D Register 3	AD3	XXh
00C7h			000000XXb
00C8h	A/D Register 4	AD4	XXh
00C9h			000000XXb
00CAh	A/D Register 5	AD5	XXh
00CBh			000000XXb
00CCh	A/D Register 6	AD6	XXh
00CDh			000000XXb
00CEh	A/D Register 7	AD7	XXh
00CFh			000000XXb
00D0h			
00D1h			
00D2h			
00D3h			
00D4h	A/D Mode Register	ADMOD	00h
00D5h	A/D Input Select Register	ADINSEL	11000000b
00D6h	A/D Control Register 0	ADCON0	00h
00D7h	A/D Control Register 1	ADCON1	00h
00D8h	D/A0 Register	DA0	00h
00D9h	D/A1 Register	DA1	00h
00DAh			
00DBh			
00DCh	D/A Control Register	DACON	00h
00DDh			
00DEh			
00DFh			
00E0h	Port P0 Register	P0	XXh
00E1h	Port P1 Register	P1	XXh
00E2h	Port P0 Direction Register	PD0	00h
00E3h	Port P1 Direction Register	PD1	00h
00E4h	Port P2 Register	P2	XXh
00E5h	Port P3 Register	P3	XXh
00E6h	Port P2 Direction Register	PD2	00h
00E7h	Port P3 Direction Register	PD3	00h
00E8h	Port P4 Register	P4	XXh
00E9h	Port P5 Register	P5	XXh
00EAh	Port P4 Direction Register	PD4	00h
00EBh	Port P5 Direction Register	PD5	00h
00ECh	Port P6 Register	P6	XXh
00EDh			
00EEh	Port P6 Direction Register	PD6	00h
00EFh			
00F0h			
00F1h			
00F2h			
00F3h			
00F4h			
00F5h			
00F6h			
00F7h			
00F8h			
00F9h			
00FAh			
00FBh			
00FCh			
00FDh			
00FEh			
00FFh			

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.7 SFR Information (7) ⁽¹⁾

Address	Register	Symbol	After Reset
0180h	Timer RA Pin Select Register	TRASR	00h
0181h	Timer RB/RC Pin Select Register	TRBRCSR	00h
0182h	Timer RC Pin Select Register 0	TRCPSR0	00h
0183h	Timer RC Pin Select Register 1	TRCPSR1	00h
0184h	Timer RD Pin Select Register 0	TRDPSR0	00h
0185h	Timer RD Pin Select Register 1	TRDPSR1	00h
0186h	Timer Pin Select Register	TIMSR	00h
0187h			
0188h	UART0 Pin Select Register	U0SR	00h
0189h	UART1 Pin Select Register	U1SR	00h
018Ah	UART2 Pin Select Register 0	U2SR0	00h
018Bh	UART2 Pin Select Register 1	U2SR1	00h
018Ch	SSU/IIC Pin Select Register	SSUICSR	00h
018Dh			
018Eh	INT Interrupt Input Pin Select Register	INTSR	00h
018Fh	I/O Function Pin Select Register	PINSR	00h
0190h			
0191h			
0192h			
0193h	SS Bit Counter Register	SSBR	11111000b
0194h	SS Transmit Data Register L / IIC bus Transmit Data Register ⁽²⁾	SSTDR / ICDRT	FFh
0195h	SS Transmit Data Register H ⁽²⁾	SSTDRH	FFh
0196h	SS Receive Data Register L / IIC bus Receive Data Register ⁽²⁾	SSRDR / ICDRR	FFh
0197h	SS Receive Data Register H ⁽²⁾	SSRDRH	FFh
0198h	SS Control Register H / IIC bus Control Register 1 ⁽²⁾	SSCRH / ICCR1	00h
0199h	SS Control Register L / IIC bus Control Register 2 ⁽²⁾	SSCRL / ICCR2	01111101b
019Ah	SS Mode Register / IIC bus Mode Register ⁽²⁾	SSMR / ICMR	00010000b / 00011000b
019Bh	SS Enable Register / IIC bus Interrupt Enable Register ⁽²⁾	SSER / ICIER	00h
019Ch	SS Status Register / IIC bus Status Register ⁽²⁾	SSSR / ICSR	00h / 0000X000b
019Dh	SS Mode Register 2 / Slave Address Register ⁽²⁾	SSMR2 / SAR	00h
019Eh			
019Fh			
01A0h			
01A1h			
01A2h			
01A3h			
01A4h			
01A5h			
01A6h			
01A7h			
01A8h			
01A9h			
01AAh			
01ABh			
01ACh			
01ADh			
01AEh			
01AFh			
01B0h			
01B1h			
01B2h	Flash Memory Status Register	FST	10000X00b
01B3h			
01B4h	Flash Memory Control Register 0	FMR0	00h
01B5h	Flash Memory Control Register 1	FMR1	00h
01B6h	Flash Memory Control Register 2	FMR2	00h
01B7h			
01B8h			
01B9h			
01BAh			
01BBh			
01BCh			
01BDh			
01BEh			
01BFh			

X: Undefined

Notes:

1. The blank areas are reserved and cannot be accessed by users.
2. Selectable by the IICSEL bit in the SSUICSR register.

Table 4.8 SFR Information (8) (1)

Address	Register	Symbol	After Reset
01C0h	Address Match Interrupt Register 0	RMAD0	XXh
01C1h			XXh
01C2h			0000XXXXb
01C3h	Address Match Interrupt Enable Register 0	AIER0	00h
01C4h	Address Match Interrupt Register 1	RMAD1	XXh
01C5h			XXh
01C6h			0000XXXXb
01C7h	Address Match Interrupt Enable Register 1	AIER1	00h
01C8h			
01C9h			
01CAh			
01CBh			
01CCh			
01CDh			
01CEh			
01CFh			
01D0h			
01D1h			
01D2h			
01D3h			
01D4h			
01D5h			
01D6h			
01D7h			
01D8h			
01D9h			
01DAh			
01DBh			
01DCh			
01DDh			
01DEh			
01DFh			
01E0h	Pull-Up Control Register 0	PUR0	00h
01E1h	Pull-Up Control Register 1	PUR1	00h
01E2h			
01E3h			
01E4h			
01E5h			
01E6h			
01E7h			
01E8h			
01E9h			
01EAh			
01EBh			
01ECh			
01EDh			
01EEh			
01EFh			
01F0h	Port P1 Drive Capacity Control Register	P1DRR	00h
01F1h	Port P2 Drive Capacity Control Register	P2DRR	00h
01F2h	Drive Capacity Control Register 0	DRR0	00h
01F3h	Drive Capacity Control Register 1	DRR1	00h
01F4h			
01F5h	Input Threshold Control Register 0	VLT0	00h
01F6h	Input Threshold Control Register 1	VLT1	00h
01F7h			
01F8h	Comparator B Control Register 0	INTCMP	00h
01F9h			
01FAh	External Input Enable Register 0	INTEN	00h
01FBh	External Input Enable Register 1	INTEN1	00h
01FCh	INT Input Filter Select Register 0	INTF	00h
01FDh	INT Input Filter Select Register 1	INTF1	00h
01FEh	Key Input Enable Register 0	KIEN	00h
01FFh			

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.12 SFR Information (12) ⁽¹⁾

Address	Register	Symbol	After Reset
2CF0h	DTC Control Data 22	DTCD22	XXh
2CF1h			XXh
2CF2h			XXh
2CF3h			XXh
2CF4h			XXh
2CF5h			XXh
2CF6h			XXh
2CF7h			XXh
2CF8h	DTC Control Data 23	DTCD23	XXh
2CF9h			XXh
2CFAh			XXh
2CFBh			XXh
2CFCh			XXh
2CFDh			XXh
2CFEh			XXh
2CFFh			XXh
2D00h			
⋮			
2FFh			

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.13 ID Code Areas and Option Function Select Area

Address	Area Name	Symbol	After Reset
⋮			
FFDBh	Option Function Select Register 2	OFS2	(Note 1)
⋮			
FFDFh	ID1		(Note 2)
⋮			
FFE3h	ID2		(Note 2)
⋮			
FFEBh	ID3		(Note 2)
⋮			
FFEFh	ID4		(Note 2)
⋮			
FFF3h	ID5		(Note 2)
⋮			
FFF7h	ID6		(Note 2)
⋮			
FFFBh	ID7		(Note 2)
⋮			
FFFFh	Option Function Select Register	OFS	(Note 1)

Notes:

1. The option function select area is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program. Do not write additions to the option function select area. If the block including the option function select area is erased, the option function select area is set to FFh. When blank products are shipped, the option function select area is set to FFh. It is set to the written value after written by the user. When factory-programming products are shipped, the value of the option function select area is the value programmed by the user.
2. The ID code areas are allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program. Do not write additions to the ID code areas. If the block including the ID code areas is erased, the ID code areas are set to FFh. When blank products are shipped, the ID code areas are set to FFh. They are set to the written value after written by the user. When factory-programming products are shipped, the value of the ID code areas is the value programmed by the user.

Table 5.2 Recommended Operating Conditions

Symbol	Parameter			Conditions	Standard			Unit	
					Min.	Typ.	Max.		
Vcc/AVcc	Supply voltage				1.8	–	5.5	V	
Vss/AVss	Supply voltage				–	0	–	V	
VIH	Input “H” voltage	Other than CMOS input				0.8 Vcc	–	Vcc	V
		CMOS input	Input level switching function (I/O port)	Input level selection : 0.35 Vcc	4.0 V ≤ Vcc ≤ 5.5 V	0.5 Vcc	–	Vcc	V
					2.7 V ≤ Vcc < 4.0 V	0.55 Vcc	–	Vcc	V
					1.8 V ≤ Vcc < 2.7 V	0.65 Vcc	–	Vcc	V
			Input level selection : 0.5 Vcc	4.0 V ≤ Vcc ≤ 5.5 V	0.65 Vcc	–	Vcc	V	
				2.7 V ≤ Vcc < 4.0 V	0.7 Vcc	–	Vcc	V	
				1.8 V ≤ Vcc < 2.7 V	0.8 Vcc	–	Vcc	V	
			Input level selection : 0.7 Vcc	4.0 V ≤ Vcc ≤ 5.5 V	0.85 Vcc	–	Vcc	V	
				2.7 V ≤ Vcc < 4.0 V	0.85 Vcc	–	Vcc	V	
				1.8 V ≤ Vcc < 2.7 V	0.85 Vcc	–	Vcc	V	
	External clock input (XOUT)				1.2	–	Vcc	V	
VIL	Input “L” voltage	Other than CMOS input				0	–	0.2 Vcc	V
		CMOS input	Input level switching function (I/O port)	Input level selection : 0.35 Vcc	4.0 V ≤ Vcc ≤ 5.5 V	0	–	0.2 Vcc	V
					2.7 V ≤ Vcc < 4.0 V	0	–	0.2 Vcc	V
					1.8 V ≤ Vcc < 2.7 V	0	–	0.2 Vcc	V
			Input level selection : 0.5 Vcc	4.0 V ≤ Vcc ≤ 5.5 V	0	–	0.4 Vcc	V	
				2.7 V ≤ Vcc < 4.0 V	0	–	0.3 Vcc	V	
				1.8 V ≤ Vcc < 2.7 V	0	–	0.2 Vcc	V	
			Input level selection : 0.7 Vcc	4.0 V ≤ Vcc ≤ 5.5 V	0	–	0.55 Vcc	V	
				2.7 V ≤ Vcc < 4.0 V	0	–	0.45 Vcc	V	
				1.8 V ≤ Vcc < 2.7 V	0	–	0.35 Vcc	V	
	External clock input (XOUT)				0	–	0.4	V	
IOH(sum)	Peak sum output “H” current	Sum of all pins IOH(peak)		–	–	–160	mA		
IOH(sum)	Average sum output “H” current	Sum of all pins IOH(avg)		–	–	–80	mA		
IOH(peak)	Peak output “H” current	Drive capacity Low		–	–	–10	mA		
		Drive capacity High		–	–	–40	mA		
IOH(avg)	Average output “H” current	Drive capacity Low		–	–	–5	mA		
		Drive capacity High		–	–	–20	mA		
IOL(sum)	Peak sum output “L” current	Sum of all pins IOL(peak)		–	–	160	mA		
IOL(sum)	Average sum output “L” current	Sum of all pins IOL(avg)		–	–	80	mA		
IOL(peak)	Peak output “L” current	Drive capacity Low		–	–	10	mA		
		Drive capacity High		–	–	40	mA		
IOL(avg)	Average output “L” current	Drive capacity Low		–	–	5	mA		
		Drive capacity High		–	–	20	mA		
f(XIN)	XIN clock input oscillation frequency			2.7 V ≤ Vcc ≤ 5.5 V	–	–	20	MHz	
				1.8 V ≤ Vcc < 2.7 V	–	–	5	MHz	
f(XCIN)	XCIN clock input oscillation frequency			1.8 V ≤ Vcc ≤ 5.5 V	–	32.768	50	kHz	
fOCO40M	When used as the count source for timer RC or timer RD (3)			2.7 V ≤ Vcc ≤ 5.5 V	32	–	40	MHz	
fOCO-F	fOCO-F frequency			2.7 V ≤ Vcc ≤ 5.5 V	–	–	20	MHz	
				1.8 V ≤ Vcc < 2.7 V	–	–	5	MHz	
–	System clock frequency			2.7 V ≤ Vcc ≤ 5.5 V	–	–	20	MHz	
				1.8 V ≤ Vcc < 2.7 V	–	–	5	MHz	
f(BCLK)	CPU clock frequency			2.7 V ≤ Vcc ≤ 5.5 V	–	–	20	MHz	
				1.8 V ≤ Vcc < 2.7 V	–	–	5	MHz	

Notes:

1. V_{CC} = 1.8 to 5.5 V and T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.
2. The average output current indicates the average value of current measured during 100 ms.
3. f_{OCO40M} can be used as the count source for timer RC or timer RD in the range of V_{CC} = 2.7 V to 5.5V.

Table 5.6 Flash Memory (Program ROM) Electrical Characteristics

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
—	Program/erase endurance ⁽²⁾		1,000 ⁽³⁾	—	—	times
—	Byte program time		—	80	500	μs
—	Block erase time		—	0.3	—	s
t _d (SR-SUS)	Time delay from suspend request until suspend		—	—	5+CPU clock × 3 cycles	ms
—	Interval from erase start/restart until following suspend request		0	—	—	μs
—	Time from suspend until erase restart		—	—	30+CPU clock × 1 cycle	μs
t _d (CMDRST-READY)	Time from when command is forcibly terminated until reading is enabled		—	—	30+CPU clock × 1 cycle	μs
—	Program, erase voltage		2.7	—	5.5	V
—	Read voltage		1.8	—	5.5	V
—	Program, erase temperature		0	—	60	°C
—	Data hold time ⁽⁷⁾	Ambient temperature = 55°C	20	—	—	year

Notes:

1. V_{CC} = 2.7 to 5.5 V and T_{opr} = 0 to 60°C, unless otherwise specified.
2. Definition of programming/erasure endurance
The programming and erasure endurance is defined on a per-block basis.
If the programming and erasure endurance is n (n = 1,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.
However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
4. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
5. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
6. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
7. The data hold time includes time that the power supply is off or the clock is not supplied.

Table 5.15 Timing Requirements of Synchronous Serial Communication Unit (SSU) (1)

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
tsucyc	SSCK clock cycle time			4	–	–	tcyc (2)
tHI	SSCK clock "H" width			0.4	–	0.6	tsucyc
tLO	SSCK clock "L" width			0.4	–	0.6	tsucyc
tRISE	SSCK clock rising time	Master		–	–	1	tcyc (2)
		Slave		–	–	1	μs
tFALL	SSCK clock falling time	Master		–	–	1	tcyc (2)
		Slave		–	–	1	μs
tsu	SSO, SSI data input setup time			100	–	–	ns
tH	SSO, SSI data input hold time			1	–	–	tcyc (2)
tLEAD	$\overline{\text{SCS}}$ setup time	Slave		1tcyc + 50	–	–	ns
tLAG	$\overline{\text{SCS}}$ hold time	Slave		1tcyc + 50	–	–	ns
tOD	SSO, SSI data output delay time			–	–	1	tcyc (2)
tSA	SSI slave access time		$2.7\text{ V} \leq V_{\text{CC}} \leq 5.5\text{ V}$	–	–	$1.5\text{tcyc} + 100$	ns
			$1.8\text{ V} \leq V_{\text{CC}} < 2.7\text{ V}$	–	–	$1.5\text{tcyc} + 200$	ns
tOR	SSI slave out open time		$2.7\text{ V} \leq V_{\text{CC}} \leq 5.5\text{ V}$	–	–	$1.5\text{tcyc} + 100$	ns
			$1.8\text{ V} \leq V_{\text{CC}} < 2.7\text{ V}$	–	–	$1.5\text{tcyc} + 200$	ns

Notes:

1. $V_{\text{CC}} = 1.8$ to 5.5 V , $V_{\text{SS}} = 0\text{ V}$ and $T_{\text{opr}} = -20$ to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
2. $1\text{tcyc} = 1/f_1(\text{s})$

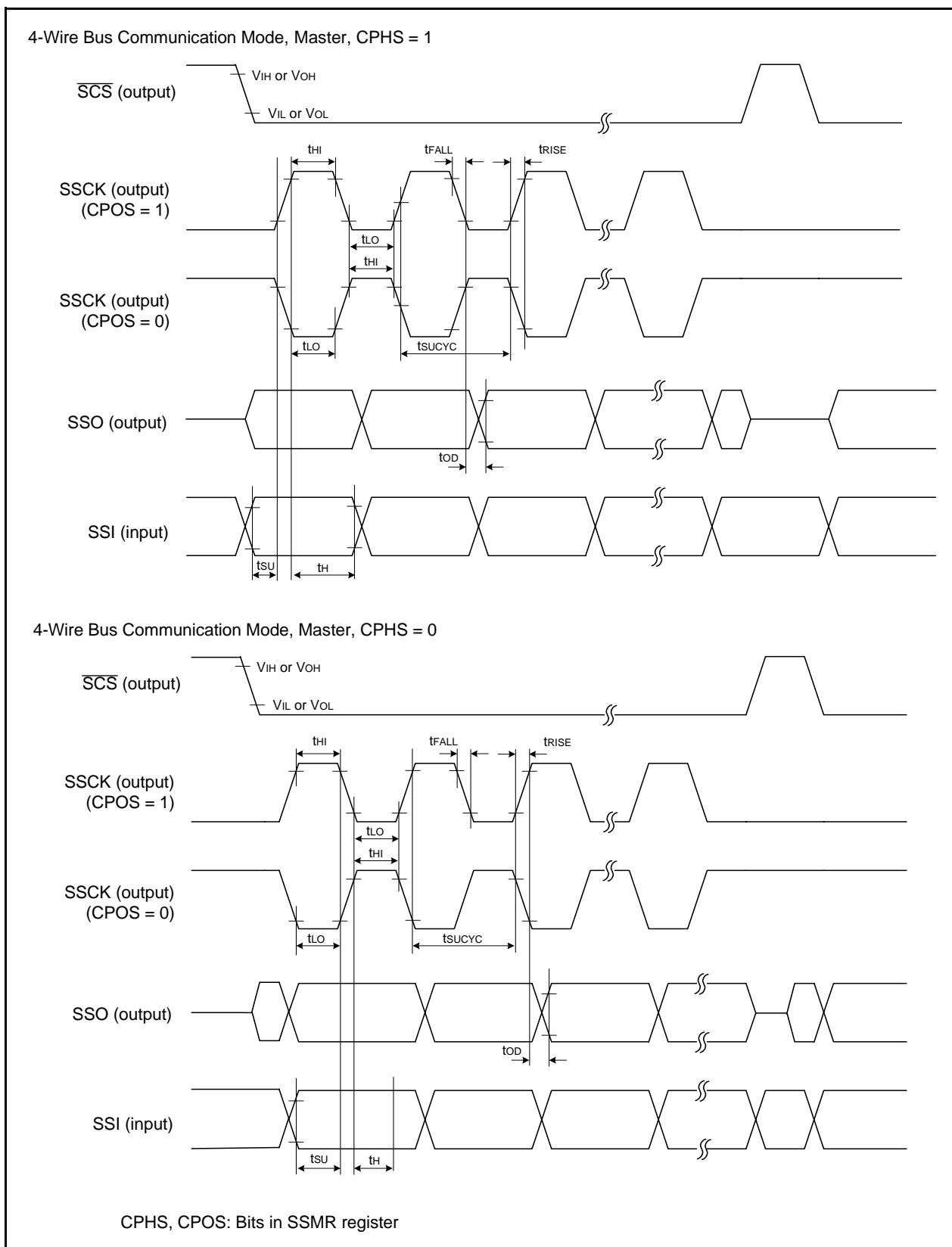


Figure 5.4 I/O Timing of Synchronous Serial Communication Unit (SSU) (Master)

Table 5.18 Electrical Characteristics (2) [$3.3\text{ V} \leq V_{CC} \leq 5.5\text{ V}$]
($T_{opr} = -20\text{ to }85^\circ\text{C}$ (N version) / $-40\text{ to }85^\circ\text{C}$ (D version), unless otherwise specified.)

Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
Icc	Power supply current (Vcc = 3.3 to 5.5 V) Single-chip mode, output pins are open, other pins are Vss	High-speed clock mode	XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	6.5	15	mA
			XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	5.3	12.5	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	3.6	–	mA
			XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	3.0	–	mA
			XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	2.2	–	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	1.5	–	mA
		High-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator on fOCO-F = 20 MHz Low-speed on-chip oscillator on = 125 kHz No division	–	7.0	15	mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 20 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	3.0	–	mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 4 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-16, MSTIC = MSTTRD = MSTTRC = 1	–	1	–	mA
		Low-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR27 = 1, VCA20 = 0	–	90	400	μA
		Low-speed clock mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz No division, FMR27 = 1, VCA20 = 0	–	85	400	μA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz No division, Program operation on RAM Flash memory off, FMSTP = 1, VCA20 = 0	–	47	–	μA
		Wait mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	15	100	μA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	4	90	μA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (peripheral clock off) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	3.5	–	μA
		Stop mode	XIN clock off, Topr = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1, Peripheral clock off VCA27 = VCA26 = VCA25 = 0	–	2.0	5.0	μA
			XIN clock off, Topr = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1, Peripheral clock off VCA27 = VCA26 = VCA25 = 0	–	5.0 (1) 15 (2)	–	μA

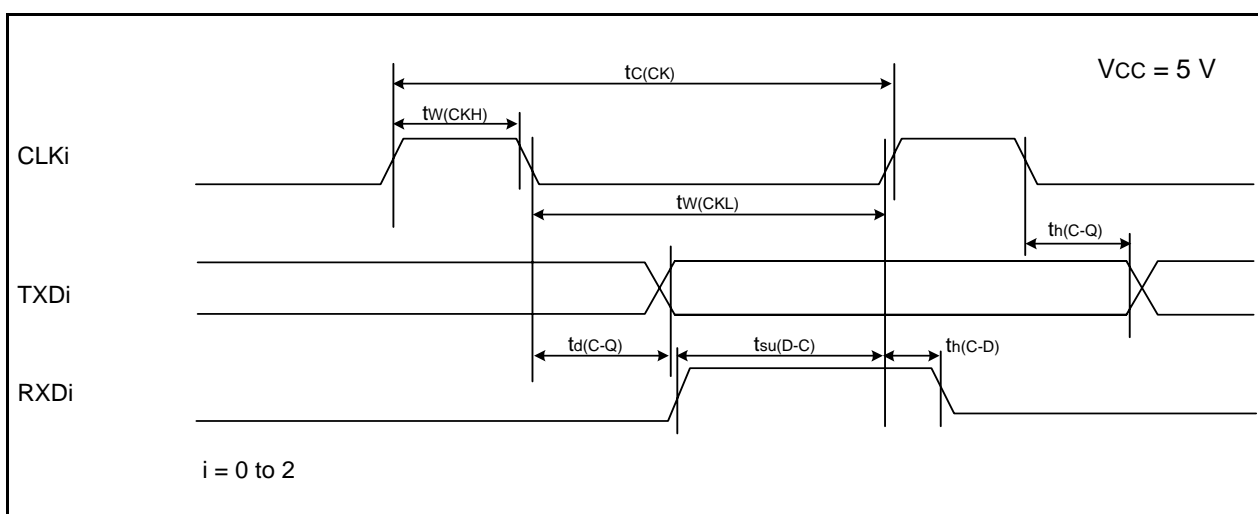
Notes:

- Value when the program ROM capacity of the product is 16 Kbytes to 32 Kbytes.
- Value when the program ROM capacity of the product is 48 Kbytes to 128 Kbytes.

Table 5.21 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	200	—	ns
$t_{w(CKH)}$	CLKi input "H" width	100	—	ns
$t_{w(CKL)}$	CLKi input "L" width	100	—	ns
$t_{d(C-Q)}$	TXDi output delay time	—	50	ns
$t_{h(C-Q)}$	TXDi hold time	0	—	ns
$t_{su(D-C)}$	RXDi input setup time	50	—	ns
$t_{h(C-D)}$	RXDi input hold time	90	—	ns

i = 0 to 2

**Figure 5.10 Serial Interface Timing Diagram when Vcc = 5 V****Table 5.22 External Interrupt \overline{INTi} (i = 0 to 4) Input, Key Input Interrupt \overline{Kli} (i = 0 to 3)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	\overline{INTi} input "H" width, \overline{Kli} input "H" width	250 (1)	—	ns
$t_{w(INL)}$	\overline{INTi} input "L" width, \overline{Kli} input "L" width	250 (2)	—	ns

Notes:

1. When selecting the digital filter by the \overline{INTi} input filter select bit, use an \overline{INTi} input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the \overline{INTi} input filter select bit, use an \overline{INTi} input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

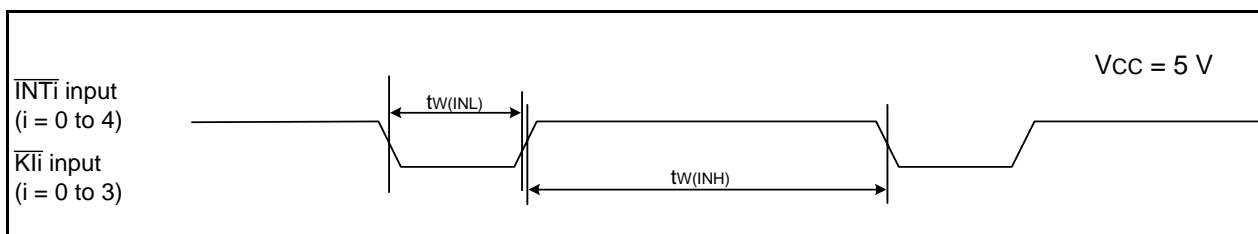
**Figure 5.11 Input Timing Diagram for External Interrupt \overline{INTi} and Key Input Interrupt \overline{Kli} when Vcc = 5 V**

Table 5.23 Electrical Characteristics (3) [$2.7\text{ V} \leq V_{CC} < 4.2\text{ V}$]

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V _{OH}	Output "H" voltage	Other than XOUT	Drive capacity High	I _{OH} = -5 mA	V _{CC} - 0.5	—	V _{CC}	V
			Drive capacity Low	I _{OH} = -1 mA	V _{CC} - 0.5	—	V _{CC}	V
		XOUT		I _{OH} = -200 μ A	1.0	—	V _{CC}	V
V _{OL}	Output "L" voltage	Other than XOUT	Drive capacity High	I _{OL} = 5 mA	—	—	0.5	V
			Drive capacity Low	I _{OL} = 1 mA	—	—	0.5	V
		XOUT		I _{OL} = 200 μ A	—	—	0.5	V
V _{T+} -V _{T-}	Hysteresis	INT0, INT1, INT2, INT3, INT4, KI0, KI1, KI2, KI3, TRAIO, TRBO, TRCIOA, TRCIOB, TRCIOC, TRCIOD, TRDIOA0, TRDIOB0, TRDIOC0, TRDIOD0, TRDIOA1, TRDIOB1, TRDIOC1, TRDIOD1, TRCTRG, TRCCLK, ADTRG, RXD0, RXD1, RXD2, CLK0, CLK1, CLK2, SSI, SCL, SDA, SSO	V _{CC} = 3.0 V		0.1	0.4	—	V
		RESET	V _{CC} = 3.0 V		0.1	0.5	—	V
I _{IH}	Input "H" current		V _I = 3 V, V _{CC} = 3.0 V		—	—	4.0	μ A
I _{IL}	Input "L" current		V _I = 0 V, V _{CC} = 3.0 V		—	—	-4.0	μ A
R _{PULLUP}	Pull-up resistance		V _I = 0 V, V _{CC} = 3.0 V		42	84	168	k Ω
R _{IXIN}	Feedback resistance	XIN			—	0.3	—	M Ω
R _{IXCIN}	Feedback resistance	XCIN			—	8	—	M Ω
V _{RAM}	RAM hold voltage		During stop mode		1.8	—	—	V

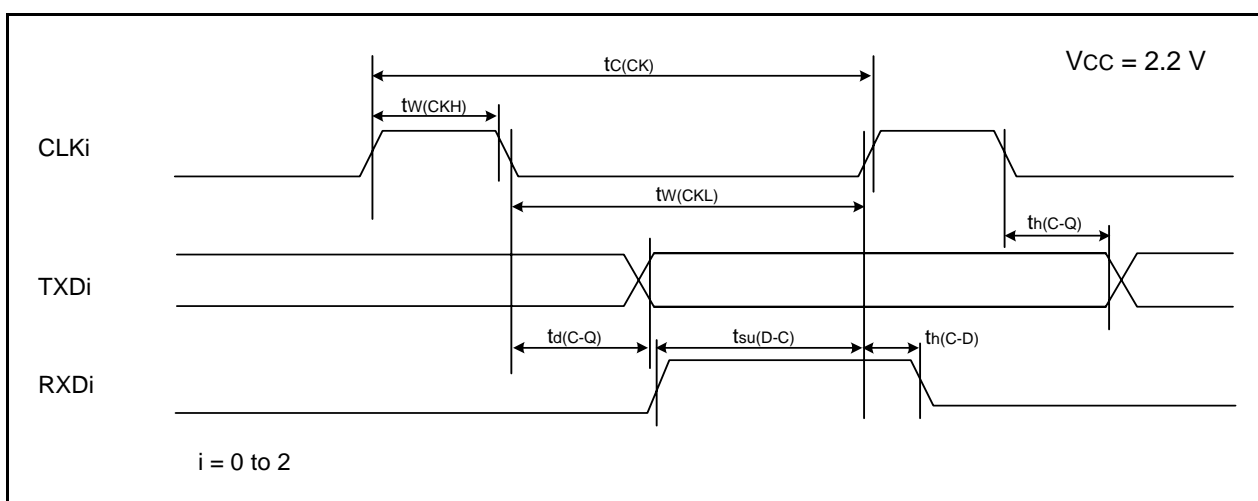
Note:

1. $2.7\text{ V} \leq V_{CC} < 4.2\text{ V}$ and T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), f(XIN) = 10 MHz, unless otherwise specified.

Table 5.33 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	800	—	ns
$t_{w(CKH)}$	CLKi input "H" width	400	—	ns
$t_{w(CKL)}$	CLKi input "L" width	400	—	ns
$t_{d(C-Q)}$	TXDi output delay time	—	200	ns
$t_{h(C-Q)}$	TXDi hold time	0	—	ns
$t_{su(D-C)}$	RXDi input setup time	150	—	ns
$t_{h(C-D)}$	RXDi input hold time	90	—	ns

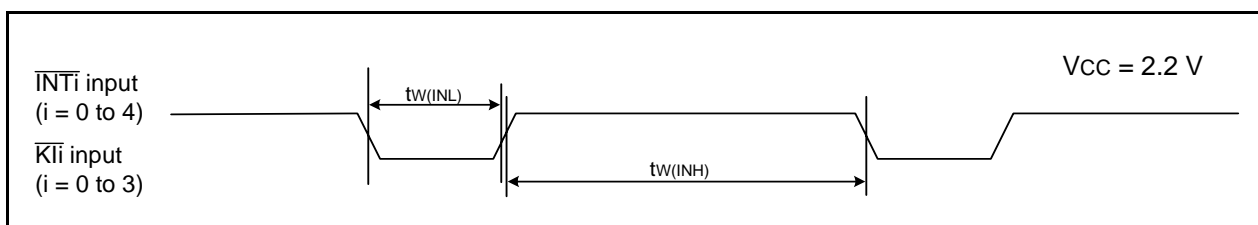
i = 0 to 2

**Figure 5.18 Serial Interface Timing Diagram when Vcc = 2.2 V****Table 5.34 External Interrupt \overline{INTi} (i = 0 to 4) Input, Key Input Interrupt \overline{Kli} (i = 0 to 3)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	\overline{INTi} input "H" width, \overline{Kli} input "H" width	1000 (1)	—	ns
$t_{w(INL)}$	\overline{INTi} input "L" width, \overline{Kli} input "L" width	1000 (2)	—	ns

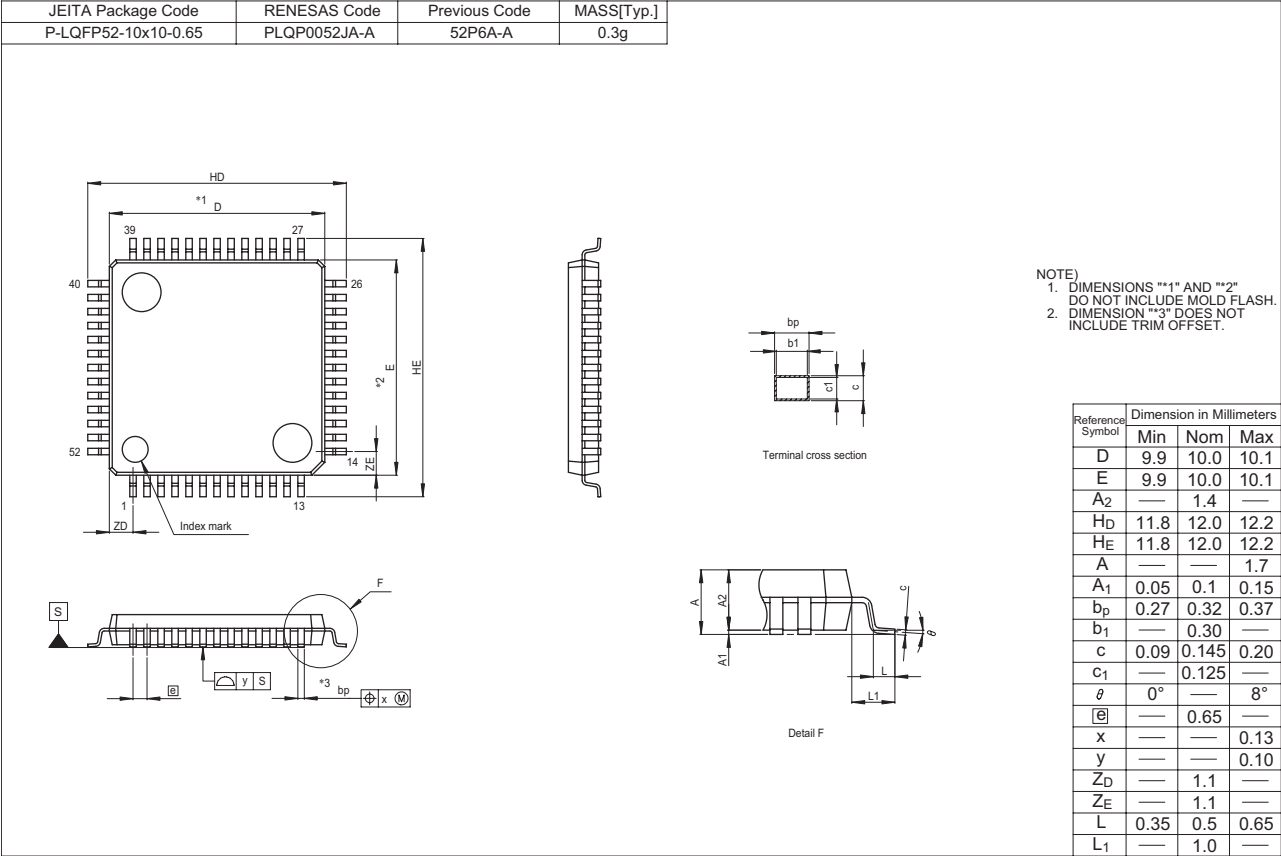
Notes:

1. When selecting the digital filter by the \overline{INTi} input filter select bit, use an \overline{INTi} input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the \overline{INTi} input filter select bit, use an \overline{INTi} input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

**Figure 5.19 Input Timing Diagram for External Interrupt \overline{INTi} and Key Input Interrupt \overline{Kli} when Vcc = 2.2 V**

Package Dimensions

Diagrams showing the latest package dimensions and mounting information are available in the “Packages” section of the Renesas Electronics website.



General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

- The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

The state of the product is undefined at the moment when power is supplied.

- The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

Access to reserved addresses is prohibited.

- The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

- When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

- The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.