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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I²C, LINbus, SIO, SSU, UART/USART
Peripherals	POR, PWM, Voltage Detect, WDT
Number of I/O	47
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	2.5K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 12x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	52-LQFP
Supplier Device Package	52-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f21356cdfp-v2

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU Registers. The CPU contains 13 registers. R0, R1, R2, R3, A0, A1, and FB configure a register bank. There are two sets of register bank.
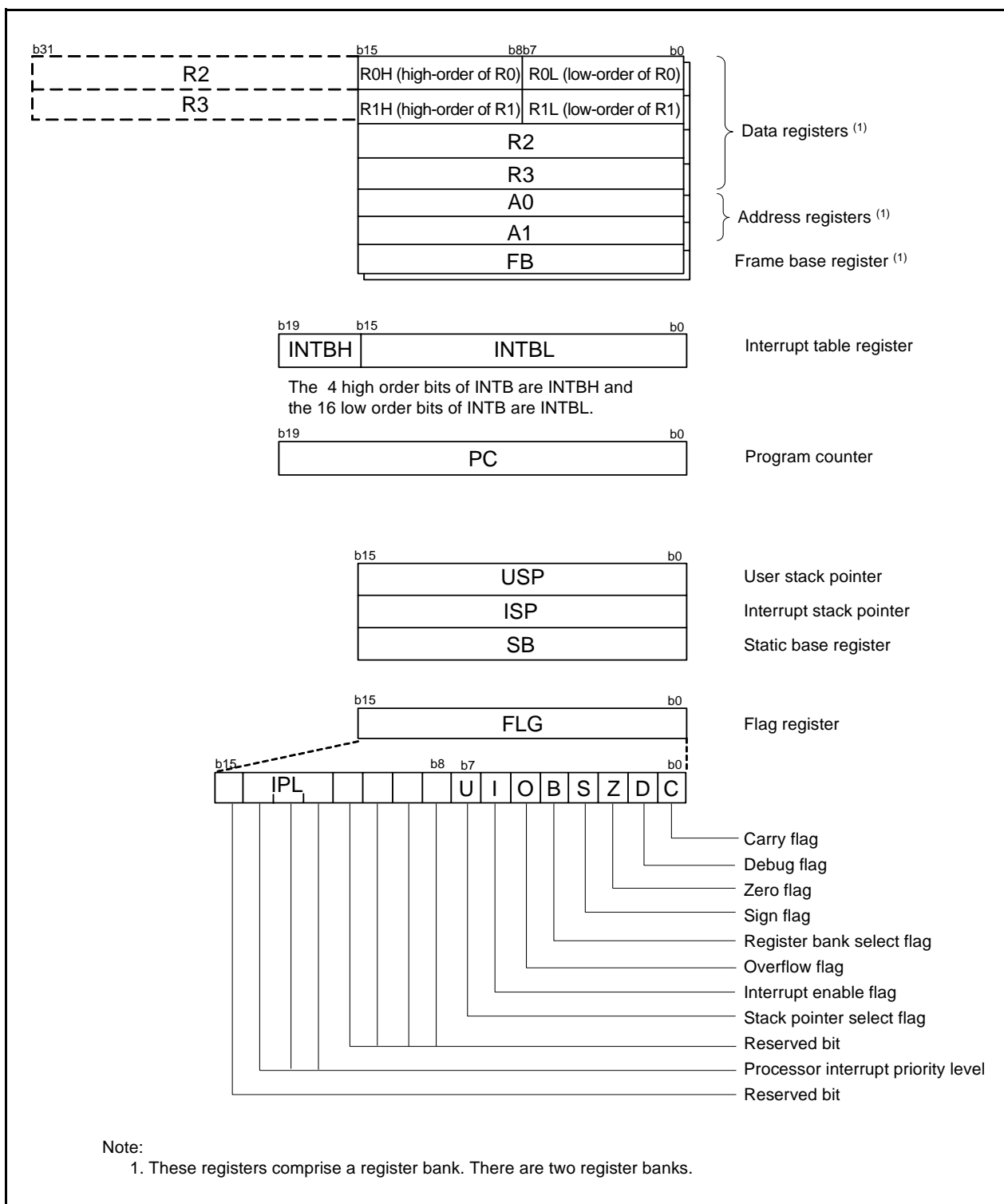

Figure 2.1   CPU Registers

2.1 Data Registers (R0, R1, R2, and R3)

R0 is a 16-bit register for transfer, arithmetic, and logic operations. The same applies to R1 to R3. R0 can be split into high-order bits (R0H) and low-order bits (R0L) to be used separately as 8-bit data registers. R1H and R1L are analogous to R0H and R0L. R2 can be combined with R0 and used as a 32-bit data register (R2R0). R3R1 is analogous to R2R0.

2.2 Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. It is also used for transfer, arithmetic, and logic operations. A1 is analogous to A0. A1 can be combined with A0 and as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is a 16-bit register for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register that indicates the starting address of an interrupt vector table.

2.5 Program Counter (PC)

PC is 20 bits wide and indicates the address of the next instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointers (SP), USP and ISP, are each 16 bits wide. The U flag of FLG is used to switch between USP and ISP.

2.7 Static Base Register (SB)

SB is a 16-bit register for SB relative addressing.

2.8 Flag Register (FLG)

FLG is an 11-bit register indicating the CPU state.

2.8.1 Carry Flag (C)

The C flag retains carry, borrow, or shift-out bits that have been generated by the arithmetic and logic unit.

2.8.2 Debug Flag (D)

The D flag is for debugging only. Set it to 0.

2.8.3 Zero Flag (Z)

The Z flag is set to 1 when an arithmetic operation results in 0; otherwise to 0.

2.8.4 Sign Flag (S)

The S flag is set to 1 when an arithmetic operation results in a negative value; otherwise to 0.

2.8.5 Register Bank Select Flag (B)

Register bank 0 is selected when the B flag is 0. Register bank 1 is selected when this flag is set to 1.

2.8.6 Overflow Flag (O)

The O flag is set to 1 when an operation results in an overflow; otherwise to 0.

2.8.7 Interrupt Enable Flag (I)

The I flag enables maskable interrupts.
Interrupts are disabled when the I flag is set to 0, and are enabled when the I flag is set to 1. The I flag is set to 0 when an interrupt request is acknowledged.

2.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is set to 0; USP is selected when the U flag is set to 1.
The U flag is set to 0 when a hardware interrupt request is acknowledged or the INT instruction of software interrupt numbers 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL is 3 bits wide and assigns processor interrupt priority levels from level 0 to level 7.
If a requested interrupt has higher priority than IPL, the interrupt is enabled.

2.8.10 Reserved Bit

If necessary, set to 0. When read, the content is undefined.

Table 4.2   SFR Information (2) [1]

Address	Register	Symbol	After Reset
003Ah	Voltage Monitor 2 Circuit Control Register	VW2C	10000010b
003Bh			
003Ch			
003Dh			
003Eh			
003Fh			
0040h			
0041h	Flash Memory Ready Interrupt Control Register	FMRDYIC	XXXXX000b
0042h			
0043h			
0044h			
0045h			
0046h	INT4 Interrupt Control Register	INT4IC	XX00X000b
0047h	Timer RC Interrupt Control Register	TRCIC	XXXXX000b
0048h	Timer RD0 Interrupt Control Register	TRD0IC	XXXXX000b
0049h	Timer RD1 Interrupt Control Register	TRD1IC	XXXXX000b
004Ah	Timer RE Interrupt Control Register	TREIC	XXXXX000b
004Bh	UART2 Transmit Interrupt Control Register	S2TIC	XXXXX000b
004Ch	UART2 Receive Interrupt Control Register	S2RIC	XXXXX000b
004Dh	Key Input Interrupt Control Register	KUPIC	XXXXX000b
004Eh	A/D Conversion Interrupt Control Register	ADIC	XXXXX000b
004Fh	SSU Interrupt Control Register / IIC bus Interrupt Control Register [2]	SSUIC / IICIC	XXXXX000b
0050h			
0051h	UART0 Transmit Interrupt Control Register	S0TIC	XXXXX000b
0052h	UART0 Receive Interrupt Control Register	S0RIC	XXXXX000b
0053h	UART1 Transmit Interrupt Control Register	S1TIC	XXXXX000b
0054h	UART1 Receive Interrupt Control Register	S1RIC	XXXXX000b
0055h	INT2 Interrupt Control Register	INT2IC	XX00X000b
0056h	Timer RA Interrupt Control Register	TRAIC	XXXXX000b
0057h			
0058h	Timer RB Interrupt Control Register	TRBIC	XXXXX000b
0059h	INT1 Interrupt Control Register	INT1IC	XX00X000b
005Ah	INT3 Interrupt Control Register	INT3IC	XX00X000b
005Bh			
005Ch			
005Dh	INT0 Interrupt Control Register	INT0IC	XX00X000b
005Eh	UART2 Bus Collision Detection Interrupt Control Register	U2BCNIC	XXXXX000b
005Fh			
0060h			
0061h			
0062h			
0063h			
0064h			
0065h			
0066h			
0067h			
0068h			
0069h			
006Ah			
006Bh			
006Ch			
006Dh			
006Eh			
006Fh			
0070h			
0071h			
0072h	Voltage Monitor 1 Interrupt Control Register	VCMP1IC	XXXXX000b
0073h	Voltage Monitor 2 Interrupt Control Register	VCMP2IC	XXXXX000b
0074h			
0075h			
0076h			
0077h			
0078h			
0079h			
007Ah			
007Bh			
007Ch			
007Dh			
007Eh			
007Fh			

X: Undefined

Notes:
1.   The blank areas are reserved and cannot be accessed by users.
2.   Selectable by the IICSEL bit in the SSUIICSR register.

Table 4.4   SFR Information (4) [1]

Address	Register	Symbol	After Reset
00C0h	A/D Register 0	AD0	XXh
00C1h			000000XXb
00C2h	A/D Register 1	AD1	XXh
00C3h			000000XXb
00C4h	A/D Register 2	AD2	XXh
00C5h			000000XXb
00C6h	A/D Register 3	AD3	XXh
00C7h			000000XXb
00C8h	A/D Register 4	AD4	XXh
00C9h			000000XXb
00CAh	A/D Register 5	AD5	XXh
00CBh			000000XXb
00CCh	A/D Register 6	AD6	XXh
00CDh			000000XXb
00CEh	A/D Register 7	AD7	XXh
00CFh			000000XXb
00D0h			
00D1h			
00D2h			
00D3h			
00D4h	A/D Mode Register	ADMOD	00h
00D5h	A/D Input Select Register	ADINSEL	11000000b
00D6h	A/D Control Register 0	ADCON0	00h
00D7h	A/D Control Register 1	ADCON1	00h
00D8h	D/A0 Register	DA0	00h
00D9h	D/A1 Register	DA1	00h
00DAh			
00DBh			
00DCh	D/A Control Register	DACON	00h
00DDh			
00DEh			
00DFh			
00E0h	Port P0 Register	P0	XXh
00E1h	Port P1 Register	P1	XXh
00E2h	Port P0 Direction Register	PD0	00h
00E3h	Port P1 Direction Register	PD1	00h
00E4h	Port P2 Register	P2	XXh
00E5h	Port P3 Register	P3	XXh
00E6h	Port P2 Direction Register	PD2	00h
00E7h	Port P3 Direction Register	PD3	00h
00E8h	Port P4 Register	P4	XXh
00E9h	Port P5 Register	P5	XXh
00EAh	Port P4 Direction Register	PD4	00h
00EBh	Port P5 Direction Register	PD5	00h
00ECh	Port P6 Register	P6	XXh
00EDh			
00EEh	Port P6 Direction Register	PD6	00h
00EFh			
00F0h			
00F1h			
00F2h			
00F3h			
00F4h			
00F5h			
00F6h			
00F7h			
00F8h			
00F9h			
00FAh			
00FBh			
00FCh			
00FDh			
00FEh			
00FFh			

X: Undefined
Note:
1.   The blank areas are reserved and cannot be accessed by users.

Table 4.5   SFR Information (5) [1]

Address	Register	Symbol	After Reset
0100h	Timer RA Control Register	TRACR	00h
0101h	Timer RA I/O Control Register	TRAIOC	00h
0102h	Timer RA Mode Register	TRAMR	00h
0103h	Timer RA Prescaler Register	TRAPRE	FFh
0104h	Timer RA Register	TRA	FFh
0105h	LIN Control Register 2	LINCR2	00h
0106h	LIN Control Register	LINCR	00h
0107h	LIN Status Register	LINST	00h
0108h	Timer RB Control Register	TRBCR	00h
0109h	Timer RB One-Shot Control Register	TRBOCR	00h
010Ah	Timer RB I/O Control Register	TRBIOC	00h
010Bh	Timer RB Mode Register	TRBMR	00h
010Ch	Timer RB Prescaler Register	TRBPRE	FFh
010Dh	Timer RB Secondary Register	TRBSC	FFh
010Eh	Timer RB Primary Register	TRBPR	FFh
010Fh			
0110h			
0111h			
0112h			
0113h			
0114h			
0115h			
0116h			
0117h			
0118h	Timer RE Second Data Register / Counter Data Register	TRESEC	00h
0119h	Timer RE Minute Data Register / Compare Data Register	TREMIN	00h
011Ah	Timer RE Hour Data Register	TREHR	00h
011Bh	Timer RE Day of Week Data Register	TREWK	00h
011Ch	Timer RE Control Register 1	TRECR1	00h
011Dh	Timer RE Control Register 2	TRECR2	00h
011Eh	Timer RE Count Source Select Register	TRECSR	00001000b
011Fh			
0120h	Timer RC Mode Register	TRCMR	01001000b
0121h	Timer RC Control Register 1	TRCCR1	00h
0122h	Timer RC Interrupt Enable Register	TRCIER	01110000b
0123h	Timer RC Status Register	TRCSR	01110000b
0124h	Timer RC I/O Control Register 0	TRCIOR0	10001000b
0125h	Timer RC I/O Control Register 1	TRCIOR1	10001000b
0126h	Timer RC Counter	TRC	00h
0127h			00h
0128h	Timer RC General Register A	TRCGRA	FFh
0129h			FFh
012Ah	Timer RC General Register B	TRCGRB	FFh
012Bh			FFh
012Ch	Timer RC General Register C	TRCGRC	FFh
012Dh			FFh
012Eh	Timer RC General Register D	TRCGRD	FFh
012Fh			FFh
0130h	Timer RC Control Register 2	TRCCR2	00011000b
0131h	Timer RC Digital Filter Function Select Register	TRCDF	00h
0132h	Timer RC Output Master Enable Register	TRCOER	01111111b
0133h	Timer RC Trigger Control Register	TRCADCR	00h
0134h			
0135h	Timer RD Control Expansion Register	TRDECR	00h
0136h	Timer RD Trigger Control Register	TRDADCR	00h
0137h	Timer RD Start Register	TRDSTR	11111100b
0138h	Timer RD Mode Register	TRDMR	00001110b
0139h	Timer RD PWM Mode Register	TRDPMR	10001000b
013Ah	Timer RD Function Control Register	TRDFCR	10000000b
013Bh	Timer RD Output Master Enable Register 1	TRDOER1	FFh
013Ch	Timer RD Output Master Enable Register 2	TRDOER2	01111111b
013Dh	Timer RD Output Control Register	TRDOCR	00h
013Eh	Timer RD Digital Filter Function Select Register 0	TRDDF0	00h
013Fh	Timer RD Digital Filter Function Select Register 1	TRDDF1	00h

Note:
1. The blank areas are reserved and cannot be accessed by users.

Table 4.8 SFR Information (8) [1]

Address	Register	Symbol	After Reset
01C0h	Address Match Interrupt Register 0	RMAD0	XXh
01C1h			XXh
01C2h			0000XXXXb
01C3h	Address Match Interrupt Enable Register 0	AIER0	00h
01C4h	Address Match Interrupt Register 1	RMAD1	XXh
01C5h			XXh
01C6h			0000XXXXb
01C7h	Address Match Interrupt Enable Register 1	AIER1	00h
01C8h			
01C9h			
01CAh			
01CBh			
01CCh			
01CDh			
01CEh			
01CFh			
01D0h			
01D1h			
01D2h			
01D3h			
01D4h			
01D5h			
01D6h			
01D7h			
01D8h			
01D9h			
01DAh			
01DBh			
01DCh			
01DDh			
01DEh			
01DFh			
01E0h	Pull-Up Control Register 0	PUR0	00h
01E1h	Pull-Up Control Register 1	PUR1	00h
01E2h			
01E3h			
01E4h			
01E5h			
01E6h			
01E7h			
01E8h			
01E9h			
01EAh			
01EBh			
01ECh			
01EDh			
01EEh			
01EFh			
01F0h	Port P1 Drive Capacity Control Register	P1DRR	00h
01F1h	Port P2 Drive Capacity Control Register	P2DRR	00h
01F2h	Drive Capacity Control Register 0	DRR0	00h
01F3h	Drive Capacity Control Register 1	DRR1	00h
01F4h			
01F5h	Input Threshold Control Register 0	VLT0	00h
01F6h	Input Threshold Control Register 1	VLT1	00h
01F7h			
01F8h	Comparator B Control Register 0	INTCMP	00h
01F9h			
01FAh	External Input Enable Register 0	INTEN	00h
01FBh	External Input Enable Register 1	INTEN1	00h
01FCh	INT Input Filter Select Register 0	INTF	00h
01FDh	INT Input Filter Select Register 1	INTF1	00h
01FEh	Key Input Enable Register 0	KIEN	00h
01FFh			

X: Undefined
Note:
 1. The blank areas are reserved and cannot be accessed by users.

Table 4.12   SFR Information (12) [(1)]

Address	Register	Symbol	After Reset
2CF0h	DTC Control Data 22	DTCD22	XXh
2CF1h			XXh
2CF2h			XXh
2CF3h			XXh
2CF4h			XXh
2CF5h			XXh
2CF6h			XXh
2CF7h			XXh
2CF8h	DTC Control Data 23	DTCD23	XXh
2CF9h			XXh
2CFAh			XXh
2CFBh			XXh
2CFCh			XXh
2CFDh			XXh
2CFEh			XXh
2CFFh			XXh
2D00h			
:			
2FFFh			

X: Undefined
Note:
1. The blank areas are reserved and cannot be accessed by users.

Table 4.13   ID Code Areas and Option Function Select Area

Address	Area Name	Symbol	After Reset
:			
FFDBh	Option Function Select Register 2	OFS2	(Note 1)
:			
FFDFh	ID1		(Note 2)
:			
FFE3h	ID2		(Note 2)
:			
FFEBh	ID3		(Note 2)
:			
FFEFh	ID4		(Note 2)
:			
FFF3h	ID5		(Note 2)
:			
FFF7h	ID6		(Note 2)
:			
FFFBh	ID7		(Note 2)
:			
FFFFh	Option Function Select Register	OFS	(Note 1)

Notes:
1. The option function select area is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
Do not write additions to the option function select area. If the block including the option function select area is erased, the option function select area is set to FFh.
When blank products are shipped, the option function select area is set to FFh. It is set to the written value after written by the user.
When factory-programming products are shipped, the value of the option function select area is the value programmed by the user.
2. The ID code areas are allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
Do not write additions to the ID code areas. If the block including the ID code areas is erased, the ID code areas are set to FFh.
When blank products are shipped, the ID code areas are set to FFh. They are set to the written value after written by the user.
When factory-programming products are shipped, the value of the ID code areas is the value programmed by the user.

5. Electrical Characteristics

Table 5.1   Absolute Maximum Ratings

Symbol	Parameter	Condition	Rated Value	Unit
V_{CC}/AV_{CC}	Supply voltage		−0.3 to 6.5	V
V_I	Input voltage		−0.3 to V_{CC} + 0.3	V
V_O	Output voltage		−0.3 to V_{CC} + 0.3	V
P_d	Power dissipation	−40°C ≤ T_{opr} ≤ 85°C	500	mW
T_{opr}	Operating ambient temperature		−20 to 85 (N version) / −40 to 85 (D version)	°C
T_{stg}	Storage temperature		−65 to 150	°C

Table 5.4   D/A Converter Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
–	Resolution		–	–	8	Bit
–	Absolute accuracy		–	–	2.5	LSB
t_{su}	Setup time		–	–	3	μs
R_O	Output resistor		–	6	–	kΩ
I_{Vref}	Reference power input current	(Note 2)	–	–	1.5	mA

Notes:
1. V_{CC}/AV_{CC} = V_{ref} = 2.7 to 5.5 V and T_{opr} = −20 to 85°C (N version) / −40 to 85°C (D version), unless otherwise specified.
2. This applies when one D/A converter is used and the value of the DAi register (i = 0 or 1) for the unused D/A converter is 00h. The resistor ladder of the A/D converter is not included.

Table 5.5   Comparator B Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
Vref	IVREF1, IVREF3 input reference voltage		0	–	V_{CC} − 1.4	V
V_I	IVCMP1, IVCMP3 input voltage		−0.3	–	V_{CC} + 0.3	V
–	Offset		–	5	100	mV
t_d	Comparator output delay time [2]	V_I = Vref ± 100 mV	–	0.1	–	μs
I_{CMP}	Comparator operating current	V_{CC} = 5.0 V	–	17.5	–	μA

Notes:
1. V_{CC} = 2.7 to 5.5 V, T_{opr} = −20 to 85°C (N version) / −40 to 85°C (D version), unless otherwise specified.
2. When the digital filter is disabled.

Table 5.6   Flash Memory (Program ROM) Electrical Characteristics

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
−	Program/erase endurance [2]		1,000 [3]	−	−	times
−	Byte program time		−	80	500	μs
−	Block erase time		−	0.3	−	s
$t_{d(SR-SUS)}$	Time delay from suspend request until suspend		−	−	5+CPU clock × 3 cycles	ms
−	Interval from erase start/restart until following suspend request		0	−	−	μs
−	Time from suspend until erase restart		−	−	30+CPU clock × 1 cycle	μs
$t_{d(CMDRST-READY)}$	Time from when command is forcibly terminated until reading is enabled		−	−	30+CPU clock × 1 cycle	μs
−	Program, erase voltage		2.7	−	5.5	V
−	Read voltage		1.8	−	5.5	V
−	Program, erase temperature		0	−	60	°C
−	Data hold time [7]	Ambient temperature = 55°C	20	−	−	year

Notes:
1. V_{CC} = 2.7 to 5.5 V and T_{opr} = 0 to 60°C, unless otherwise specified.
2. Definition of programming/erasure endurance
   The programming and erasure endurance is defined on a per-block basis.
   If the programming and erasure endurance is n (n = 1,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.
   However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
4. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
5. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
6. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
7. The data hold time includes time that the power supply is off or the clock is not supplied.

Table 5.7   **Flash Memory (Data flash Block A to Block D) Electrical Characteristics**

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
–	Program/erase endurance [2]		10,000 [3]	–	–	times
–	Byte program time (program/erase endurance $\leq$ 1,000 times)		–	160	1,500	μs
–	Byte program time (program/erase endurance $>$ 1,000 times)		–	300	1,500	μs
–	Block erase time (program/erase endurance $\leq$ 1,000 times)		–	0.2	1	s
–	Block erase time (program/erase endurance $>$ 1,000 times)		–	0.3	1	s
$t_{d(SR\text{-}SUS)}$	Time delay from suspend request until suspend		–	–	5+CPU clock × 3 cycles	ms
–	Interval from erase start/restart until following suspend request		0	–	–	μs
–	Time from suspend until erase restart		–	–	30+CPU clock × 1 cycle	μs
$t_{d(CMDRST\text{-}READY)}$	Time from when command is forcibly terminated until reading is enabled		–	–	30+CPU clock × 1 cycle	μs
–	Program, erase voltage		2.7	–	5.5	V
–	Read voltage		1.8	–	5.5	V
–	Program, erase temperature		−20 [7]	–	85	°C
–	Data hold time [8]	Ambient temperature = 55 °C	20	–	–	year

Notes:
1. V_{CC} = 2.7 to 5.5 V and T_{opr} = −20 to 85°C (N version) / −40 to 85°C (D version), unless otherwise specified.
2. Definition of programming/erasure endurance
   The programming and erasure endurance is defined on a per-block basis.
   If the programming and erasure endurance is n (n = 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.
   However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
4. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. In addition, averaging the erasure endurance between blocks A to D can further reduce the actual erasure endurance. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
5. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
6. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
7. −40°C for D version.
8. The data hold time includes time that the power supply is off or the clock is not supplied.
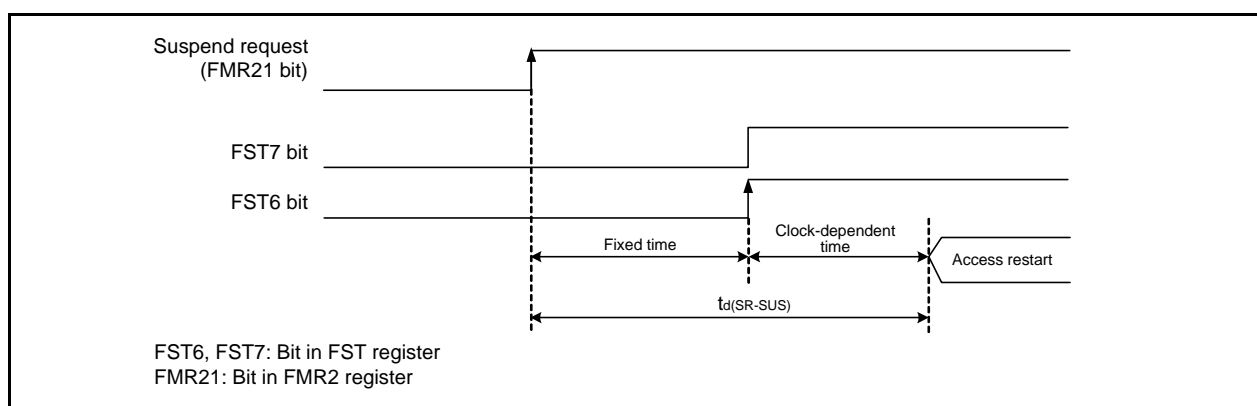

FST6, FST7: Bit in FST register
FMR21: Bit in FMR2 register

Figure 5.2   **Time delay until Suspend**

Table 5.10   Voltage Detection 2 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V$_{det2}$	Voltage detection level Vdet2_0	At the falling of V$_{CC}$	3.70	4.00	4.30	V
−	Hysteresis width at the rising of Vcc in voltage detection 2 circuit		−	0.10	−	V
−	Voltage detection 2 circuit response time [2]	At the falling of Vcc from 5 V to (Vdet2_0 − 0.1) V	−	20	150	μs
−	Voltage detection circuit self power consumption	VCA27 = 1, Vcc = 5.0 V	−	1.7	−	μA
t$_{d(E-A)}$	Waiting time until voltage detection circuit operation starts [3]		−	−	100	μs

Notes:
1. The measurement condition is V$_{CC}$ = 1.8 V to 5.5 V and T$_{opr}$ = −20 to 85°C (N version) / −40 to 85°C (D version).
2. Time until the voltage monitor 2 interrupt request is generated after the voltage passes V$_{det2}$.
3. Necessary time until the voltage detection circuit operates after setting to 1 again after setting the VCA27 bit in the VCA2 register to 0.

Table 5.11   Power-on Reset Circuit [2]

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
t$_{rth}$	External power V$_{CC}$ rise gradient	[1]	0	−	50,000	mV/msec

Notes:
1. The measurement condition is T$_{opr}$ = −20 to 85°C (N version) / −40 to 85°C (D version), unless otherwise specified.
2. To use the power-on reset function, enable voltage monitor 0 reset by setting the LVDAS bit in the OFS register to 0.
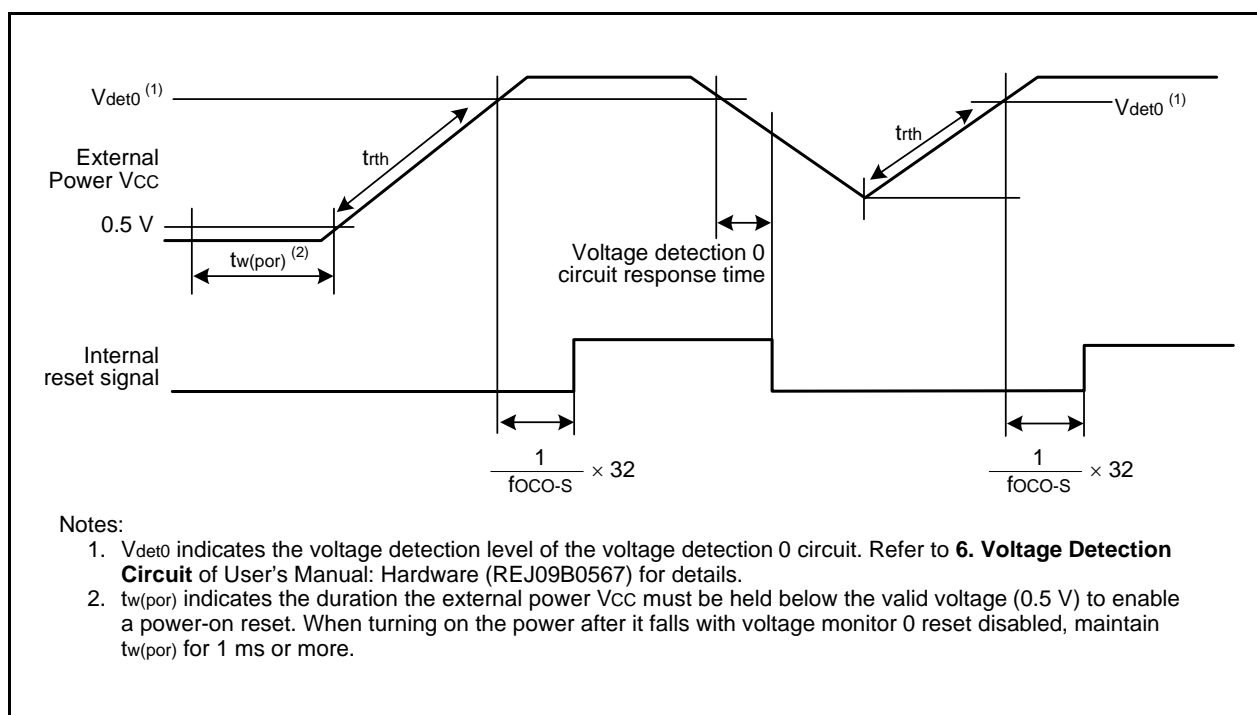

Notes:
1. V$_{det0}$ indicates the voltage detection level of the voltage detection 0 circuit. Refer to **6. Voltage Detection Circuit** of User's Manual: Hardware (REJ09B0567) for details.
2. t$_{w(por)}$ indicates the duration the external power V$_{CC}$ must be held below the valid voltage (0.5 V) to enable a power-on reset. When turning on the power after it falls with voltage monitor 0 reset disabled, maintain t$_{w(por)}$ for 1 ms or more.

Figure 5.3   Power-on Reset Circuit Electrical Characteristics

Table 5.12   High-speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
−	High-speed on-chip oscillator frequency after reset	V_{CC} = 1.8 V to 5.5 V −20°C ≤ T_{opr} ≤ 85°C	38.4	40	41.6	MHz
		V_{CC} = 1.8 V to 5.5 V −40°C ≤ T_{opr} ≤ 85°C	38.0	40	42.0	MHz
	High-speed on-chip oscillator frequency when the FRA4 register correction value is written into the FRA1 register and the FRA5 register correction value into the FRA3 register [2]	V_{CC} = 1.8 V to 5.5 V −20°C ≤ T_{opr} ≤ 85°C	35.389	36.864	38.338	MHz
		V_{CC} = 1.8 V to 5.5 V −40°C ≤ T_{opr} ≤ 85°C	35.020	36.864	38.707	MHz
	High-speed on-chip oscillator frequency when the FRA6 register correction value is written into the FRA1 register and the FRA7 register correction value into the FRA3 register	V_{CC} = 1.8 V to 5.5 V −20°C ≤ T_{opr} ≤ 85°C	30.72	32	33.28	MHz
		V_{CC} = 1.8 V to 5.5 V −40°C ≤ T_{opr} ≤ 85°C	30.40	32	33.60	MHz
−	Oscillation stability time	V_{CC} = 5.0 V, T_{opr} = 25°C	−	0.5	3	ms
−	Self power consumption at oscillation	V_{CC} = 5.0 V, T_{opr} = 25°C	−	400	−	μA

Notes:
  1. V_{CC} = 1.8 to 5.5 V, T_{opr} = −20 to 85°C (N version) / −40 to 85°C (D version), unless otherwise specified.
  2. This enables the setting errors of bit rates such as 9600 bps and 38400 bps to be 0% when the serial interface is used in UART mode.

Table 5.13   Low-speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
fOCO-S	Low-speed on-chip oscillator frequency		60	125	250	kHz
−	Oscillation stability time	V_{CC} = 5.0 V, T_{opr} = 25°C	−	30	100	μs
−	Self power consumption at oscillation	V_{CC} = 5.0 V, T_{opr} = 25°C	−	2	−	μA

Note:
  1. V_{CC} = 1.8 to 5.5 V, T_{opr} = −20 to 85°C (N version) / −40 to 85°C (D version), unless otherwise specified.

Table 5.14   Power Supply Circuit Timing Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
td(P-R)	Time for internal power supply stabilization during power-on [2]		−	−	2,000	μs

Notes:
  1. The measurement condition is V_{CC} = 1.8 to 5.5 V and T_{opr} = 25°C.
  2. Waiting time until the internal power supply generation circuit stabilizes during power-on.
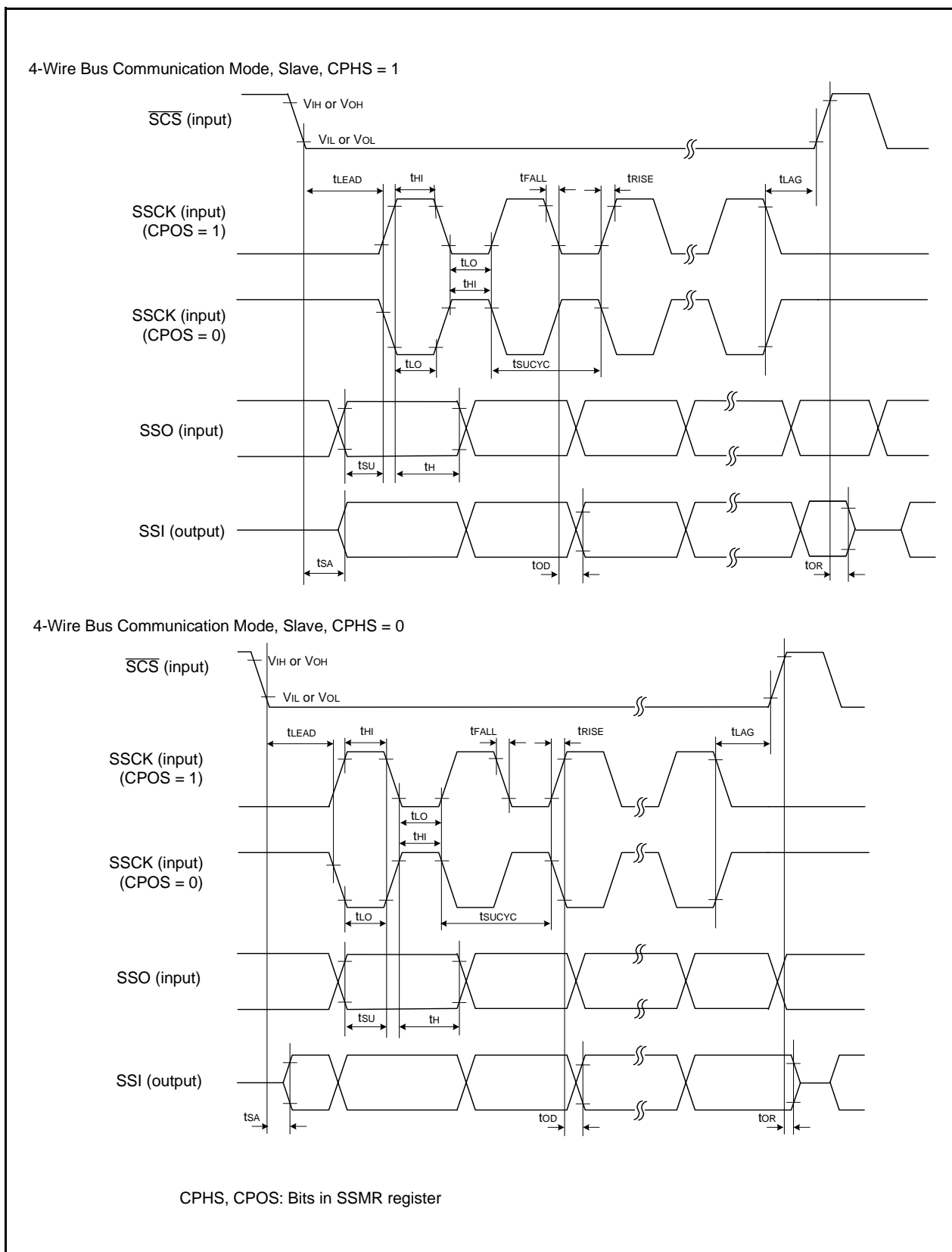
Figure 5.5   I/O Timing of Synchronous Serial Communication Unit (SSU) (Slave)
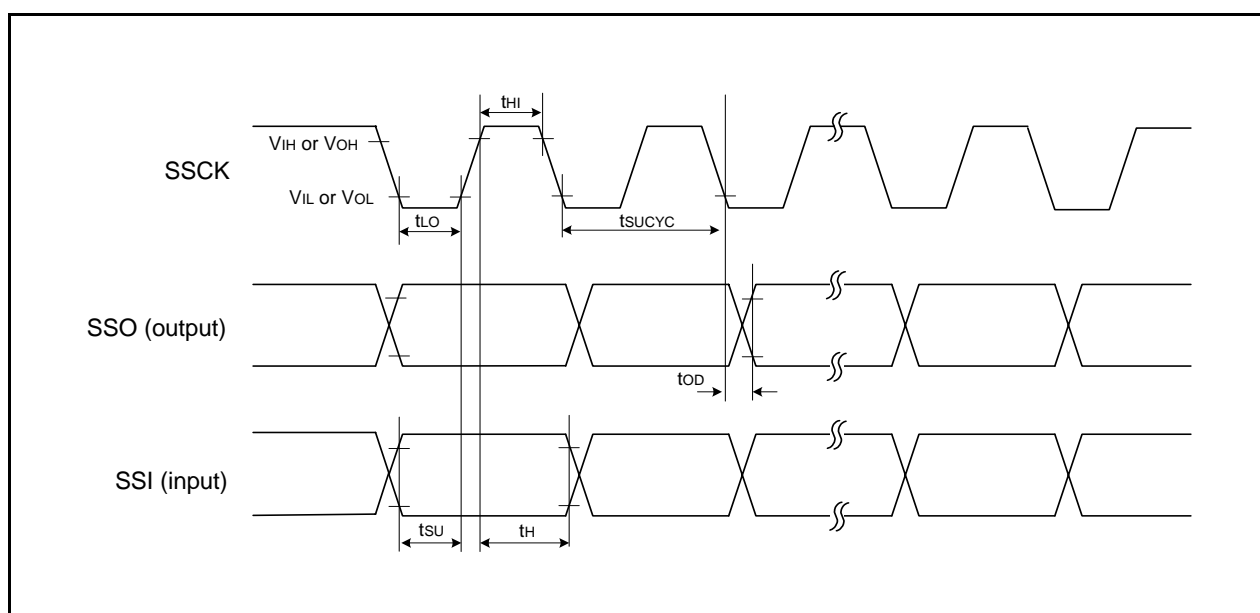
Figure 5.6   I/O Timing of Synchronous Serial Communication Unit (SSU) (Clock Synchronous Communication Mode)

Table 5.16   Timing Requirements of I2C bus Interface [1]

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
t_{SCL}	SCL input cycle time		$12t_{CYC} + 600$ [2]	–	–	ns
t_{SCLH}	SCL input "H" width		$3t_{CYC} + 300$ [2]	–	–	ns
t_{SCLL}	SCL input "L" width		$5t_{CYC} + 500$ [2]	–	–	ns
t_{sf}	SCL, SDA input fall time		–	–	300	ns
t_{SP}	SCL, SDA input spike pulse rejection time		–	–	$1t_{CYC}$ [2]	ns
t_{BUF}	SDA input bus-free time		$5t_{CYC}$ [2]	–	–	ns
t_{STAH}	Start condition input hold time		$3t_{CYC}$ [2]	–	–	ns
t_{STAS}	Retransmit start condition input setup time		$3t_{CYC}$ [2]	–	–	ns
t_{STOP}	Stop condition input setup time		$3t_{CYC}$ [2]	–	–	ns
t_{SDAS}	Data input setup time		$1t_{CYC} + 40$ [2]	–	–	ns
t_{SDAH}	Data input hold time		10	–	–	ns

Notes:
1. V_{CC} = 1.8 to 5.5 V, V_{SS} = 0 V and T_{opr} = −20 to 85°C (N version) / −40 to 85°C (D version), unless otherwise specified.
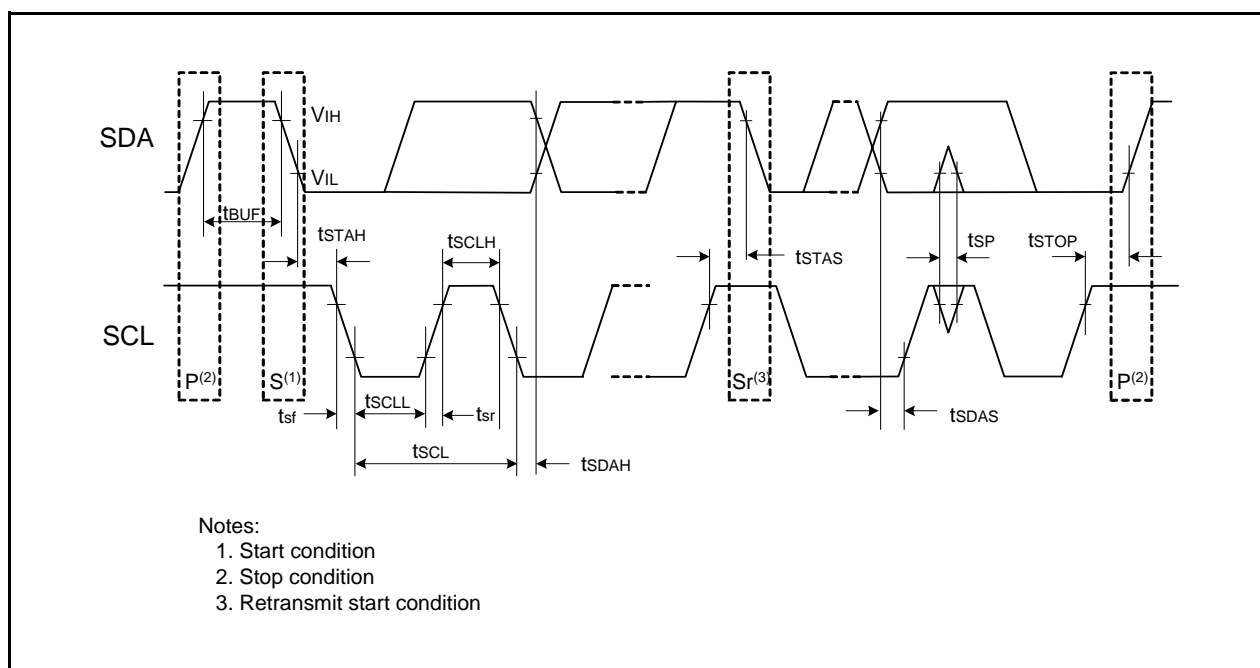2. $1t_{CYC}$ = 1/f1(s)

Figure 5.7   I/O Timing of I2C bus Interface

Table 5.23   Electrical Characteristics (3) [2.7 V ≤ Vcc < 4.2 V]

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V$_{OH}$	Output "H" voltage	Other than XOUT	Drive capacity High	I$_{OH}$ = −5 mA	V$_{CC}$ − 0.5	−	V$_{CC}$	V
			Drive capacity Low	I$_{OH}$ = −1 mA	V$_{CC}$ − 0.5	−	V$_{CC}$	V
		XOUT		I$_{OH}$ = −200 μA	1.0	−	V$_{CC}$	V
V$_{OL}$	Output "L" voltage	Other than XOUT	Drive capacity High	I$_{OL}$ = 5 mA	−	−	0.5	V
			Drive capacity Low	I$_{OL}$ = 1 mA	−	−	0.5	V
		XOUT		I$_{OL}$ = 200 μA	−	−	0.5	V
V$_{T+}$-V$_{T-}$	Hysteresis	INT0, INT1, INT2, INT3, INT4, KI0, KI1, KI2, KI3, TRAIO, TRBO, TRCIOA, TRCIOB, TRCIOC, TRCIOD, TRDIOA0, TRDIOB0, TRDIOC0, TRDIOD0, TRDIOA1, TRDIOB1, TRDIOC1, TRDIOD1, TRCTRG, TRCCLK, ADTRG, RXD0, RXD1, RXD2, CLK0, CLK1, CLK2, SSI, SCL, SDA, SSO	V$_{CC}$ = 3.0 V		0.1	0.4	−	V
		RESET	V$_{CC}$ = 3.0 V		0.1	0.5	−	V
I$_{IH}$	Input "H" current		VI = 3 V, V$_{CC}$ = 3.0 V		−	−	4.0	μA
I$_{IL}$	Input "L" current		VI = 0 V, V$_{CC}$ = 3.0 V		−	−	−4.0	μA
R$_{PULLUP}$	Pull-up resistance		VI = 0 V, V$_{CC}$ = 3.0 V		42	84	168	kΩ
R$_{fXIN}$	Feedback resistance	XIN			−	0.3	−	MΩ
R$_{fXCIN}$	Feedback resistance	XCIN			−	8	−	MΩ
V$_{RAM}$	RAM hold voltage		During stop mode		1.8	−	−	V

Note:
1. 2.7 V ≤ V$_{CC}$ < 4.2 V and T$_{opr}$ = −20 to 85°C (N version) / −40 to 85°C (D version), f(XIN) = 10 MHz, unless otherwise specified.

Table 5.29   Electrical Characteristics (5) [1.8 V ≤ Vcc < 2.7 V]

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
VOH	Output "H" voltage	Other than XOUT	Drive capacity High	IOH = −2 mA	Vcc − 0.5	–	Vcc	V
			Drive capacity Low	IOH = −1 mA	Vcc − 0.5	–	Vcc	V
		XOUT		IOH = −200 μA	1.0	–	Vcc	V
VOL	Output "L" voltage	Other than XOUT	Drive capacity High	IOL = 2 mA	–	–	0.5	V
			Drive capacity Low	IOL = 1 mA	–	–	0.5	V
		XOUT		IOL = 200 μA	–	–	0.5	V
VT+-VT-	Hysteresis	INT0, INT1, INT2, INT3, INT4, KI0, KI1, KI2, KI3, TRAIO, TRBO, TRCIOA, TRCIOB, TRCIOC, TRCIOD, TRDIOA0, TRDIOB0, TRDIOC0, TRDIOD0, TRDIOA1, TRDIOB1, TRDIOC1, TRDIOD1, TRCTRG, TRCCLK, ADTRG, RXD0, RXD1, RXD2, CLK0, CLK1, CLK2, SSI, SCL, SDA, SSO			0.05	0.2	–	V
		RESET			0.05	0.20	–	V
IIH	Input "H" current		VI = 2.2 V, Vcc = 2.2 V		–	–	4.0	μA
IIL	Input "L" current		VI = 0 V, Vcc = 2.2 V		–	–	−4.0	μA
RPULLUP	Pull-up resistance		VI = 0 V, Vcc = 2.2 V		70	140	300	kΩ
RfXIN	Feedback resistance	XIN			–	0.3	–	MΩ
RfXCIN	Feedback resistance	XCIN			–	8	–	MΩ
VRAM	RAM hold voltage		During stop mode		1.8	–	–	V

Note:
1. 1.8 V ≤ Vcc < 2.7 V and Topr = −20 to 85°C (N version) / −40 to 85°C (D version), f(XIN) = 5 MHz, unless otherwise specified.

REVISION HISTORY		R8C/35C Group Datasheet		

Rev.	Date	Description		
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1.00	Aug. 24, 2010	All	"Preliminary" and "Under development" deleted	
		4	Table1.3 revised	
		27 to 53	5. Electrical Characteristics added	

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