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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I ² C, LINbus, SIO, SSU, UART/USART
Peripherals	POR, PWM, Voltage Detect, WDT
Number of I/O	47
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	2.5K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 12x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	52-LQFP
Supplier Device Package	52-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f21356cnfp-v2

1.1.2 Specifications

Tables 1.1 and 1.2 outline the Specifications for R8C/35C Group.

Table 1.1 Specifications for R8C/35C Group (1)

Item	Function	Specification
CPU	Central processing unit	R8C CPU core <ul style="list-style-type: none"> • Number of fundamental instructions: 89 • Minimum instruction execution time: <ul style="list-style-type: none"> 50 ns ($f(XIN) = 20\text{ MHz}$, $VCC = 2.7\text{ to }5.5\text{ V}$) 200 ns ($f(XIN) = 5\text{ MHz}$, $VCC = 1.8\text{ to }5.5\text{ V}$) • Multiplier: 16 bits \times 16 bits \rightarrow 32 bits • Multiply-accumulate instruction: 16 bits \times 16 bits + 32 bits \rightarrow 32 bits • Operation mode: Single-chip mode (address space: 1 Mbyte)
Memory	ROM, RAM, Data flash	Refer to Table 1.3 Product List for R8C/35C Group .
Power Supply Voltage Detection	Voltage detection circuit	<ul style="list-style-type: none"> • Power-on reset • Voltage detection 3 (detection level of voltage detection 0 and voltage detection 1 selectable)
I/O Ports	Programmable I/O ports	<ul style="list-style-type: none"> • Input-only: 1 pin • CMOS I/O ports: 47, selectable pull-up resistor • High current drive ports: 47
Clock	Clock generation circuits	4 circuits: XIN clock oscillation circuit, XCIN clock oscillation circuit (32 kHz), High-speed on-chip oscillator (with frequency adjustment function), Low-speed on-chip oscillator <ul style="list-style-type: none"> • Oscillation stop detection: XIN clock oscillation stop detection function • Frequency divider circuit: Dividing selectable 1, 2, 4, 8, and 16 • Low power consumption modes: <ul style="list-style-type: none"> Standard operating mode (high-speed clock, low-speed clock, high-speed on-chip oscillator, low-speed on-chip oscillator), wait mode, stop mode
Interrupts		Real-time clock (timer RE) <ul style="list-style-type: none"> • Number of interrupt vectors: 69 • External Interrupt: 9 (INT \times 5, Key input \times 4) • Priority levels: 7 levels
Watchdog Timer		<ul style="list-style-type: none"> • 14 bits \times 1 (with prescaler) • Reset start selectable • Low-speed on-chip oscillator for watchdog timer selectable
DTC (Data Transfer Controller)		<ul style="list-style-type: none"> • 1 channel • Activation sources: 33 • Transfer modes: 2 (normal mode, repeat mode)
Timer	Timer RA	8 bits \times 1 (with 8-bit prescaler) Timer mode (period timer), pulse output mode (output level inverted every period), event counter mode, pulse width measurement mode, pulse period measurement mode
	Timer RB	8 bits \times 1 (with 8-bit prescaler) Timer mode (period timer), programmable waveform generation mode (PWM output), programmable one-shot generation mode, programmable wait one-shot generation mode
	Timer RC	16 bits \times 1 (with 4 capture/compare registers) Timer mode (input capture function, output compare function), PWM mode (output 3 pins), PWM2 mode (PWM output pin)
	Timer RD	16 bits \times 2 (with 4 capture/compare registers) Timer mode (input capture function, output compare function), PWM mode (output 6 pins), reset synchronous PWM mode (output three-phase waveforms (6 pins), sawtooth wave modulation), complementary PWM mode (output three-phase waveforms (6 pins), triangular wave modulation), PWM3 mode (PWM output 2 pins with fixed period)
	Timer RE	8 bits \times 1 Real-time clock mode (count seconds, minutes, hours, days of week), output compare mode

Table 1.5 Pin Name Information by Pin Number (2)

Pin Number	Control Pin	Port	I/O Pin Functions for Peripheral Modules					
			Interrupt	Timer	Serial Interface	SSU	I ² C bus	A/D Converter, D/A Converter, Comparator B
36		P1_2	$\overline{KI2}$	(TRCIOB)				AN10
37		P1_1	$\overline{KI1}$	(TRCIOA/TRCTRG)				AN9
38		P1_0	$\overline{KI0}$	(TRCIOD)				AN8
39		P0_7		(TRCIOA)				AN0/DA1
40		P0_6		(TRCIOD)				AN1/DA0
41		P0_5		(TRCIOB)				AN2
42		P0_4		TREO (/TRCIOB)				AN3
43		P0_3		(TRCIOB)	(CLK1)			AN4
44		P0_2		(TRCIOA/TRCTRG)	(RXD1)			AN5
45		P0_1		(TRCIOA/TRCTRG)	(TXD1)			AN6
46		P0_0		(TRCIOA/TRCTRG)				AN7
47		P6_4			(RXD1)			
48		P6_3			(TXD1)			
49		P6_2			(CLK1)			
50		P6_1						
51		P6_0		(TREO)				
52		P5_7						

Note:

1. Can be assigned to the pin in parentheses by a program.

1.5 Pin Functions

Tables 1.6 and 1.7 list Pin Functions.

Table 1.6 Pin Functions (1)

Item	Pin Name	I/O Type	Description
Power supply input	VCC, VSS	–	Apply 1.8 V to 5.5 V to the VCC pin. Apply 0 V to the VSS pin.
Analog power supply input	AVCC, AVSS	–	Power supply for the A/D converter. Connect a capacitor between AVCC and AVSS.
Reset input	$\overline{\text{RESET}}$	I	Input “L” on this pin resets the MCU.
MODE	MODE	I	Connect this pin to VCC via a resistor.
XIN clock input	XIN	I	These pins are provided for XIN clock generation circuit I/O. Connect a ceramic resonator or a crystal oscillator between the XIN and XOUT pins ⁽¹⁾ . To use an external clock, input it to the XOUT pin and leave the XIN pin open.
XIN clock output	XOUT	I/O	
XCIN clock input	XCIN	I	These pins are provided for XCIN clock generation circuit I/O. Connect a crystal oscillator between the XCIN and XCOU pins ⁽¹⁾ . To use an external clock, input it to the XCIN pin and leave the XCOU pin open.
XCIN clock output	XCOU	O	
$\overline{\text{INT}}$ interrupt input	$\overline{\text{INT0}}$ to $\overline{\text{INT4}}$	I	$\overline{\text{INT}}$ interrupt input pins. $\overline{\text{INT0}}$ is timer RB, RC and RD input pin.
Key input interrupt	$\overline{\text{KI0}}$ to $\overline{\text{KI3}}$	I	Key input interrupt input pins
Timer RA	TRAIO	I/O	Timer RA I/O pin
	TRA0	O	Timer RA output pin
Timer RB	TRBO	O	Timer RB output pin
Timer RC	TRCLK	I	External clock input pin
	TRCTR	I	External trigger input pin
	TRCIOA, TRCIOB, TRCIO, TRCIOD	I/O	Timer RC I/O pins
Timer RD	TRDIOA0, TRDIOA1, TRDIOB0, TRDIOB1, TRDIOC0, TRDIOC1, TRDIOD0, TRDIOD1	I/O	Timer RD I/O pins
	TRDCLK	I	External clock input pin
Timer RE	TREO	O	Divided clock output pin
Serial interface	CLK0, CLK1, CLK2	I/O	Transfer clock I/O pins
	RXD0, RXD1, RXD2	I	Serial data input pins
	TXD0, TXD1, TXD2	O	Serial data output pins
	$\overline{\text{CTS2}}$	I	Transmission control input pin
	$\overline{\text{RTS2}}$	O	Reception control output pin
	SCL2	I/O	I ² C mode clock I/O pin
	SDA2	I/O	I ² C mode data I/O pin
I ² C bus	SCL	I/O	Clock I/O pin
	SDA	I/O	Data I/O pin
SSU	SSI	I/O	Data I/O pin
	$\overline{\text{SCS}}$	I/O	Chip-select signal I/O pin
	SSCK	I/O	Clock I/O pin
	SSO	I/O	Data I/O pin

I: Input O: Output I/O: Input and output

Note:

1. Refer to the oscillator manufacturer for oscillation characteristics.

4. Special Function Registers (SFRs)

An SFR (special function register) is a control register for a peripheral function. Tables 4.1 to 4.12 list the special function registers and Table 4.13 lists the ID Code Areas and Option Function Select Area.

Table 4.1 SFR Information (1) (1)

Address	Register	Symbol	After Reset
0000h			
0001h			
0002h			
0003h			
0004h	Processor Mode Register 0	PM0	00h
0005h	Processor Mode Register 1	PM1	00h
0006h	System Clock Control Register 0	CM0	00101000b
0007h	System Clock Control Register 1	CM1	00100000b
0008h	Module Standby Control Register	MSTCR	00h
0009h	System Clock Control Register 3	CM3	00h
000Ah	Protect Register	PRCR	00h
000Bh	Reset Source Determination Register	RSTFR	0XXXXXXb (2)
000Ch	Oscillation Stop Detection Register	OCD	00000100b
000Dh	Watchdog Timer Reset Register	WDTR	XXh
000Eh	Watchdog Timer Start Register	WDTS	XXh
000Fh	Watchdog Timer Control Register	WDTC	00111111b
0010h			
0011h			
0012h			
0013h			
0014h			
0015h	High-Speed On-Chip Oscillator Control Register 7	FRA7	When shipping
0016h			
0017h			
0018h			
0019h			
001Ah			
001Bh			
001Ch	Count Source Protection Mode Register	CSPR	00h 10000000b (3)
001Dh			
001Eh			
001Fh			
0020h			
0021h			
0022h			
0023h	High-Speed On-Chip Oscillator Control Register 0	FRA0	00h
0024h	High-Speed On-Chip Oscillator Control Register 1	FRA1	When shipping
0025h	High-Speed On-Chip Oscillator Control Register 2	FRA2	00h
0026h	On-Chip Reference Voltage Control Register	OCVREFCR	00h
0027h			
0028h	Clock Prescaler Reset Flag	CPSRF	00h
0029h	High-Speed On-Chip Oscillator Control Register 4	FRA4	When Shipping
002Ah	High-Speed On-Chip Oscillator Control Register 5	FRA5	When Shipping
002Bh	High-Speed On-Chip Oscillator Control Register 6	FRA6	When Shipping
002Ch			
002Dh			
002Eh			
002Fh	High-Speed On-Chip Oscillator Control Register 3	FRA3	When shipping
0030h	Voltage Monitor Circuit Control Register	CMPA	00h
0031h	Voltage Monitor Circuit Edge Select Register	VCAC	00h
0032h			
0033h	Voltage Detect Register 1	VCA1	00001000b
0034h	Voltage Detect Register 2	VCA2	00h (4) 00100000b (5)
0035h			
0036h	Voltage Detection 1 Level Select Register	VD1LS	00000111b
0037h			
0038h	Voltage Monitor 0 Circuit Control Register	VW0C	1100X010b (4) 1100X011b (5)
0039h	Voltage Monitor 1 Circuit Control Register	VW1C	10001010b

X: Undefined

Notes:

1. The blank areas are reserved and cannot be accessed by users.
2. The CWR bit in the RSTFR register is set to 0 after power-on and voltage monitor 0 reset. Hardware reset, software reset, or watchdog timer reset does not affect this bit.
3. The CSPROINI bit in the OFS register is set to 0.
4. The LVDAS bit in the OFS register is set to 1.
5. The LVDAS bit in the OFS register is set to 0.

Table 4.7 SFR Information (7) ⁽¹⁾

Address	Register	Symbol	After Reset
0180h	Timer RA Pin Select Register	TRASR	00h
0181h	Timer RB/RC Pin Select Register	TRBRCSR	00h
0182h	Timer RC Pin Select Register 0	TRCPSR0	00h
0183h	Timer RC Pin Select Register 1	TRCPSR1	00h
0184h	Timer RD Pin Select Register 0	TRDPSR0	00h
0185h	Timer RD Pin Select Register 1	TRDPSR1	00h
0186h	Timer Pin Select Register	TIMSR	00h
0187h			
0188h	UART0 Pin Select Register	U0SR	00h
0189h	UART1 Pin Select Register	U1SR	00h
018Ah	UART2 Pin Select Register 0	U2SR0	00h
018Bh	UART2 Pin Select Register 1	U2SR1	00h
018Ch	SSU/IIC Pin Select Register	SSUICSR	00h
018Dh			
018Eh	INT Interrupt Input Pin Select Register	INTSR	00h
018Fh	I/O Function Pin Select Register	PINSR	00h
0190h			
0191h			
0192h			
0193h	SS Bit Counter Register	SSBR	11111000b
0194h	SS Transmit Data Register L / IIC bus Transmit Data Register ⁽²⁾	SSTDR / ICDRT	FFh
0195h	SS Transmit Data Register H ⁽²⁾	SSTDRH	FFh
0196h	SS Receive Data Register L / IIC bus Receive Data Register ⁽²⁾	SSRDR / ICDRR	FFh
0197h	SS Receive Data Register H ⁽²⁾	SSRDRH	FFh
0198h	SS Control Register H / IIC bus Control Register 1 ⁽²⁾	SSCRH / ICCR1	00h
0199h	SS Control Register L / IIC bus Control Register 2 ⁽²⁾	SSCRL / ICCR2	01111101b
019Ah	SS Mode Register / IIC bus Mode Register ⁽²⁾	SSMR / ICMR	00010000b / 00011000b
019Bh	SS Enable Register / IIC bus Interrupt Enable Register ⁽²⁾	SSER / ICIER	00h
019Ch	SS Status Register / IIC bus Status Register ⁽²⁾	SSSR / ICSR	00h / 0000X000b
019Dh	SS Mode Register 2 / Slave Address Register ⁽²⁾	SSMR2 / SAR	00h
019Eh			
019Fh			
01A0h			
01A1h			
01A2h			
01A3h			
01A4h			
01A5h			
01A6h			
01A7h			
01A8h			
01A9h			
01AAh			
01ABh			
01ACh			
01ADh			
01AEh			
01AFh			
01B0h			
01B1h			
01B2h	Flash Memory Status Register	FST	10000X00b
01B3h			
01B4h	Flash Memory Control Register 0	FMR0	00h
01B5h	Flash Memory Control Register 1	FMR1	00h
01B6h	Flash Memory Control Register 2	FMR2	00h
01B7h			
01B8h			
01B9h			
01BAh			
01BBh			
01BCh			
01BDh			
01BEh			
01BFh			

X: Undefined

Notes:

1. The blank areas are reserved and cannot be accessed by users.
2. Selectable by the IICSEL bit in the SSUICSR register.

Table 4.10 SFR Information (10) (1)

Address	Register	Symbol	After Reset
2C70h	DTC Control Data 6	DTCD6	XXh
2C71h			XXh
2C72h			XXh
2C73h			XXh
2C74h			XXh
2C75h			XXh
2C76h			XXh
2C77h			XXh
2C78h	DTC Control Data 7	DTCD7	XXh
2C79h			XXh
2C7Ah			XXh
2C7Bh			XXh
2C7Ch			XXh
2C7Dh			XXh
2C7Eh			XXh
2C7Fh			XXh
2C80h	DTC Control Data 8	DTCD8	XXh
2C81h			XXh
2C82h			XXh
2C83h			XXh
2C84h			XXh
2C85h			XXh
2C86h			XXh
2C87h			XXh
2C88h	DTC Control Data 9	DTCD9	XXh
2C89h			XXh
2C8Ah			XXh
2C8Bh			XXh
2C8Ch			XXh
2C8Dh			XXh
2C8Eh			XXh
2C8Fh			XXh
2C90h	DTC Control Data 10	DTCD10	XXh
2C91h			XXh
2C92h			XXh
2C93h			XXh
2C94h			XXh
2C95h			XXh
2C96h			XXh
2C97h			XXh
2C98h	DTC Control Data 11	DTCD11	XXh
2C99h			XXh
2C9Ah			XXh
2C9Bh			XXh
2C9Ch			XXh
2C9Dh			XXh
2C9Eh			XXh
2C9Fh			XXh
2CA0h	DTC Control Data 12	DTCD12	XXh
2CA1h			XXh
2CA2h			XXh
2CA3h			XXh
2CA4h			XXh
2CA5h			XXh
2CA6h			XXh
2CA7h			XXh
2CA8h	DTC Control Data 13	DTCD13	XXh
2CA9h			XXh
2CAAh			XXh
2CABh			XXh
2CACH			XXh
2CADh			XXh
2CAEh			XXh
2CAFh			XXh

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.12 SFR Information (12) ⁽¹⁾

Address	Register	Symbol	After Reset
2CF0h	DTC Control Data 22	DTCD22	XXh
2CF1h			XXh
2CF2h			XXh
2CF3h			XXh
2CF4h			XXh
2CF5h			XXh
2CF6h			XXh
2CF7h			XXh
2CF8h	DTC Control Data 23	DTCD23	XXh
2CF9h			XXh
2CFAh			XXh
2CFBh			XXh
2CFCh			XXh
2CFDh			XXh
2CFEh			XXh
2CFFh			XXh
2D00h			
⋮			
2FFFh			

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.13 ID Code Areas and Option Function Select Area

Address	Area Name	Symbol	After Reset
⋮			
FFDBh	Option Function Select Register 2	OFS2	(Note 1)
⋮			
FFDFh	ID1		(Note 2)
⋮			
FFE3h	ID2		(Note 2)
⋮			
FFEBh	ID3		(Note 2)
⋮			
FFEFh	ID4		(Note 2)
⋮			
FFF3h	ID5		(Note 2)
⋮			
FFF7h	ID6		(Note 2)
⋮			
FFFBh	ID7		(Note 2)
⋮			
FFFFh	Option Function Select Register	OFS	(Note 1)

Notes:

1. The option function select area is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program. Do not write additions to the option function select area. If the block including the option function select area is erased, the option function select area is set to FFh. When blank products are shipped, the option function select area is set to FFh. It is set to the written value after written by the user. When factory-programming products are shipped, the value of the option function select area is the value programmed by the user.
2. The ID code areas are allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program. Do not write additions to the ID code areas. If the block including the ID code areas is erased, the ID code areas are set to FFh. When blank products are shipped, the ID code areas are set to FFh. They are set to the written value after written by the user. When factory-programming products are shipped, the value of the ID code areas is the value programmed by the user.

Table 5.4 D/A Converter Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
—	Resolution		—	—	8	Bit
—	Absolute accuracy		—	—	2.5	LSB
t_{su}	Setup time		—	—	3	μs
R_o	Output resistor		—	6	—	$k\Omega$
I_{Vref}	Reference power input current	(Note 2)	—	—	1.5	mA

Notes:

1. $V_{CC}/AV_{CC} = V_{ref} = 2.7$ to 5.5 V and $T_{opr} = -20$ to $85^{\circ}C$ (N version) / -40 to $85^{\circ}C$ (D version), unless otherwise specified.
2. This applies when one D/A converter is used and the value of the DA_i register ($i = 0$ or 1) for the unused D/A converter is $00h$. The resistor ladder of the A/D converter is not included.

Table 5.5 Comparator B Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{ref}	$IVREF1$, $IVREF3$ input reference voltage		0	—	$V_{CC} - 1.4$	V
V_I	$IVCMP1$, $IVCMP3$ input voltage		-0.3	—	$V_{CC} + 0.3$	V
—	Offset		—	5	100	mV
t_d	Comparator output delay time ⁽²⁾	$V_I = V_{ref} \pm 100$ mV	—	0.1	—	μs
I_{CMP}	Comparator operating current	$V_{CC} = 5.0$ V	—	17.5	—	μA

Notes:

1. $V_{CC} = 2.7$ to 5.5 V, $T_{opr} = -20$ to $85^{\circ}C$ (N version) / -40 to $85^{\circ}C$ (D version), unless otherwise specified.
2. When the digital filter is disabled.

Table 5.6 Flash Memory (Program ROM) Electrical Characteristics

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
—	Program/erase endurance ⁽²⁾		1,000 ⁽³⁾	—	—	times
—	Byte program time		—	80	500	μs
—	Block erase time		—	0.3	—	s
t _d (SR-SUS)	Time delay from suspend request until suspend		—	—	5+CPU clock × 3 cycles	ms
—	Interval from erase start/restart until following suspend request		0	—	—	μs
—	Time from suspend until erase restart		—	—	30+CPU clock × 1 cycle	μs
t _d (CMDRST-READY)	Time from when command is forcibly terminated until reading is enabled		—	—	30+CPU clock × 1 cycle	μs
—	Program, erase voltage		2.7	—	5.5	V
—	Read voltage		1.8	—	5.5	V
—	Program, erase temperature		0	—	60	°C
—	Data hold time ⁽⁷⁾	Ambient temperature = 55°C	20	—	—	year

Notes:

1. V_{CC} = 2.7 to 5.5 V and T_{opr} = 0 to 60°C, unless otherwise specified.

2. Definition of programming/erasure endurance

The programming and erasure endurance is defined on a per-block basis.

If the programming and erasure endurance is n (n = 1,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.

However, the same address must not be programmed more than once per erase operation (overwriting prohibited).

3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).

4. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.

5. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.

6. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.

7. The data hold time includes time that the power supply is off or the clock is not supplied.

Table 5.7 Flash Memory (Data flash Block A to Block D) Electrical Characteristics

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
—	Program/erase endurance ⁽²⁾		10,000 ⁽³⁾	—	—	times
—	Byte program time (program/erase endurance ≤ 1,000 times)		—	160	1,500	μs
—	Byte program time (program/erase endurance > 1,000 times)		—	300	1,500	μs
—	Block erase time (program/erase endurance ≤ 1,000 times)		—	0.2	1	s
—	Block erase time (program/erase endurance > 1,000 times)		—	0.3	1	s
t _d (SR-SUS)	Time delay from suspend request until suspend		—	—	5+CPU clock × 3 cycles	ms
—	Interval from erase start/restart until following suspend request		0	—	—	μs
—	Time from suspend until erase restart		—	—	30+CPU clock × 1 cycle	μs
t _d (CMDRST-READY)	Time from when command is forcibly terminated until reading is enabled		—	—	30+CPU clock × 1 cycle	μs
—	Program, erase voltage		2.7	—	5.5	V
—	Read voltage		1.8	—	5.5	V
—	Program, erase temperature		−20 ⁽⁷⁾	—	85	°C
—	Data hold time ⁽⁸⁾	Ambient temperature = 55 °C	20	—	—	year

Notes:

1. V_{CC} = 2.7 to 5.5 V and T_{opr} = −20 to 85°C (N version) / −40 to 85°C (D version), unless otherwise specified.
2. Definition of programming/erasure endurance
The programming and erasure endurance is defined on a per-block basis.
If the programming and erasure endurance is n (n = 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.
However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
4. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. In addition, averaging the erasure endurance between blocks A to D can further reduce the actual erasure endurance. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
5. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
6. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
7. −40°C for D version.
8. The data hold time includes time that the power supply is off or the clock is not supplied.

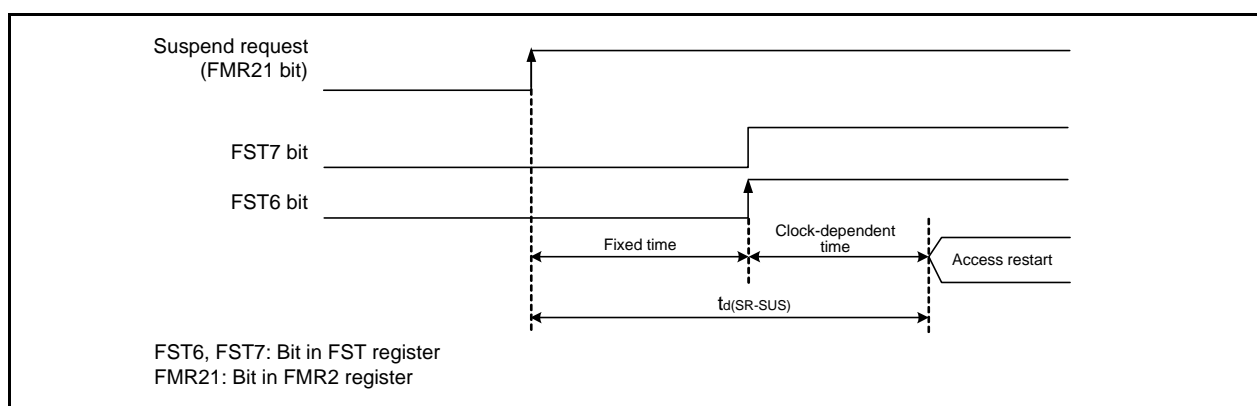
**Figure 5.2 Time delay until Suspend**

Table 5.8 Voltage Detection 0 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V _{det0}	Voltage detection level V _{det0_0} (2)		1.80	1.90	2.05	V
	Voltage detection level V _{det0_1} (2)		2.15	2.35	2.50	V
	Voltage detection level V _{det0_2} (2)		2.70	2.85	3.05	V
	Voltage detection level V _{det0_3} (2)		3.55	3.80	4.05	V
—	Voltage detection 0 circuit response time (4)	At the falling of V _{CC} from 5 V to (V _{det0_0} – 0.1) V	—	6	150	μs
—	Voltage detection circuit self power consumption	VCA25 = 1, V _{CC} = 5.0 V	—	1.5	—	μA
t _{d(E-A)}	Waiting time until voltage detection circuit operation starts (3)		—	—	100	μs

Notes:

1. The measurement condition is V_{CC} = 1.8 V to 5.5 V and T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version).
2. Select the voltage detection level with bits VDSEL0 and VDSEL1 in the OFS register.
3. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA25 bit in the VCA2 register to 0.
4. Time until the voltage monitor 0 reset is generated after the voltage passes V_{det0}.

Table 5.9 Voltage Detection 1 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V _{det1}	Voltage detection level V _{det1_0} (2)	At the falling of V _{CC}	2.00	2.20	2.40	V
	Voltage detection level V _{det1_1} (2)	At the falling of V _{CC}	2.15	2.35	2.55	V
	Voltage detection level V _{det1_2} (2)	At the falling of V _{CC}	2.30	2.50	2.70	V
	Voltage detection level V _{det1_3} (2)	At the falling of V _{CC}	2.45	2.65	2.85	V
	Voltage detection level V _{det1_4} (2)	At the falling of V _{CC}	2.60	2.80	3.00	V
	Voltage detection level V _{det1_5} (2)	At the falling of V _{CC}	2.75	2.95	3.15	V
	Voltage detection level V _{det1_6} (2)	At the falling of V _{CC}	2.85	3.10	3.40	V
	Voltage detection level V _{det1_7} (2)	At the falling of V _{CC}	3.00	3.25	3.55	V
	Voltage detection level V _{det1_8} (2)	At the falling of V _{CC}	3.15	3.40	3.70	V
	Voltage detection level V _{det1_9} (2)	At the falling of V _{CC}	3.30	3.55	3.85	V
	Voltage detection level V _{det1_A} (2)	At the falling of V _{CC}	3.45	3.70	4.00	V
	Voltage detection level V _{det1_B} (2)	At the falling of V _{CC}	3.60	3.85	4.15	V
	Voltage detection level V _{det1_C} (2)	At the falling of V _{CC}	3.75	4.00	4.30	V
	Voltage detection level V _{det1_D} (2)	At the falling of V _{CC}	3.90	4.15	4.45	V
	Voltage detection level V _{det1_E} (2)	At the falling of V _{CC}	4.05	4.30	4.60	V
	Voltage detection level V _{det1_F} (2)	At the falling of V _{CC}	4.20	4.45	4.75	V
—	Hysteresis width at the rising of V _{CC} in voltage detection 1 circuit	V _{det1_0} to V _{det1_5} selected	—	0.07	—	V
		V _{det1_6} to V _{det1_F} selected	—	0.10	—	V
—	Voltage detection 1 circuit response time (3)	At the falling of V _{CC} from 5 V to (V _{det1_0} – 0.1) V	—	60	150	μs
—	Voltage detection circuit self power consumption	VCA26 = 1, V _{CC} = 5.0 V	—	1.7	—	μA
t _{d(E-A)}	Waiting time until voltage detection circuit operation starts (4)		—	—	100	μs

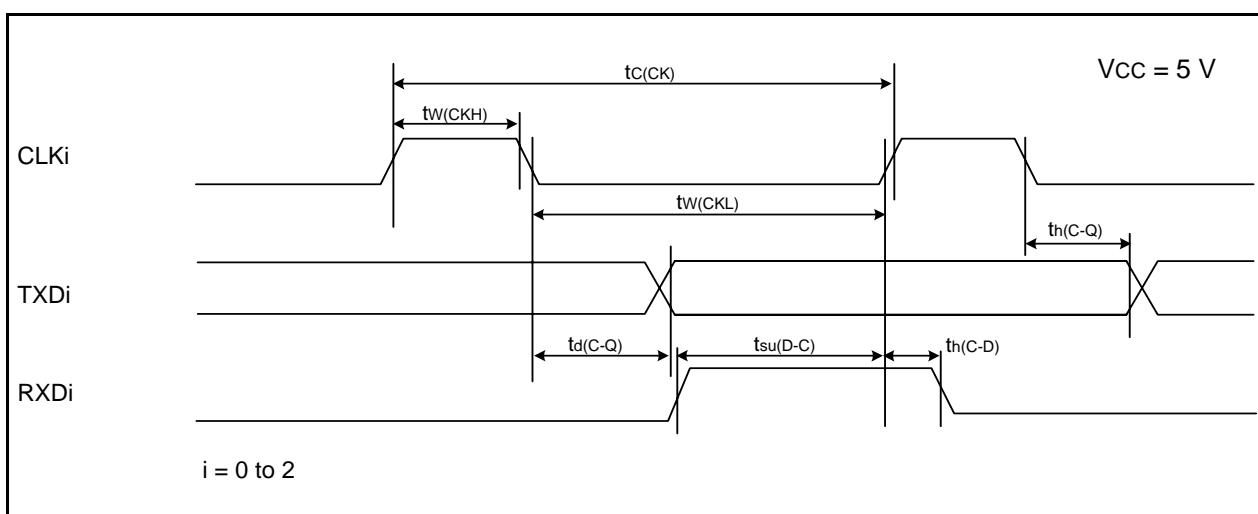
Notes:

1. The measurement condition is V_{CC} = 1.8 V to 5.5 V and T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version).
2. Select the voltage detection level with bits VD1S0 to VD1S3 in the VD1LS register.
3. Time until the voltage monitor 1 interrupt request is generated after the voltage passes V_{det1}.
4. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA26 bit in the VCA2 register to 0.

Table 5.21 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	200	—	ns
$t_{w(CKH)}$	CLKi input "H" width	100	—	ns
$t_{w(CKL)}$	CLKi input "L" width	100	—	ns
$t_{d(C-Q)}$	TXDi output delay time	—	50	ns
$t_{h(C-Q)}$	TXDi hold time	0	—	ns
$t_{su(D-C)}$	RXDi input setup time	50	—	ns
$t_{h(C-D)}$	RXDi input hold time	90	—	ns

i = 0 to 2

**Figure 5.10 Serial Interface Timing Diagram when Vcc = 5 V****Table 5.22 External Interrupt \overline{INTi} (i = 0 to 4) Input, Key Input Interrupt \overline{Kli} (i = 0 to 3)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	\overline{INTi} input "H" width, \overline{Kli} input "H" width	250 (1)	—	ns
$t_{w(INL)}$	\overline{INTi} input "L" width, \overline{Kli} input "L" width	250 (2)	—	ns

Notes:

1. When selecting the digital filter by the \overline{INTi} input filter select bit, use an \overline{INTi} input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the \overline{INTi} input filter select bit, use an \overline{INTi} input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

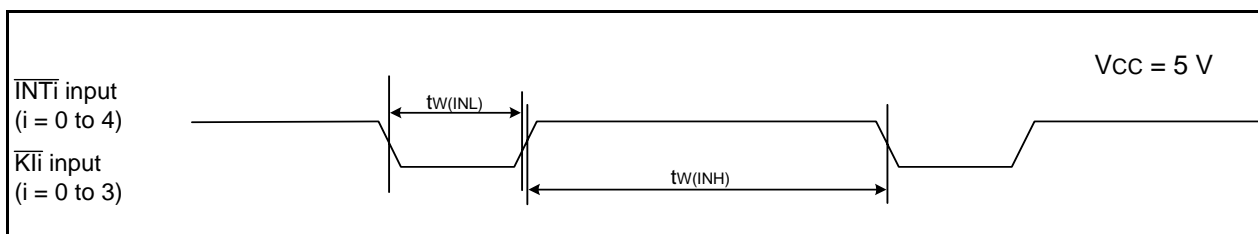
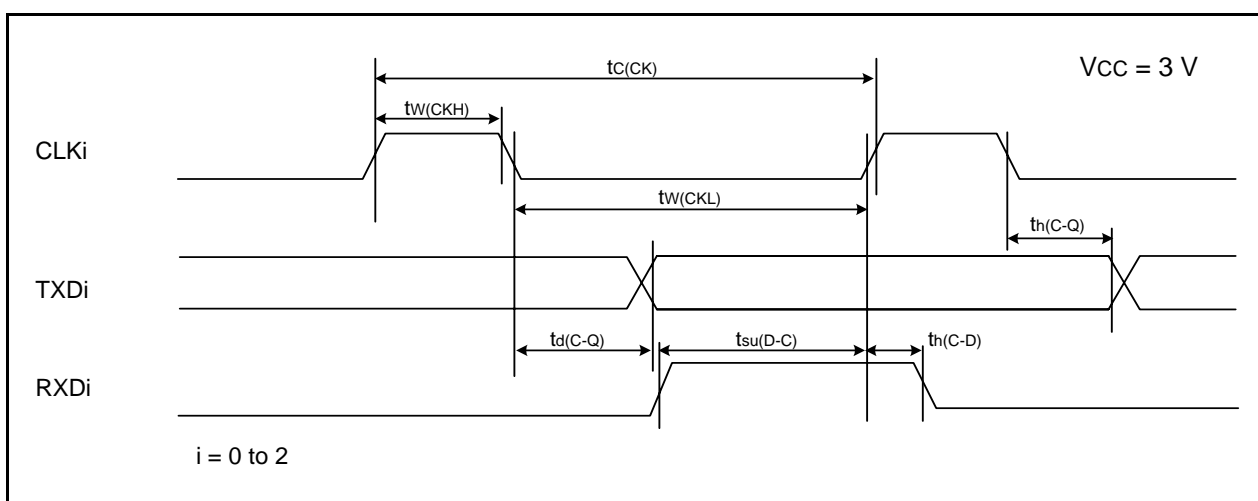
**Figure 5.11 Input Timing Diagram for External Interrupt \overline{INTi} and Key Input Interrupt \overline{Kli} when Vcc = 5 V**

Table 5.27 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	300	—	ns
$t_{w(CKH)}$	CLKi input "H" width	150	—	ns
$t_{w(CKL)}$	CLKi Input "L" width	150	—	ns
$t_{d(C-Q)}$	TXDi output delay time	—	80	ns
$t_{h(C-Q)}$	TXDi hold time	0	—	ns
$t_{su(D-C)}$	RXDi input setup time	70	—	ns
$t_{h(C-D)}$	RXDi input hold time	90	—	ns

i = 0 to 2

**Figure 5.14 Serial Interface Timing Diagram when Vcc = 3 V****Table 5.28 External Interrupt \overline{INTi} (i = 0 to 4) Input, Key Input Interrupt \overline{Kli} (i = 0 to 3)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	\overline{INTi} input "H" width, \overline{Kli} input "H" width	380 (1)	—	ns
$t_{w(INL)}$	\overline{INTi} input "L" width, \overline{Kli} input "L" width	380 (2)	—	ns

Notes:

1. When selecting the digital filter by the \overline{INTi} input filter select bit, use an \overline{INTi} input HIGH width of either (1/digital filter clock frequency \times 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the \overline{INTi} input filter select bit, use an \overline{INTi} input LOW width of either (1/digital filter clock frequency \times 3) or the minimum value of standard, whichever is greater.

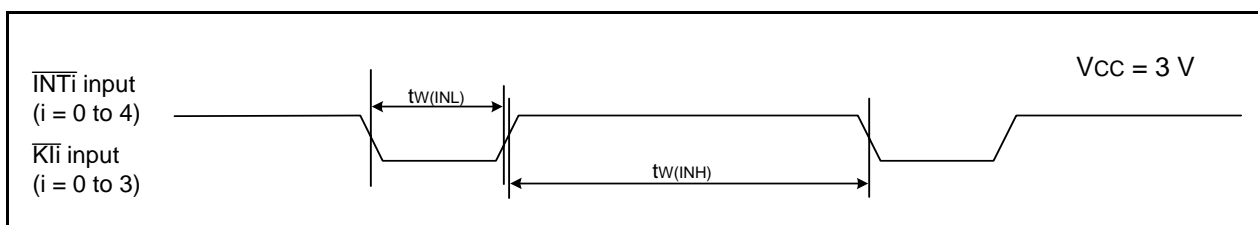
**Figure 5.15 Input Timing Diagram for External Interrupt \overline{INTi} and Key Input Interrupt \overline{Kli} when Vcc = 3 V**

Table 5.29 Electrical Characteristics (5) [$1.8\text{ V} \leq V_{CC} < 2.7\text{ V}$]

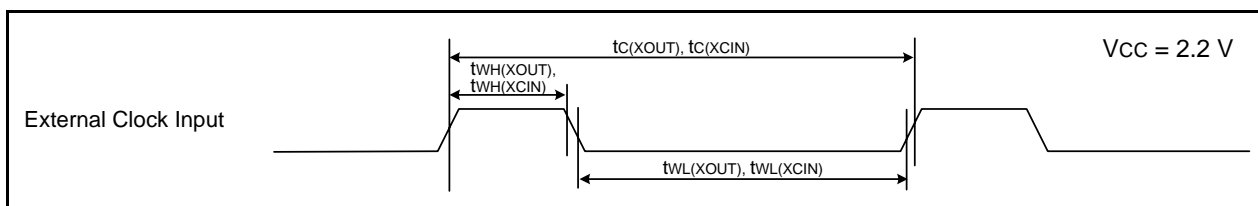
Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V _{OH}	Output "H" voltage	Other than XOUT	Drive capacity High	I _{OH} = -2 mA	V _{CC} - 0.5	—	V _{CC}	V
			Drive capacity Low	I _{OH} = -1 mA	V _{CC} - 0.5	—	V _{CC}	V
		XOUT		I _{OH} = -200 μ A	1.0	—	V _{CC}	V
V _{OL}	Output "L" voltage	Other than XOUT	Drive capacity High	I _{OL} = 2 mA	—	—	0.5	V
			Drive capacity Low	I _{OL} = 1 mA	—	—	0.5	V
		XOUT		I _{OL} = 200 μ A	—	—	0.5	V
V _{T+} -V _{T-}	Hysteresis	INT0, INT1, INT2, INT3, INT4, KI0, KI1, KI2, KI3, TRAIO, TRBO, TRCIOA, TRCIOB, TRCIOC, TRCIOD, TRDIOA0, TRDIOB0, TRDIOC0, TRDIOD0, TRDIOA1, TRDIOB1, TRDIOC1, TRDIOD1, TRCTRG, TRCCLK, ADTRG, RXD0, RXD1, RXD2, CLK0, CLK1, CLK2, SSI, SCL, SDA, SSO			0.05	0.2	—	V
		RESET			0.05	0.20	—	V
I _{IH}	Input "H" current		V _I = 2.2 V, V _{CC} = 2.2 V		—	—	4.0	μ A
I _{IL}	Input "L" current		V _I = 0 V, V _{CC} = 2.2 V		—	—	-4.0	μ A
R _{PULLUP}	Pull-up resistance		V _I = 0 V, V _{CC} = 2.2 V		70	140	300	k Ω
R _{FXIN}	Feedback resistance	XIN			—	0.3	—	M Ω
R _{FXCIN}	Feedback resistance	XCIN			—	8	—	M Ω
V _{RAM}	RAM hold voltage		During stop mode		1.8	—	—	V

Note:

1. $1.8\text{ V} \leq V_{CC} < 2.7\text{ V}$ and T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), f(XIN) = 5 MHz, unless otherwise specified.

Timing Requirements**(Unless Otherwise Specified: $V_{CC} = 2.2\text{ V}$, $V_{SS} = 0\text{ V}$ at $T_{opr} = 25^{\circ}\text{C}$)****Table 5.31 External Clock Input (XOUT, XCIN)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_c(\text{XOUT})$	XOUT input cycle time	200	–	ns
$t_{WH}(\text{XOUT})$	XOUT input “H” width	90	–	ns
$t_{WL}(\text{XOUT})$	XOUT input “L” width	90	–	ns
$t_c(\text{XCIN})$	XCIN input cycle time	14	–	μs
$t_{WH}(\text{XCIN})$	XCIN input “H” width	7	–	μs
$t_{WL}(\text{XCIN})$	XCIN input “L” width	7	–	μs

**Figure 5.16 External Clock Input Timing Diagram when $V_{CC} = 2.2\text{ V}$** **Table 5.32 TRAIO Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_c(\text{TRAIO})$	TRAIO input cycle time	500	–	ns
$t_{WH}(\text{TRAIO})$	TRAIO input “H” width	200	–	ns
$t_{WL}(\text{TRAIO})$	TRAIO input “L” width	200	–	ns

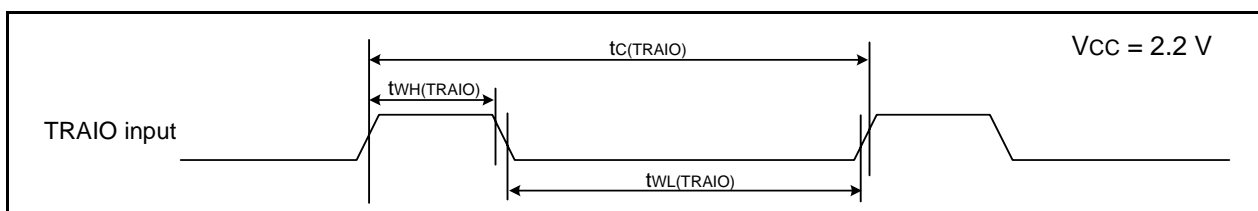
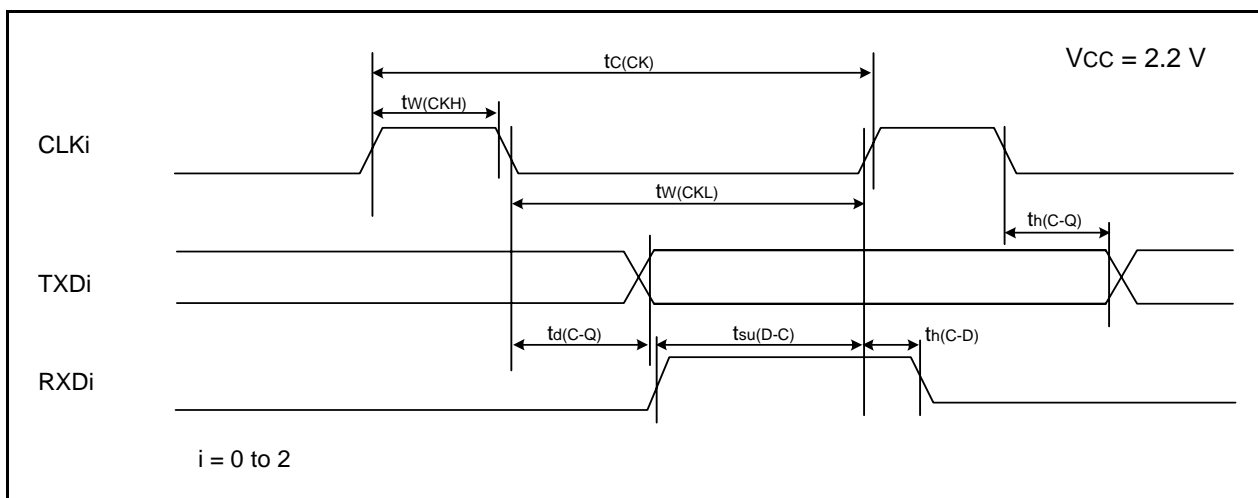
**Figure 5.17 TRAIO Input Timing Diagram when $V_{CC} = 2.2\text{ V}$**

Table 5.33 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	800	—	ns
$t_{w(CKH)}$	CLKi input "H" width	400	—	ns
$t_{w(CKL)}$	CLKi input "L" width	400	—	ns
$t_{d(C-Q)}$	TXDi output delay time	—	200	ns
$t_{h(C-Q)}$	TXDi hold time	0	—	ns
$t_{su(D-C)}$	RXDi input setup time	150	—	ns
$t_{h(C-D)}$	RXDi input hold time	90	—	ns

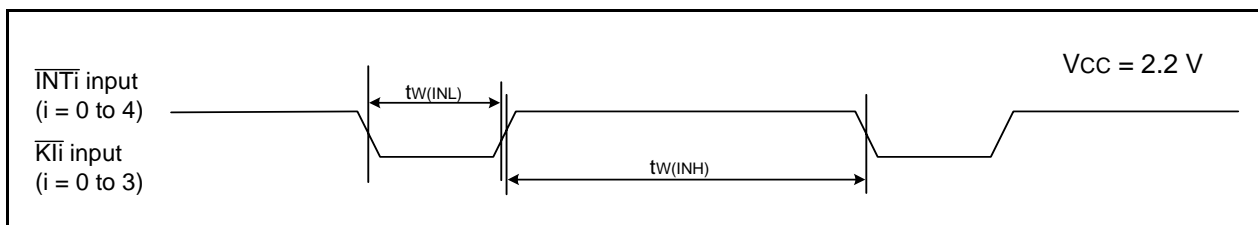
i = 0 to 2

**Figure 5.18 Serial Interface Timing Diagram when Vcc = 2.2 V****Table 5.34 External Interrupt \overline{INTi} (i = 0 to 4) Input, Key Input Interrupt \overline{Kli} (i = 0 to 3)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	\overline{INTi} input "H" width, \overline{Kli} input "H" width	1000 (1)	—	ns
$t_{w(INL)}$	\overline{INTi} input "L" width, \overline{Kli} input "L" width	1000 (2)	—	ns

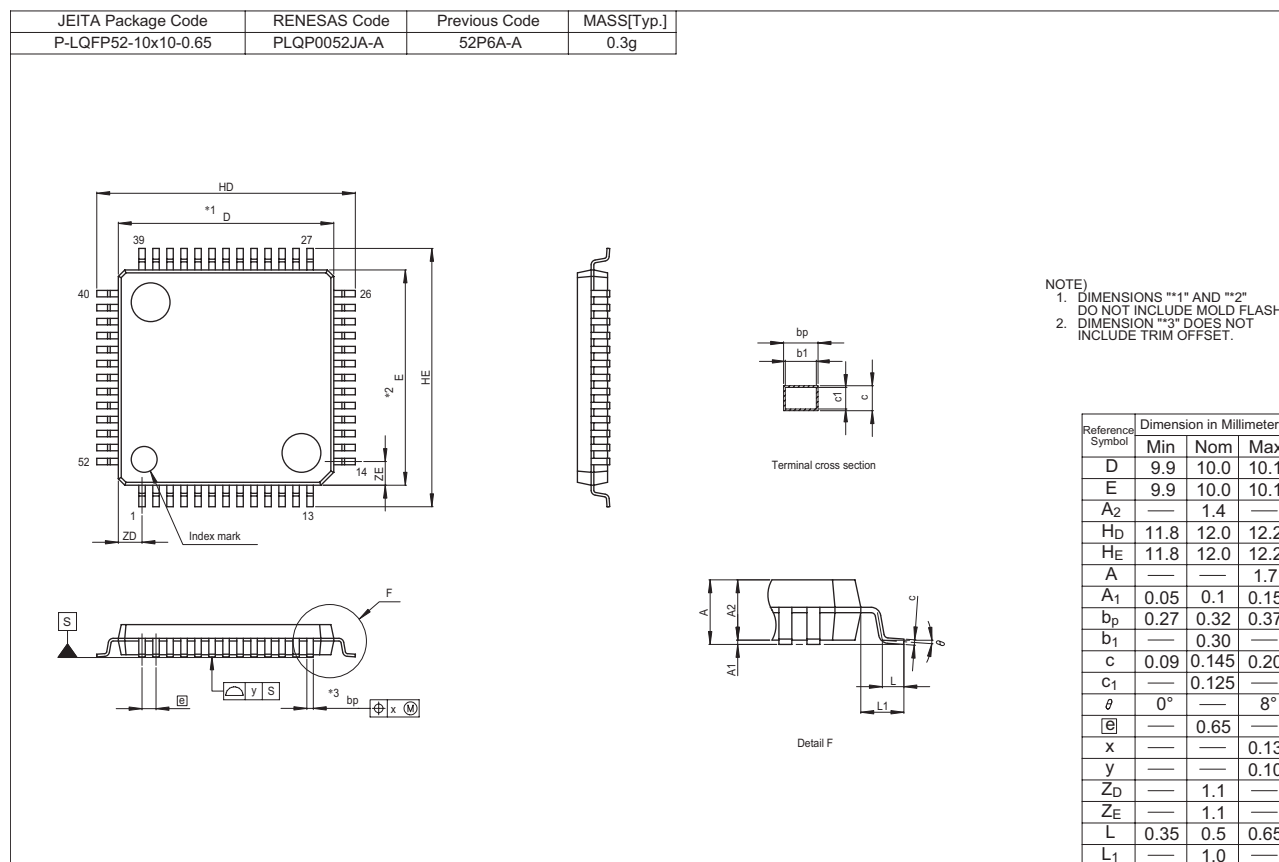
Notes:

1. When selecting the digital filter by the \overline{INTi} input filter select bit, use an \overline{INTi} input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the \overline{INTi} input filter select bit, use an \overline{INTi} input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

**Figure 5.19 Input Timing Diagram for External Interrupt \overline{INTi} and Key Input Interrupt \overline{Kli} when Vcc = 2.2 V**

Package Dimensions

Diagrams showing the latest package dimensions and mounting information are available in the “Packages” section of the Renesas Electronics website.



REVISION HISTORY	R8C/35C Group Datasheet
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Rev.	Date	Description	
		Page	Summary
0.10	Sep. 01, 2009	–	First Edition issued
1.00	Aug. 24, 2010	All 4 27 to 53	"Preliminary" and "Under development" deleted Table1.3 revised 5. Electrical Characteristics added

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General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

- The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

The state of the product is undefined at the moment when power is supplied.

- The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

Access to reserved addresses is prohibited.

- The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

- When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

- The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

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