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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I²C, LINbus, SIO, SSU, UART/USART
Peripherals	POR, PWM, Voltage Detect, WDT
Number of I/O	47
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	10K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 12x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	52-LQFP
Supplier Device Package	52-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f2135ccdfp-50

1.1.2   Specifications

Tables 1.1 and 1.2 outline the Specifications for R8C/35C Group.

Table 1.1   Specifications for R8C/35C Group (1)

Item	Function	Specification

CPU	Central processing unit	R8C CPU core
		• Number of fundamental instructions: 89
		• Minimum instruction execution time:
		    50 ns (f(XIN) = 20 MHz, VCC = 2.7 to 5.5 V)
		    200 ns (f(XIN) = 5 MHz, VCC = 1.8 to 5.5 V)
		• Multiplier: 16 bits × 16 bits → 32 bits
		• Multiply-accumulate instruction: 16 bits × 16 bits + 32 bits → 32 bits
		• Operation mode: Single-chip mode (address space: 1 Mbyte)

Memory	ROM, RAM, Data flash	Refer to **Table 1.3 Product List for R8C/35C Group**.
Power Supply Voltage Detection	Voltage detection circuit	• Power-on reset • Voltage detection 3 (detection level of voltage detection 0 and voltage detection 1 selectable)
I/O Ports	Programmable I/O ports	• Input-only: 1 pin • CMOS I/O ports: 47, selectable pull-up resistor • High current drive ports: 47

Clock	Clock generation circuits	4 circuits: XIN clock oscillation circuit,
		            XCIN clock oscillation circuit (32 kHz),
		            High-speed on-chip oscillator (with frequency adjustment function),
		            Low-speed on-chip oscillator
		• Oscillation stop detection: XIN clock oscillation stop detection function
		• Frequency divider circuit: Dividing selectable 1, 2, 4, 8, and 16
		• Low power consumption modes:
		    Standard operating mode (high-speed clock, low-speed clock, high-speed on-chip oscillator, low-speed on-chip oscillator), wait mode, stop mode

		Real-time clock (timer RE)
Interrupts		• Number of interrupt vectors: 69 • External Interrupt: 9 (INT × 5, Key input × 4) • Priority levels: 7 levels
Watchdog Timer		• 14 bits × 1 (with prescaler) • Reset start selectable • Low-speed on-chip oscillator for watchdog timer selectable
DTC (Data Transfer Controller)		• 1 channel • Activation sources: 33 • Transfer modes: 2 (normal mode, repeat mode)
Timer	Timer RA	8 bits × 1 (with 8-bit prescaler) Timer mode (period timer), pulse output mode (output level inverted every period), event counter mode, pulse width measurement mode, pulse period measurement mode
	Timer RB	8 bits × 1 (with 8-bit prescaler) Timer mode (period timer), programmable waveform generation mode (PWM output), programmable one-shot generation mode, programmable wait one-shot generation mode
	Timer RC	16 bits × 1 (with 4 capture/compare registers) Timer mode (input capture function, output compare function), PWM mode (output 3 pins), PWM2 mode (PWM output pin)
	Timer RD	16 bits × 2 (with 4 capture/compare registers) Timer mode (input capture function, output compare function), PWM mode (output 6 pins), reset synchronous PWM mode (output three-phase waveforms (6 pins), sawtooth wave modulation), complementary PWM mode (output three-phase waveforms (6 pins), triangular wave modulation), PWM3 mode (PWM output 2 pins with fixed period)
	Timer RE	8 bits × 1 Real-time clock mode (count seconds, minutes, hours, days of week), output compare mode

Table 1.5   Pin Name Information by Pin Number (2)

Pin Number	Control Pin	Port	I/O Pin Functions for Peripheral Modules					
			Interrupt	Timer	Serial Interface	SSU	I²C bus	A/D Converter, D/A Converter, Comparator B
36		P1_2	$\overline{KI2}$	(TRCIOB)				AN10
37		P1_1	$\overline{KI1}$	(TRCIOA/ TRCTRG)				AN9
38		P1_0	$\overline{KI0}$	(TRCIOD)				AN8
39		P0_7		(TRCIOC)				AN0/DA1
40		P0_6		(TRCIOD)				AN1/DA0
41		P0_5		(TRCIOB)				AN2
42		P0_4		TREO (/TRCIOB)				AN3
43		P0_3		(TRCIOB)	(CLK1)			AN4
44		P0_2		(TRCIOA/ TRCTRG)	(RXD1)			AN5
45		P0_1		(TRCIOA/ TRCTRG)	(TXD1)			AN6
46		P0_0		(TRCIOA/ TRCTRG)				AN7
47		P6_4			(RXD1)			
48		P6_3			(TXD1)			
49		P6_2			(CLK1)			
50		P6_1						
51		P6_0		(TREO)				
52		P5_7						

Note:
1. Can be assigned to the pin in parentheses by a program.

1.5   Pin Functions

Tables 1.6 and 1.7 list Pin Functions.

Table 1.6   Pin Functions (1)

Item	Pin Name	I/O Type	Description
Power supply input	VCC, VSS	–	Apply 1.8 V to 5.5 V to the VCC pin. Apply 0 V to the VSS pin.
Analog power supply input	AVCC, AVSS	–	Power supply for the A/D converter. Connect a capacitor between AVCC and AVSS.
Reset input	$\overline{\text{RESET}}$	I	Input "L" on this pin resets the MCU.
MODE	MODE	I	Connect this pin to VCC via a resistor.
XIN clock input	XIN	I	These pins are provided for XIN clock generation circuit I/O. Connect a ceramic resonator or a crystal oscillator between the XIN and XOUT pins [1]. To use an external clock, input it to the XOUT pin and leave the XIN pin open.
XIN clock output	XOUT	I/O	
XCIN clock input	XCIN	I	These pins are provided for XCIN clock generation circuit I/O. Connect a crystal oscillator between the XCIN and XCOUT pins [1]. To use an external clock, input it to the XCIN pin and leave the XCOUT pin open.
XCIN clock output	XCOUT	O	
$\overline{\text{INT}}$ interrupt input	$\overline{\text{INT0}}$ to $\overline{\text{INT4}}$	I	$\overline{\text{INT}}$ interrupt input pins. INT0 is timer RB, RC and RD input pin.
Key input interrupt	$\overline{\text{KI0}}$ to $\overline{\text{KI3}}$	I	Key input interrupt input pins
Timer RA	TRAIO	I/O	Timer RA I/O pin
	TRAO	O	Timer RA output pin
Timer RB	TRBO	O	Timer RB output pin
Timer RC	TRCCLK	I	External clock input pin
	TRCTRG	I	External trigger input pin
	TRCIOA, TRCIOB, TRCIOC, TRCIOD	I/O	Timer RC I/O pins
Timer RD	TRDIOA0, TRDIOA1, TRDIOB0, TRDIOB1, TRDIOC0, TRDIOC1, TRDIOD0, TRDIOD1	I/O	Timer RD I/O pins
	TRDCLK	I	External clock input pin
Timer RE	TREO	O	Divided clock output pin
Serial interface	CLK0, CLK1, CLK2	I/O	Transfer clock I/O pins
	RXD0, RXD1, RXD2	I	Serial data input pins
	TXD0, TXD1, TXD2	O	Serial data output pins
	$\overline{\text{CTS2}}$	I	Transmission control input pin
	$\overline{\text{RTS2}}$	O	Reception control output pin
	SCL2	I/O	I2C mode clock I/O pin
	SDA2	I/O	I2C mode data I/O pin
I2C bus	SCL	I/O	Clock I/O pin
	SDA	I/O	Data I/O pin
SSU	SSI	I/O	Data I/O pin
	$\overline{\text{SCS}}$	I/O	Chip-select signal I/O pin
	SSCK	I/O	Clock I/O pin
	SSO	I/O	Data I/O pin

I: Input   O: Output   I/O: Input and output
Note:
    1. Refer to the oscillator manufacturer for oscillation characteristics.

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU Registers. The CPU contains 13 registers. R0, R1, R2, R3, A0, A1, and FB configure a register bank. There are two sets of register bank.
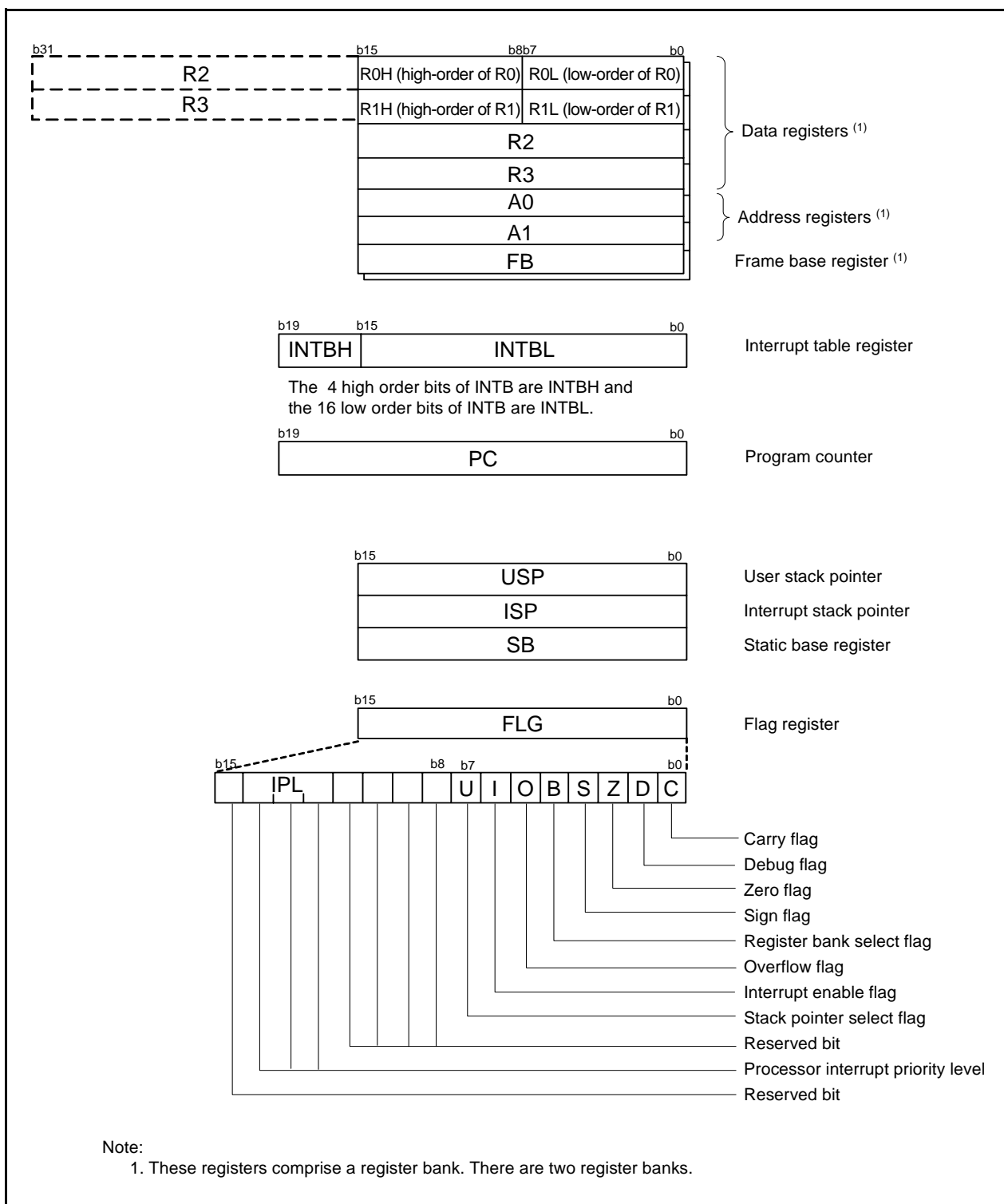

Figure 2.1   CPU Registers

2.1 Data Registers (R0, R1, R2, and R3)

R0 is a 16-bit register for transfer, arithmetic, and logic operations. The same applies to R1 to R3. R0 can be split into high-order bits (R0H) and low-order bits (R0L) to be used separately as 8-bit data registers. R1H and R1L are analogous to R0H and R0L. R2 can be combined with R0 and used as a 32-bit data register (R2R0). R3R1 is analogous to R2R0.

2.2 Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. It is also used for transfer, arithmetic, and logic operations. A1 is analogous to A0. A1 can be combined with A0 and as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is a 16-bit register for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register that indicates the starting address of an interrupt vector table.

2.5 Program Counter (PC)

PC is 20 bits wide and indicates the address of the next instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointers (SP), USP and ISP, are each 16 bits wide. The U flag of FLG is used to switch between USP and ISP.

2.7 Static Base Register (SB)

SB is a 16-bit register for SB relative addressing.

2.8 Flag Register (FLG)

FLG is an 11-bit register indicating the CPU state.

2.8.1 Carry Flag (C)

The C flag retains carry, borrow, or shift-out bits that have been generated by the arithmetic and logic unit.

2.8.2 Debug Flag (D)

The D flag is for debugging only. Set it to 0.

2.8.3 Zero Flag (Z)

The Z flag is set to 1 when an arithmetic operation results in 0; otherwise to 0.

2.8.4 Sign Flag (S)

The S flag is set to 1 when an arithmetic operation results in a negative value; otherwise to 0.

2.8.5 Register Bank Select Flag (B)

Register bank 0 is selected when the B flag is 0. Register bank 1 is selected when this flag is set to 1.

2.8.6 Overflow Flag (O)

The O flag is set to 1 when an operation results in an overflow; otherwise to 0.

2.8.7   Interrupt Enable Flag (I)

The I flag enables maskable interrupts.
Interrupts are disabled when the I flag is set to 0, and are enabled when the I flag is set to 1. The I flag is set to 0 when an interrupt request is acknowledged.

2.8.8   Stack Pointer Select Flag (U)

ISP is selected when the U flag is set to 0; USP is selected when the U flag is set to 1.
The U flag is set to 0 when a hardware interrupt request is acknowledged or the INT instruction of software interrupt numbers 0 to 31 is executed.

2.8.9   Processor Interrupt Priority Level (IPL)

IPL is 3 bits wide and assigns processor interrupt priority levels from level 0 to level 7.
If a requested interrupt has higher priority than IPL, the interrupt is enabled.

2.8.10   Reserved Bit

If necessary, set to 0. When read, the content is undefined.

Table 4.4 SFR Information (4) [(1)]

Address	Register	Symbol	After Reset
00C0h	A/D Register 0	AD0	XXh
00C1h			000000XXb
00C2h	A/D Register 1	AD1	XXh
00C3h			000000XXb
00C4h	A/D Register 2	AD2	XXh
00C5h			000000XXb
00C6h	A/D Register 3	AD3	XXh
00C7h			000000XXb
00C8h	A/D Register 4	AD4	XXh
00C9h			000000XXb
00CAh	A/D Register 5	AD5	XXh
00CBh			000000XXb
00CCh	A/D Register 6	AD6	XXh
00CDh			000000XXb
00CEh	A/D Register 7	AD7	XXh
00CFh			000000XXb
00D0h			
00D1h			
00D2h			
00D3h			
00D4h	A/D Mode Register	ADMOD	00h
00D5h	A/D Input Select Register	ADINSEL	11000000b
00D6h	A/D Control Register 0	ADCON0	00h
00D7h	A/D Control Register 1	ADCON1	00h
00D8h	D/A0 Register	DA0	00h
00D9h	D/A1 Register	DA1	00h
00DAh			
00DBh			
00DCh	D/A Control Register	DACON	00h
00DDh			
00DEh			
00DFh			
00E0h	Port P0 Register	P0	XXh
00E1h	Port P1 Register	P1	XXh
00E2h	Port P0 Direction Register	PD0	00h
00E3h	Port P1 Direction Register	PD1	00h
00E4h	Port P2 Register	P2	XXh
00E5h	Port P3 Register	P3	XXh
00E6h	Port P2 Direction Register	PD2	00h
00E7h	Port P3 Direction Register	PD3	00h
00E8h	Port P4 Register	P4	XXh
00E9h	Port P5 Register	P5	XXh
00EAh	Port P4 Direction Register	PD4	00h
00EBh	Port P5 Direction Register	PD5	00h
00ECh	Port P6 Register	P6	XXh
00EDh			
00EEh	Port P6 Direction Register	PD6	00h
00EFh			
00F0h			
00F1h			
00F2h			
00F3h			
00F4h			
00F5h			
00F6h			
00F7h			
00F8h			
00F9h			
00FAh			
00FBh			
00FCh			
00FDh			
00FEh			
00FFh			

X: Undefined
Note:
1. The blank areas are reserved and cannot be accessed by users.

Table 4.5   SFR Information (5) [1]

Address	Register	Symbol	After Reset
0100h	Timer RA Control Register	TRACR	00h
0101h	Timer RA I/O Control Register	TRAIOC	00h
0102h	Timer RA Mode Register	TRAMR	00h
0103h	Timer RA Prescaler Register	TRAPRE	FFh
0104h	Timer RA Register	TRA	FFh
0105h	LIN Control Register 2	LINCR2	00h
0106h	LIN Control Register	LINCR	00h
0107h	LIN Status Register	LINST	00h
0108h	Timer RB Control Register	TRBCR	00h
0109h	Timer RB One-Shot Control Register	TRBOCR	00h
010Ah	Timer RB I/O Control Register	TRBIOC	00h
010Bh	Timer RB Mode Register	TRBMR	00h
010Ch	Timer RB Prescaler Register	TRBPRE	FFh
010Dh	Timer RB Secondary Register	TRBSC	FFh
010Eh	Timer RB Primary Register	TRBPR	FFh
010Fh			
0110h			
0111h			
0112h			
0113h			
0114h			
0115h			
0116h			
0117h			
0118h	Timer RE Second Data Register / Counter Data Register	TRESEC	00h
0119h	Timer RE Minute Data Register / Compare Data Register	TREMIN	00h
011Ah	Timer RE Hour Data Register	TREHR	00h
011Bh	Timer RE Day of Week Data Register	TREWK	00h
011Ch	Timer RE Control Register 1	TRECR1	00h
011Dh	Timer RE Control Register 2	TRECR2	00h
011Eh	Timer RE Count Source Select Register	TRECSR	00001000b
011Fh			
0120h	Timer RC Mode Register	TRCMR	01001000b
0121h	Timer RC Control Register 1	TRCCR1	00h
0122h	Timer RC Interrupt Enable Register	TRCIER	01110000b
0123h	Timer RC Status Register	TRCSR	01110000b
0124h	Timer RC I/O Control Register 0	TRCIOR0	10001000b
0125h	Timer RC I/O Control Register 1	TRCIOR1	10001000b
0126h	Timer RC Counter	TRC	00h
0127h			00h
0128h	Timer RC General Register A	TRCGRA	FFh
0129h			FFh
012Ah	Timer RC General Register B	TRCGRB	FFh
012Bh			FFh
012Ch	Timer RC General Register C	TRCGRC	FFh
012Dh			FFh
012Eh	Timer RC General Register D	TRCGRD	FFh
012Fh			FFh
0130h	Timer RC Control Register 2	TRCCR2	00011000b
0131h	Timer RC Digital Filter Function Select Register	TRCDF	00h
0132h	Timer RC Output Master Enable Register	TRCOER	01111111b
0133h	Timer RC Trigger Control Register	TRCADCR	00h
0134h			
0135h	Timer RD Control Expansion Register	TRDECR	00h
0136h	Timer RD Trigger Control Register	TRDADCR	00h
0137h	Timer RD Start Register	TRDSTR	11111100b
0138h	Timer RD Mode Register	TRDMR	00001110b
0139h	Timer RD PWM Mode Register	TRDPMR	10001000b
013Ah	Timer RD Function Control Register	TRDFCR	10000000b
013Bh	Timer RD Output Master Enable Register 1	TRDOER1	FFh
013Ch	Timer RD Output Master Enable Register 2	TRDOER2	01111111b
013Dh	Timer RD Output Control Register	TRDOCR	00h
013Eh	Timer RD Digital Filter Function Select Register 0	TRDDF0	00h
013Fh	Timer RD Digital Filter Function Select Register 1	TRDDF1	00h

Note:
1.   The blank areas are reserved and cannot be accessed by users.

Table 4.7 SFR Information (7) [1]

Address	Register	Symbol	After Reset
0180h	Timer RA Pin Select Register	TRASR	00h
0181h	Timer RB/RC Pin Select Register	TRBRCSR	00h
0182h	Timer RC Pin Select Register 0	TRCPSR0	00h
0183h	Timer RC Pin Select Register 1	TRCPSR1	00h
0184h	Timer RD Pin Select Register 0	TRDPSR0	00h
0185h	Timer RD Pin Select Register 1	TRDPSR1	00h
0186h	Timer Pin Select Register	TIMSR	00h
0187h			
0188h	UART0 Pin Select Register	U0SR	00h
0189h	UART1 Pin Select Register	U1SR	00h
018Ah	UART2 Pin Select Register 0	U2SR0	00h
018Bh	UART2 Pin Select Register 1	U2SR1	00h
018Ch	SSU/IIC Pin Select Register	SSUIICSR	00h
018Dh			
018Eh	INT Interrupt Input Pin Select Register	INTSR	00h
018Fh	I/O Function Pin Select Register	PINSR	00h
0190h			
0191h			
0192h			
0193h	SS Bit Counter Register	SSBR	11111000b
0194h	SS Transmit Data Register L / IIC bus Transmit Data Register [2]	SSTDR / ICDRT	FFh
0195h	SS Transmit Data Register H [2]	SSTDRH	FFh
0196h	SS Receive Data Register L / IIC bus Receive Data Register [2]	SSRDR / ICDRR	FFh
0197h	SS Receive Data Register H [2]	SSRDRH	FFh
0198h	SS Control Register H / IIC bus Control Register 1 [2]	SSCRH / ICCR1	00h
0199h	SS Control Register L / IIC bus Control Register 2 [2]	SSCRL / ICCR2	01111101b
019Ah	SS Mode Register / IIC bus Mode Register [2]	SSMR / ICMR	00010000b / 00011000b
019Bh	SS Enable Register / IIC bus Interrupt Enable Register [2]	SSER / ICIER	00h
019Ch	SS Status Register / IIC bus Status Register [2]	SSSR / ICSR	00h / 0000X000b
019Dh	SS Mode Register 2 / Slave Address Register [2]	SSMR2 / SAR	00h
019Eh			
019Fh			
01A0h			
01A1h			
01A2h			
01A3h			
01A4h			
01A5h			
01A6h			
01A7h			
01A8h			
01A9h			
01AAh			
01ABh			
01ACh			
01ADh			
01AEh			
01AFh			
01B0h			
01B1h			
01B2h	Flash Memory Status Register	FST	10000X00b
01B3h			
01B4h	Flash Memory Control Register 0	FMR0	00h
01B5h	Flash Memory Control Register 1	FMR1	00h
01B6h	Flash Memory Control Register 2	FMR2	00h
01B7h			
01B8h			
01B9h			
01BAh			
01BBh			
01BCh			
01BDh			
01BEh			
01BFh			

X: Undefined
Notes:
1. The blank areas are reserved and cannot be accessed by users.
2. Selectable by the IICSEL bit in the SSUIICSR register.

Table 4.12   SFR Information (12) [1]

Address	Register	Symbol	After Reset
2CF0h	DTC Control Data 22	DTCD22	XXh
2CF1h			XXh
2CF2h			XXh
2CF3h			XXh
2CF4h			XXh
2CF5h			XXh
2CF6h			XXh
2CF7h			XXh
2CF8h	DTC Control Data 23	DTCD23	XXh
2CF9h			XXh
2CFAh			XXh
2CFBh			XXh
2CFCh			XXh
2CFDh			XXh
2CFEh			XXh
2CFFh			XXh
2D00h			
:			
2FFFh			

X: Undefined

Note:
1. The blank areas are reserved and cannot be accessed by users.

Table 4.13   ID Code Areas and Option Function Select Area

Address	Area Name	Symbol	After Reset
:			
FFDBh	Option Function Select Register 2	OFS2	(Note 1)
:			
FFDFh	ID1		(Note 2)
:			
FFE3h	ID2		(Note 2)
:			
FFEBh	ID3		(Note 2)
:			
FFEFh	ID4		(Note 2)
:			
FFF3h	ID5		(Note 2)
:			
FFF7h	ID6		(Note 2)
:			
FFFBh	ID7		(Note 2)
:			
FFFFh	Option Function Select Register	OFS	(Note 1)

Notes:
1. The option function select area is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
   Do not write additions to the option function select area. If the block including the option function select area is erased, the option function select area is set to FFh.
   When blank products are shipped, the option function select area is set to FFh. It is set to the written value after written by the user.
   When factory-programming products are shipped, the value of the option function select area is the value programmed by the user.
2. The ID code areas are allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
   Do not write additions to the ID code areas. If the block including the ID code areas is erased, the ID code areas are set to FFh.
   When blank products are shipped, the ID code areas are set to FFh. They are set to the written value after written by the user.
   When factory-programming products are shipped, the value of the ID code areas is the value programmed by the user.

Table 5.2　Recommended Operating Conditions

Symbol	Parameter			Conditions	Standard			Unit
					Min.	Typ.	Max.	
V$_{CC}$/AV$_{CC}$	Supply voltage				1.8	–	5.5	V
V$_{SS}$/AV$_{SS}$	Supply voltage				–	0	–	V
V$_{IH}$	Input "H" voltage	Other than CMOS input			0.8 V$_{CC}$	–	V$_{CC}$	V
		CMOS input	Input level switching function (I/O port)	Input level selection : 0.35 V$_{CC}$	4.0 V ≤ V$_{CC}$ ≤ 5.5 V	0.5 V$_{CC}$	–	V$_{CC}$	V
					2.7 V ≤ V$_{CC}$ < 4.0 V	0.55 V$_{CC}$	–	V$_{CC}$	V
					1.8 V ≤ V$_{CC}$ < 2.7 V	0.65 V$_{CC}$	–	V$_{CC}$	V
				Input level selection : 0.5 V$_{CC}$	4.0 V ≤ V$_{CC}$ ≤ 5.5 V	0.65 V$_{CC}$	–	V$_{CC}$	V
					2.7 V ≤ V$_{CC}$ < 4.0 V	0.7 V$_{CC}$	–	V$_{CC}$	V
					1.8 V ≤ V$_{CC}$ < 2.7 V	0.8 V$_{CC}$	–	V$_{CC}$	V
				Input level selection : 0.7 V$_{CC}$	4.0 V ≤ V$_{CC}$ ≤ 5.5 V	0.85 V$_{CC}$	–	V$_{CC}$	V
					2.7 V ≤ V$_{CC}$ < 4.0 V	0.85 V$_{CC}$	–	V$_{CC}$	V
					1.8 V ≤ V$_{CC}$ < 2.7 V	0.85 V$_{CC}$	–	V$_{CC}$	V
		External clock input (XOUT)			1.2	–	V$_{CC}$	V
V$_{IL}$	Input "L" voltage	Other than CMOS input			0	–	0.2 V$_{CC}$	V
		CMOS input	Input level switching function (I/O port)	Input level selection : 0.35 V$_{CC}$	4.0 V ≤ V$_{CC}$ ≤ 5.5 V	0	–	0.2 V$_{CC}$	V
					2.7 V ≤ V$_{CC}$ < 4.0 V	0	–	0.2 V$_{CC}$	V
					1.8 V ≤ V$_{CC}$ < 2.7 V	0	–	0.2 V$_{CC}$	V
				Input level selection : 0.5 V$_{CC}$	4.0 V ≤ V$_{CC}$ ≤ 5.5 V	0	–	0.4 V$_{CC}$	V
					2.7 V ≤ V$_{CC}$ < 4.0 V	0	–	0.3 V$_{CC}$	V
					1.8 V ≤ V$_{CC}$ < 2.7 V	0	–	0.2 V$_{CC}$	V
				Input level selection : 0.7 V$_{CC}$	4.0 V ≤ V$_{CC}$ ≤ 5.5 V	0	–	0.55 V$_{CC}$	V
					2.7 V ≤ V$_{CC}$ < 4.0 V	0	–	0.45 V$_{CC}$	V
					1.8 V ≤ V$_{CC}$ < 2.7 V	0	–	0.35 V$_{CC}$	V
		External clock input (XOUT)			0	–	0.4	V
I$_{OH(sum)}$	Peak sum output "H" current	Sum of all pins I$_{OH(peak)}$			–	–	−160	mA
I$_{OH(sum)}$	Average sum output "H" current	Sum of all pins I$_{OH(avg)}$			–	–	−80	mA
I$_{OH(peak)}$	Peak output "H" current	Drive capacity Low			–	–	−10	mA
		Drive capacity High			–	–	−40	mA
I$_{OH(avg)}$	Average output "H" current	Drive capacity Low			–	–	−5	mA
		Drive capacity High			–	–	−20	mA
I$_{OL(sum)}$	Peak sum output "L" current	Sum of all pins I$_{OL(peak)}$			–	–	160	mA
I$_{OL(sum)}$	Average sum output "L" current	Sum of all pins I$_{OL(avg)}$			–	–	80	mA
I$_{OL(peak)}$	Peak output "L" current	Drive capacity Low			–	–	10	mA
		Drive capacity High			–	–	40	mA
I$_{OL(avg)}$	Average output "L" current	Drive capacity Low			–	–	5	mA
		Drive capacity High			–	–	20	mA
f$_{(XIN)}$	XIN clock input oscillation frequency			2.7 V ≤ V$_{CC}$ ≤ 5.5 V	–	–	20	MHz
				1.8 V ≤ V$_{CC}$ < 2.7 V	–	–	5	MHz
f$_{(XCIN)}$	XCIN clock input oscillation frequency			1.8 V ≤ V$_{CC}$ ≤ 5.5 V	–	32.768	50	kHz
fOCO40M	When used as the count source for timer RC or timer RD [3]			2.7 V ≤ V$_{CC}$ ≤ 5.5 V	32	–	40	MHz
fOCO-F	fOCO-F frequency			2.7 V ≤ V$_{CC}$ ≤ 5.5 V	–	–	20	MHz
				1.8 V ≤ V$_{CC}$ < 2.7 V	–	–	5	MHz
–	System clock frequency			2.7 V ≤ V$_{CC}$ ≤ 5.5 V	–	–	20	MHz
				1.8 V ≤ V$_{CC}$ < 2.7 V	–	–	5	MHz
f$_{(BCLK)}$	CPU clock frequency			2.7 V ≤ V$_{CC}$ ≤ 5.5 V	–	–	20	MHz
				1.8 V ≤ V$_{CC}$ < 2.7 V	–	–	5	MHz

Notes:
1. V$_{CC}$ = 1.8 to 5.5 V and T$_{opr}$ = −20 to 85°C (N version) / −40 to 85°C (D version), unless otherwise specified.
2. The average output current indicates the average value of current measured during 100 ms.
3. fOCO40M can be used as the count source for timer RC or timer RD in the range of V$_{CC}$ = 2.7 V to 5.5V.

Table 5.6 Flash Memory (Program ROM) Electrical Characteristics

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
−	Program/erase endurance [2]		1,000 [3]	−	−	times
−	Byte program time		−	80	500	μs
−	Block erase time		−	0.3	−	s
$t_{d(SR-SUS)}$	Time delay from suspend request until suspend		−	−	5+CPU clock × 3 cycles	ms
−	Interval from erase start/restart until following suspend request		0	−	−	μs
−	Time from suspend until erase restart		−	−	30+CPU clock × 1 cycle	μs
$t_{d(CMDRST-READY)}$	Time from when command is forcibly terminated until reading is enabled		−	−	30+CPU clock × 1 cycle	μs
−	Program, erase voltage		2.7	−	5.5	V
−	Read voltage		1.8	−	5.5	V
−	Program, erase temperature		0	−	60	°C
−	Data hold time [7]	Ambient temperature = 55°C	20	−	−	year

Notes:
1. V_{CC} = 2.7 to 5.5 V and T_{opr} = 0 to 60°C, unless otherwise specified.
2. Definition of programming/erasure endurance
   The programming and erasure endurance is defined on a per-block basis.
   If the programming and erasure endurance is n (n = 1,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.
   However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
4. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
5. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
6. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
7. The data hold time includes time that the power supply is off or the clock is not supplied.

Table 5.7   Flash Memory (Data flash Block A to Block D) Electrical Characteristics

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
–	Program/erase endurance [2]		10,000 [3]	–	–	times
–	Byte program time (program/erase endurance ≤ 1,000 times)		–	160	1,500	μs
–	Byte program time (program/erase endurance > 1,000 times)		–	300	1,500	μs
–	Block erase time (program/erase endurance ≤ 1,000 times)		–	0.2	1	s
–	Block erase time (program/erase endurance > 1,000 times)		–	0.3	1	s
$t_{d(SR-SUS)}$	Time delay from suspend request until suspend		–	–	5+CPU clock × 3 cycles	ms
–	Interval from erase start/restart until following suspend request		0	–	–	μs
–	Time from suspend until erase restart		–	–	30+CPU clock × 1 cycle	μs
$t_{d(CMDRST-READY)}$	Time from when command is forcibly terminated until reading is enabled		–	–	30+CPU clock × 1 cycle	μs
–	Program, erase voltage		2.7	–	5.5	V
–	Read voltage		1.8	–	5.5	V
–	Program, erase temperature		−20 [7]	–	85	°C
–	Data hold time [8]	Ambient temperature = 55 °C	20	–	–	year

Notes:
1. V_{CC} = 2.7 to 5.5 V and T_{opr} = −20 to 85°C (N version) / −40 to 85°C (D version), unless otherwise specified.
2. Definition of programming/erasure endurance
   The programming and erasure endurance is defined on a per-block basis.
   If the programming and erasure endurance is n (n = 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.
   However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
4. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. In addition, averaging the erasure endurance between blocks A to D can further reduce the actual erasure endurance. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
5. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
6. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
7. −40°C for D version.
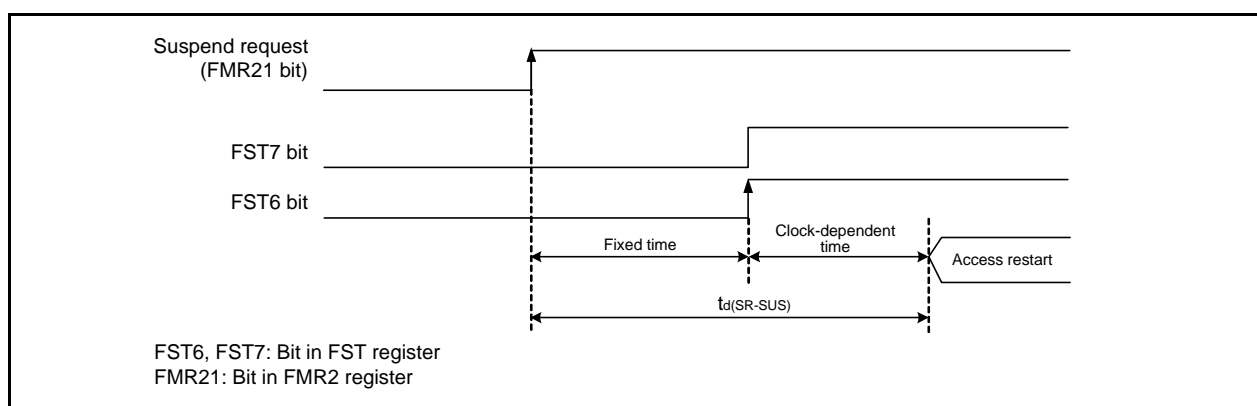8. The data hold time includes time that the power supply is off or the clock is not supplied.

Figure 5.2   Time delay until Suspend

Table 5.8   Voltage Detection 0 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det0}	Voltage detection level Vdet0_0 [2]		1.80	1.90	2.05	V
	Voltage detection level Vdet0_1 [2]		2.15	2.35	2.50	V
	Voltage detection level Vdet0_2 [2]		2.70	2.85	3.05	V
	Voltage detection level Vdet0_3 [2]		3.55	3.80	4.05	V
–	Voltage detection 0 circuit response time [4]	At the falling of V_{CC} from 5 V to (Vdet0_0 − 0.1) V	–	6	150	μs
–	Voltage detection circuit self power consumption	VCA25 = 1, V_{CC} = 5.0 V	–	1.5	–	μA
$t_{d(E-A)}$	Waiting time until voltage detection circuit operation starts [3]		–	–	100	μs

Notes:
1. The measurement condition is V_{CC} = 1.8 V to 5.5 V and T_{opr} = −20 to 85°C (N version) / −40 to 85°C (D version).
2. Select the voltage detection level with bits VDSEL0 and VDSEL1 in the OFS register.
3. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA25 bit in the VCA2 register to 0.
4. Time until the voltage monitor 0 reset is generated after the voltage passes V_{det0}.

Table 5.9   Voltage Detection 1 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det1}	Voltage detection level Vdet1_0 [2]	At the falling of V_{CC}	2.00	2.20	2.40	V
	Voltage detection level Vdet1_1 [2]	At the falling of V_{CC}	2.15	2.35	2.55	V
	Voltage detection level Vdet1_2 [2]	At the falling of V_{CC}	2.30	2.50	2.70	V
	Voltage detection level Vdet1_3 [2]	At the falling of V_{CC}	2.45	2.65	2.85	V
	Voltage detection level Vdet1_4 [2]	At the falling of V_{CC}	2.60	2.80	3.00	V
	Voltage detection level Vdet1_5 [2]	At the falling of V_{CC}	2.75	2.95	3.15	V
	Voltage detection level Vdet1_6 [2]	At the falling of V_{CC}	2.85	3.10	3.40	V
	Voltage detection level Vdet1_7 [2]	At the falling of V_{CC}	3.00	3.25	3.55	V
	Voltage detection level Vdet1_8 [2]	At the falling of V_{CC}	3.15	3.40	3.70	V
	Voltage detection level Vdet1_9 [2]	At the falling of V_{CC}	3.30	3.55	3.85	V
	Voltage detection level Vdet1_A [2]	At the falling of V_{CC}	3.45	3.70	4.00	V
	Voltage detection level Vdet1_B [2]	At the falling of V_{CC}	3.60	3.85	4.15	V
	Voltage detection level Vdet1_C [2]	At the falling of V_{CC}	3.75	4.00	4.30	V
	Voltage detection level Vdet1_D [2]	At the falling of V_{CC}	3.90	4.15	4.45	V
	Voltage detection level Vdet1_E [2]	At the falling of V_{CC}	4.05	4.30	4.60	V
	Voltage detection level Vdet1_F [2]	At the falling of V_{CC}	4.20	4.45	4.75	V
–	Hysteresis width at the rising of Vcc in voltage detection 1 circuit	Vdet1_0 to Vdet1_5 selected	–	0.07	–	V
		Vdet1_6 to Vdet1_F selected	–	0.10	–	V
–	Voltage detection 1 circuit response time [3]	At the falling of V_{CC} from 5 V to (Vdet1_0 − 0.1) V	–	60	150	μs
–	Voltage detection circuit self power consumption	VCA26 = 1, V_{CC} = 5.0 V	–	1.7	–	μA
$t_{d(E-A)}$	Waiting time until voltage detection circuit operation starts [4]		–	–	100	μs

Notes:
1. The measurement condition is V_{CC} = 1.8 V to 5.5 V and T_{opr} = −20 to 85°C (N version) / −40 to 85°C (D version).
2. Select the voltage detection level with bits VD1S0 to VD1S3 in the VD1LS register.
3. Time until the voltage monitor 1 interrupt request is generated after the voltage passes V_{det1}.
4. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA26 bit in the VCA2 register to 0.
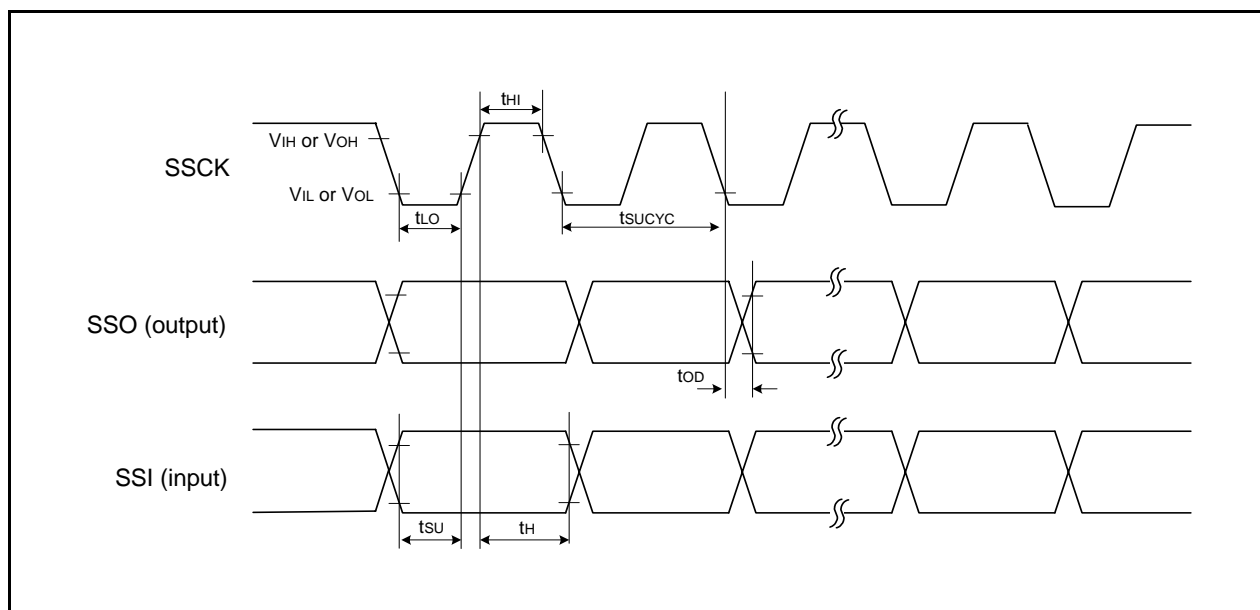
Figure 5.6   I/O Timing of Synchronous Serial Communication Unit (SSU) (Clock Synchronous Communication Mode)

Table 5.17 Electrical Characteristics (1) [4.2 V ≤ Vcc ≤ 5.5 V]

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
VOH	Output "H" voltage	Other than XOUT	Drive capacity High Vcc = 5 V	IOH = −20 mA	Vcc − 2.0	–	Vcc	V
			Drive capacity Low Vcc = 5 V	IOH = −5 mA	Vcc − 2.0	–	Vcc	V
		XOUT	Vcc = 5 V	IOH = −200 μA	1.0	–	Vcc	V
VOL	Output "L" voltage	Other than XOUT	Drive capacity High Vcc = 5 V	IOL = 20 mA	–	–	2.0	V
			Drive capacity Low Vcc = 5 V	IOL = 5 mA	–	–	2.0	V
		XOUT	Vcc = 5 V	IOL = 200 μA	–	–	0.5	V
VT+-VT-	Hysteresis	INT0, INT1, INT2, INT3, INT4, KI0, KI1, KI2, KI3, TRAIO, TRBO, TRCIOA, TRCIOB, TRCIOC, TRCIOD, TRDIOA0, TRDIOB0, TRDIOC0, TRDIOD0, TRDIOA1, TRDIOB1, TRDIOC1, TRDIOD1, TRCTRG, TRCCLK, ADTRG, RXD0, RXD1, RXD2, CLK0, CLK1, CLK2, SSI, SCL, SDA, SSO			0.1	1.2	–	V
		RESET			0.1	1.2	–	V
IIH	Input "H" current		VI = 5 V, Vcc = 5.0 V		–	–	5.0	μA
IIL	Input "L" current		VI = 0 V, Vcc = 5.0 V		–	–	−5.0	μA
RPULLUP	Pull-up resistance		VI = 0 V, Vcc = 5.0 V		25	50	100	kΩ
RfXIN	Feedback resistance	XIN			–	0.3	–	MΩ
RfXCIN	Feedback resistance	XCIN			–	8	–	MΩ
VRAM	RAM hold voltage		During stop mode		1.8	–	–	V

Note:
1. 4.2 V ≤ Vcc ≤ 5.5 V and Topr = −20 to 85°C (N version) / −40 to 85°C (D version), f(XIN) = 20 MHz, unless otherwise specified.

**Table 5.23   Electrical Characteristics (3) [2.7 V ≤ Vcc < 4.2 V]**

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
VOH	Output "H" voltage	Other than XOUT	Drive capacity High	IOH = −5 mA	Vcc − 0.5	–	Vcc	V
			Drive capacity Low	IOH = −1 mA	Vcc − 0.5	–	Vcc	V
		XOUT		IOH = −200 μA	1.0	–	Vcc	V
VOL	Output "L" voltage	Other than XOUT	Drive capacity High	IOL = 5 mA	–	–	0.5	V
			Drive capacity Low	IOL = 1 mA	–	–	0.5	V
		XOUT		IOL = 200 μA	–	–	0.5	V
VT+-VT-	Hysteresis	INT0, INT1, INT2, INT3, INT4, KI0, KI1, KI2, KI3, TRAIO, TRBO, TRCIOA, TRCIOB, TRCIOC, TRCIOD, TRDIOA0, TRDIOB0, TRDIOC0, TRDIOD0, TRDIOA1, TRDIOB1, TRDIOC1, TRDIOD1, TRCTRG, TRCCLK, ADTRG, RXD0, RXD1, RXD2, CLK0, CLK1, CLK2, SSI, SCL, SDA, SSO	Vcc = 3.0 V		0.1	0.4	–	V
		RESET	Vcc = 3.0 V		0.1	0.5	–	V
IIH	Input "H" current		VI = 3 V, Vcc = 3.0 V		–	–	4.0	μA
IIL	Input "L" current		VI = 0 V, Vcc = 3.0 V		–	–	−4.0	μA
RPULLUP	Pull-up resistance		VI = 0 V, Vcc = 3.0 V		42	84	168	kΩ
RfXIN	Feedback resistance	XIN			–	0.3	–	MΩ
RfXCIN	Feedback resistance	XCIN			–	8	–	MΩ
VRAM	RAM hold voltage		During stop mode		1.8	–	–	V

Note:
1. 2.7 V ≤ Vcc < 4.2 V and Topr = −20 to 85°C (N version) / −40 to 85°C (D version), f(XIN) = 10 MHz, unless otherwise specified.

Timing Requirements
(Unless Otherwise Specified: V$_{CC}$ = 3 V, V$_{SS}$ = 0 V at T$_{opr}$ = 25°C)

Table 5.25   External Clock Input (XOUT, XCIN)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t$_{C(XOUT)}$	XOUT input cycle time	50	–	ns
t$_{WH(XOUT)}$	XOUT input "H" width	24	–	ns
t$_{WL(XOUT)}$	XOUT input "L" width	24	–	ns
t$_{C(XCIN)}$	XCIN input cycle time	14	–	μs
t$_{WH(XCIN)}$	XCIN input "H" width	7	–	μs
t$_{WL(XCIN)}$	XCIN input "L" width	7	–	μs
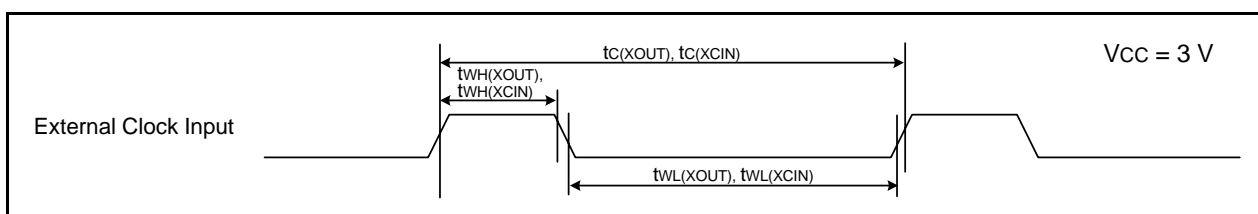
Figure 5.12   External Clock Input Timing Diagram when VCC = 3 V

Table 5.26   TRAIO Input

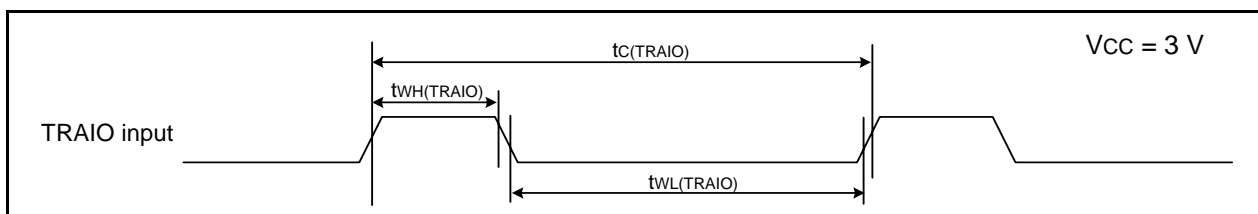| Symbol	Parameter	Standard		Unit
		Min.	Max.	
t$_{C(TRAIO)}$	TRAIO input cycle time	300	–	ns
t$_{WH(TRAIO)}$	TRAIO input "H" width	120	–	ns
t$_{WL(TRAIO)}$	TRAIO input "L" width	120	–	ns

Figure 5.13   TRAIO Input Timing Diagram when VCC = 3 V

Table 5.30 Electrical Characteristics (6) [1.8 V ≤ Vcc < 2.7 V]
(Topr = −20 to 85°C (N version) / −40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
Icc	Power supply current (Vcc = 1.8 to 2.7 V) Single-chip mode, output pins are open, other pins are Vss	High-speed clock mode	XIN = 5 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	−	2.2	−	mA
			XIN = 5 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	−	0.8	−	mA
		High-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator on fOCO-F = 5 MHz Low-speed on-chip oscillator on = 125 kHz No division	−	2.5	10	mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 5 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	−	1.7	−	mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 4 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-16 MSTIIC = MSTTRD = MSTTRC = 1	−	1	−	mA
		Low-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR27 = 1, VCA20 = 0	−	90	300	μA
		Low-speed clock mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz No division, FMR27 = 1, VCA20 = 0	−	80	350	μA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz No division, Program operation on RAM Flash memory off, FMSTP = 1, VCA20 = 0	−	40	−	μA
		Wait mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	−	15	90	μA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	−	4	80	μA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (peripheral clock off) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	−	3.5	−	μA
		Stop mode	XIN clock off, Topr = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	−	2.0	5	μA
			XIN clock off, Topr = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	−	5.0 [1] / 15 [2]	−	μA

Notes:
1. Value when the program ROM capacity of the product is 16 Kbytes to 32 Kbytes.
2. Value when the program ROM capacity of the product is 48 Kbytes to 128 Kbytes.

Rev.	Date	Description	
		Page	Summary
0.10	Sep. 01, 2009	–	First Edition issued
1.00	Aug. 24, 2010	All	"Preliminary" and "Under development" deleted
		4	Table1.3 revised
		27 to 53	5. Electrical Characteristics added