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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

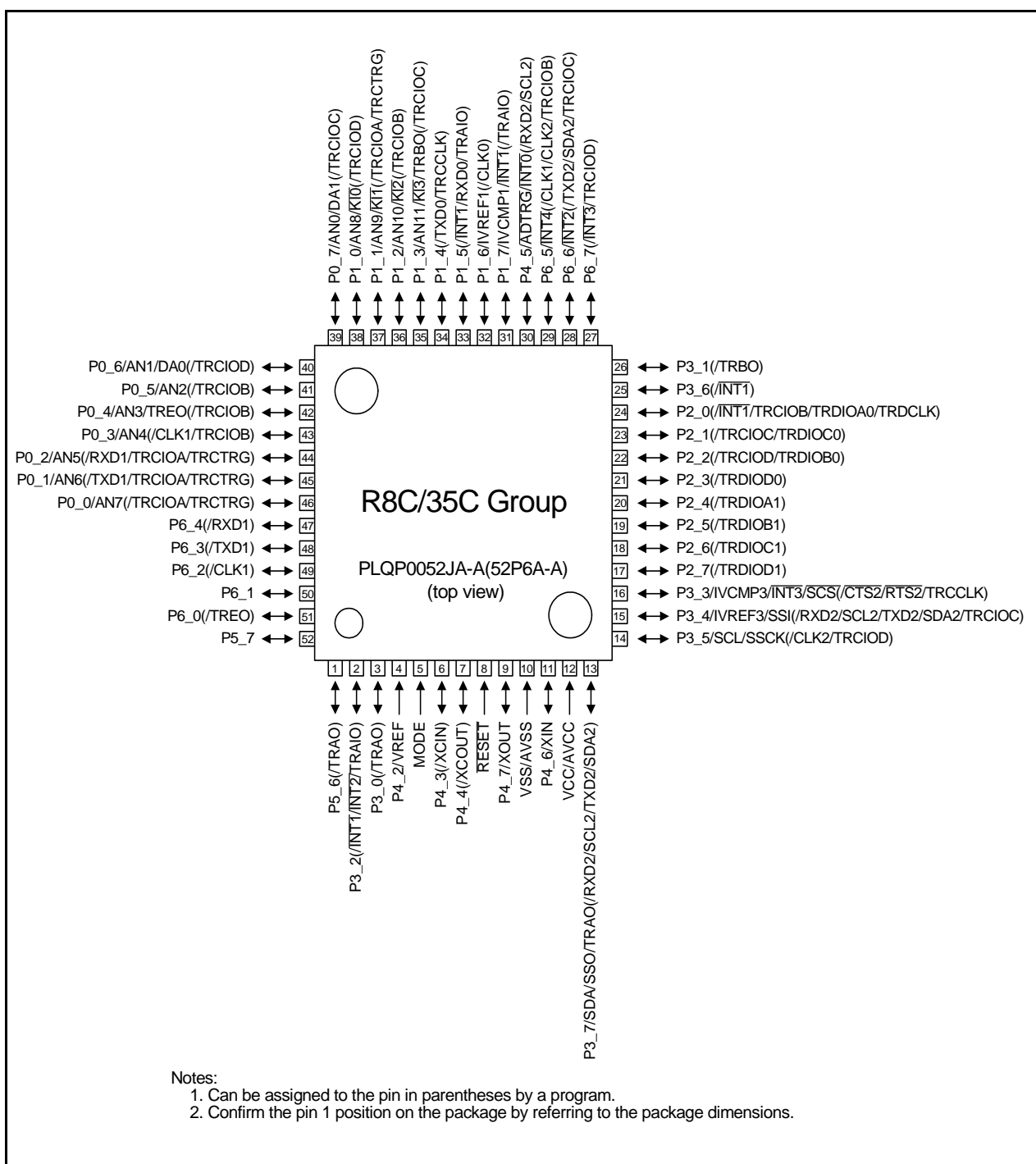
### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Obsolete
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I <sup>2</sup> C, LINbus, SIO, SSU, UART/USART
Peripherals	POR, PWM, Voltage Detect, WDT
Number of I/O	47
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	10K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 12x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	52-LQFP
Supplier Device Package	52-LQFP (10x10)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f2135ccnfp-v0">https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f2135ccnfp-v0</a>

## 1.4 Pin Assignment

Figure 1.3 shows the Pin Assignment (Top View). Tables 1.4 and 1.5 outline the Pin Name Information by Pin Number.



**Figure 1.3 Pin Assignment (Top View)**

**Table 1.4 Pin Name Information by Pin Number (1)**

Pin Number	Control Pin	Port	I/O Pin Functions for Peripheral Modules					
			Interrupt	Timer	Serial Interface	SSU	I <sup>2</sup> C bus	A/D Converter, D/A Converter, Comparator B
1		P5_6		(TRA0)				
2		P3_2	( $\overline{\text{INT1}}/\text{INT2}$ )	(TRAIO)				
3		P3_0		(TRA0)				
4		P4_2						VREF
5	MODE							
6	(XCIN)	P4_3						
7	(XCOUT)	P4_4						
8	$\overline{\text{RESET}}$							
9	XOUT	P4_7						
10	VSS/AVSS							
11	XIN	P4_6						
12	VCC/AVCC							
13		P3_7		TRA0	(RXD2/SCL2/TXD2/SDA2)	SSO	SDA	
14		P3_5		(TRCIOD)	(CLK2)	SSCK	SCL	
15		P3_4		(TRCIOB)	(RXD2/SCL2/TXD2/SDA2)	SSI		IVREF3
16		P3_3	$\overline{\text{INT3}}$	(TRCCLK)	( $\overline{\text{CTS2}}/\text{RTS2}$ )	$\overline{\text{SCS}}$		IVCMP3
17		P2_7		(TRDIOD1)				
18		P2_6		(TRDIOB1)				
19		P2_5		(TRDIOA1)				
20		P2_4		(TRDIOA1)				
21		P2_3		(TRDIOD0)				
22		P2_2		(TRCIOB/TRDIOB0)				
23		P2_1		(TRCIOB/TRDIOB0)				
24		P2_0	( $\overline{\text{INT1}}$ )	(TRCIOB/TRDIOA0/TRDCLK)				
25		P3_6	( $\overline{\text{INT1}}$ )					
26		P3_1		(TRBO)				
27		P6_7	( $\overline{\text{INT3}}$ )	(TRCIOD)				
28		P6_6	$\overline{\text{INT2}}$	(TRCIOB)	(TXD2/SDA2)			
29		P6_5	$\overline{\text{INT4}}$	(TRCIOB)	(CLK1/CLK2)			
30		P4_5	$\overline{\text{INT0}}$		(RXD2/SCL2)			$\overline{\text{ADTRG}}$
31		P1_7	$\overline{\text{INT1}}$	(TRAIO)				IVCMP1
32		P1_6			(CLK0)			IVREF1
33		P1_5	( $\overline{\text{INT1}}$ )	(TRAIO)	(RXD0)			
34		P1_4		(TRCCLK)	(TXD0)			
35		P1_3	$\overline{\text{KI3}}$	TRBO (/TRCIOB)				AN11

Note:

1. Can be assigned to the pin in parentheses by a program.

**Table 1.7 Pin Functions (2)**

Item	Pin Name	I/O Type	Description
Reference voltage input	VREF	I	Reference voltage input pin to A/D converter and D/A converter
A/D converter	AN0 to AN11	I	Analog input pins to A/D converter
	ADTRG	I	A/D external trigger input pin
D/A converter	DA0, DA1	O	D/A converter output pins
Comparator B	IVCMP1, IVCMP3	I	Comparator B analog voltage input pins
	IVREF1, IVREF3	I	Comparator B reference voltage input pins
I/O port	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_3 to P4_7, P5_6, P5_7, P6_0 to P6_7	I/O	CMOS I/O ports. Each port has an I/O select direction register, allowing each pin in the port to be directed for input or output individually. Any port set to input can be set to use a pull-up resistor or not by a program. All ports can be used as LED drive ports.
Input port	P4_2	I	Input-only port

I: Input      O: Output      I/O: Input and output

### **2.8.7 Interrupt Enable Flag (I)**

The I flag enables maskable interrupts.

Interrupts are disabled when the I flag is set to 0, and are enabled when the I flag is set to 1. The I flag is set to 0 when an interrupt request is acknowledged.

### **2.8.8 Stack Pointer Select Flag (U)**

ISP is selected when the U flag is set to 0; USP is selected when the U flag is set to 1.

The U flag is set to 0 when a hardware interrupt request is acknowledged or the INT instruction of software interrupt numbers 0 to 31 is executed.

### **2.8.9 Processor Interrupt Priority Level (IPL)**

IPL is 3 bits wide and assigns processor interrupt priority levels from level 0 to level 7.

If a requested interrupt has higher priority than IPL, the interrupt is enabled.

### **2.8.10 Reserved Bit**

If necessary, set to 0. When read, the content is undefined.

### 3. Memory

#### 3.1 R8C/35C Group

Figure 3.1 is a Memory Map of R8C/35C Group. The R8C/35C Group has a 1-Mbyte address space from addresses 00000h to FFFFFh. The internal ROM (program ROM) is allocated lower addresses, beginning with address 00000h. For example, a 32-Kbyte internal ROM area is allocated addresses 08000h to 0FFFFh.

The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. The starting address of each interrupt routine is stored here.

The internal ROM (data flash) is allocated addresses 03000h to 03FFFh.

The internal RAM is allocated higher addresses, beginning with address 00400h. For example, a 2.5-Kbyte internal RAM area is allocated addresses 00400h to 00DFFh. The internal RAM is used not only for data storage but also as a stack area when a subroutine is called or when an interrupt request is acknowledged.

Special function registers (SFRs) are allocated addresses 00000h to 002FFh and 02C00h to 02FFFh. Peripheral function control registers are allocated here. All unallocated spaces within the SFRs are reserved and cannot be accessed by users.

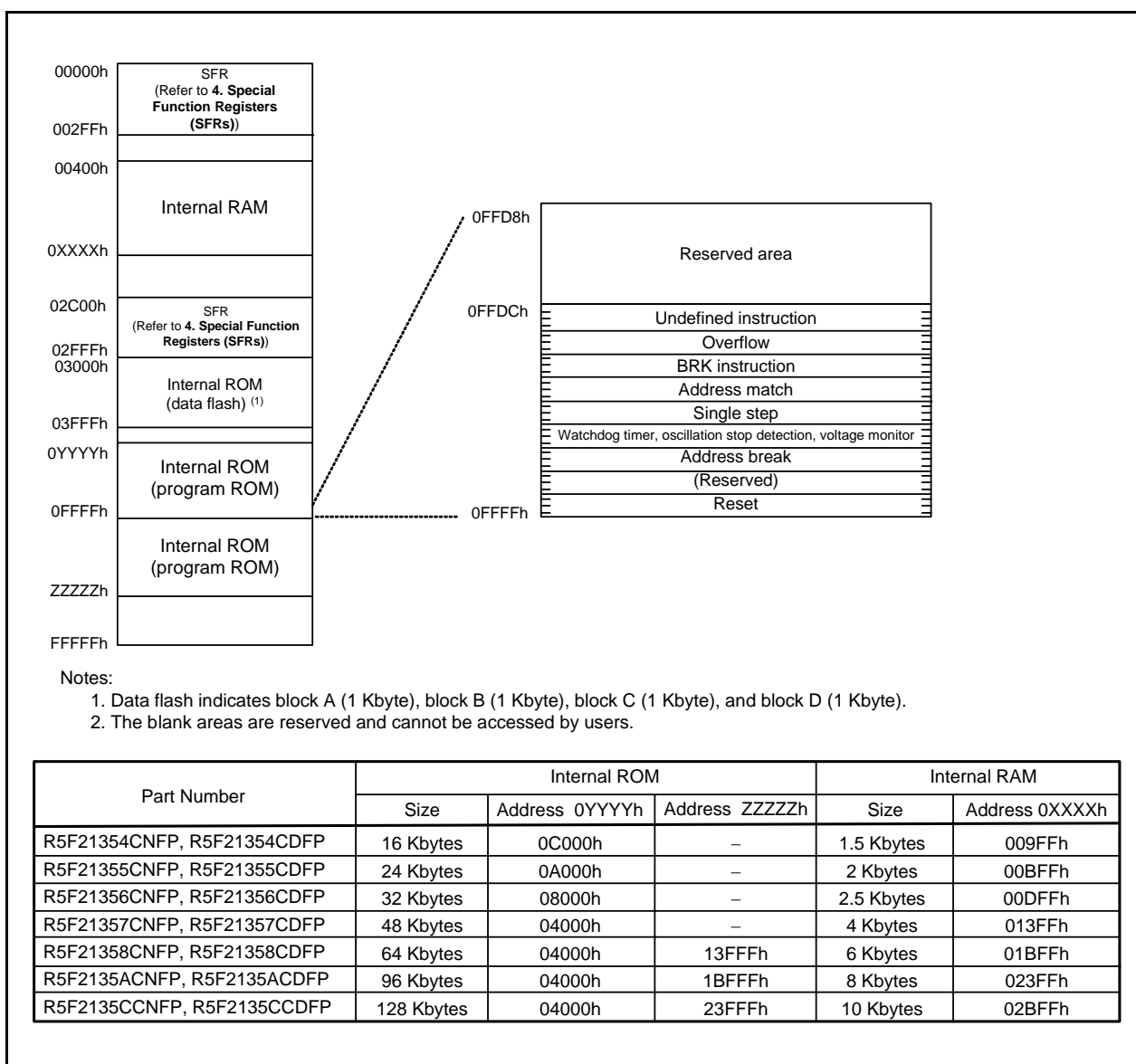


Figure 3.1 Memory Map of R8C/35C Group

**Table 4.4 SFR Information (4) (1)**

Address	Register	Symbol	After Reset
00C0h	A/D Register 0	AD0	XXh
00C1h			000000XXb
00C2h	A/D Register 1	AD1	XXh
00C3h			000000XXb
00C4h	A/D Register 2	AD2	XXh
00C5h			000000XXb
00C6h	A/D Register 3	AD3	XXh
00C7h			000000XXb
00C8h	A/D Register 4	AD4	XXh
00C9h			000000XXb
00CAh	A/D Register 5	AD5	XXh
00CBh			000000XXb
00CCh	A/D Register 6	AD6	XXh
00CDh			000000XXb
00CEh	A/D Register 7	AD7	XXh
00CFh			000000XXb
00D0h			
00D1h			
00D2h			
00D3h			
00D4h	A/D Mode Register	ADMOD	00h
00D5h	A/D Input Select Register	ADINSEL	11000000b
00D6h	A/D Control Register 0	ADCON0	00h
00D7h	A/D Control Register 1	ADCON1	00h
00D8h	D/A0 Register	DA0	00h
00D9h	D/A1 Register	DA1	00h
00DAh			
00DBh			
00DCh	D/A Control Register	DACON	00h
00DDh			
00DEh			
00DFh			
00E0h	Port P0 Register	P0	XXh
00E1h	Port P1 Register	P1	XXh
00E2h	Port P0 Direction Register	PD0	00h
00E3h	Port P1 Direction Register	PD1	00h
00E4h	Port P2 Register	P2	XXh
00E5h	Port P3 Register	P3	XXh
00E6h	Port P2 Direction Register	PD2	00h
00E7h	Port P3 Direction Register	PD3	00h
00E8h	Port P4 Register	P4	XXh
00E9h	Port P5 Register	P5	XXh
00EAh	Port P4 Direction Register	PD4	00h
00EBh	Port P5 Direction Register	PD5	00h
00ECh	Port P6 Register	P6	XXh
00EDh			
00EEh	Port P6 Direction Register	PD6	00h
00EFh			
00F0h			
00F1h			
00F2h			
00F3h			
00F4h			
00F5h			
00F6h			
00F7h			
00F8h			
00F9h			
00FAh			
00FBh			
00FCh			
00FDh			
00FEh			
00FFh			

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

**Table 4.8 SFR Information (8) (1)**

Address	Register	Symbol	After Reset
01C0h	Address Match Interrupt Register 0	RMAD0	XXh
01C1h			XXh
01C2h			0000XXXXb
01C3h	Address Match Interrupt Enable Register 0	AIER0	00h
01C4h	Address Match Interrupt Register 1	RMAD1	XXh
01C5h			XXh
01C6h			0000XXXXb
01C7h	Address Match Interrupt Enable Register 1	AIER1	00h
01C8h			
01C9h			
01CAh			
01CBh			
01CCh			
01CDh			
01CEh			
01CFh			
01D0h			
01D1h			
01D2h			
01D3h			
01D4h			
01D5h			
01D6h			
01D7h			
01D8h			
01D9h			
01DAh			
01DBh			
01DCh			
01DDh			
01DEh			
01DFh			
01E0h	Pull-Up Control Register 0	PUR0	00h
01E1h	Pull-Up Control Register 1	PUR1	00h
01E2h			
01E3h			
01E4h			
01E5h			
01E6h			
01E7h			
01E8h			
01E9h			
01EAh			
01EBh			
01ECh			
01EDh			
01EEh			
01EFh			
01F0h	Port P1 Drive Capacity Control Register	P1DRR	00h
01F1h	Port P2 Drive Capacity Control Register	P2DRR	00h
01F2h	Drive Capacity Control Register 0	DRR0	00h
01F3h	Drive Capacity Control Register 1	DRR1	00h
01F4h			
01F5h	Input Threshold Control Register 0	VLT0	00h
01F6h	Input Threshold Control Register 1	VLT1	00h
01F7h			
01F8h	Comparator B Control Register 0	INTCMP	00h
01F9h			
01FAh	External Input Enable Register 0	INTEN	00h
01FBh	External Input Enable Register 1	INTEN1	00h
01FCh	INT Input Filter Select Register 0	INTF	00h
01FDh	INT Input Filter Select Register 1	INTF1	00h
01FEh	Key Input Enable Register 0	KIEN	00h
01FFh			

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.



**Table 4.9 SFR Information (9) (1)**

Address	Register	Symbol	After Reset
2C00h	DTC Transfer Vector Area		XXh
2C01h	DTC Transfer Vector Area		XXh
2C02h	DTC Transfer Vector Area		XXh
2C03h	DTC Transfer Vector Area		XXh
2C04h	DTC Transfer Vector Area		XXh
2C05h	DTC Transfer Vector Area		XXh
2C06h	DTC Transfer Vector Area		XXh
2C07h	DTC Transfer Vector Area		XXh
2C08h	DTC Transfer Vector Area		XXh
2C09h	DTC Transfer Vector Area		XXh
2C0Ah	DTC Transfer Vector Area		XXh
:	DTC Transfer Vector Area		XXh
:	DTC Transfer Vector Area		XXh
2C3Ah	DTC Transfer Vector Area		XXh
2C3Bh	DTC Transfer Vector Area		XXh
2C3Ch	DTC Transfer Vector Area		XXh
2C3Dh	DTC Transfer Vector Area		XXh
2C3Eh	DTC Transfer Vector Area		XXh
2C3Fh	DTC Transfer Vector Area		XXh
2C40h	DTC Control Data 0	DTCD0	XXh
2C41h			XXh
2C42h			XXh
2C43h			XXh
2C44h			XXh
2C45h			XXh
2C46h			XXh
2C47h			XXh
2C48h	DTC Control Data 1	DTCD1	XXh
2C49h			XXh
2C4Ah			XXh
2C4Bh			XXh
2C4Ch			XXh
2C4Dh			XXh
2C4Eh			XXh
2C4Fh			XXh
2C50h	DTC Control Data 2	DTCD2	XXh
2C51h			XXh
2C52h			XXh
2C53h			XXh
2C54h			XXh
2C55h			XXh
2C56h			XXh
2C57h			XXh
2C58h	DTC Control Data 3	DTCD3	XXh
2C59h			XXh
2C5Ah			XXh
2C5Bh			XXh
2C5Ch			XXh
2C5Dh			XXh
2C5Eh			XXh
2C5Fh			XXh
2C60h	DTC Control Data 4	DTCD4	XXh
2C61h			XXh
2C62h			XXh
2C63h			XXh
2C64h			XXh
2C65h			XXh
2C66h			XXh
2C67h			XXh
2C68h	DTC Control Data 5	DTCD5	XXh
2C69h			XXh
2C6Ah			XXh
2C6Bh			XXh
2C6Ch			XXh
2C6Dh			XXh
2C6Eh			XXh
2C6Fh			XXh

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

**Table 4.10 SFR Information (10) (1)**

Address	Register	Symbol	After Reset
2C70h	DTC Control Data 6	DTCD6	XXh
2C71h			XXh
2C72h			XXh
2C73h			XXh
2C74h			XXh
2C75h			XXh
2C76h			XXh
2C77h			XXh
2C78h	DTC Control Data 7	DTCD7	XXh
2C79h			XXh
2C7Ah			XXh
2C7Bh			XXh
2C7Ch			XXh
2C7Dh			XXh
2C7Eh			XXh
2C7Fh			XXh
2C80h	DTC Control Data 8	DTCD8	XXh
2C81h			XXh
2C82h			XXh
2C83h			XXh
2C84h			XXh
2C85h			XXh
2C86h			XXh
2C87h			XXh
2C88h	DTC Control Data 9	DTCD9	XXh
2C89h			XXh
2C8Ah			XXh
2C8Bh			XXh
2C8Ch			XXh
2C8Dh			XXh
2C8Eh			XXh
2C8Fh			XXh
2C90h	DTC Control Data 10	DTCD10	XXh
2C91h			XXh
2C92h			XXh
2C93h			XXh
2C94h			XXh
2C95h			XXh
2C96h			XXh
2C97h			XXh
2C98h	DTC Control Data 11	DTCD11	XXh
2C99h			XXh
2C9Ah			XXh
2C9Bh			XXh
2C9Ch			XXh
2C9Dh			XXh
2C9Eh			XXh
2C9Fh			XXh
2CA0h	DTC Control Data 12	DTCD12	XXh
2CA1h			XXh
2CA2h			XXh
2CA3h			XXh
2CA4h			XXh
2CA5h			XXh
2CA6h			XXh
2CA7h			XXh
2CA8h	DTC Control Data 13	DTCD13	XXh
2CA9h			XXh
2CAAh			XXh
2CABh			XXh
2CACH			XXh
2CADh			XXh
2CAEh			XXh
2CAFh			XXh

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

**Table 4.12 SFR Information (12) <sup>(1)</sup>**

Address	Register	Symbol	After Reset
2CF0h	DTC Control Data 22	DTCD22	XXh
2CF1h			XXh
2CF2h			XXh
2CF3h			XXh
2CF4h			XXh
2CF5h			XXh
2CF6h			XXh
2CF7h			XXh
2CF8h	DTC Control Data 23	DTCD23	XXh
2CF9h			XXh
2CFAh			XXh
2CFBh			XXh
2CFCh			XXh
2CFDh			XXh
2CFEh			XXh
2CFFh			XXh
2D00h			
⋮			
2FFh			

X: Undefined

Note:

- The blank areas are reserved and cannot be accessed by users.

**Table 4.13 ID Code Areas and Option Function Select Area**

Address	Area Name	Symbol	After Reset
⋮			
FFDBh	Option Function Select Register 2	OFS2	(Note 1)
⋮			
FFDFh	ID1		(Note 2)
⋮			
FFE3h	ID2		(Note 2)
⋮			
FFEBh	ID3		(Note 2)
⋮			
FFEFh	ID4		(Note 2)
⋮			
FFF3h	ID5		(Note 2)
⋮			
FFF7h	ID6		(Note 2)
⋮			
FFFBh	ID7		(Note 2)
⋮			
FFFFh	Option Function Select Register	OFS	(Note 1)

Notes:

- The option function select area is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program. Do not write additions to the option function select area. If the block including the option function select area is erased, the option function select area is set to FFh. When blank products are shipped, the option function select area is set to FFh. It is set to the written value after written by the user. When factory-programming products are shipped, the value of the option function select area is the value programmed by the user.
- The ID code areas are allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program. Do not write additions to the ID code areas. If the block including the ID code areas is erased, the ID code areas are set to FFh. When blank products are shipped, the ID code areas are set to FFh. They are set to the written value after written by the user. When factory-programming products are shipped, the value of the ID code areas is the value programmed by the user.

## 5. Electrical Characteristics

**Table 5.1 Absolute Maximum Ratings**

Symbol	Parameter	Condition	Rated Value	Unit
V <sub>CC</sub> /AV <sub>CC</sub>	Supply voltage		−0.3 to 6.5	V
V <sub>I</sub>	Input voltage		−0.3 to V <sub>CC</sub> + 0.3	V
V <sub>O</sub>	Output voltage		−0.3 to V <sub>CC</sub> + 0.3	V
P <sub>d</sub>	Power dissipation	−40°C ≤ T <sub>opr</sub> ≤ 85°C	500	mW
T <sub>opr</sub>	Operating ambient temperature		−20 to 85 (N version) / −40 to 85 (D version)	°C
T <sub>stg</sub>	Storage temperature		−65 to 150	°C

**Table 5.3 A/D Converter Characteristics**

Symbol	Parameter		Conditions		Standard			Unit
					Min.	Typ.	Max.	
–	Resolution		Vref = AVCC		–	–	10	Bit
–	Absolute accuracy	10-bit mode	Vref = AVCC = 5.0 V	AN0 to AN7 input, AN8 to AN11 input	–	–	±3	LSB
			Vref = AVCC = 3.3 V	AN0 to AN7 input, AN8 to AN11 input	–	–	±5	LSB
			Vref = AVCC = 3.0 V	AN0 to AN7 input, AN8 to AN11 input	–	–	±5	LSB
			Vref = AVCC = 2.2 V	AN0 to AN7 input, AN8 to AN11 input	–	–	±5	LSB
		8-bit mode	Vref = AVCC = 5.0 V	AN0 to AN7 input, AN8 to AN11 input	–	–	±2	LSB
			Vref = AVCC = 3.3 V	AN0 to AN7 input, AN8 to AN11 input	–	–	±2	LSB
			Vref = AVCC = 3.0 V	AN0 to AN7 input, AN8 to AN11 input	–	–	±2	LSB
			Vref = AVCC = 2.2 V	AN0 to AN7 input, AN8 to AN11 input	–	–	±2	LSB
φAD	A/D conversion clock		4.0 V ≤ Vref = AVCC ≤ 5.5 V (2)		2	–	20	MHz
			3.2 V ≤ Vref = AVCC ≤ 5.5 V (2)		2	–	16	MHz
			2.7 V ≤ Vref = AVCC ≤ 5.5 V (2)		2	–	10	MHz
			2.2 V ≤ Vref = AVCC ≤ 5.5 V (2)		2	–	5	MHz
–	Tolerance level impedance				–	3	–	kΩ
tCONV	Conversion time	10-bit mode	Vref = AVCC = 5.0 V, φAD = 20 MHz		2.2	–	–	μs
		8-bit mode	Vref = AVCC = 5.0 V, φAD = 20 MHz		2.2	–	–	μs
tsAMP	Sampling time		φAD = 20 MHz		0.8	–	–	μs
IVref	Vref current		VCC = 5 V, XIN = f1 = φAD = 20 MHz		–	45	–	μA
Vref	Reference voltage				2.2	–	AVCC	V
VIA	Analog input voltage (3)				0	–	Vref	V
OCVREF	On-chip reference voltage		2 MHz ≤ φAD ≤ 4 MHz		1.19	1.34	1.49	V

## Notes:

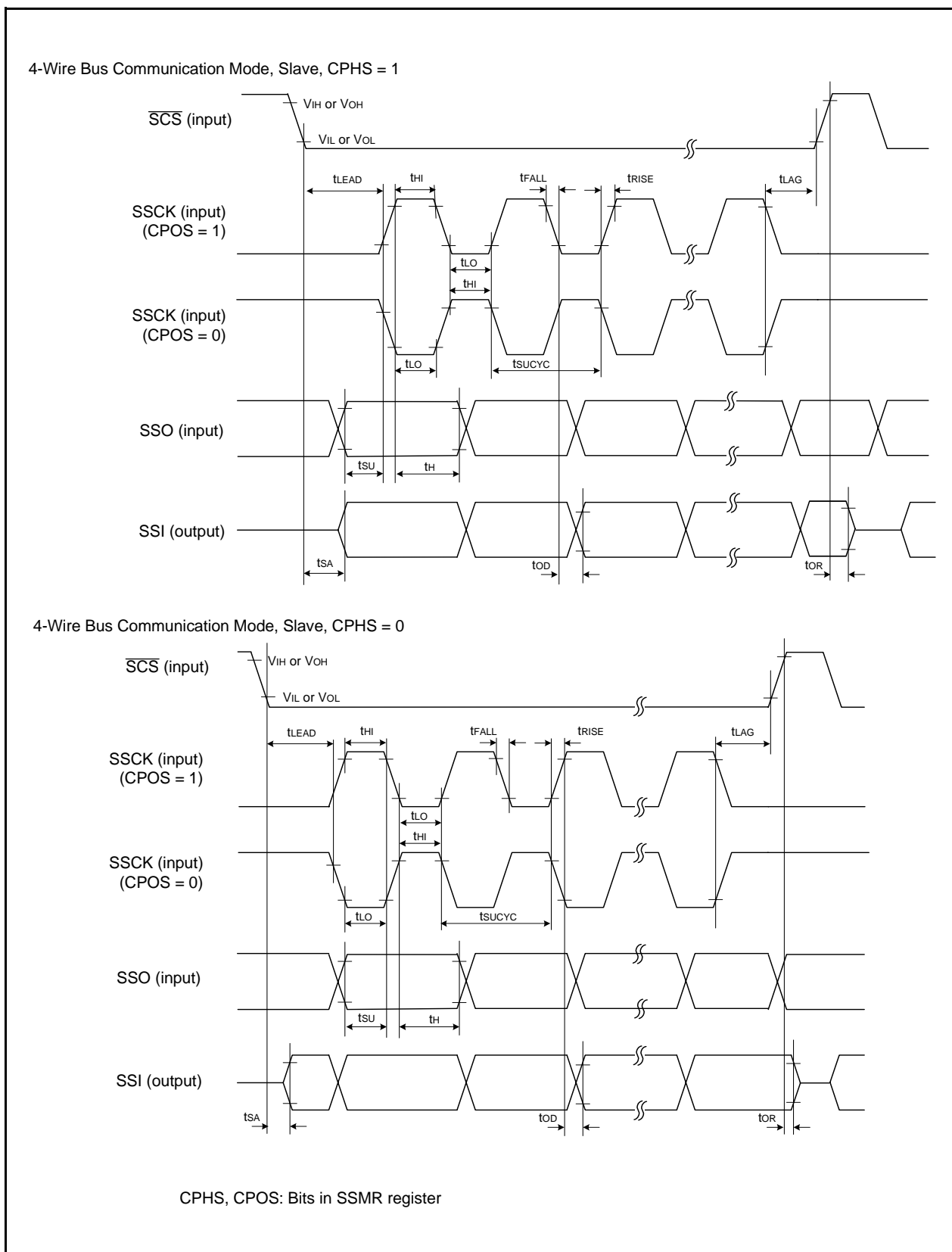
1.  $V_{CC}/AV_{CC} = V_{ref} = 2.2$  to  $5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$  and  $T_{opr} = -20$  to  $85^\circ\text{C}$  (N version) /  $-40$  to  $85^\circ\text{C}$  (D version), unless otherwise specified.
2. The A/D conversion result will be undefined in wait mode, stop mode, when the flash memory stops, and in low-current-consumption mode. Do not perform A/D conversion in these states or transition to these states during A/D conversion.
3. When the analog input voltage is over the reference voltage, the A/D conversion result will be 3FFh in 10-bit mode and FFh in 8-bit mode.

**Table 5.15 Timing Requirements of Synchronous Serial Communication Unit (SSU) (1)**

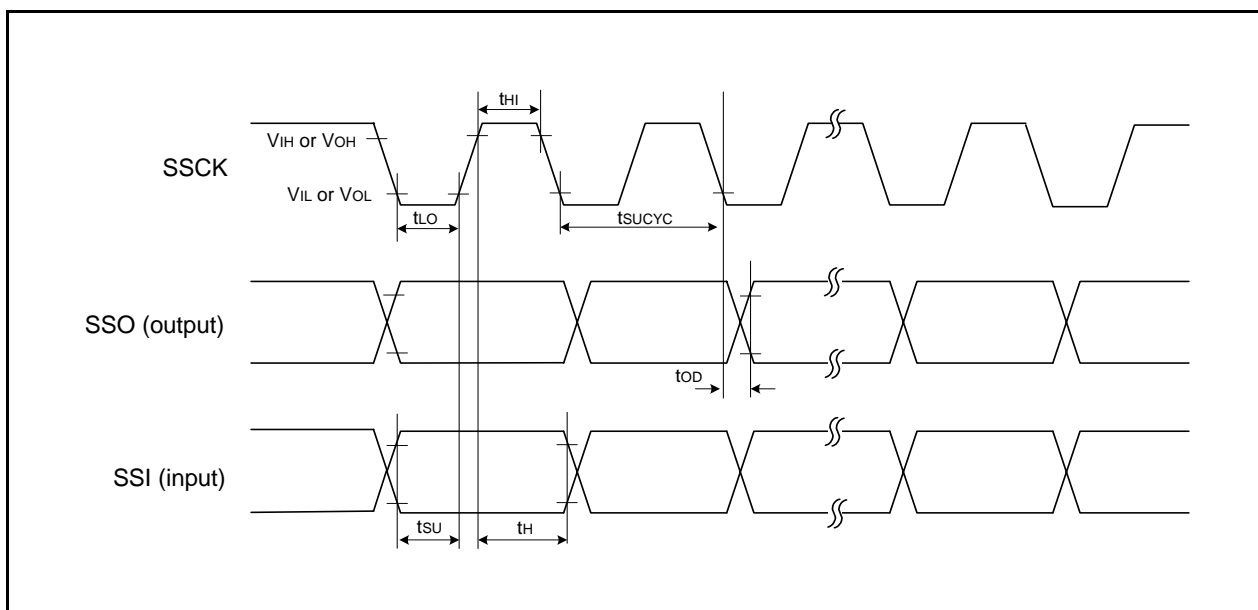
Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
tsucyc	SSCK clock cycle time			4	–	–	tcyc (2)
tHI	SSCK clock "H" width			0.4	–	0.6	tsucyc
tLO	SSCK clock "L" width			0.4	–	0.6	tsucyc
tRISE	SSCK clock rising time	Master		–	–	1	tcyc (2)
		Slave		–	–	1	μs
tFALL	SSCK clock falling time	Master		–	–	1	tcyc (2)
		Slave		–	–	1	μs
tsu	SSO, SSI data input setup time			100	–	–	ns
tH	SSO, SSI data input hold time			1	–	–	tcyc (2)
tLEAD	$\overline{\text{SCS}}$ setup time	Slave		1tcyc + 50	–	–	ns
tLAG	$\overline{\text{SCS}}$ hold time	Slave		1tcyc + 50	–	–	ns
tOD	SSO, SSI data output delay time			–	–	1	tcyc (2)
tSA	SSI slave access time		$2.7\text{ V} \leq V_{\text{CC}} \leq 5.5\text{ V}$	–	–	$1.5\text{tcyc} + 100$	ns
			$1.8\text{ V} \leq V_{\text{CC}} < 2.7\text{ V}$	–	–	$1.5\text{tcyc} + 200$	ns
tOR	SSI slave out open time		$2.7\text{ V} \leq V_{\text{CC}} \leq 5.5\text{ V}$	–	–	$1.5\text{tcyc} + 100$	ns
			$1.8\text{ V} \leq V_{\text{CC}} < 2.7\text{ V}$	–	–	$1.5\text{tcyc} + 200$	ns

Notes:

1.  $V_{\text{CC}} = 1.8$  to  $5.5\text{ V}$ ,  $V_{\text{SS}} = 0\text{ V}$  and  $T_{\text{opr}} = -20$  to  $85^\circ\text{C}$  (N version) /  $-40$  to  $85^\circ\text{C}$  (D version), unless otherwise specified.
2.  $1\text{tcyc} = 1/f_1(\text{s})$



**Figure 5.5 I/O Timing of Synchronous Serial Communication Unit (SSU) (Slave)**



**Figure 5.6 I/O Timing of Synchronous Serial Communication Unit (SSU) (Clock Synchronous Communication Mode)**



**Table 5.17 Electrical Characteristics (1) [4.2 V ≤ Vcc ≤ 5.5 V]**

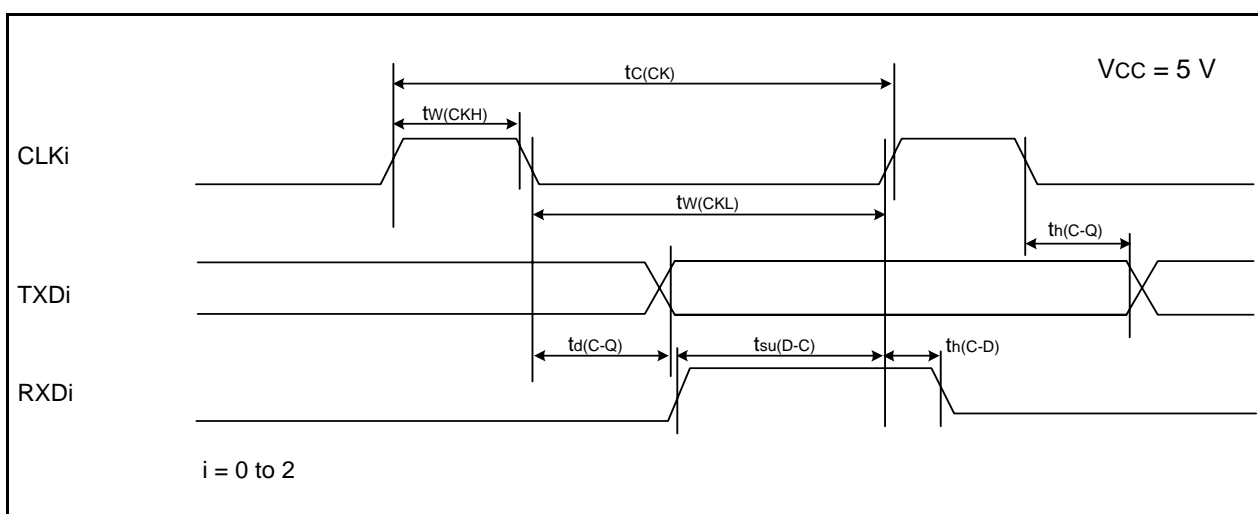
Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
VOH	Output "H" voltage	Other than XOUT	Drive capacity High Vcc = 5 V	IOH = -20 mA	Vcc - 2.0	—	Vcc	V
			Drive capacity Low Vcc = 5 V	IOH = -5 mA	Vcc - 2.0	—	Vcc	V
		XOUT	Vcc = 5 V	IOH = -200 μA	1.0	—	Vcc	V
VOL	Output "L" voltage	Other than XOUT	Drive capacity High Vcc = 5 V	IOL = 20 mA	—	—	2.0	V
			Drive capacity Low Vcc = 5 V	IOL = 5 mA	—	—	2.0	V
		XOUT	Vcc = 5 V	IOL = 200 μA	—	—	0.5	V
VT+-VT-	Hysteresis	INT0, INT1, INT2, INT3, INT4, KI0, KI1, KI2, KI3, TRAIO, TRBO, TRCIOA, TRCIOB, TRCIOC, TRCIOD, TRDIOA0, TRDIOB0, TRDIOC0, TRDIOD0, TRDIOA1, TRDIOB1, TRDIOC1, TRDIOD1, TRCTRG, TRCCLK, ADTRG, RXD0, RXD1, RXD2, CLK0, CLK1, CLK2, SSI, SCL, SDA, SSO			0.1	1.2	—	V
		RESET			0.1	1.2	—	V
IiH	Input "H" current		VI = 5 V, Vcc = 5.0 V		—	—	5.0	μA
IiL	Input "L" current		VI = 0 V, Vcc = 5.0 V		—	—	-5.0	μA
RPULLUP	Pull-up resistance		VI = 0 V, Vcc = 5.0 V		25	50	100	kΩ
RfXIN	Feedback resistance	XIN			—	0.3	—	MΩ
RfXCIN	Feedback resistance	XCIN			—	8	—	MΩ
VRAM	RAM hold voltage		During stop mode		1.8	—	—	V

Note:

1. 4.2 V ≤ Vcc ≤ 5.5 V and Topr = -20 to 85°C (N version) / -40 to 85°C (D version), f(XIN) = 20 MHz, unless otherwise specified.

**Table 5.21 Serial Interface**

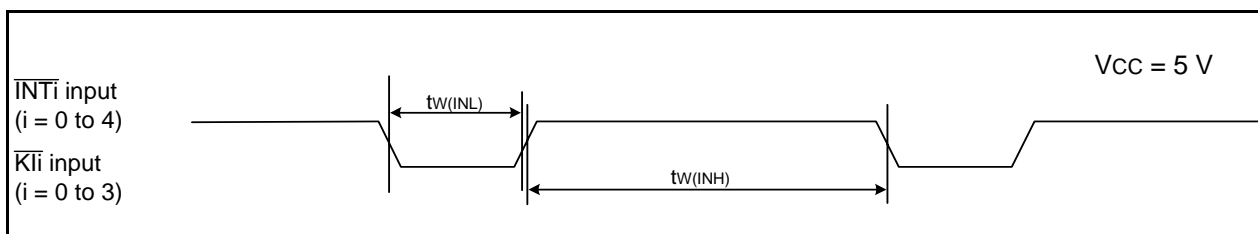
Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	200	—	ns
$t_{w(CKH)}$	CLKi input “H” width	100	—	ns
$t_{w(CKL)}$	CLKi input “L” width	100	—	ns
$t_{d(C-Q)}$	TXDi output delay time	—	50	ns
$t_{h(C-Q)}$	TXDi hold time	0	—	ns
$t_{su(D-C)}$	RXDi input setup time	50	—	ns
$t_{h(C-D)}$	RXDi input hold time	90	—	ns

 $i = 0 \text{ to } 2$ **Figure 5.10 Serial Interface Timing Diagram when Vcc = 5 V****Table 5.22 External Interrupt  $\overline{INTi}$  ( $i = 0 \text{ to } 4$ ) Input, Key Input Interrupt  $\overline{Kli}$  ( $i = 0 \text{ to } 3$ )**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INTi}$ input “H” width, $\overline{Kli}$ input “H” width	250 (1)	—	ns
$t_{w(INL)}$	$\overline{INTi}$ input “L” width, $\overline{Kli}$ input “L” width	250 (2)	—	ns

Notes:

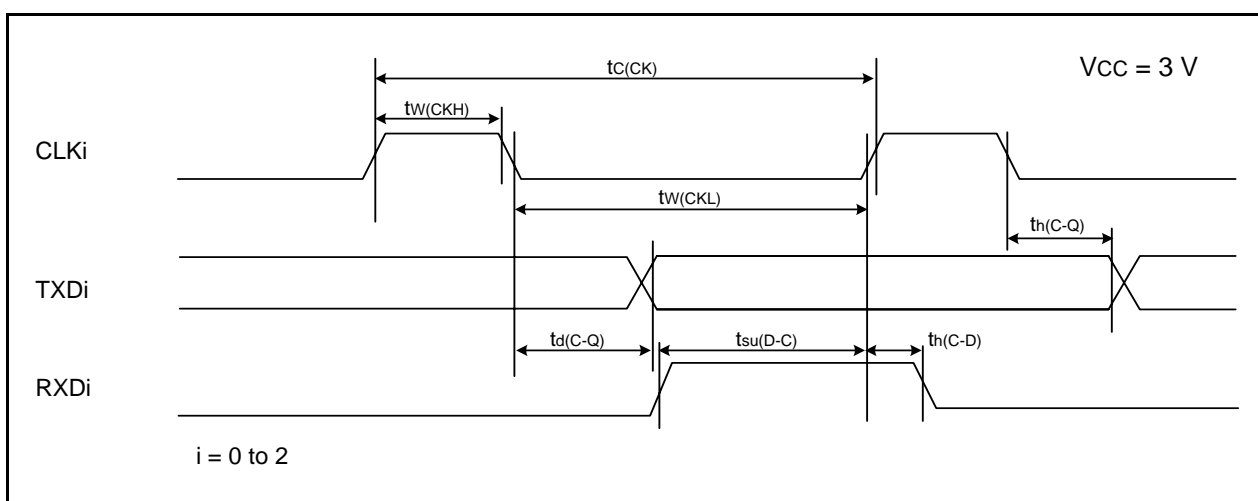
1. When selecting the digital filter by the  $\overline{INTi}$  input filter select bit, use an  $\overline{INTi}$  input HIGH width of either (1/digital filter clock frequency  $\times 3$ ) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the  $\overline{INTi}$  input filter select bit, use an  $\overline{INTi}$  input LOW width of either (1/digital filter clock frequency  $\times 3$ ) or the minimum value of standard, whichever is greater.

**Figure 5.11 Input Timing Diagram for External Interrupt  $\overline{INTi}$  and Key Input Interrupt  $\overline{Kli}$  when Vcc = 5 V**

**Table 5.27 Serial Interface**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	300	—	ns
$t_{w(CKH)}$	CLKi input "H" width	150	—	ns
$t_{w(CKL)}$	CLKi Input "L" width	150	—	ns
$t_{d(C-Q)}$	TXDi output delay time	—	80	ns
$t_{h(C-Q)}$	TXDi hold time	0	—	ns
$t_{su(D-C)}$	RXDi input setup time	70	—	ns
$t_{h(C-D)}$	RXDi input hold time	90	—	ns

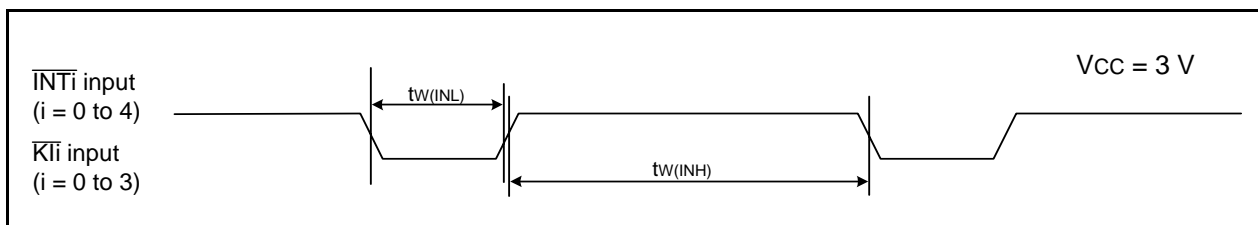
i = 0 to 2

**Figure 5.14 Serial Interface Timing Diagram when Vcc = 3 V****Table 5.28 External Interrupt  $\overline{INTi}$  (i = 0 to 4) Input, Key Input Interrupt  $\overline{Kli}$  (i = 0 to 3)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INTi}$ input "H" width, $\overline{Kli}$ input "H" width	380 (1)	—	ns
$t_{w(INL)}$	$\overline{INTi}$ input "L" width, $\overline{Kli}$ input "L" width	380 (2)	—	ns

Notes:

1. When selecting the digital filter by the  $\overline{INTi}$  input filter select bit, use an  $\overline{INTi}$  input HIGH width of either (1/digital filter clock frequency  $\times$  3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the  $\overline{INTi}$  input filter select bit, use an  $\overline{INTi}$  input LOW width of either (1/digital filter clock frequency  $\times$  3) or the minimum value of standard, whichever is greater.

**Figure 5.15 Input Timing Diagram for External Interrupt  $\overline{INTi}$  and Key Input Interrupt  $\overline{Kli}$  when Vcc = 3 V**

**Table 5.30 Electrical Characteristics (6) [ $1.8\text{ V} \leq V_{CC} < 2.7\text{ V}$ ]**  
**( $T_{opr} = -20\text{ to }85^{\circ}\text{C}$  (N version) /  $-40\text{ to }85^{\circ}\text{C}$  (D version), unless otherwise specified.)**

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
I <sub>CC</sub>	Power supply current ( $V_{CC} = 1.8\text{ to }2.7\text{ V}$ ) Single-chip mode, output pins are open, other pins are V <sub>SS</sub>	High-speed clock mode	–	2.2	–	mA
				0.8	–	
		High-speed on-chip oscillator mode	–	2.5	10	mA
				1.7	–	
				1	–	
				–	–	
		Low-speed on-chip oscillator mode	–	90	300	$\mu\text{A}$
				80	350	
		Low-speed clock mode	–	40	–	$\mu\text{A}$
				–	–	
		Wait mode	–	15	90	$\mu\text{A}$
				4	80	
				3.5	–	
				–	–	
		Stop mode	–	2.0	5	$\mu\text{A}$
				5.0 (1)	–	
		Stop mode	–	15 (2)	–	$\mu\text{A}$
				–	–	

Notes:

- Value when the program ROM capacity of the product is 16 Kbytes to 32 Kbytes.
- Value when the program ROM capacity of the product is 48 Kbytes to 128 Kbytes.

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