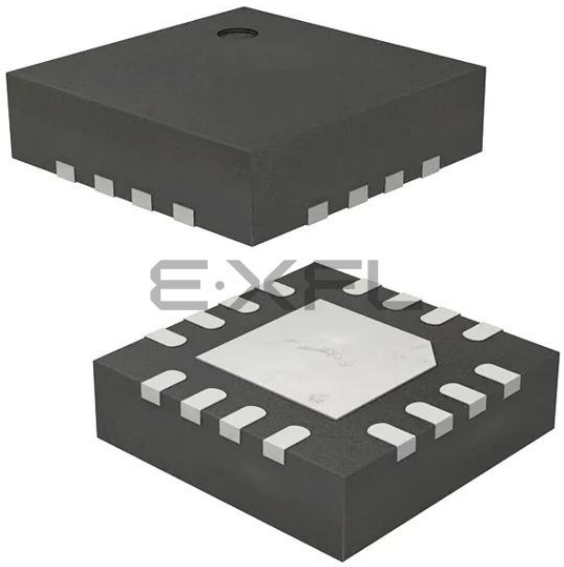

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Details	
Product Status	Active
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Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LVD, POR, PWM, WDT
Number of I/O	14
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 7x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	16-UFQFN Exposed Pad
Supplier Device Package	16-QFN (3x3)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mkl03z32vfg4

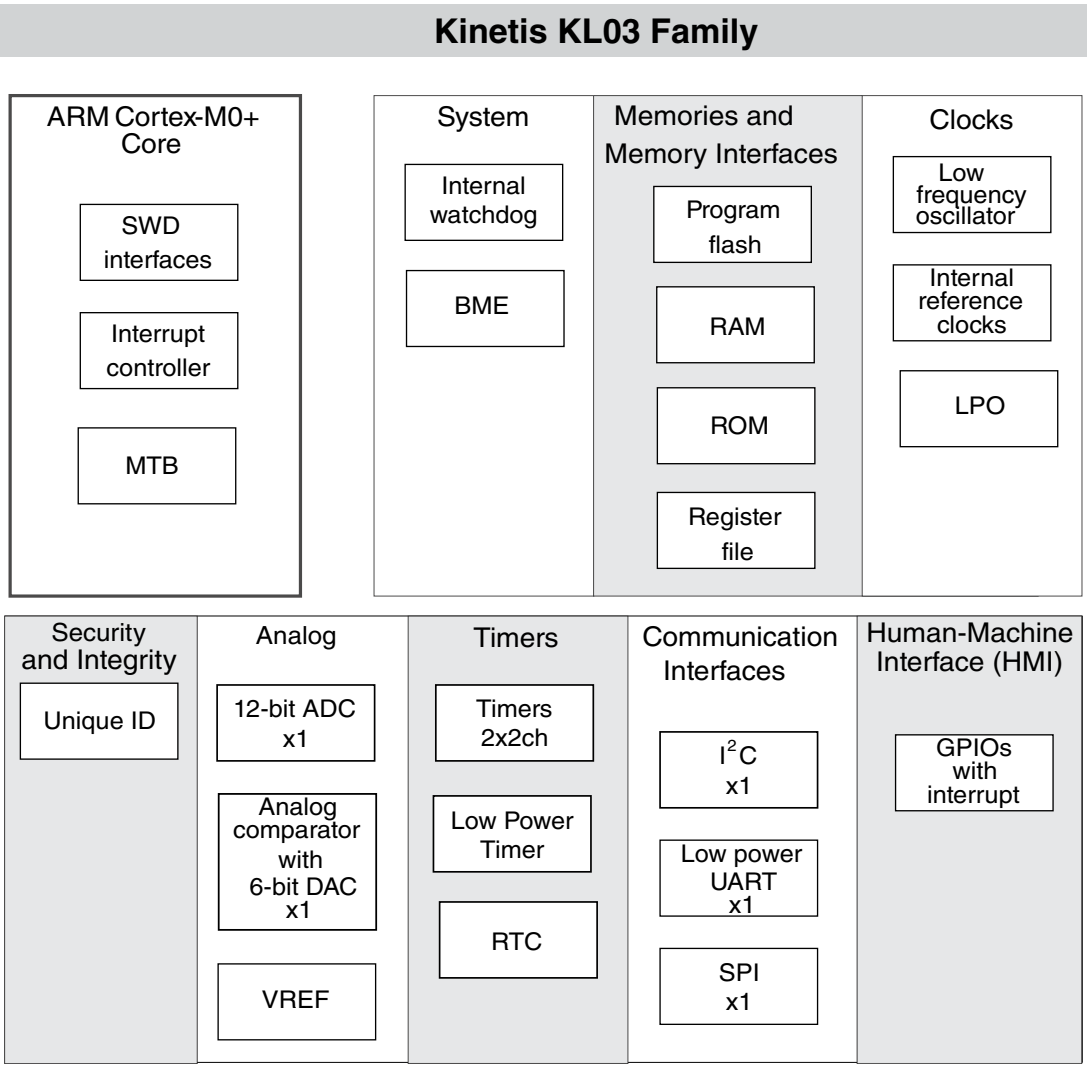


Figure 1. Functional block diagram

1 Ratings

1.1 Thermal handling ratings

Table 1. Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T_{STG}	Storage temperature	–55	150	°C	1
T_{SDR}	Solder temperature, lead-free	—	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

1.2 Moisture handling ratings

Table 2. Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

1.3 ESD handling ratings

Table 3. ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V_{HBM}	Electrostatic discharge voltage, human body model	–2000	+2000	V	1
V_{CDM}	Electrostatic discharge voltage, charged-device model	–500	+500	V	2
I_{LAT}	Latch-up current at ambient temperature of 105 °C	–100	+100	mA	3

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.
3. Determined according to JEDEC Standard JESD78, *IC Latch-Up Test*.

Table 6. V_{DD} supply LVD and POR operating requirements (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{LVW3H}	• Level 3 falling (LVWV = 10)	2.82	2.90	2.98	V	
V_{LVW4H}	• Level 4 falling (LVWV = 11)	2.92	3.00	3.08	V	
V_{HYSH}	Low-voltage inhibit reset/recover hysteresis — high range	—	±60	—	mV	—
V_{LVDL}	Falling low-voltage detect threshold — low range (LVDV=00)	1.54	1.60	1.66	V	—
	Low-voltage warning thresholds — low range					1
V_{LVW1L}	• Level 1 falling (LVWV = 00)	1.74	1.80	1.86	V	
V_{LVW2L}	• Level 2 falling (LVWV = 01)	1.84	1.90	1.96	V	
V_{LVW3L}	• Level 3 falling (LVWV = 10)	1.94	2.00	2.06	V	
V_{LVW4L}	• Level 4 falling (LVWV = 11)	2.04	2.10	2.16	V	
V_{HYSL}	Low-voltage inhibit reset/recover hysteresis — low range	—	±40	—	mV	—
V_{BG}	Bandgap voltage reference	0.97	1.00	1.03	V	—
t_{LPO}	Internal low power oscillator period — factory trimmed	900	1000	1100	µs	—

1. Rising thresholds are falling threshold + hysteresis voltage

2.2.3 Voltage and current operating behaviors

Table 7. Voltage and current operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
V_{OH}	Output high voltage — Normal drive pad (except $\overline{\text{RESET}}$)				1, 2
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OH} = –5 mA	V_{DD} – 0.5	—	V	
	• 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OH} = –2.5 mA	V_{DD} – 0.5	—	V	
V_{OH}	Output high voltage — High drive pad (except $\overline{\text{RESET}}$)				1, 2
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OH} = –20 mA	V_{DD} – 0.5	—	V	
	• 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OH} = –10 mA	V_{DD} – 0.5	—	V	
I_{OHT}	Output high current total for all ports	—	100	mA	—
V_{OL}	Output low voltage — Normal drive pad				1
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OL} = 5 mA	—	0.5	V	
	• 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OL} = 2.5 mA	—	0.5	V	
V_{OL}	Output low voltage — High drive pad				1

Table continues on the next page...

Table 8. Power mode transition operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Note
	• VLLS3 → RUN	—	93	104	µs	—
	• VLPS → RUN	—	7.5	8	µs	—
	• STOP → RUN	—	7.5	8	µs	—

1. Normal boot (FTFA_FOPT[LPBOOT]=11).

2.2.5 Power consumption operating behaviors

Table 9. KL03 QFN packages power consumption operating behaviors

Symbol	Description	Min.	Typ.	Max.[1]	Unit	Notes
I_{DDA}	Analog supply current	—	—	See note	mA	2
I_{DD_RUNCO}	Running CoreMark in flash in compute operation mode—48M HIRC mode, 48 MHz core / 24 MHz flash, V_{DD} = 3.0 V					3
	• at 25 °C	—	5.49	5.71	mA	
	• at 105 °C	—	5.62	5.84		
I_{DD_RUNCO}	Running While(1) loop in flash in compute operation mode—48M HIRC mode, 48 MHz core / 24 MHz flash, V_{DD} = 3.0 V					3
	• at 25 °C	—	5.16	5.37	mA	
	• at 105 °C	—	5.27	5.48		
I_{DD_RUN}	Run mode current—48M HIRC mode, running CoreMark in Flash all peripheral clock disable 48 MHz core/24 MHz flash, V_{DD} = 3.0 V					3
	• at 25 °C	—	6.03	6.27	mA	
	• at 105 °C	—	6.16	6.41		
I_{DD_RUN}	Run mode current—48M HIRC mode, running CoreMark in flash all peripheral clock disable, 24 MHz core/12 MHz flash, V_{DD} = 3.0 V					3
	• at 25 °C	—	3.71	3.86	mA	
	• at 105 °C	—	3.81	3.96		
I_{DD_RUN}	Run mode current—48M HIRC mode, running CoreMark in Flash all peripheral clock disable 12 MHz core/6 MHz flash, V_{DD} = 3.0 V					3
	• at 25 °C	—	2.47	2.57	mA	
	• at 105 °C	—	2.58	2.68		

Table continues on the next page...

Table 9. KL03 QFN packages power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.[1]	Unit	Notes
I_{DD_RUN}	Run mode current—48M HIRC mode, running CoreMark in Flash all peripheral clock enable 48 MHz core/24 MHz flash, V_{DD} = 3.0 V • at 25 °C • at 105 °C	 — —	 6.43 6.56	 6.69 6.82	 mA	3
I_{DD_RUN}	Run mode current—48M HIRC mode, running While(1) loop in flash all peripheral clock disable, 48 MHz core/24 MHz flash, V_{DD} = 3.0 V • at 25 °C • at 105 °C	 — —	 5.71 5.82	 5.94 6.05	 mA	—
I_{DD_RUN}	Run mode current—48M HIRC mode, running While(1) loop in Flash all peripheral clock disable, 24 MHz core/12 MHz flash, V_{DD} = 3.0 V • at 25 °C • at 105 °C	 — —	 3.3 3.4	 3.43 3.54	 mA	—
I_{DD_RUN}	Run mode current—48M HIRC mode, Running While(1) loop in Flash all peripheral clock disable, 12 MHz core/6 MHz flash, V_{DD} = 3.0 V • at 25 °C • at 105 °C	 — —	 2.28 2.38	 2.37 2.48	 mA	—
I_{DD_RUN}	Run mode current—48M HIRC mode, Running While(1) loop in Flash all peripheral clock enable, 48 MHz core/24 MHz flash, V_{DD} = 3.0 V • at 25 °C • at 105 °C	 — —	 6.1 6.22	 6.34 6.47	 mA	—
I_{DD_RUN}	Run mode current—48M HIRC mode, running While(1) loop in SRAM all peripheral clock disable, 48 MHz core/24 MHz flash, V_{DD} = 3.0 V • at 25 °C • at 105 °C	 — —	 3.14 3.27	 3.23 3.36	 mA	—
I_{DD_RUN}	Run mode current—48M HIRC mode, running While(1) loop in SRAM all peripheral clock enable, 48 MHz core/24 MHz flash, V_{DD} = 3.0 V • at 25 °C • at 105 °C	 — —	 3.54 3.67	 3.63 3.76	 mA	—
I_{DD_VLPRCO}	Very-low-power run While(1) loop in flash in compute operation mode— 2 MHz LIRC mode, 2 MHz core/0.5 MHz flash, V_{DD} = 3.0 V • at 25 °C	 —	 500	 750	 µA	—
I_{DD_VLPRCO}	Very-low-power-run While(1) loop in SRAM in compute operation mode— 8 MHz LIRC mode, 4 MHz core / 1 MHz flash, V_{DD} = 3.0 V • at 25 °C	 —	 188	 217	 µA	—

Table continues on the next page...

Table 9. KL03 QFN packages power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.[1]	Unit	Notes
I_{DD_VLLS0}	Very-low-leakage stop mode 0 current all peripheral disabled (SMC_STOPCTRL[PORPO] = 1) at 3 V					4
	• at 25 °C and below	—	77	350	nA	
	• at 50 °C	—	255	465.70		
	• at 85 °C	—	1640	1994		
	• at 105 °C	—	4080	4956		

1. The maximum values represent characterized results equivalent to the mean plus three times the standard deviation (mean + 3 sigma).
2. The analog supply current is the sum of the active or disabled current for each of the analog modules on the device. See each module's specification for its supply current.
3. MCG_Lite configured for HIRC mode. CoreMark benchmark compiled using IAR 7.10 with optimization level high, optimized for balanced.
4. No brownout

Table 10. KL03 WLCSP package power consumption operating behaviors

Symbol	Description	Min.	Typ.	Max.[1]	Unit	Notes
I_{DDA}	Analog supply current	—	—	See note	mA	2
I_{DD_RUNCO}	Running CoreMark in flash in compute operation mode—48M HIRC mode, 48 MHz core / 24 MHz flash, V_{DD} = 3.0 V					3
	• at 25 °C	—	5.49	5.71	mA	
	• at 85 °C	—	5.59	5.81		
I_{DD_RUNCO}	Running While(1) loop in flash in compute operation mode—48M HIRC mode, 48 MHz core / 24 MHz flash, V_{DD} = 3.0 V					3
	• at 25 °C	—	5.16	5.37	mA	
	• at 85 °C	—	5.24	5.45		
I_{DD_RUN}	Run mode current—48M HIRC mode, running CoreMark in Flash all peripheral clock disable 48 MHz core/24 MHz flash, V_{DD} = 3.0 V					3
	• at 25 °C	—	6.03	6.27	mA	
	• at 85 °C	—	6.13	6.38		
I_{DD_RUN}	Run mode current—48M HIRC mode, running CoreMark in flash all peripheral clock disable, 24 MHz core/12 MHz flash, V_{DD} = 3.0 V					3
	• at 25 °C	—	3.71	3.86	mA	
	• at 85 °C	—	3.78	3.93		
I_{DD_RUN}	Run mode current—48M HIRC mode, running CoreMark in Flash all peripheral clock disable 12 MHz core/6 MHz flash, V_{DD} = 3.0 V	—	2.47	2.57	mA	3

Table continues on the next page...

Table 10. KL03 WLCSP package power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.[1]	Unit	Notes
	• at 25 °C • at 85 °C	— —	2.55 2.65	2.65 2.80		
I_{DD_RUN}	Run mode current—48M HIRC mode, running CoreMark in Flash all peripheral clock enable 48 MHz core/24 MHz flash, V_{DD} = 3.0 V • at 25 °C • at 85 °C	 — —	 6.43 6.53	 6.69 6.79	 mA	3
I_{DD_RUN}	Run mode current—48M HIRC mode, running While(1) loop in flash all peripheral clock disable, 48 MHz core/24 MHz flash, V_{DD} = 3.0 V • at 25 °C • at 85 °C	 — —	 5.71 5.79	 5.94 6.02	 mA	—
I_{DD_RUN}	Run mode current—48M HIRC mode, running While(1) loop in Flash all peripheral clock disable, 24 MHz core/12 MHz flash, V_{DD} = 3.0 V • at 25 °C • at 85 °C	 — —	 3.3 3.37	 3.43 3.50	 mA	—
I_{DD_RUN}	Run mode current—48M HIRC mode, Running While(1) loop in Flash all peripheral clock disable, 12 MHz core/6 MHz flash, V_{DD} = 3.0 V • at 25 °C • at 85 °C	 — —	 2.28 2.35	 2.37 2.44	 mA	—
I_{DD_RUN}	Run mode current—48M HIRC mode, Running While(1) loop in Flash all peripheral clock enable, 48 MHz core/24 MHz flash, V_{DD} = 3.0 V • at 25 °C • at 85 °C	 — —	 6.1 6.19	 6.34 6.44	 mA	—
I_{DD_RUN}	Run mode current—48M HIRC mode, running While(1) loop in SRAM all peripheral clock disable, 48 MHz core/24 MHz flash, V_{DD} = 3.0 V • at 25 °C • at 85 °C	 — —	 3.14 3.24	 3.23 3.33	 mA	—
I_{DD_RUN}	Run mode current—48M HIRC mode, running While(1) loop in SRAM all peripheral clock enable, 48 MHz core/24 MHz flash, V_{DD} = 3.0 V • at 25 °C • at 85 °C	 — —	 3.54 3.64	 3.63 3.73	 mA	—

Table continues on the next page...

Table 10. KL03 WLCSP package power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.[1]	Unit	Notes
	• at 50 °C • at 85 °C	— —	3.45 3.96	3.96		
I_{DD_VLLS3}	Very-low-leakage stop mode 3 current with RTC current, at 3.0 V • at 25 °C and below • at 50 °C • at 85 °C	— — —	1.47 1.82 3.93	1.56 1.94 4.44	µA	—
I_{DD_VLLS3}	Very-low-leakage stop mode 3 current with RTC current, at 1.8 V • at 25 °C and below • at 50 °C • at 85 °C	— — —	1.33 1.65 3.56	1.42 1.77 4.07	µA	—
I_{DD_VLLS1}	Very-low-leakage stop mode 1 current all peripheral disabled at 3.0 V • at 25 °C and below • at 50°C • at 85°C	— — —	566 788 2270	690 839 2600	nA	—
I_{DD_VLLS1}	Very-low-leakage stop mode 1 current RTC enabled at 3.0 V • at 25 °C and below • at 50°C • at 85°C	— — —	969 1200 2740	1059 1251 3070	nA	—
I_{DD_VLLS1}	Very-low-leakage stop mode 1 current RTC enabled at 1.8 V • at 25 °C and below • at 50°C • at 85°C	— — —	826 1040 2400	916 1091 2730	nA	—
I_{DD_VLLS0}	Very-low-leakage stop mode 0 current all peripheral disabled (SMC_STOPCTRL[PORPO] = 0) at 3.0 V • at 25 °C and below • at 50 °C • at 85 °C	— — —	265 467 1920	373 512.9 2256	nA	—
I_{DD_VLLS0}	Very-low-leakage stop mode 0 current all peripheral disabled (SMC_STOPCTRL[PORPO] = 1) at 3 V • at 25 °C and below • at 50 °C • at 85 °C	— — —	77 255 1640	350 465.70 1994	nA	4

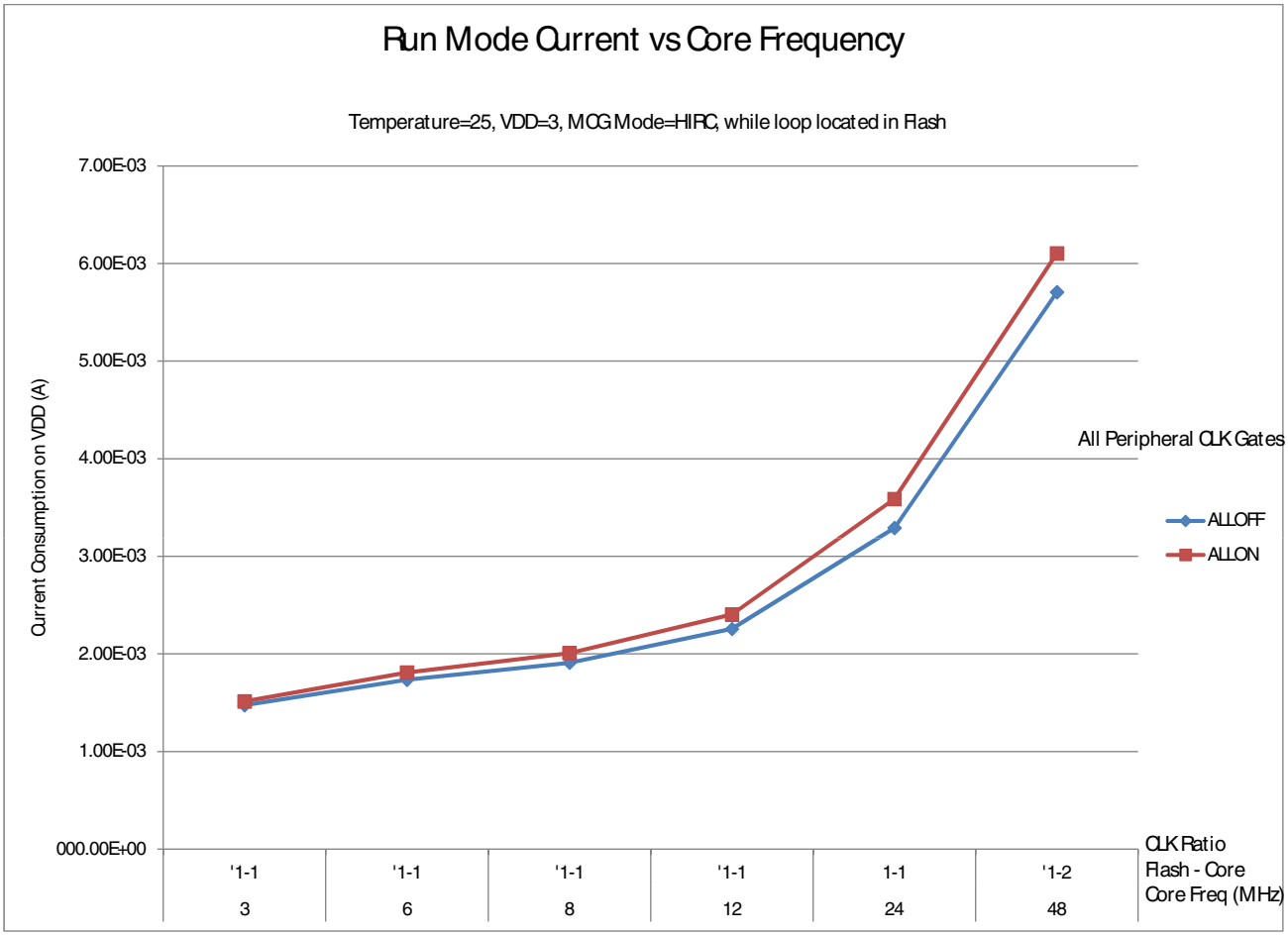


Figure 3. Run mode supply current vs. core frequency (loop located in flash)

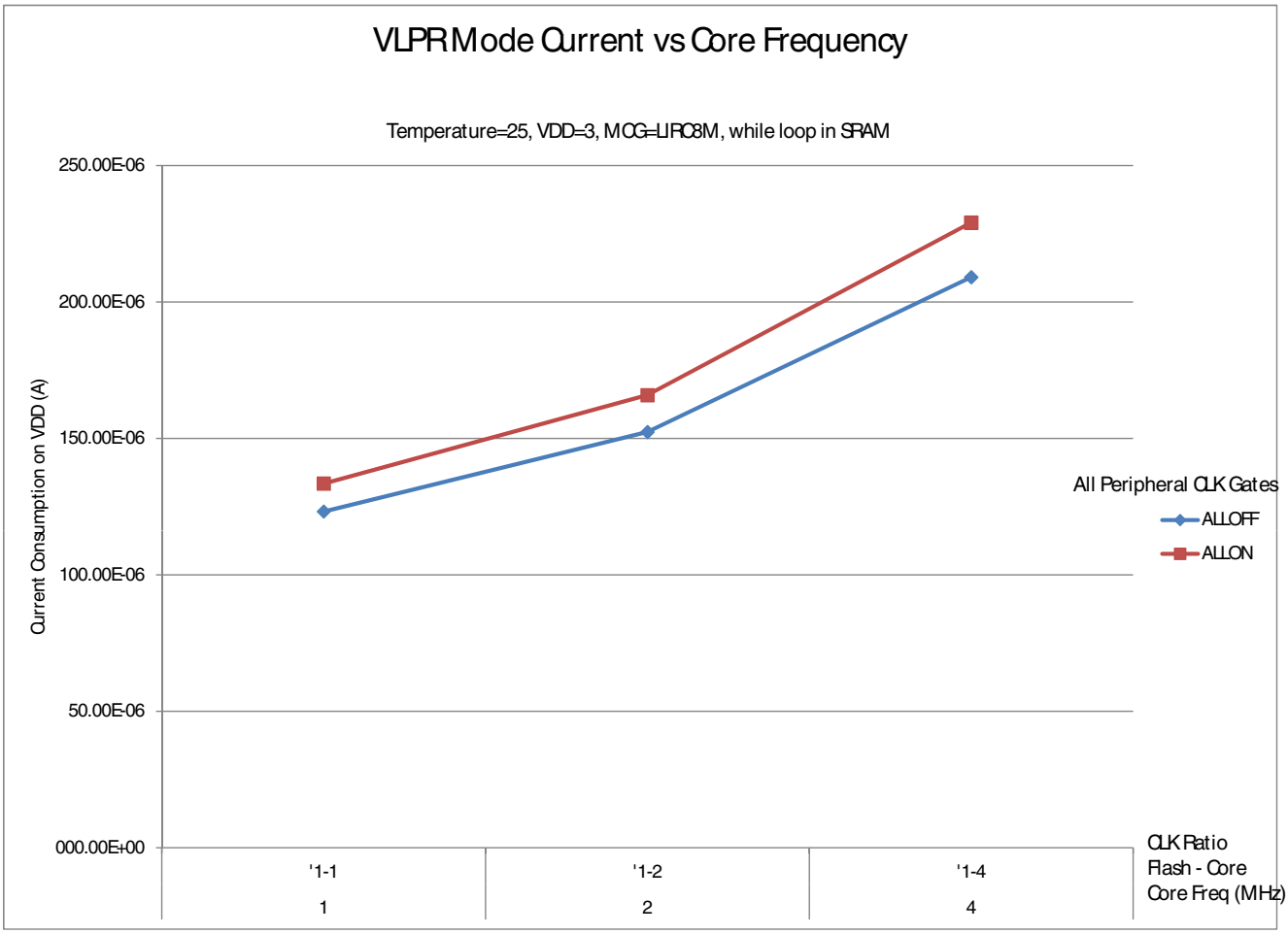


Figure 5. VLPR mode current vs. core frequency (loop in SRAM)

2.2.6 EMC radiated emissions operating behaviors

Table 12. EMC radiated emissions operating behaviors for 24-pin QFN package

Symbol	Description	Frequency band (MHz)	Typ.	Unit	Notes
V_{RE1}	Radiated emissions voltage, band 1	0.15–50	5	dBµV	1, 2
V_{RE2}	Radiated emissions voltage, band 2	50–150	7	dBµV	
V_{RE3}	Radiated emissions voltage, band 3	150–500	5	dBµV	
V_{RE4}	Radiated emissions voltage, band 4	500–1000	5	dBµV	
V_{RE_IEC}	IEC/SAE level	0.15–1000	N	—	2, 3

1. Determined according to IEC 61967-2 (and SAE J1752/3) radiated radio frequency (RF) emissions measurement standard. Typical Configuration: Appendix B: DUT Software Configuration—2. Typical Configuration.
2. V_{DD} = 3.3 V, T_A = 25 °C, f_{irc48m} = 48 MHz, f_{SYS} = 48 MHz, f_{BUS} = 24 MHz

1. The frequency limitations in VLPR and VLPS modes here override any frequency specification listed in the timing specification for any other module. These same frequency limits apply to VLPS, whether VLPS was entered from RUN or from VLPR.
2. The LPTMR can be clocked at this speed in VLPR or VLPS only when the source is an external pin.

2.3.2 General switching specifications

These general-purpose specifications apply to all signals configured for GPIO and UART signals.

Table 15. General switching specifications

Description	Min.	Max.	Unit	Notes
GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path	1.5	—	Bus clock cycles	1
External RESET and NMI pin interrupt pulse width — Asynchronous path	100	—	ns	2
GPIO pin interrupt pulse width — Asynchronous path	16	—	ns	2
Port rise and fall time	—	36	ns	3

1. The greater synchronous and asynchronous timing must be met.
2. This is the shortest pulse that is guaranteed to be recognized.
3. 75 pF load

2.4 Thermal specifications

2.4.1 Thermal operating requirements

Table 16. Thermal operating requirements of WLCSP package

Symbol	Description	Min.	Max.	Unit
T_J	Die junction temperature	–40	95	°C
T_A	Ambient temperature	–40	85	°C

Table 17. Thermal operating requirements of other packages

Symbol	Description	Min.	Max.	Unit
T_J	Die junction temperature	–40	125	°C
T_A	Ambient temperature	–40	105	°C

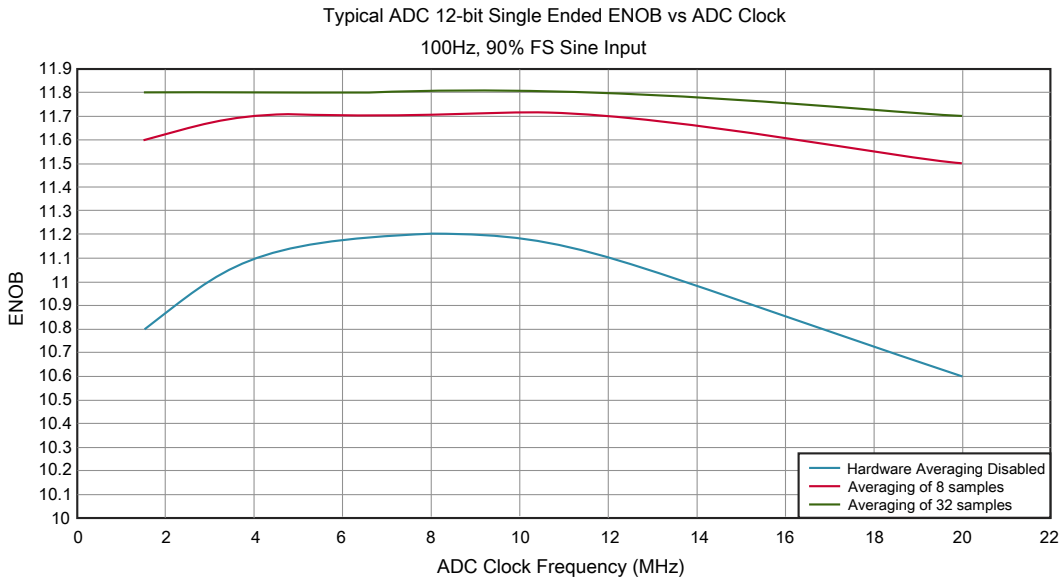


Figure 9. Typical ENOB vs. ADC_CLK for 12-bit single-ended mode

3.6.2 CMP and 6-bit DAC electrical specifications

Table 31. Comparator and 6-bit DAC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage	1.71	—	3.6	V
I_{DDHS}	Supply current, High-speed mode (EN=1, PMODE=1)	—	—	200	µA
I_{DDLS}	Supply current, low-speed mode (EN=1, PMODE=0)	—	—	20	µA
V_{AIN}	Analog input voltage	V_{SS} – 0.3	—	V_{DD}	V
V_{AIO}	Analog input offset voltage	—	—	20	mV
V_H	Analog comparator hysteresis[1]				
	• CR0[HYSTCTR] = 00	—	5	—	mV
	• CR0[HYSTCTR] = 01	—	10	—	mV
	• CR0[HYSTCTR] = 10	—	20	—	mV
	• CR0[HYSTCTR] = 11	—	30	—	mV
V_{CMPOh}	Output high	V_{DD} – 0.5	—	—	V
V_{CMPOl}	Output low	—	—	0.5	V
t_{DHS}	Propagation delay, high-speed mode (EN=1, PMODE=1)	20	50	200	ns
t_{DLS}	Propagation delay, low-speed mode (EN=1, PMODE=0)	80	250	600	ns
	Analog comparator initialization delay[2]	—	—	40	µs

Table continues on the next page...

Table 31. Comparator and 6-bit DAC electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit
I_{DAC6b}	6-bit DAC current adder (enabled)	—	7	—	µA
INL	6-bit DAC integral non-linearity	–0.5	—	0.5	LSB[3]
DNL	6-bit DAC differential non-linearity	–0.3	—	0.3	LSB

1. Typical hysteresis is measured with input voltage range limited to 0.6 to V_{DD}–0.6 V.
2. Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to CMP_DACCR[DACEN], CMP_DACCR[VRSEL], CMP_DACCR[VOSEL], CMP_MUXCR[PSEL], and CMP_MUXCR[MSEL]) and the comparator output settling to a stable level.
3. 1 LSB = $V_{reference}$/64

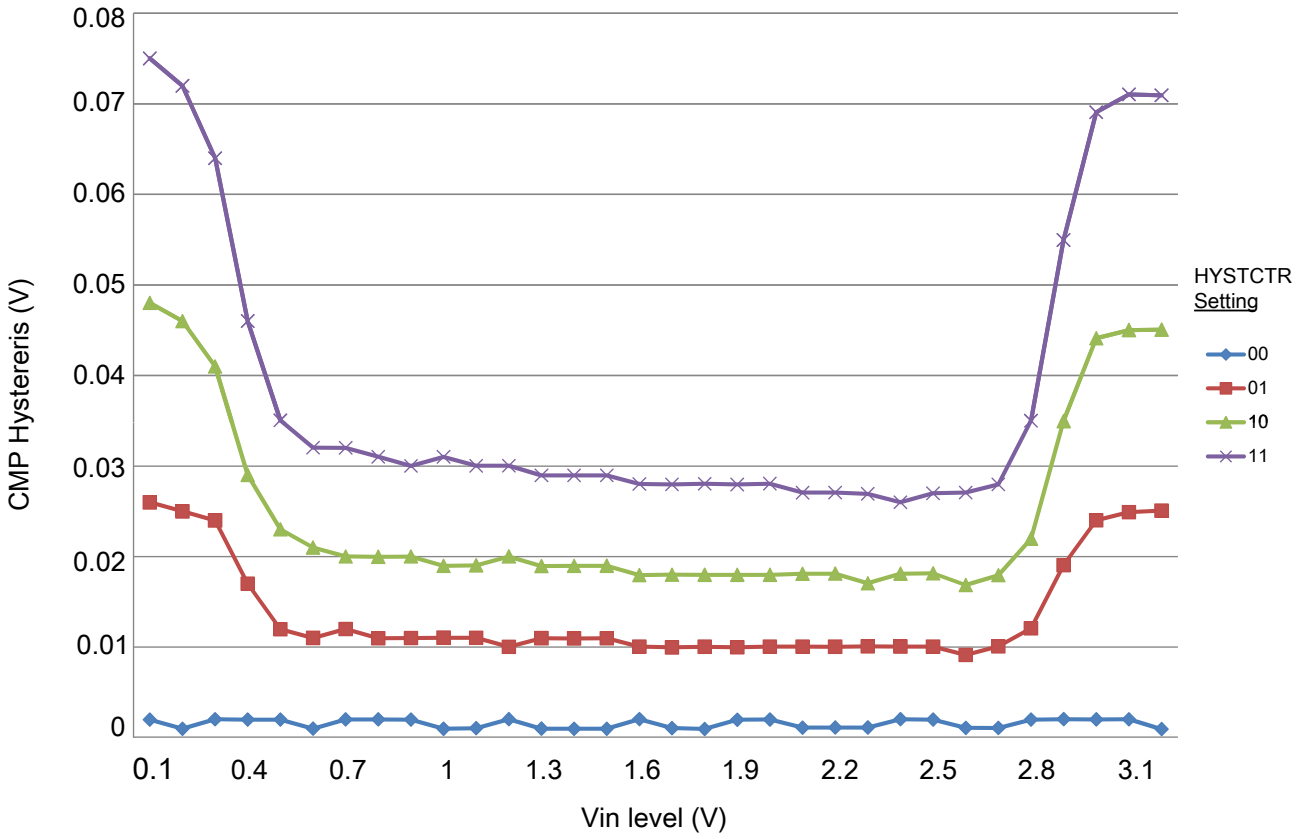
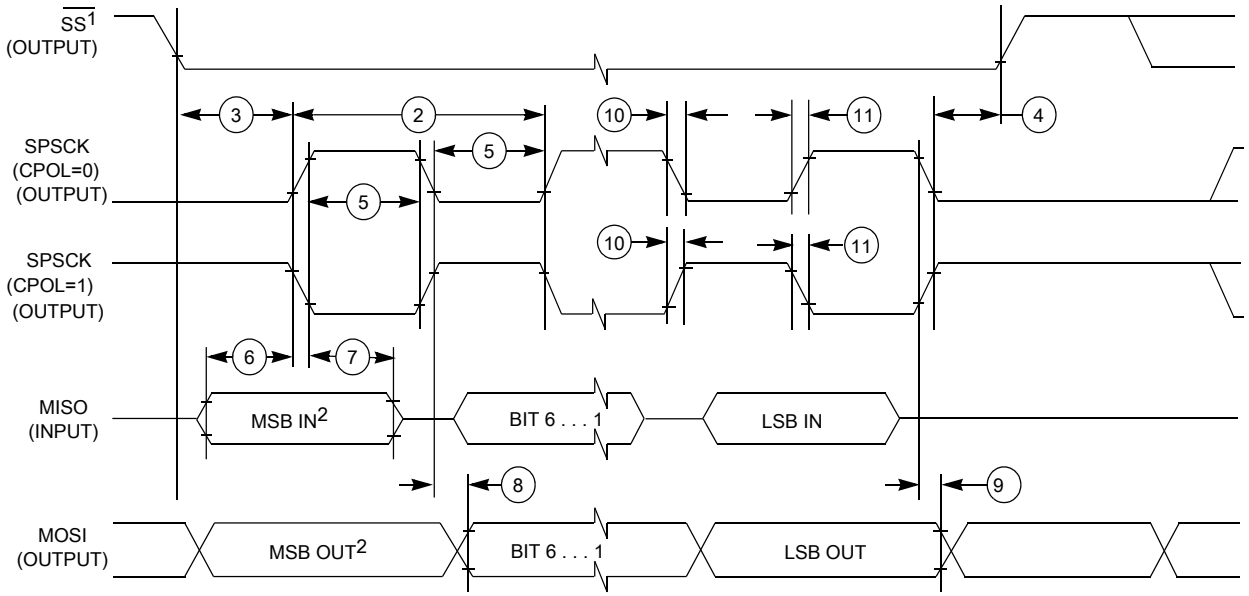


Figure 10. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 0)

Table 37. SPI master mode timing on slew rate enabled pads (continued)

Num.	Symbol	Description	Min.	Max.	Unit	Note
5	t_{WSPSCK}	Clock (SPSCK) high or low time	$t_{periph} - 30$	1024 x t_{periph}	ns	—
6	t_{SU}	Data setup time (inputs)	96	—	ns	—
7	t_{HI}	Data hold time (inputs)	0	—	ns	—
8	t_v	Data valid (after SPSCK edge)	—	52	ns	—
9	t_{HO}	Data hold time (outputs)	0	—	ns	—
10	t_{RI}	Rise time input	—	$t_{periph} - 25$	ns	—
	t_{FI}	Fall time input				
11	t_{RO}	Rise time output	—	36	ns	—
	t_{FO}	Fall time output				

1. For SPI0, f_{periph} is the bus clock (f_{BUS}).
2. $t_{periph} = 1/f_{periph}$



1. If configured as an output.
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 12. SPI master mode timing (CPHA = 0)

Table 39. SPI slave mode timing on slew rate enabled pads

Num.	Symbol	Description	Min.	Max.	Unit	Note
1	f_{op}	Frequency of operation	0	$f_{periph}/4$	Hz	1
2	t_{SPSCK}	SPSCK period	4 x t_{periph}	—	ns	2
3	t_{Lead}	Enable lead time	1	—	t_{periph}	—
4	t_{Lag}	Enable lag time	1	—	t_{periph}	—
5	t_{WSPSCK}	Clock (SPSCK) high or low time	t_{periph} – 30	—	ns	—
6	t_{SU}	Data setup time (inputs)	2	—	ns	—
7	t_{HI}	Data hold time (inputs)	7	—	ns	—
8	t_a	Slave access time	—	t_{periph}	ns	3
9	t_{dis}	Slave MISO disable time	—	t_{periph}	ns	4
10	t_v	Data valid (after SPSCK edge)	—	122	ns	—
11	t_{HO}	Data hold time (outputs)	0	—	ns	—
12	t_{RI}	Rise time input	—	t_{periph} – 25	ns	—
	t_{FI}	Fall time input				
13	t_{RO}	Rise time output	—	36	ns	—
	t_{FO}	Fall time output				

1. For SPI0, f_{periph} is the bus clock (f_{BUS}).
2. $t_{periph} = 1/f_{periph}$
3. Time to data active from high-impedance state
4. Hold time to high-impedance state

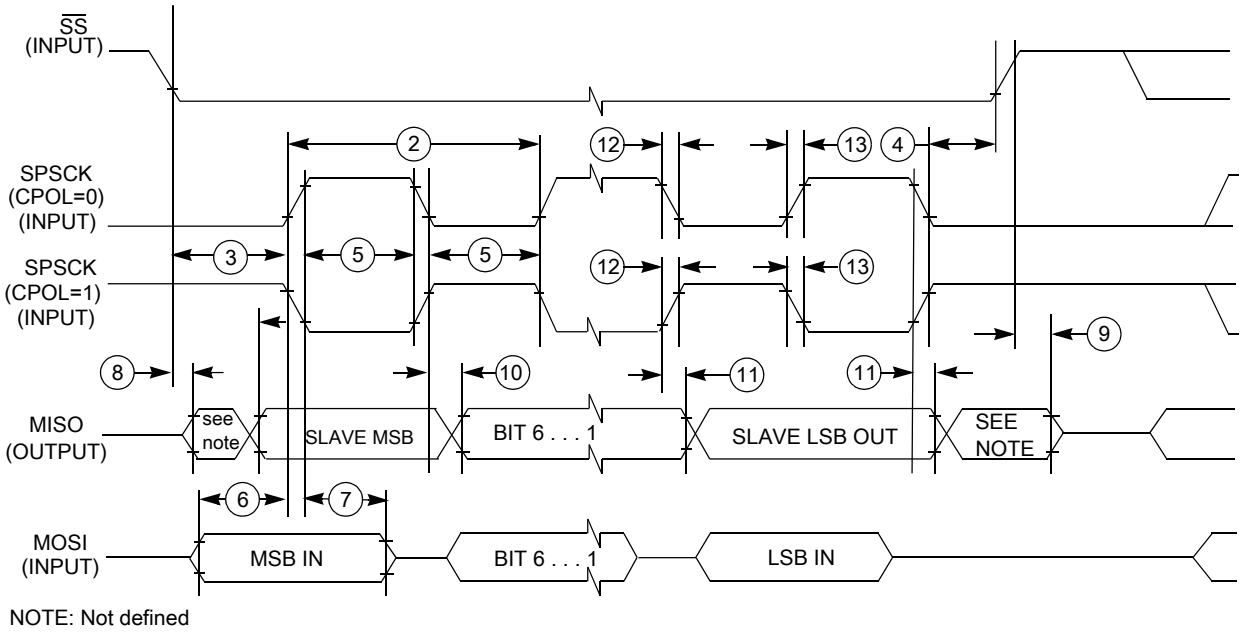


Figure 14. SPI slave mode timing (CPHA = 0)

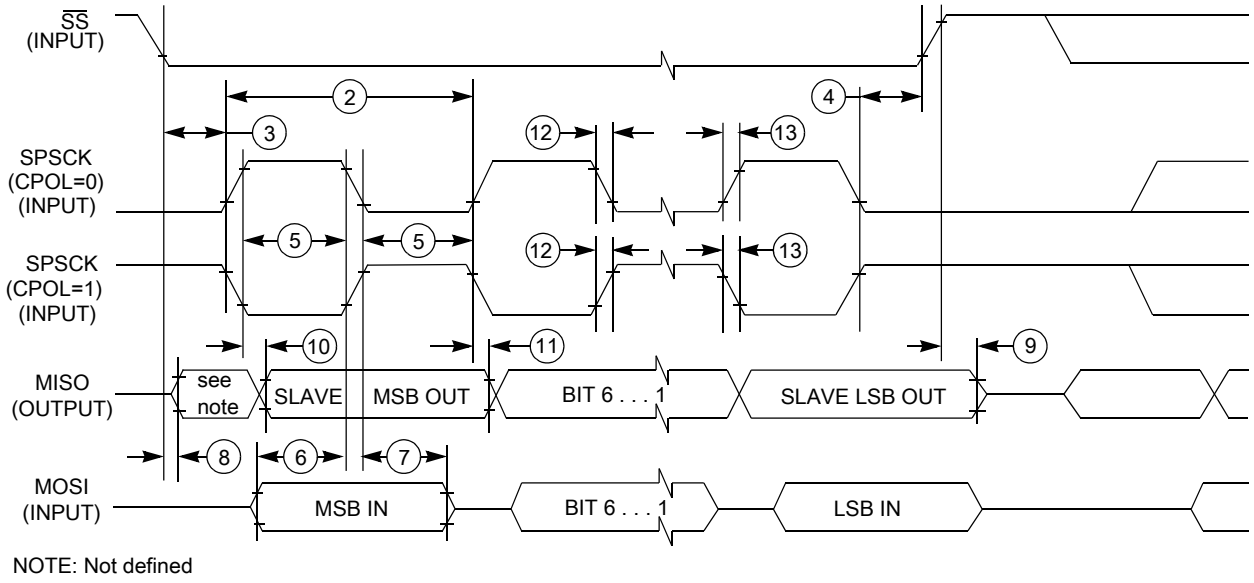


Figure 15. SPI slave mode timing (CPHA = 1)

3.8.2 Inter-Integrated Circuit Interface (I2C) timing

Table 40. I2C timing

Characteristic	Symbol	Standard Mode		Fast Mode[1]		Unit
		Minimum	Maximum	Minimum	Maximum	
SCL Clock Frequency	f_{SCL}	0	100	0	400[2]	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated.	t_{HD}; STA	4	—	0.6	—	µs
LOW period of the SCL clock	t_{LOW}	4.7	—	1.3	—	µs
HIGH period of the SCL clock	t_{HIGH}	4	—	0.6	—	µs
Set-up time for a repeated START condition	t_{SU}; STA	4.7	—	0.6	—	µs
Data hold time for I²C bus devices	t_{HD}; DAT	0[3]	3.45[4]	0[5]	0.9[3]	µs
Data set-up time	t_{SU}; DAT	250[6]	—	100[4, 7]	—	ns
Rise time of SDA and SCL signals	t_r	—	1000	20 +0.1C_b[8]	300	ns
Fall time of SDA and SCL signals	t_f	—	300	20 +0.1C_b[7]	300	ns
Set-up time for STOP condition	t_{SU}; STO	4	—	0.6	—	µs
Bus free time between STOP and START condition	t_{BUF}	4.7	—	1.3	—	µs
Pulse width of spikes that must be suppressed by the input filter	t_{SP}	N/A	N/A	0	50	ns

1. Fast mode is fully supported on all pins at VDD > 2.7 V. If VDD < 2.7 V, only pins that support high drive strength can support fast mode with maximum bus loading.

2. The maximum SCL Clock Frequency in Fast mode with maximum bus loading can only achieved when using the High drive pins (see Voltage and current operating behaviors) or when using the Normal drive pins and VDD ≥ 2.7 V
3. The master mode I²C deasserts ACK of an address byte simultaneously with the falling edge of SCL. If no slaves acknowledge this address byte, then a negative hold time can result, depending on the edge rates of the SDA and SCL lines.
4. The maximum tHD; DAT must be met only if the device does not stretch the LOW period (tLOW) of the SCL signal.
5. Input signal Slew = 10 ns and Output Load = 50 pF
6. Set-up time in slave-transmitter mode is 1 IPBus clock period, if the TX FIFO is empty.
7. A Fast mode I²C bus device can be used in a Standard mode I2C bus system, but the requirement $t_{SU;\ DAT} \geq 250$ ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, then it must output the next data bit to the SDA line $t_{rmax} + t_{SU;\ DAT} = 1000 + 250 = 1250$ ns (according to the Standard mode I²C bus specification) before the SCL line is released.
8. C_b = total capacitance of the one bus line in pF.

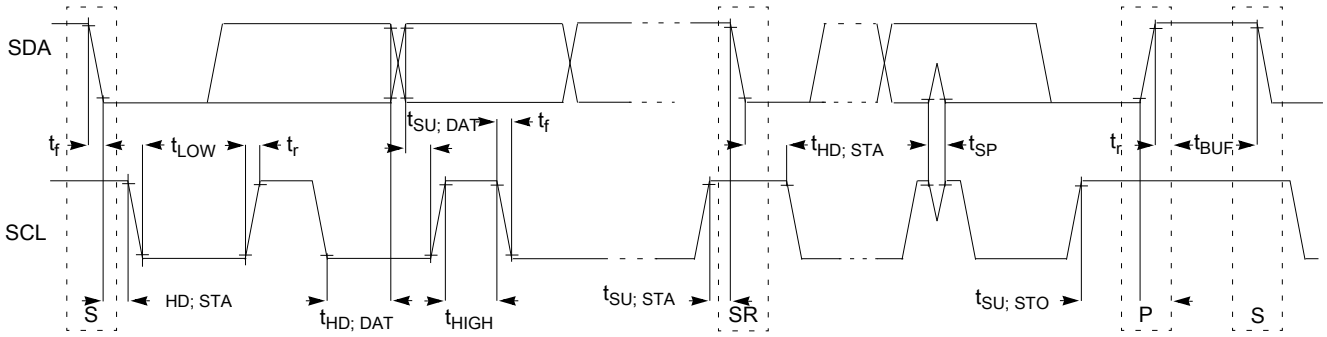


Figure 16. Timing definition for fast and standard mode devices on the I²C bus

3.8.3 UART

See General switching specifications.

4 Dimensions

4.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to **freescale.com** and perform a keyword search for the drawing's document number:

If you want the drawing for this package	Then use this document number
16-pin QFN	98ASA00525D
24-pin QFN	98ASA00602D
20-pin WLCSP	98ASA00676D

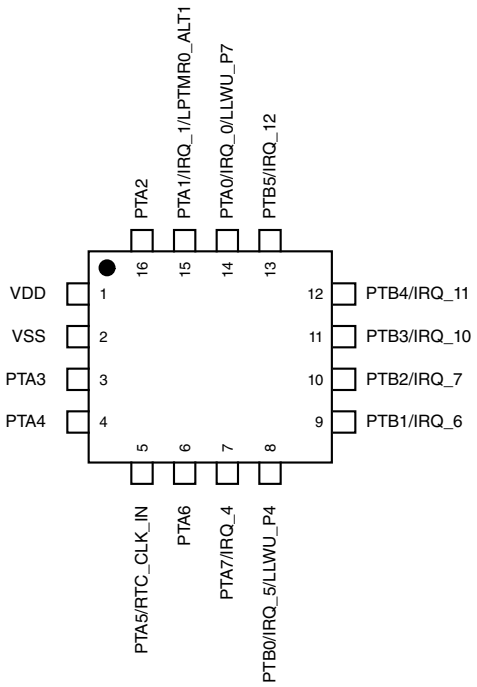


Figure 19. KL03 16-pin QFN pinout diagram

6 Ordering parts

6.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to **freescale.com** and perform a part number search for the following device numbers:

7 Part identification

7.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

- During normal operation, don't exceed any of the chip's operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

8.8 Definition: Typical value

A *typical value* is a specified value for a technical characteristic that:

- Lies within the range of values specified by the operating behavior
- Given the typical manufacturing process, is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions

Typical values are provided as design guidelines and are neither tested nor guaranteed.

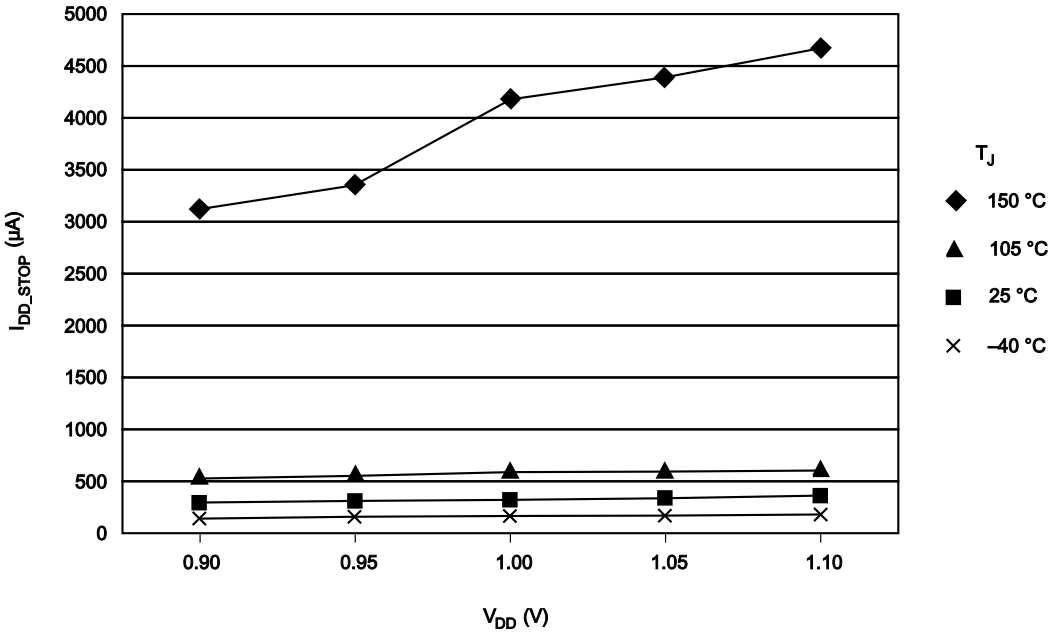
8.8.1 Example 1

This is an example of an operating behavior that includes a typical value:

Symbol	Description	Min.	Typ.	Max.	Unit
I_{WP}	Digital I/O weak pullup/pulldown current	10	70	130	µA

8.8.2 Example 2

This is an example of a chart that shows typical values for various voltage and temperature conditions:



8.9 Typical value conditions

Typical values assume you meet the following conditions (or other conditions as specified):

Table 42. Typical value conditions

Symbol	Description	Value	Unit
T_A	Ambient temperature	25	°C
V_{DD}	3.3 V supply voltage	3.3	V

9 Revision history

The following table provides a revision history for this document.

Table 43. Revision history

Rev. No.	Date	Substantial Changes
3.1	07/2014	Initial public release.
4	08/2014	Changed pinout signal names ADC0_SE5, ADC0_SE6, and ADC0_SE12 to ADC0_SE8, ADC0_SE9 and ADC0_SE15 respectively.