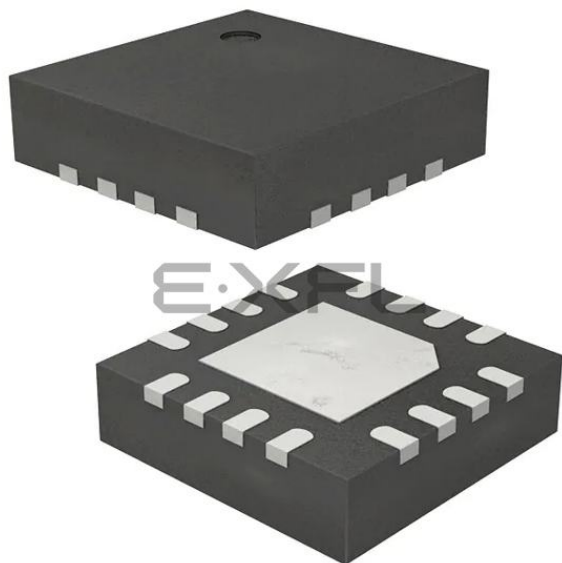




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Details

Product Status	Active
Core Processor	ARM® Cortex® -M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LVD, POR, PWM, WDT
Number of I/O	14
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 7x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	16-UFQFN Exposed Pad
Supplier Device Package	16-QFN (3x3)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mkl03z8vfg4

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1.4 Voltage and current operating ratings

Table 4. Voltage and current operating ratings

Symbol	Description	Min.	Max.	Unit
V_{DD}	Digital supply voltage	-0.3	3.8	V
I_{DD}	Digital supply current	—	120	mA
V_{IO}	IO pin input voltage	-0.3	$V_{DD} + 0.3$	V
I_D	Instantaneous maximum current single pin limit (applies to all port pins)	-25	25	mA
V_{DDA}	Analog supply voltage	$V_{DD} - 0.3$	$V_{DD} + 0.3$	V

2 General

2.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.

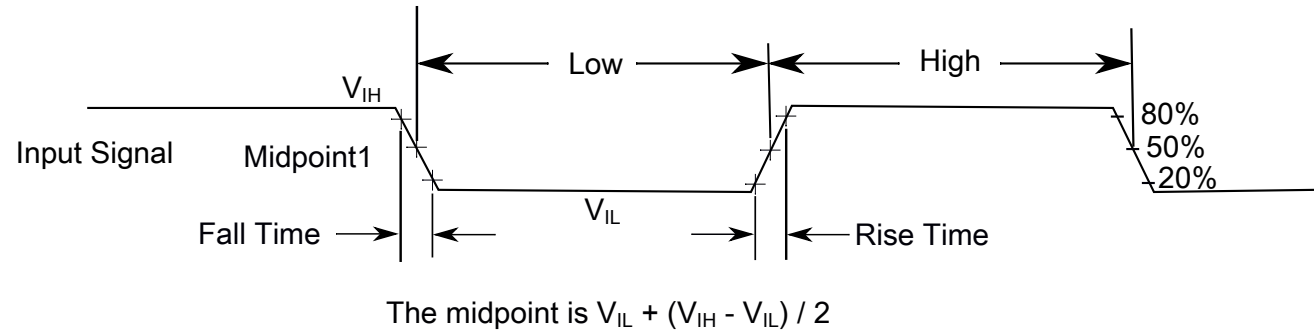


Figure 2. Input signal measurement reference

All digital I/O switching characteristics, unless otherwise specified, assume the output pins have the following characteristics.

- $C_L=30$ pF loads
- Slew rate disabled
- Normal drive strength

2.2 Nonswitching electrical specifications

Table 6. V_{DD} supply LVD and POR operating requirements (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{LVW3H}	• Level 3 falling (LVWV = 10)	2.82	2.90	2.98	V	
V_{LVW4H}	• Level 4 falling (LVWV = 11)	2.92	3.00	3.08	V	
V_{HYSH}	Low-voltage inhibit reset/recover hysteresis — high range	—	±60	—	mV	—
V_{LVDL}	Falling low-voltage detect threshold — low range (LVDV=00)	1.54	1.60	1.66	V	—
V_{LVW1L}	Low-voltage warning thresholds — low range • Level 1 falling (LVWV = 00)	1.74	1.80	1.86	V	1
V_{LVW2L}	• Level 2 falling (LVWV = 01)	1.84	1.90	1.96	V	
V_{LVW3L}	• Level 3 falling (LVWV = 10)	1.94	2.00	2.06	V	
V_{LVW4L}	• Level 4 falling (LVWV = 11)	2.04	2.10	2.16	V	
V_{HYSL}	Low-voltage inhibit reset/recover hysteresis — low range	—	±40	—	mV	—
V_{BG}	Bandgap voltage reference	0.97	1.00	1.03	V	—
t_{LPO}	Internal low power oscillator period — factory trimmed	900	1000	1100	μs	—

1. Rising thresholds are falling threshold + hysteresis voltage

2.2.3 Voltage and current operating behaviors

Table 7. Voltage and current operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
V_{OH}	Output high voltage — Normal drive pad (except RESET) • $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$, $I_{OH} = -5\text{ mA}$ • $1.71\text{ V} \leq V_{DD} \leq 2.7\text{ V}$, $I_{OH} = -2.5\text{ mA}$	$V_{DD} - 0.5$ $V_{DD} - 0.5$	— —	V V	1, 2
V_{OH}	Output high voltage — High drive pad (except RESET) • $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$, $I_{OH} = -20\text{ mA}$ • $1.71\text{ V} \leq V_{DD} \leq 2.7\text{ V}$, $I_{OH} = -10\text{ mA}$	$V_{DD} - 0.5$ $V_{DD} - 0.5$	— —	V V	1, 2
I_{OHT}	Output high current total for all ports	—	100	mA	—
V_{OL}	Output low voltage — Normal drive pad • $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$, $I_{OL} = 5\text{ mA}$ • $1.71\text{ V} \leq V_{DD} \leq 2.7\text{ V}$, $I_{OL} = 2.5\text{ mA}$	— —	0.5 0.5	V V	1
V_{OL}	Output low voltage — High drive pad				1

Table continues on the next page...

Table 7. Voltage and current operating behaviors (continued)

Symbol	Description	Min.	Max.	Unit	Notes
	$2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$, $I_{OL} = 20\text{ mA}$ $1.71\text{ V} \leq V_{DD} \leq 2.7\text{ V}$, $I_{OL} = 10\text{ mA}$	—	0.5	V	
		—	0.5	V	
I_{OLT}	Output low current total for all ports	—	100	mA	—
I_{IN}	Input leakage current (per pin) for full temperature range	—	1	μA	3
I_{IN}	Input leakage current (per pin) at 25 °C	—	0.025	μA	3
I_{IN}	Input leakage current (total all pins) for full temperature range	—	41	μA	3
I_{OZ}	Hi-Z (off-state) leakage current (per pin)	—	1	μA	—
R_{PU}	Internal pullup resistors	20	50	k Ω	4

1. I/O have both high drive and normal drive capability selected by the associated PTx_PCRn[DSE] control bit. All other GPIOs are normal drive only.
2. The reset pin only contains an active pull down device when configured as the RESET signal or as a GPIO. When configured as a GPIO output, it acts as a pseudo open drain output.
3. Measured at $V_{DD} = 3.6\text{ V}$
4. Measured at V_{DD} supply voltage = V_{DD} min and $V_{input} = V_{SS}$

2.2.4 Power mode transition operating behaviors

All specifications except t_{POR} and $VLLSx \rightarrow \text{RUN}$ recovery times in the following table assume this clock configuration:

- CPU and system clocks = 48 MHz
- Bus and flash clock = 24 MHz
- HIRC clock mode

$VLLSx \rightarrow \text{RUN}$ recovery uses LIRC clock mode at the default CPU and system frequency of 8 MHz, and a bus and flash clock frequency of 4 MHz.

Table 8. Power mode transition operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Note
t_{POR}	After a POR event, amount of time from the point V_{DD} reaches 1.8 V to execution of the first instruction across the operating temperature range of the chip.	—	—	300	μs	1
	• $VLLS0 \rightarrow \text{RUN}$	—	152	166	μs	—
	• $VLLS1 \rightarrow \text{RUN}$	—	152	166	μs	—

Table continues on the next page...

Table 8. Power mode transition operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Note
	• VLLS3 → RUN	—	93	104	μs	—
	• VLPS → RUN	—	7.5	8	μs	—
	• STOP → RUN	—	7.5	8	μs	—

1. Normal boot (FTFA_FOPT[LPBOOT]=11).

2.2.5 Power consumption operating behaviors

Table 9. KL03 QFN packages power consumption operating behaviors

Symbol	Description	Min.	Typ.	Max. ¹	Unit	Notes
I _{DDA}	Analog supply current	—	—	See note	mA	2
I _{DD_RUNCO}	Running CoreMark in flash in compute operation mode—48M HIRC mode, 48 MHz core / 24 MHz flash, V _{DD} = 3.0 V • at 25 °C • at 105 °C	— —	5.49 5.62	5.71 5.84	mA	3
I _{DD_RUNCO}	Running While(1) loop in flash in compute operation mode—48M HIRC mode, 48 MHz core / 24 MHz flash, V _{DD} = 3.0 V • at 25 °C • at 105 °C	— —	5.16 5.27	5.37 5.48	mA	3
I _{DD_RUN}	Run mode current—48M HIRC mode, running CoreMark in Flash all peripheral clock disable 48 MHz core/24 MHz flash, V _{DD} = 3.0 V • at 25 °C • at 105 °C	— —	6.03 6.16	6.27 6.41	mA	3
I _{DD_RUN}	Run mode current—48M HIRC mode, running CoreMark in flash all peripheral clock disable, 24 MHz core/12 MHz flash, V _{DD} = 3.0 V • at 25 °C • at 105 °C	— —	3.71 3.81	3.86 3.96	mA	3
I _{DD_RUN}	Run mode current—48M HIRC mode, running CoreMark in Flash all peripheral clock disable 12 MHz core/6 MHz flash, V _{DD} = 3.0 V • at 25 °C • at 105 °C	— —	2.47 2.58	2.57 2.68	mA	3

Table continues on the next page...

Table 9. KL03 QFN packages power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max. ¹	Unit	Notes
I _{DD_VLLS3}	Very-low-leakage stop mode 3 current with RTC current, at 3.0 V - at 25 °C and below - at 50 °C - at 85 °C - at 105 °C	—	1.47	1.56	μA	—
		—	1.82	1.94		
		—	3.93	4.44		
		—	7.6	8.77		
I _{DD_VLLS3}	Very-low-leakage stop mode 3 current with RTC current, at 1.8 V - at 25 °C and below - at 50 °C - at 85 °C - at 105 °C	—	1.33	1.42	μA	—
		—	1.65	1.77		
		—	3.56	4.07		
		—	6.92	8.09		
I _{DD_VLLS1}	Very-low-leakage stop mode 1 current all peripheral disabled at 3.0 V - at 25 °C and below - at 50 °C - at 85 °C - at 105 °C	—	566	690	nA	—
		—	788	839		
		—	2270	2600		
		—	4980	5820		
I _{DD_VLLS1}	Very-low-leakage stop mode 1 current RTC enabled at 3.0 V - at 25 °C and below - at 50 °C - at 85 °C - at 105 °C	—	969	1059	nA	—
		—	1200	1251		
		—	2740	3070		
		—	5610	6450		
I _{DD_VLLS1}	Very-low-leakage stop mode 1 current RTC enabled at 1.8 V - at 25 °C and below - at 50 °C - at 85 °C - at 105 °C	—	826	916	nA	—
		—	1040	1091		
		—	2400	2730		
		—	4910	5750		
I _{DD_VLLS0}	Very-low-leakage stop mode 0 current all peripheral disabled (SMC_STOPCTRL[PORPO] = 0) at 3.0 V - at 25 °C and below - at 50 °C - at 85 °C - at 105 °C	—	265	373	nA	—
		—	467	512.9		
		—	1920	2256		
		—	4540	5395		

Table continues on the next page...

1. The maximum values represent characterized results equivalent to the mean plus three times the standard deviation (mean + 3 sigma).
2. The analog supply current is the sum of the active or disabled current for each of the analog modules on the device. See each module's specification for its supply current.
3. MCG_Lite configured for HIRC mode. CoreMark benchmark compiled using IAR 7.10 with optimization level high, optimized for balanced.
4. No brownout

Table 11. Low power mode peripheral adders — typical value

Symbol	Description	Temperature (°C)						Unit
		-40	25	50	70	85	105 ¹	
I _{LIRC8MHz}	8 MHz internal reference clock (LIRC) adder. Measured by entering STOP or VLPS mode with 8 MHz LIRC enabled, MCG_SC[FCRDIV]=000b, MCG_MC[LIRC_DIV2]=000b.	68	68	68	68	68	68	μA
I _{LIRC2MHz}	2 MHz internal reference clock (LIRC) adder. Measured by entering STOP mode with the 2 MHz LIRC enabled, MCG_SC[FCRDIV]=000b, MCG_MC[LIRC_DIV2]=000b.	27	27	27	27	27	27	μA
I _{EREFSTEN32KHz}	External 32 kHz crystal clock adder by means of the OSC0_CR[EREFSTEN and EREFSTEN] bits. Measured by entering all modes with the crystal enabled. • VLLS1 • VLLS3 • VLPS • STOP	340	410	460	470	480	600	nA
		340	410	460	490	530	600	
		340	420	480	570	610	850	
		340	420	480	570	610	850	
I _{LPTMR}	LPTMR peripheral adder measured by placing the device in VLLS1 mode with LPTMR enabled using LPO.	30	30	30	85	100	200	nA
I _{CMP}	CMP peripheral adder measured by placing the device in VLLS1 mode with CMP enabled using the 6-bit DAC and a single external input for compare. Includes 6-bit DAC power consumption.	15	15	15	15	15	15	μA
I _{RTC}	RTC peripheral adder measured by placing the device in VLLS1 mode with external 32 kHz crystal enabled by means of the RTC_CR[OSCE] bit and the RTC ALARM set for 1 minute. Includes ERCLK32K (32 kHz external crystal) power consumption.	340	440	440	480	520	620	nA
I _{UART}	UART peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source waiting for RX data at 115200 baud rate.							

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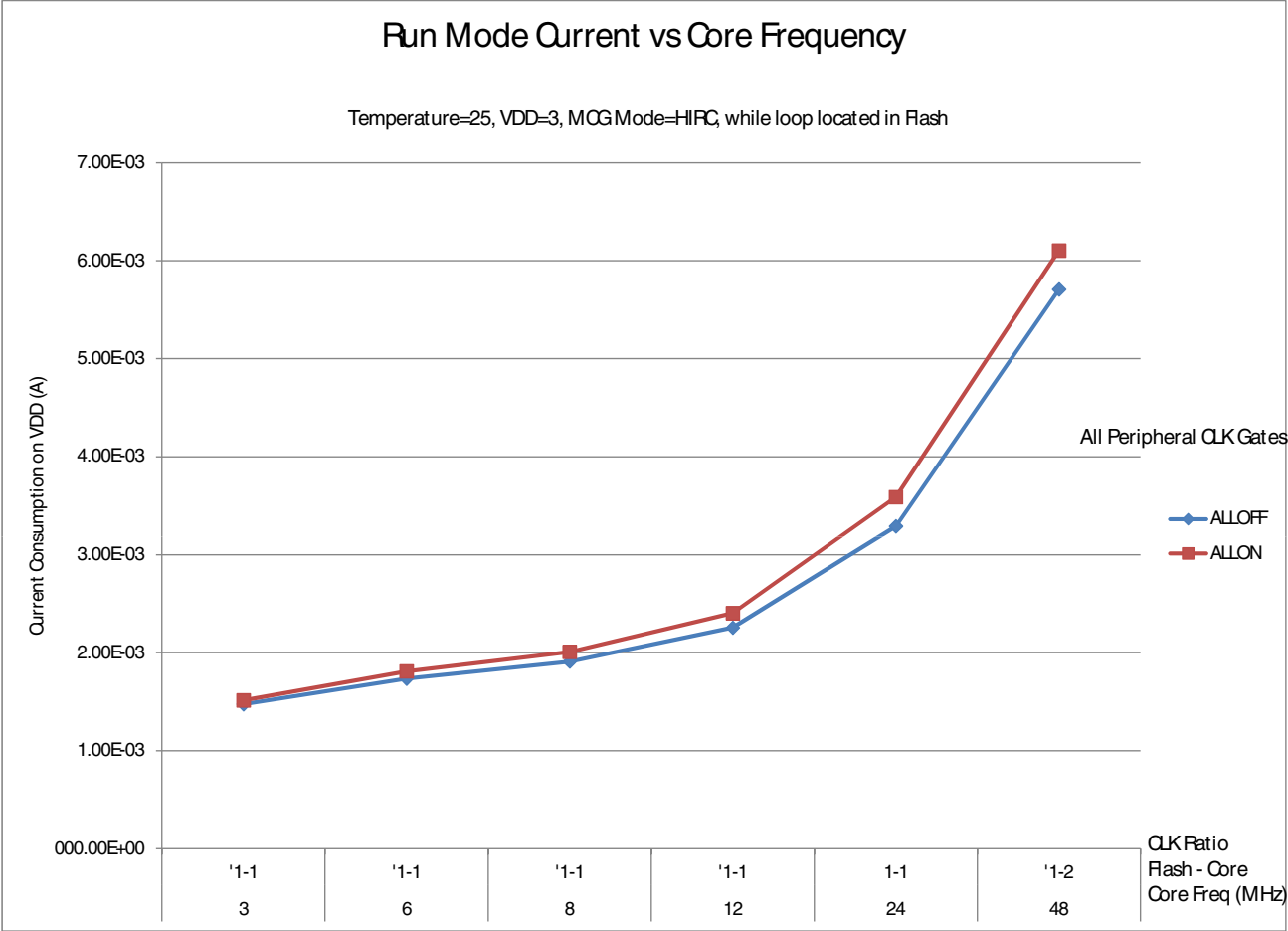


Figure 3. Run mode supply current vs. core frequency (loop located in flash)

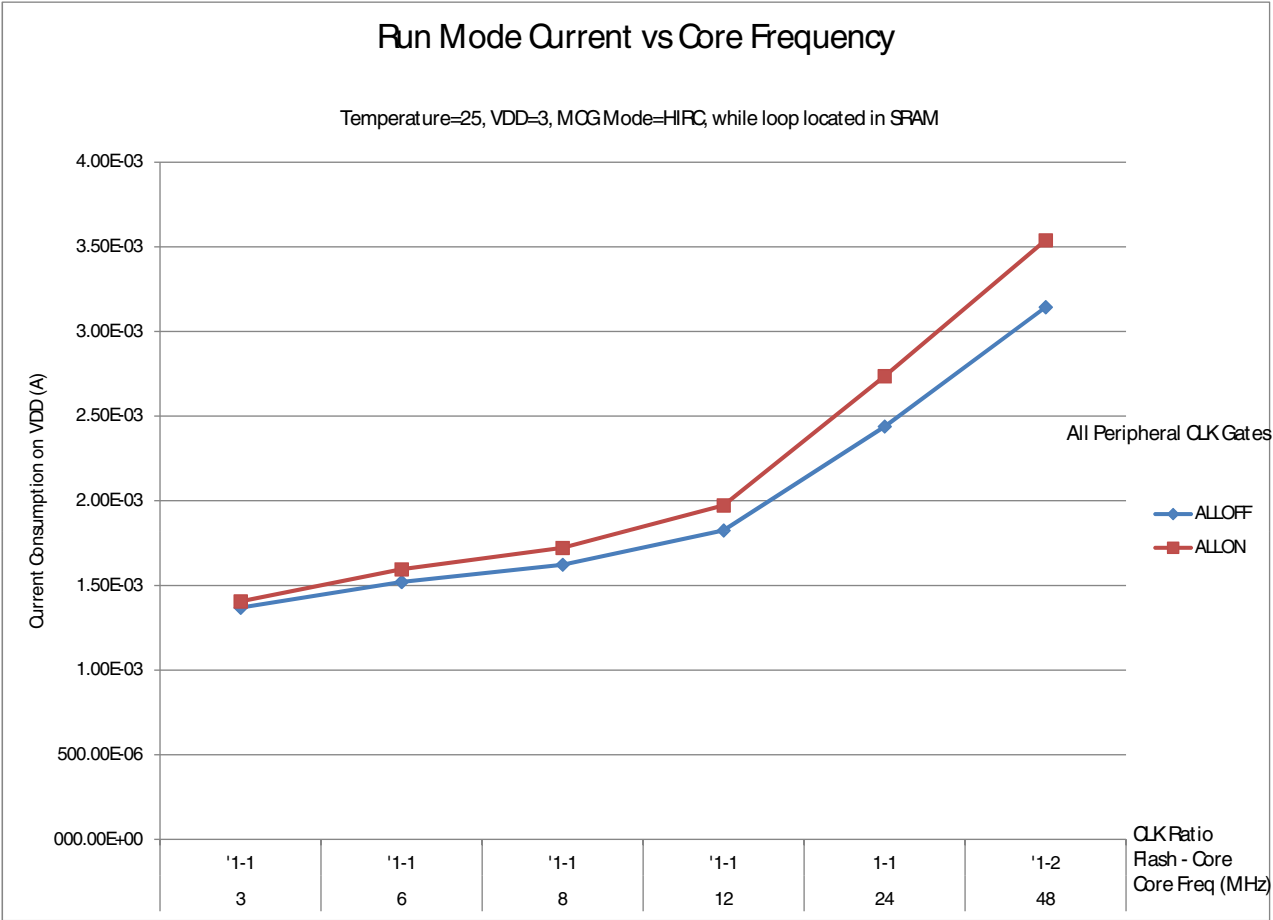


Figure 4. Run mode supply current vs. core frequency (loop located in SRAM)

3.1.1 SWD electricals

Table 19. SWD full voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
J1	SWD_CLK frequency of operation Serial wire debug	0	25	MHz
J2	SWD_CLK cycle period	1/J1	—	ns
J3	SWD_CLK clock pulse width Serial wire debug	20	—	ns
J4	SWD_CLK rise and fall times	—	3	ns
J9	SWD_DIO input data setup time to SWD_CLK rise	10	—	ns
J10	SWD_DIO input data hold time after SWD_CLK rise	0	—	ns
J11	SWD_CLK high to SWD_DIO data valid	—	32	ns
J12	SWD_CLK high to SWD_DIO high-Z	5	—	ns

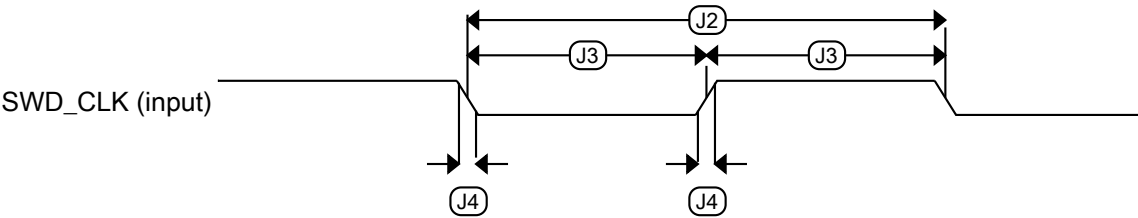


Figure 6. Serial wire clock input timing

Table 20. HIRC48M specification (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$\Delta f_{irc48m_ol_hv}$	total deviation of IRC48M frequency at high voltage (VDD=1.89V-3.6V) over temperature	—	± 0.5	± 1.0	$\%f_{irc48m}$	—
J_{cyc_irc48m}	Period Jitter (RMS)	—	35	150	ps	—
$t_{irc48mst}$	Startup time	—	2	3	μs	1

1. IRC48M startup time is defined as the time between clock enablement and clock availability for system use. Enable the clock by setting MCG_MC[HIRCEN] = 1. See reference manual for details.

Table 21. LIRC8M/2M specification

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.08	—	1.47	V	—
T	Temperature range	-40	—	125	°C	—
I_{DD_2M}	Supply current in 2 MHz mode	—	14	17	μA	—
I_{DD_8M}	Supply current in 8 MHz mode	—	30	35	μA	—
f_{IRC_2M}	Output frequency	—	2	—	MHz	—
f_{IRC_8M}	Output frequency	—	8	—	MHz	—
$f_{IRC_T_2M}$	Output frequency range (trimmed)	—	—	± 3	$\%f_{IRC}$	$V_{DD} \geq 1.89 V$
$f_{IRC_T_8M}$	Output frequency range (trimmed)	—	—	± 3	$\%f_{IRC}$	$V_{DD} \geq 1.89 V$
T_{su_2M}	Startup time	—	—	12.5	μs	—
T_{su_8M}	Startup time	—	—	12.5	μs	—

3.3.2 Oscillator electrical specifications

3.3.2.1 Oscillator DC electrical specifications

Table 22. Oscillator DC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.71	—	3.6	V	—
I_{DDOSC}	Supply current — low-power mode • 32 kHz	—	500	—	nA	1
C_x	EXTAL load capacitance	—	—	—		2, 3
C_y	XTAL load capacitance	—	—	—		2, 3
R_F	Feedback resistor — low-frequency, low-power mode	—	—	—	M Ω	2, 4
R_S	Series resistor — low-frequency, low-power mode	—	—	—	k Ω	—

Table continues on the next page...

Table 22. Oscillator DC electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{pp}^5	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, low-power mode	—	0.6	—	V	—

1. $V_{DD}=3.3$ V, Temperature =25 °C
2. See crystal or resonator manufacturer's recommendation
3. C_x, C_y can be provided by using either the integrated capacitors or by using external components.
4. When low power mode is selected, R_F is integrated and must not be attached externally.
5. The EXTAL and XTAL pins should only be connected to required oscillator components and must not be connected to any other devices.

3.3.2.2 Oscillator frequency specifications

Table 23. Oscillator frequency specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{osc_lo}	Oscillator crystal or resonator frequency — low frequency mode	32	—	40	kHz	—
t_{dc_extal}	Input clock duty cycle (external clock mode)	40	50	60	%	—
t_{cst}	Crystal startup time — 32 kHz low-frequency, low-power mode	—	750	—	ms	1, 2

1. Proper PC board layout procedures must be followed to achieve specifications.
2. Crystal startup time is defined as the time between the oscillator being enabled and the OSCINIT bit in the MCG_S register being set.

3.4 Memories and memory interfaces

3.4.1 Flash electrical specifications

This section describes the electrical characteristics of the flash memory module.

3.4.1.1 Flash timing specifications — program and erase

The following specifications represent the amount of time the internal charge pumps are active and do not include command overhead.

Table 24. NVM program/erase timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{hvpqm4}	Longword Program high-voltage time	—	7.5	18	μ s	—
$t_{hversscr}$	Sector Erase high-voltage time	—	13	113	ms	1
$t_{hversall}$	Erase All high-voltage time	—	52	452	ms	1

1. Maximum time based on expectations at cycling end-of-life.

3.4.1.2 Flash timing specifications — commands

Table 25. Flash command timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{rd1sec1k}$	Read 1s Section execution time (flash sector)	—	—	60	μ s	1
t_{pgmchk}	Program Check execution time	—	—	45	μ s	1
t_{rdsrc}	Read Resource execution time	—	—	30	μ s	1
t_{pgm4}	Program Longword execution time	—	65	145	μ s	—
t_{ersscr}	Erase Flash Sector execution time	—	14	114	ms	2
t_{rd1all}	Read 1s All Blocks execution time	—	—	0.5	ms	—
t_{rdonce}	Read Once execution time	—	—	25	μ s	1
$t_{pgmonce}$	Program Once execution time	—	65	—	μ s	—
t_{ersall}	Erase All Blocks execution time	—	61	500	ms	2
t_{vfykey}	Verify Backdoor Access Key execution time	—	—	30	μ s	1

1. Assumes 25 MHz flash clock frequency.
2. Maximum times for erase parameters based on expectations at cycling end-of-life.

3.4.1.3 Flash high voltage current behaviors

Table 26. Flash high voltage current behaviors

Symbol	Description	Min.	Typ.	Max.	Unit
I_{DD_PGM}	Average current adder during high voltage flash programming operation	—	2.5	6.0	mA
I_{DD_ERS}	Average current adder during high voltage flash erase operation	—	1.5	4.0	mA

3.4.1.4 Reliability specifications

Table 27. NVM reliability specifications

Symbol	Description	Min.	Typ. ¹	Max.	Unit	Notes
Program Flash						
$t_{nvmretp10k}$	Data retention after up to 10 K cycles	5	50	—	years	—
$t_{nvmretp1k}$	Data retention after up to 1 K cycles	20	100	—	years	—
$n_{nvmcycp}$	Cycling endurance	10 K	50 K	—	cycles	2

1. Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25 °C use profile. Engineering Bulletin EB618 does not apply to this technology. Typical endurance defined in Engineering Bulletin EB619.
2. Cycling endurance represents number of program/erase cycles at $-40\text{ °C} \leq T_j \leq 125\text{ °C}$.

Peripheral operating requirements and behaviors

- For packages without dedicated VREFH and VREFL pins, V_{REFH} is internally tied to V_{DDA} , and V_{REFL} is internally tied to V_{SSA} .
- This resistance is external to MCU. To achieve the best results, the analog source resistance must be kept as low as possible. The results in this data sheet were derived from a system that had $< 8 \Omega$ analog source resistance. The R_{AS}/C_{AS} time constant should be kept to < 1 ns.
- To use the maximum ADC conversion clock frequency, CFG2[ADHSC] must be set and CFG1[ADLPC] must be clear.
- For guidelines and examples of conversion rate calculation, download the [ADC calculator tool](#).

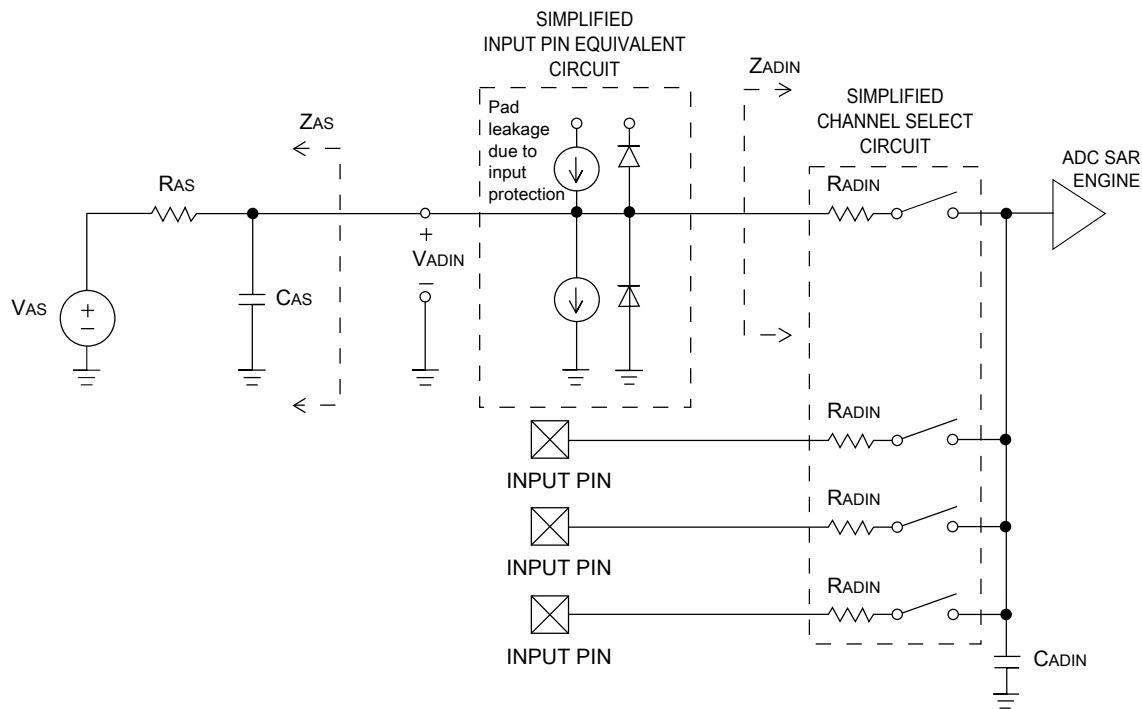


Figure 8. ADC input impedance equivalency diagram

3.6.1.2 12-bit ADC electrical characteristics

Table 29. 12-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$)

Symbol	Description	Conditions ¹	Min.	Typ. ²	Max.	Unit	Notes
I _{DDA_ADC}	Supply current		0.215	—	1.7	mA	3
f _{ADACK}	ADC asynchronous clock source	• ADLPC = 1, ADHSC = 0 • ADLPC = 1, ADHSC = 1 • ADLPC = 0, ADHSC = 0 • ADLPC = 0, ADHSC = 1	1.2 2.4 3.0 4.4	2.4 4.0 5.2 6.2	3.9 6.1 7.3 9.5	MHz MHz MHz MHz	t _{ADACK} = 1/f _{ADACK}
	Sample Time	See Reference Manual chapter for sample times					
TUE	Total unadjusted error	• 12-bit modes • <12-bit modes	— —	±6 ±3	— ±6	LSB ⁴	5

Table continues on the next page...

Table 29. 12-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$) (continued)

Symbol	Description	Conditions ¹	Min.	Typ. ²	Max.	Unit	Notes
DNL	Differential non-linearity	12-bit modes <12-bit modes	—	±0.9	–1.1 to +1.9	LSB ⁴	5
INL	Integral non-linearity	12-bit modes <12-bit modes	—	±1.5	–2.7 to +1.9	LSB ⁴	5
E _{FS}	Full-scale error	12-bit modes <12-bit modes	—	5	—	LSB ⁴	V _{ADIN} = V _{DDA} ⁵
E _Q	Quantization error	12-bit modes	—	—	±0.5	LSB ⁴	
E _{IL}	Input leakage error		I _{in} × R _{AS}			mV	I _{in} = leakage current (refer to the MCU's voltage and current operating ratings)
	Temp sensor slope	Across the full temperature range of the device	1.55	1.62	1.69	mV/°C	6
V _{TEMP25}	Temp sensor voltage	25 °C	706	716	726	mV	6

1. All accuracy numbers assume the ADC is calibrated with $V_{REFH} = V_{DDA}$
2. Typical values assume $V_{DDA} = 3.0$ V, Temp = 25 °C, $f_{ADCK} = 2.0$ MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
3. The ADC supply current depends on the ADC conversion clock speed, conversion rate and ADC_CFG1[ADLPC] (low power). For lowest power operation, ADC_CFG1[ADLPC] must be set, the ADC_CFG2[ADHSC] bit must be clear with 1 MHz ADC conversion clock speed.
4. 1 LSB = $(V_{REFH} - V_{REFL})/2^N$
5. ADC conversion clock < 16 MHz, Max hardware averaging (AVGE = %1, AVGS = %11)
6. ADC conversion clock < 3 MHz

Table 30. 12-bit ADC characteristics ($V_{REFH} = V_{REFO}$, $V_{REFL} = V_{SSA}$)

Symbol	Description	Conditions ¹	Min.	Typ. ²	Max.	Unit	Notes
I _{DDA_ADC}	Supply current		0.215	—	1.7	mA	3
f _{ADACK}	ADC asynchronous clock source	- ADLPC = 1, ADHSC = 0 - ADLPC = 1, ADHSC = 1 - ADLPC = 0, ADHSC = 0 - ADLPC = 0, ADHSC = 1	1.2	2.4	3.9	MHz	t _{ADACK} = 1/f _{ADACK}
			2.4	4.0	6.1	MHz	
			3.0	5.2	7.3	MHz	
			4.4	6.2	9.5	MHz	

Table continues on the next page...

3.8.1 SPI switching specifications

The Serial Peripheral Interface (SPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The following tables provide timing characteristics for classic SPI timing modes. See the SPI chapter of the chip's Reference Manual for information about the modified transfer formats used for communicating with slower peripheral devices.

All timing is shown with respect to 20% V_{DD} and 80% V_{DD} thresholds, unless noted, as well as input signal transitions of 3 ns and a 30 pF maximum load on all SPI pins.

Table 36. SPI master mode timing on slew rate disabled pads

Num.	Symbol	Description	Min.	Max.	Unit	Note
1	f_{op}	Frequency of operation	$f_{periph}/2048$	$f_{periph}/2$	Hz	1
2	t_{SPCK}	SPSCK period	$2 \times t_{periph}$	$2048 \times t_{periph}$	ns	2
3	t_{Lead}	Enable lead time	1/2	—	t_{SPCK}	—
4	t_{Lag}	Enable lag time	1/2	—	t_{SPCK}	—
5	t_{WSPCK}	Clock (SPSCK) high or low time	$t_{periph} - 30$	$1024 \times t_{periph}$	ns	—
6	t_{SU}	Data setup time (inputs)	22	—	ns	—
7	t_{HI}	Data hold time (inputs)	0	—	ns	—
8	t_v	Data valid (after SPSCK edge)	—	10	ns	—
9	t_{HO}	Data hold time (outputs)	0	—	ns	—
10	t_{RI}	Rise time input	—	$t_{periph} - 25$	ns	—
	t_{FI}	Fall time input				
11	t_{RO}	Rise time output	—	25	ns	—
	t_{FO}	Fall time output				

1. For SPI0, f_{periph} is the bus clock (f_{BUS}).

2. $t_{periph} = 1/f_{periph}$

Table 37. SPI master mode timing on slew rate enabled pads

Num.	Symbol	Description	Min.	Max.	Unit	Note
1	f_{op}	Frequency of operation	$f_{periph}/2048$	$f_{periph}/2$	Hz	1
2	t_{SPCK}	SPSCK period	$2 \times t_{periph}$	$2048 \times t_{periph}$	ns	2
3	t_{Lead}	Enable lead time	1/2	—	t_{SPCK}	—
4	t_{Lag}	Enable lag time	1/2	—	t_{SPCK}	—

Table continues on the next page...

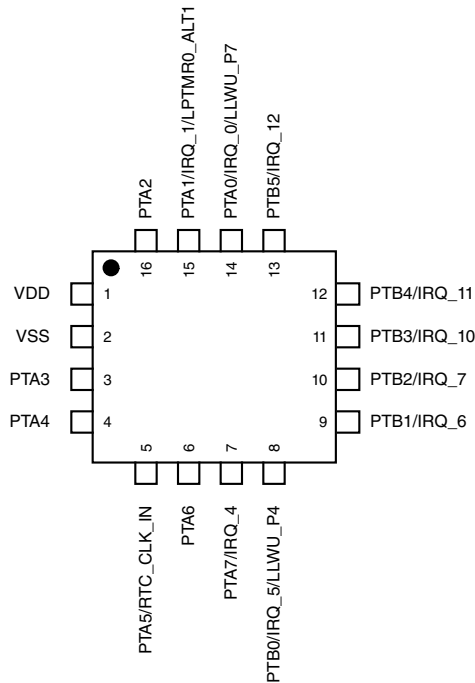


Figure 19. KL03 16-pin QFN pinout diagram

6 Ordering parts

6.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to freescale.com and perform a part number search for the following device numbers:

7 Part identification

7.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

8 Terminology and guidelines

8.1 Definition: Operating requirement

An *operating requirement* is a specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip.

8.1.1 Example

This is an example of an operating requirement:

Symbol	Description	Min.	Max.	Unit
V _{DD}	1.0 V core supply voltage	0.9	1.1	V

8.2 Definition: Operating behavior

Unless otherwise specified, an *operating behavior* is a specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions.

8.2.1 Example

This is an example of an operating behavior:

Symbol	Description	Min.	Max.	Unit
I _{WP}	Digital I/O weak pullup/pulldown current	10	130	μA

8.3 Definition: Attribute

An *attribute* is a specified value or range of values for a technical characteristic that are guaranteed, regardless of whether you meet the operating requirements.

8.3.1 Example

This is an example of an attribute:

Symbol	Description	Min.	Max.	Unit
CIN_D	Input capacitance: digital pins	—	7	pF

8.4 Definition: Rating

A *rating* is a minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure:

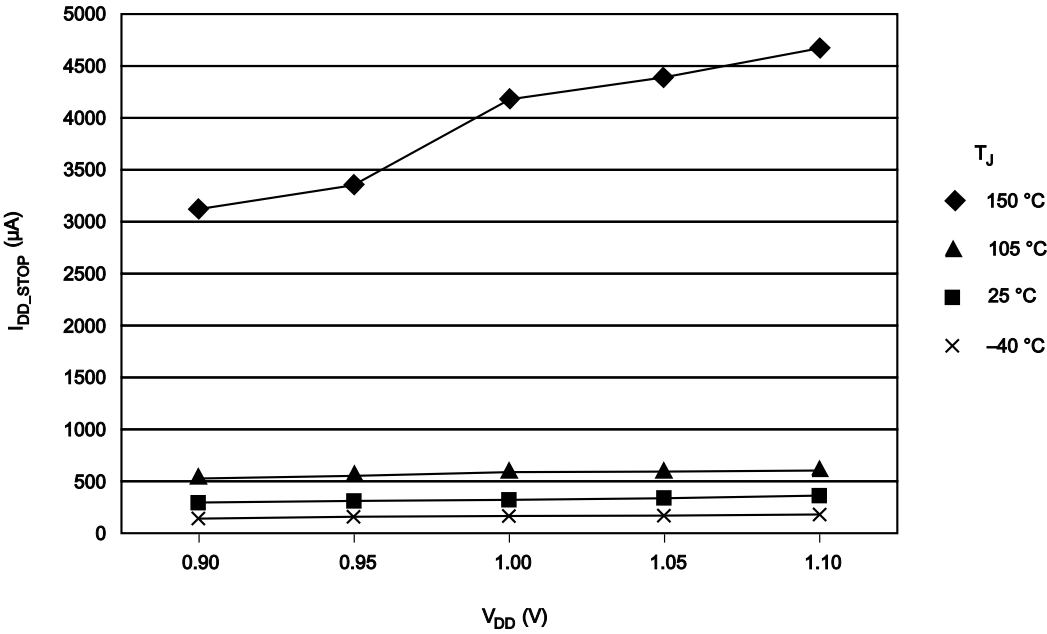
- *Operating ratings* apply during operation of the chip.
- *Handling ratings* apply when the chip is not powered.

8.4.1 Example

This is an example of an operating rating:

Symbol	Description	Min.	Max.	Unit
V _{DD}	1.0 V core supply voltage	−0.3	1.2	V

Revision history



8.9 Typical value conditions

Typical values assume you meet the following conditions (or other conditions as specified):

Table 42. Typical value conditions

Symbol	Description	Value	Unit
T _A	Ambient temperature	25	°C
V _{DD}	3.3 V supply voltage	3.3	V

9 Revision history

The following table provides a revision history for this document.

Table 43. Revision history

Rev. No.	Date	Substantial Changes
3.1	07/2014	Initial public release.
4	08/2014	Changed pinout signal names ADC0_SE5, ADC0_SE6, and ADC0_SE12 to ADC0_SE8, ADC0_SE9 and ADC0_SE15 respectively.