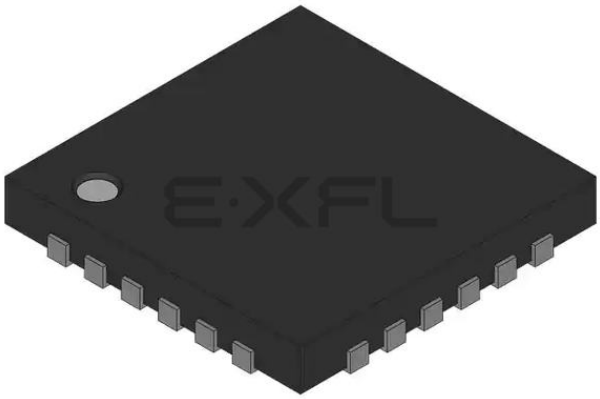

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Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LVD, POR, PWM, WDT
Number of I/O	22
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 7x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	24-UFQFN Exposed Pad
Supplier Device Package	24-QFN (4x4)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mkl03z8vfk4

Ordering Information[1]

Part Number	Memory		Maximum number of I\O's
	Flash (KB)	SRAM (KB)	
MKL03Z8VFG4(R)	8	2	14
MKL03Z16VFG4(R)	16	2	14
MKL03Z32VFG4(R)	32	2	14
MKL03Z32CAF4R	32	2	18
MKL03Z8VFK4(R)	8	2	22
MKL03Z16VFK4(R)	16	2	22
MKL03Z32VFK4(R)	32	2	22

1. To confirm current availability of ordererable part numbers, go to http://www.freescale.com and perform a part number search.

Related Resources

Type	Description	Resource
Selector Guide	The Freescale Solution Advisor is a web-based tool that features interactive application wizards and a dynamic product selector.	Solution Advisor
Product Brief	The Product Brief contains concise overview/summary information to enable quick evaluation of a device for design suitability.	KL03PB[1]
Reference Manual	The Reference Manual contains a comprehensive description of the structure and function (operation) of a device.	KL03P24M48SF0RM[1]
Data Sheet	The Data Sheet includes electrical characteristics and signal connections.	KL03P24M48SF0[1]
Chip Errata	The chip mask set Errata provides additional or corrective information for a particular device mask set.	KL03Z_1N86K[1]
Package drawing	Package dimensions are provided in package drawings.	QFN 16-pin: 98ASA00525D[1] QFN 24-pin: 98ASA00602D[1] WLCSP 20-pin: 98ASA00676D[1]

1. To find the associated resource, go to http://www.freescale.com and perform a search using this term.

Figure 1 shows the functional modules in the chip.

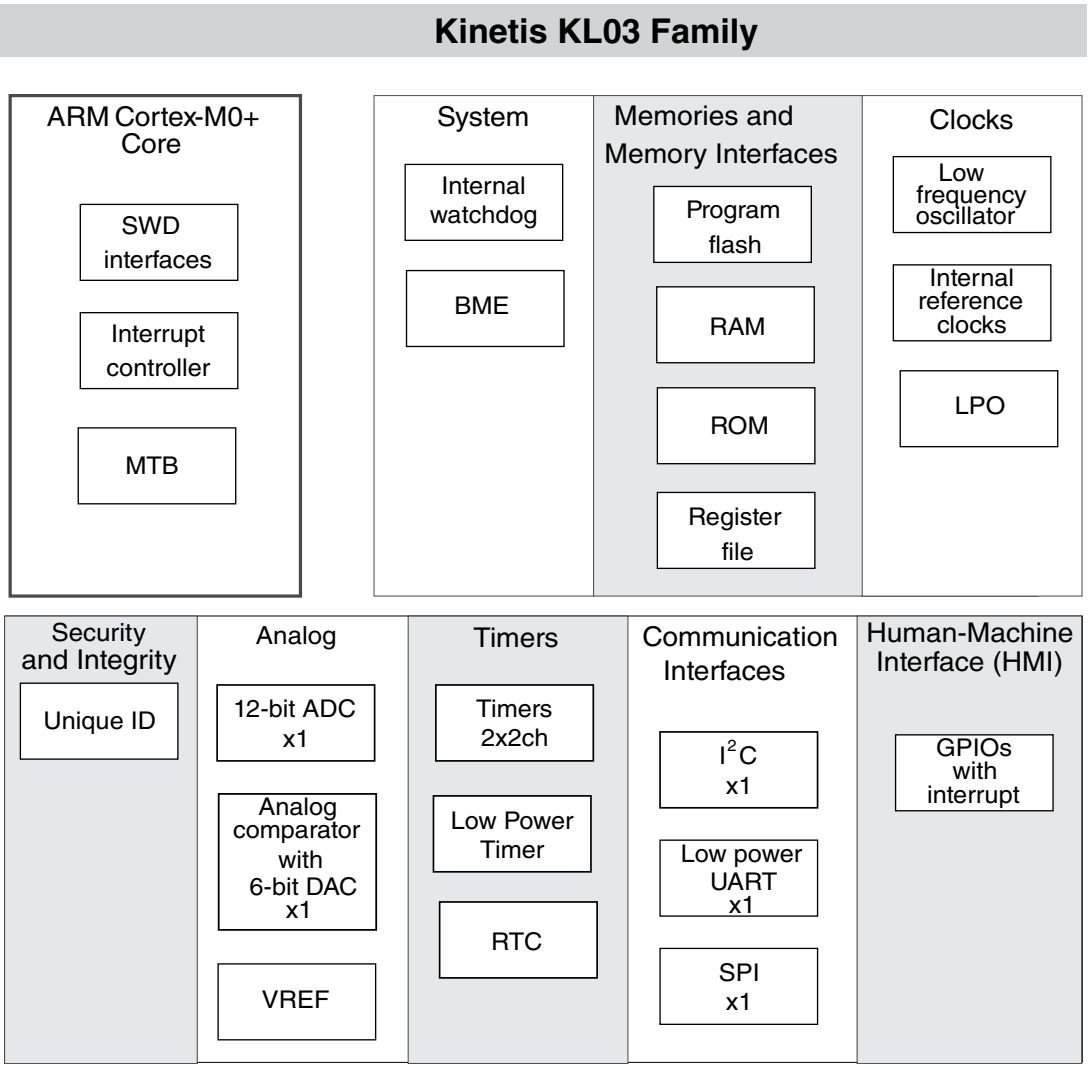

Figure 1. Functional block diagram

Table 7. Voltage and current operating behaviors (continued)

Symbol	Description	Min.	Max.	Unit	Notes
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OL} = 20 mA	—	0.5	V	
	• 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OL} = 10 mA	—	0.5	V	
I_{OLT}	Output low current total for all ports	—	100	mA	—
I_{IN}	Input leakage current (per pin) for full temperature range	—	1	µA	3
I_{IN}	Input leakage current (per pin) at 25 °C	—	0.025	µA	3
I_{IN}	Input leakage current (total all pins) for full temperature range	—	41	µA	3
I_{OZ}	Hi-Z (off-state) leakage current (per pin)	—	1	µA	—
R_{PU}	Internal pullup resistors	20	50	kΩ	4

1. I/O have both high drive and normal drive capability selected by the associated PTx_PCRn[DSE] control bit. All other GPIOs are normal drive only.
2. The reset pin only contains an active pull down device when configured as the RESET signal or as a GPIO. When configured as a GPIO output, it acts as a pseudo open drain output.
3. Measured at V_{DD} = 3.6 V
4. Measured at V_{DD} supply voltage = V_{DD} min and Vinput = V_{SS}

2.2.4 Power mode transition operating behaviors

All specifications except t_{POR} and VLLSx→RUN recovery times in the following table assume this clock configuration:

- CPU and system clocks = 48 MHz
- Bus and flash clock = 24 MHz
- HIRC clock mode

VLLSx→RUN recovery uses LIRC clock mode at the default CPU and system frequency of 8 MHz, and a bus and flash clock frequency of 4 MHz.

Table 8. Power mode transition operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Note
t_{POR}	After a POR event, amount of time from the point V_{DD} reaches 1.8 V to execution of the first instruction across the operating temperature range of the chip.	—	—	300	µs	1
	• VLLS0 → RUN	—	152	166	µs	—
	• VLLS1 → RUN	—	152	166	µs	—

Table continues on the next page...

Table 9. KL03 QFN packages power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.[1]	Unit	Notes
I_{DD_RUN}	Run mode current—48M HIRC mode, running CoreMark in Flash all peripheral clock enable 48 MHz core/24 MHz flash, V_{DD} = 3.0 V • at 25 °C • at 105 °C	 — —	 6.43 6.56	 6.69 6.82	 mA	3
I_{DD_RUN}	Run mode current—48M HIRC mode, running While(1) loop in flash all peripheral clock disable, 48 MHz core/24 MHz flash, V_{DD} = 3.0 V • at 25 °C • at 105 °C	 — —	 5.71 5.82	 5.94 6.05	 mA	—
I_{DD_RUN}	Run mode current—48M HIRC mode, running While(1) loop in Flash all peripheral clock disable, 24 MHz core/12 MHz flash, V_{DD} = 3.0 V • at 25 °C • at 105 °C	 — —	 3.3 3.4	 3.43 3.54	 mA	—
I_{DD_RUN}	Run mode current—48M HIRC mode, Running While(1) loop in Flash all peripheral clock disable, 12 MHz core/6 MHz flash, V_{DD} = 3.0 V • at 25 °C • at 105 °C	 — —	 2.28 2.38	 2.37 2.48	 mA	—
I_{DD_RUN}	Run mode current—48M HIRC mode, Running While(1) loop in Flash all peripheral clock enable, 48 MHz core/24 MHz flash, V_{DD} = 3.0 V • at 25 °C • at 105 °C	 — —	 6.1 6.22	 6.34 6.47	 mA	—
I_{DD_RUN}	Run mode current—48M HIRC mode, running While(1) loop in SRAM all peripheral clock disable, 48 MHz core/24 MHz flash, V_{DD} = 3.0 V • at 25 °C • at 105 °C	 — —	 3.14 3.27	 3.23 3.36	 mA	—
I_{DD_RUN}	Run mode current—48M HIRC mode, running While(1) loop in SRAM all peripheral clock enable, 48 MHz core/24 MHz flash, V_{DD} = 3.0 V • at 25 °C • at 105 °C	 — —	 3.54 3.67	 3.63 3.76	 mA	—
I_{DD_VLPRCO}	Very-low-power run While(1) loop in flash in compute operation mode— 2 MHz LIRC mode, 2 MHz core/0.5 MHz flash, V_{DD} = 3.0 V • at 25 °C	 —	 500	 750	 µA	—
I_{DD_VLPRCO}	Very-low-power-run While(1) loop in SRAM in compute operation mode— 8 MHz LIRC mode, 4 MHz core / 1 MHz flash, V_{DD} = 3.0 V • at 25 °C	 —	 188	 217	 µA	—

Table continues on the next page...

Table 9. KL03 QFN packages power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.[1]	Unit	Notes
I_{DD_WAIT}	Wait mode current—core disabled, 24 MHz system/12 MHz bus, flash disabled (flash doze enabled), all peripheral clocks disabled, MCG_Lite under HIRC mode, V_{DD} = 3.0 V	—	1.02	1.24	mA	—
I_{DD_VLPW}	Very-low-power run wait current, core disabled, 4 MHz system/ 1 MHz bus and flash, all peripheral clocks disabled, V_{DD} = 3.0 V	—	121	181	µA	—
I_{DD_VLPW}	Very-low-power run wait current, core disabled, 2 MHz system/ 0.5 MHz bus and flash, all peripheral clocks disabled, V_{DD} = 3.0 V	—	59	97	µA	—
I_{DD_VLPW}	Very-low-power run wait current, core disabled, 125 kHz system/ 31.25 kHz bus and flash, all peripheral clocks disabled, V_{DD} = 3.0 V	—	28	42	µA	—
I_{DD_PSTOP2}	Partial Stop 2, core and system clock disabled, 12 MHz bus and flash, V_{DD} = 3.0 V	—	1.53	2.03	mA	—
I_{DD_PSTOP2}	Partial Stop 2, core and system clock disabled, flash doze enabled, 12 MHz bus, V_{DD} = 3.0 V	—	0.881	1.18	mA	—
I_{DD_STOP}	Stop mode current at 3.0 V • at 25 °C and below • at 50 °C • at 85 °C • at 105 °C	— — — —	158 164 187 219	175.7 179.48 199.54 236.43	µA	—
I_{DD_VLPS}	Very-low-power stop mode current at 3.0 V • at 25 °C and below • at 50 °C • at 85 °C • at 105 °C	— — — —	2.2 3.9 13.9 28.4	2.71 6.63 18.25 36.59	µA	—
I_{DD_VLPS}	Very-low-power stop mode current at 1.8 V • at 25 °C and below • at 50 °C • at 85 °C • at 105 °C	— — — —	2.2 3.8 13.2 27.8	2.674 6.44 17.37 35.54	µA	—
I_{DD_VLLS3}	Very-low-leakage stop mode 3 current, all peripheral disable, at 3.0 V • at 25 °C and below • at 50 °C • at 85 °C • at 105 °C	— — — —	1.08 1.4 3.45 7.02	1.17 1.52 3.96 8.19	µA	—

Table continues on the next page...

Table 9. KL03 QFN packages power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.[1]	Unit	Notes
I_{DD_VLLS3}	Very-low-leakage stop mode 3 current with RTC current, at 3.0 V • at 25 °C and below • at 50 °C • at 85 °C • at 105 °C	 — — — —	 1.47 1.82 3.93 7.6	 1.56 1.94 4.44 8.77	µA	—
I_{DD_VLLS3}	Very-low-leakage stop mode 3 current with RTC current, at 1.8 V • at 25 °C and below • at 50 °C • at 85 °C • at 105 °C	 — — — —	 1.33 1.65 3.56 6.92	 1.42 1.77 4.07 8.09	µA	—
I_{DD_VLLS1}	Very-low-leakage stop mode 1 current all peripheral disabled at 3.0 V • at 25 °C and below • at 50°C • at 85°C • at 105 °C	 — — — —	 566 788 2270 4980	 690 839 2600 5820	nA	—
I_{DD_VLLS1}	Very-low-leakage stop mode 1 current RTC enabled at 3.0 V • at 25 °C and below • at 50°C • at 85°C • at 105 °C	 — — — —	 969 1200 2740 5610	 1059 1251 3070 6450	nA	—
I_{DD_VLLS1}	Very-low-leakage stop mode 1 current RTC enabled at 1.8 V • at 25 °C and below • at 50°C • at 85°C • at 105 °C	 — — — —	 826 1040 2400 4910	 916 1091 2730 5750	nA	—
I_{DD_VLLS0}	Very-low-leakage stop mode 0 current all peripheral disabled (SMC_STOPCTRL[PORPO] = 0) at 3.0 V • at 25 °C and below • at 50 °C • at 85 °C • at 105 °C	 — — — —	 265 467 1920 4540	 373 512.9 2256 5395	nA	—

Table continues on the next page...

Table 10. KL03 WLCSP package power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.[1]	Unit	Notes
I_{DD_VLPRCO}	Very-low-power run While(1) loop in flash in compute operation mode— 2 MHz LIRC mode, 2 MHz core/0.5 MHz flash, V_{DD} = 3.0 V • at 25 °C	—	500	750	µA	—
I_{DD_VLPRCO}	Very-low-power-run While(1) loop in SRAM in compute operation mode— 8 MHz LIRC mode, 4 MHz core / 1 MHz flash, V_{DD} = 3.0 V • at 25 °C	—	188	217	µA	—
I_{DD_VLPRCO}	Very-low-power run While(1) loop in SRAM in compute operation mode:—2 MHz LIRC mode, 2 MHz core / 0.5 MHz flash, V_{DD} = 3.0 V • at 25 °C	—	82	123	µA	—
I_{DD_VLPR}	Very-low-power run mode current— 2 MHz LIRC mode, While(1) loop in flash all peripheral clock disable, 2 MHz core / 0.5 MHz flash, V_{DD} = 3.0 V • at 25 °C	—	503	754	µA	—
I_{DD_VLPR}	Very-low-power run mode current— 2 MHz LIRC mode, While(1) loop in flash all peripheral clock disable, 125 kHz core / 31.25 kHz flash, V_{DD} = 3.0 V • at 25 °C	—	60	90	µA	—
I_{DD_VLPR}	Very-low-power run mode current— 2 MHz LIRC mode, While(1) loop in flash all peripheral clock enable, 2 MHz core / 0.5 MHz flash, V_{DD} = 3.0 V • at 25 °C	—	516	774	µA	—
I_{DD_VLPR}	Very-low-power run mode current— 8 MHz LIRC mode, While(1) loop in SRAM in all peripheral clock disable, 4 MHz core / 1 MHz flash, V_{DD} = 3.0 V • at 25 °C	—	209	350	µA	—
I_{DD_VLPR}	Very-low-power run mode current— 8 MHz LIRC mode, While(1) loop in SRAM all peripheral clock enable, 4 MHz core / 1 MHz flash, V_{DD} = 3.0 V • at 25 °C	—	229	370	µA	—
I_{DD_VLPR}	Very-low-power run mode current—2 MHz LIRC mode, While(1) loop in SRAM in all peripheral clock disable, 2 MHz core / 0.5 MHz flash, V_{DD} = 3.0 V • at 25 °C	—	93	140	µA	—
I_{DD_VLPR}	Very-low-power run mode current—2 MHz LIRC mode, While(1) loop in SRAM all peripheral clock disable, 125 kHz core / 31.25 kHz flash, V_{DD} = 3.0 V • at 25 °C	—	31	81	µA	—
I_{DD_VLPR}	Very-low-power run mode current—2 MHz LIRC mode, While(1) loop in SRAM all					—

Table continues on the next page...

Table 10. KL03 WLCSP package power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.[1]	Unit	Notes
	• at 50 °C • at 85 °C	— —	3.45 3.96	3.96		
I_{DD_VLLS3}	Very-low-leakage stop mode 3 current with RTC current, at 3.0 V • at 25 °C and below • at 50 °C • at 85 °C	— — —	1.47 1.82 3.93	1.56 1.94 4.44	µA	—
I_{DD_VLLS3}	Very-low-leakage stop mode 3 current with RTC current, at 1.8 V • at 25 °C and below • at 50 °C • at 85 °C	— — —	1.33 1.65 3.56	1.42 1.77 4.07	µA	—
I_{DD_VLLS1}	Very-low-leakage stop mode 1 current all peripheral disabled at 3.0 V • at 25 °C and below • at 50°C • at 85°C	— — —	566 788 2270	690 839 2600	nA	—
I_{DD_VLLS1}	Very-low-leakage stop mode 1 current RTC enabled at 3.0 V • at 25 °C and below • at 50°C • at 85°C	— — —	969 1200 2740	1059 1251 3070	nA	—
I_{DD_VLLS1}	Very-low-leakage stop mode 1 current RTC enabled at 1.8 V • at 25 °C and below • at 50°C • at 85°C	— — —	826 1040 2400	916 1091 2730	nA	—
I_{DD_VLLS0}	Very-low-leakage stop mode 0 current all peripheral disabled (SMC_STOPCTRL[PORPO] = 0) at 3.0 V • at 25 °C and below • at 50 °C • at 85 °C	— — —	265 467 1920	373 512.9 2256	nA	—
I_{DD_VLLS0}	Very-low-leakage stop mode 0 current all peripheral disabled (SMC_STOPCTRL[PORPO] = 1) at 3 V • at 25 °C and below • at 50 °C • at 85 °C	— — —	77 255 1640	350 465.70 1994	nA	4

1. The maximum values represent characterized results equivalent to the mean plus three times the standard deviation (mean + 3 sigma).
2. The analog supply current is the sum of the active or disabled current for each of the analog modules on the device. See each module's specification for its supply current.
3. MCG_Lite configured for HIRC mode. CoreMark benchmark compiled using IAR 7.10 with optimization level high, optimized for balanced.
4. No brownout

Table 11. Low power mode peripheral adders — typical value

Symbol	Description	Temperature (°C)						Unit
		-40	25	50	70	85	105[1]	
$I_{LIRC8MHz}$	8 MHz internal reference clock (LIRC) adder. Measured by entering STOP or VLPS mode with 8 MHz LIRC enabled, MCG_SC[FCRDIV]=000b, MCG_MC[LIRC_DIV2]=000b.	68	68	68	68	68	68	µA
$I_{LIRC2MHz}$	2 MHz internal reference clock (LIRC) adder. Measured by entering STOP mode with the 2 MHz LIRC enabled, MCG_SC[FCRDIV]=000b, MCG_MC[LIRC_DIV2]=000b.	27	27	27	27	27	27	µA
$I_{EREFSTEN32KHz}$	External 32 kHz crystal clock adder by means of the OSC0_CR[EREFSTEN and EREFSTEN] bits. Measured by entering all modes with the crystal enabled. • VLLS1 • VLLS3 • VLPS • STOP	 340 340 340 340	 410 410 420 420	 460 460 480 480	 470 490 570 570	 480 530 610 610	 600 600 850 850	nA
I_{LPTMR}	LPTMR peripheral adder measured by placing the device in VLLS1 mode with LPTMR enabled using LPO.	30	30	30	85	100	200	nA
I_{CMP}	CMP peripheral adder measured by placing the device in VLLS1 mode with CMP enabled using the 6-bit DAC and a single external input for compare. Includes 6-bit DAC power consumption.	15	15	15	15	15	15	µA
I_{RTC}	RTC peripheral adder measured by placing the device in VLLS1 mode with external 32 kHz crystal enabled by means of the RTC_CR[OSCE] bit and the RTC ALARM set for 1 minute. Includes ERCLK32K (32 kHz external crystal) power consumption.	340	440	440	480	520	620	nA
I_{UART}	UART peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source waiting for RX data at 115200 baud rate.							

Table continues on the next page...

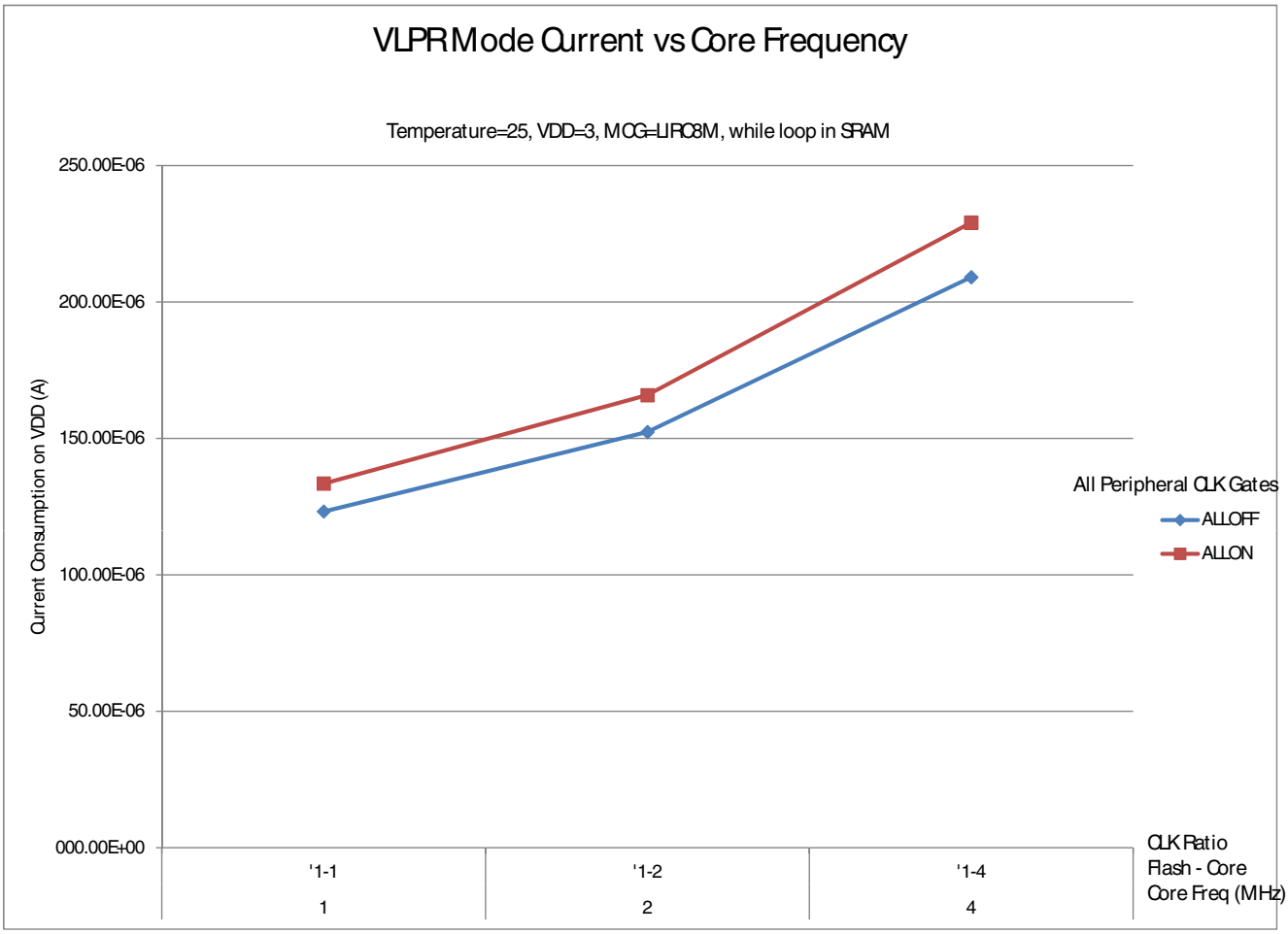

Figure 5. VLPR mode current vs. core frequency (loop in SRAM)

2.2.6 EMC radiated emissions operating behaviors

Table 12. EMC radiated emissions operating behaviors for 24-pin QFN package

Symbol	Description	Frequency band (MHz)	Typ.	Unit	Notes
V_{RE1}	Radiated emissions voltage, band 1	0.15–50	5	dBµV	1, 2
V_{RE2}	Radiated emissions voltage, band 2	50–150	7	dBµV	
V_{RE3}	Radiated emissions voltage, band 3	150–500	5	dBµV	
V_{RE4}	Radiated emissions voltage, band 4	500–1000	5	dBµV	
V_{RE_IEC}	IEC/SAE level	0.15–1000	N	—	2, 3

1. Determined according to IEC 61967-2 (and SAE J1752/3) radiated radio frequency (RF) emissions measurement standard. Typical Configuration: Appendix B: DUT Software Configuration—2. Typical Configuration.
2. V_{DD} = 3.3 V, T_A = 25 °C, f_{irc48m} = 48 MHz, f_{SYS} = 48 MHz, f_{BUS} = 24 MHz

2.4.2 Thermal attributes

Table 18. Thermal attributes

Board type	Symbol	Description	16 QFN	20 WLCSP	24 QFN	Unit	Notes
Single-layer (1S)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	64.2	69.8	60.7	°C/W	1,2
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	53.3	57.5	48.5	°C/W	1,2,3
Single-layer (1S)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	55.4	62.03	51.0	°C/W	1,3
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	48.9	54.3	43.6	°C/W	1,3
—	$R_{\theta JB}$	Thermal resistance, junction to board	33.5	51.64	30.4	°C/W	4
—	$R_{\theta JC}$	Thermal resistance, junction to case	20.9	0.73	9.8	°C/W	5
—	Ψ_{JT}	Thermal characterization parameter, junction to package top outside center (natural convection)	0.2	0.2	0.2	°C/W	6
—	Ψ_{JB}	Thermal characterization parameter, junction to package bottom outside center (natural convection)	22.4	–	21.8	°C/W	7

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.
7. Thermal characterization parameter indicating the temperature difference between package bottom center and the junction temperature per JEDEC JESD51-12. When Greek letters are not available, the thermal characterization parameter is written as Psi-JB.

3 Peripheral operating requirements and behaviors

3.1 Core modules

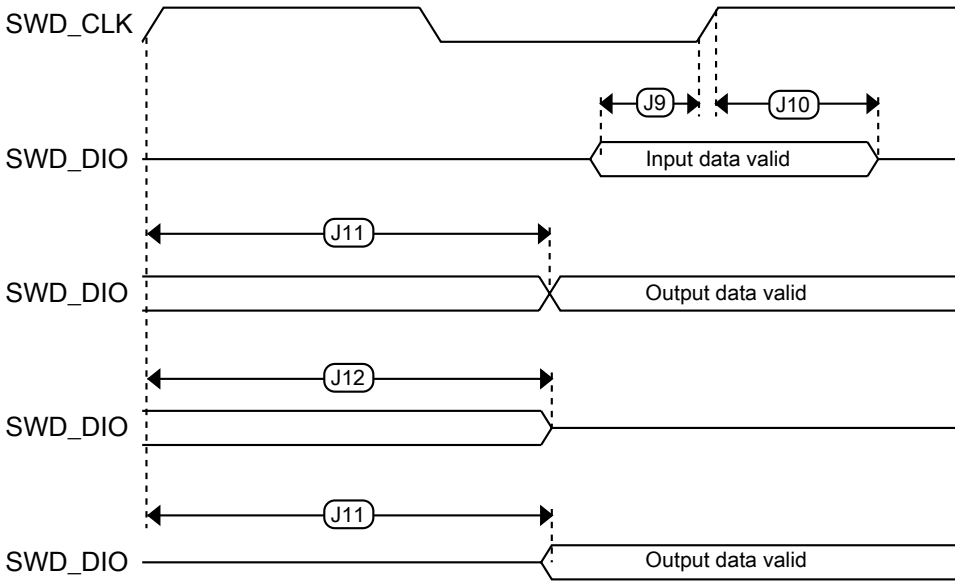

Figure 7. Serial wire data timing

3.2 System modules

There are no specifications necessary for the device's system modules.

3.3 Clock modules

3.3.1 MCG-Lite specifications

Table 20. HIRC48M specification

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.71	—	3.6	V	—
I_{DD48M}	Supply current	—	400	500	µA	—
f_{irc48m}	Internal reference frequency	—	48	—	MHz	—
$\Delta f_{irc48m\_ol\_lv}$	total deviation of IRC48M frequency at low voltage (VDD=1.71V-1.89V) over temperature	—	± 0.5	±1.5	$\%f_{irc48m}$	—

Table continues on the next page...

Table 20. HIRC48M specification (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$\Delta f_{irc48m\_ol\_hv}$	total deviation of IRC48M frequency at high voltage (VDD=1.89V-3.6V) over temperature	—	± 0.5	±1.0	$\%f_{irc48m}$	—
J_{cyc_irc48m}	Period Jitter (RMS)	—	35	150	ps	—
$t_{irc48mst}$	Startup time	—	2	3	µs	1

1. IRC48M startup time is defined as the time between clock enablement and clock availability for system use. Enable the clock by setting MCG_MC[HIRCEN] = 1. See reference manual for details.

Table 21. LIRC8M/2M specification

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.08	—	1.47	V	—
T	Temperature range	-40	—	125	°C	—
I_{DD_2M}	Supply current in 2 MHz mode	—	14	17	µA	—
I_{DD_8M}	Supply current in 8 MHz mode	—	30	35	µA	—
f_{IRC_2M}	Output frequency	—	2	—	MHz	—
f_{IRC_8M}	Output frequency	—	8	—	MHz	—
$f_{IRC\_T\_2M}$	Output frequency range (trimmed)	—	—	±3	$\%f_{IRC}$	V_{DD}≥1.89 V
$f_{IRC\_T\_8M}$	Output frequency range (trimmed)	—	—	±3	$\%f_{IRC}$	V_{DD}≥1.89 V
T_{su_2M}	Startup time	—	—	12.5	µs	—
T_{su_8M}	Startup time	—	—	12.5	µs	—

3.3.2 Oscillator electrical specifications

3.3.2.1 Oscillator DC electrical specifications

Table 22. Oscillator DC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.71	—	3.6	V	—
I_{DDOSC}	Supply current — low-power mode • 32 kHz	—	500	—	nA	1
C_x	EXTAL load capacitance	—	—	—		2, 3
C_y	XTAL load capacitance	—	—	—		2, 3
R_F	Feedback resistor — low-frequency, low-power mode	—	—	—	MΩ	2, 4
R_S	Series resistor — low-frequency, low-power mode	—	—	—	kΩ	—

Table continues on the next page...

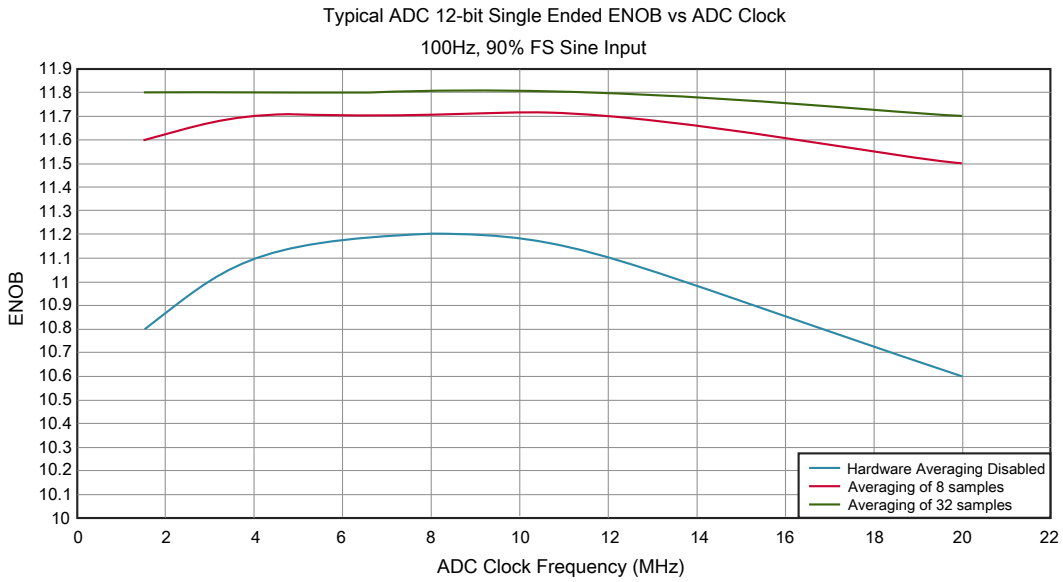

Figure 9. Typical ENOB vs. ADC_CLK for 12-bit single-ended mode

3.6.2 CMP and 6-bit DAC electrical specifications

Table 31. Comparator and 6-bit DAC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage	1.71	—	3.6	V
I_{DDHS}	Supply current, High-speed mode (EN=1, PMODE=1)	—	—	200	µA
I_{DDLS}	Supply current, low-speed mode (EN=1, PMODE=0)	—	—	20	µA
V_{AIN}	Analog input voltage	V_{SS} – 0.3	—	V_{DD}	V
V_{AIO}	Analog input offset voltage	—	—	20	mV
V_H	Analog comparator hysteresis[1]				
	• CR0[HYSTCTR] = 00	—	5	—	mV
	• CR0[HYSTCTR] = 01	—	10	—	mV
	• CR0[HYSTCTR] = 10	—	20	—	mV
	• CR0[HYSTCTR] = 11	—	30	—	mV
V_{CMPOh}	Output high	V_{DD} – 0.5	—	—	V
V_{CMPOl}	Output low	—	—	0.5	V
t_{DHS}	Propagation delay, high-speed mode (EN=1, PMODE=1)	20	50	200	ns
t_{DLS}	Propagation delay, low-speed mode (EN=1, PMODE=0)	80	250	600	ns
	Analog comparator initialization delay[2]	—	—	40	µs

Table continues on the next page...

Table 33. VREF full-range operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{out}	Voltage reference output with factory trim at nominal V_{DDA} and temperature=25C	1.1915	1.195	1.1977	V	1
V_{out}	Voltage reference output — factory trim	1.1584	—	1.2376	V	1
V_{out}	Voltage reference output — user trim	1.193	—	1.197	V	1
V_{step}	Voltage reference trim step	—	0.5	—	mV	1
V_{tdrift}	Temperature drift (Vmax -Vmin across the full temperature range: 0 to 70°C)	—	—	50	mV	1
Ac	Aging coefficient	—	—	400	uV/yr	—
I_{bg}	Bandgap only current	—	—	80	µA	1
I_{lp}	Low-power buffer current	—	—	360	uA	1
I_{hp}	High-power buffer current	—	—	1	mA	1
ΔV_{LOAD}	Load regulation • current = ± 1.0 mA	—	200	—	µV	1, 2
T_{stup}	Buffer startup time	—	—	100	µs	—
V_{vdrift}	Voltage drift (Vmax -Vmin across the full voltage range)	—	2	—	mV	1

1. See the chip's Reference Manual for the appropriate settings of the VREF Status and Control register.
2. Load regulation voltage is the difference between the VREF_OUT voltage with no load vs. voltage with defined load

Table 34. VREF limited-range operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
T_A	Temperature	0	50	°C	—

Table 35. VREF limited-range operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
V_{out}	Voltage reference output with factory trim	1.173	1.225	V	—

3.7 Timers

See General switching specifications.

3.8 Communication interfaces

3.8.1 SPI switching specifications

The Serial Peripheral Interface (SPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The following tables provide timing characteristics for classic SPI timing modes. See the SPI chapter of the chip's Reference Manual for information about the modified transfer formats used for communicating with slower peripheral devices.

All timing is shown with respect to 20% V_{DD} and 80% V_{DD} thresholds, unless noted, as well as input signal transitions of 3 ns and a 30 pF maximum load on all SPI pins.

Table 36. SPI master mode timing on slew rate disabled pads

Num.	Symbol	Description	Min.	Max.	Unit	Note
1	f_{op}	Frequency of operation	$f_{periph}/2048$	$f_{periph}/2$	Hz	1
2	t_{SPSCK}	SPSCK period	2 x t_{periph}	2048 x t_{periph}	ns	2
3	t_{Lead}	Enable lead time	1/2	—	t_{SPSCK}	—
4	t_{Lag}	Enable lag time	1/2	—	t_{SPSCK}	—
5	t_{WSPSCK}	Clock (SPSCK) high or low time	t_{periph} – 30	1024 x t_{periph}	ns	—
6	t_{SU}	Data setup time (inputs)	22	—	ns	—
7	t_{HI}	Data hold time (inputs)	0	—	ns	—
8	t_{v}	Data valid (after SPSCK edge)	—	10	ns	—
9	t_{HO}	Data hold time (outputs)	0	—	ns	—
10	t_{RI}	Rise time input	—	t_{periph} – 25	ns	—
	t_{FI}	Fall time input				
11	t_{RO}	Rise time output	—	25	ns	—
	t_{FO}	Fall time output				

1. For SPI0, f_{periph} is the bus clock (f_{BUS}).
2. $t_{periph} = 1/f_{periph}$

Table 37. SPI master mode timing on slew rate enabled pads

Num.	Symbol	Description	Min.	Max.	Unit	Note
1	f_{op}	Frequency of operation	$f_{periph}/2048$	$f_{periph}/2$	Hz	1
2	t_{SPSCK}	SPSCK period	2 x t_{periph}	2048 x t_{periph}	ns	2
3	t_{Lead}	Enable lead time	1/2	—	t_{SPSCK}	—
4	t_{Lag}	Enable lag time	1/2	—	t_{SPSCK}	—

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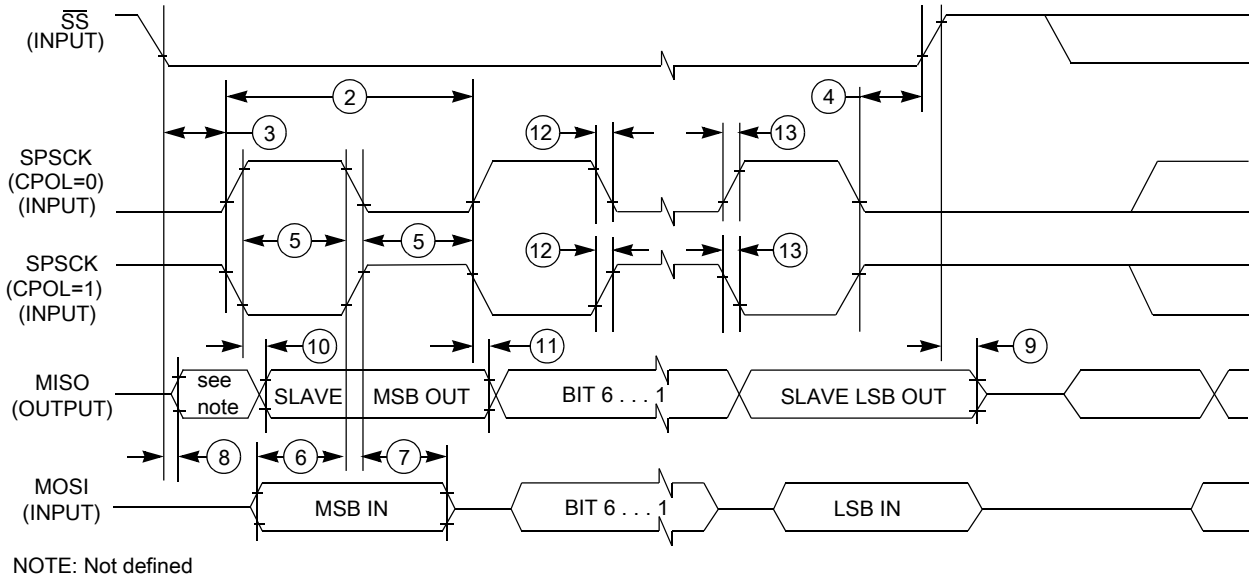

Figure 15. SPI slave mode timing (CPHA = 1)

3.8.2 Inter-Integrated Circuit Interface (I2C) timing

Table 40. I2C timing

Characteristic	Symbol	Standard Mode		Fast Mode[1]		Unit
		Minimum	Maximum	Minimum	Maximum	
SCL Clock Frequency	f_{SCL}	0	100	0	400[2]	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated.	t_{HD}; STA	4	—	0.6	—	µs
LOW period of the SCL clock	t_{LOW}	4.7	—	1.3	—	µs
HIGH period of the SCL clock	t_{HIGH}	4	—	0.6	—	µs
Set-up time for a repeated START condition	t_{SU}; STA	4.7	—	0.6	—	µs
Data hold time for I²C bus devices	t_{HD}; DAT	0[3]	3.45[4]	0[5]	0.9[3]	µs
Data set-up time	t_{SU}; DAT	250[6]	—	100[4, 7]	—	ns
Rise time of SDA and SCL signals	t_r	—	1000	20 +0.1C_b[8]	300	ns
Fall time of SDA and SCL signals	t_f	—	300	20 +0.1C_b[7]	300	ns
Set-up time for STOP condition	t_{SU}; STO	4	—	0.6	—	µs
Bus free time between STOP and START condition	t_{BUF}	4.7	—	1.3	—	µs
Pulse width of spikes that must be suppressed by the input filter	t_{SP}	N/A	N/A	0	50	ns

1. Fast mode is fully supported on all pins at VDD > 2.7 V. If VDD < 2.7 V, only pins that support high drive strength can support fast mode with maximum bus loading.

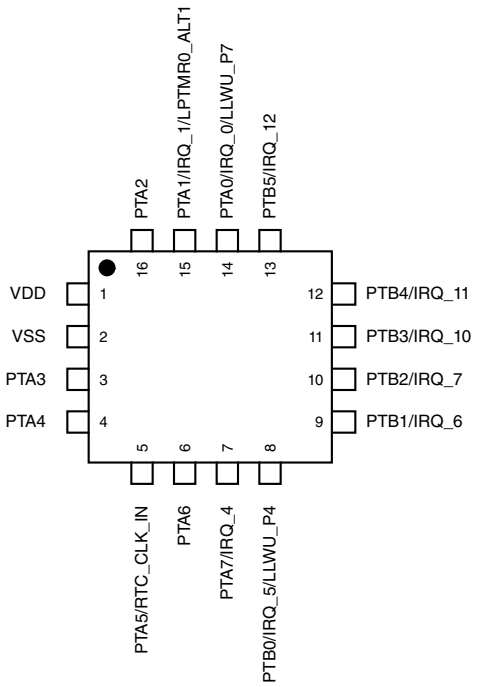

Figure 19. KL03 16-pin QFN pinout diagram

6 Ordering parts

6.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to **freescale.com** and perform a part number search for the following device numbers:

7 Part identification

7.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

8 Terminology and guidelines

8.1 Definition: Operating requirement

An *operating requirement* is a specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip.

8.1.1 Example

This is an example of an operating requirement:

Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	0.9	1.1	V

8.2 Definition: Operating behavior

Unless otherwise specified, an *operating behavior* is a specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions.

8.2.1 Example

This is an example of an operating behavior:

Symbol	Description	Min.	Max.	Unit
I_{WP}	Digital I/O weak pullup/ pulldown current	10	130	µA

8.3 Definition: Attribute

An *attribute* is a specified value or range of values for a technical characteristic that are guaranteed, regardless of whether you meet the operating requirements.

8.3.1 Example

This is an example of an attribute:

Symbol	Description	Min.	Max.	Unit
CIN_D	Input capacitance: digital pins	—	7	pF

8.4 Definition: Rating

A *rating* is a minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure:

- *Operating ratings* apply during operation of the chip.
- *Handling ratings* apply when the chip is not powered.

8.4.1 Example

This is an example of an operating rating:

Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	–0.3	1.2	V