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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	68000
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	25MHz
Co-Processors/DSP	-
RAM Controllers	-
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	5.0V
Operating Temperature	-55°C ~ 125°C (TC)
Security Features	-
Package / Case	196-BCQFP
Supplier Device Package	196-CQFP (34x34)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/ts68040mf25a

CQFP 196

Figure 3. Pin Assignments

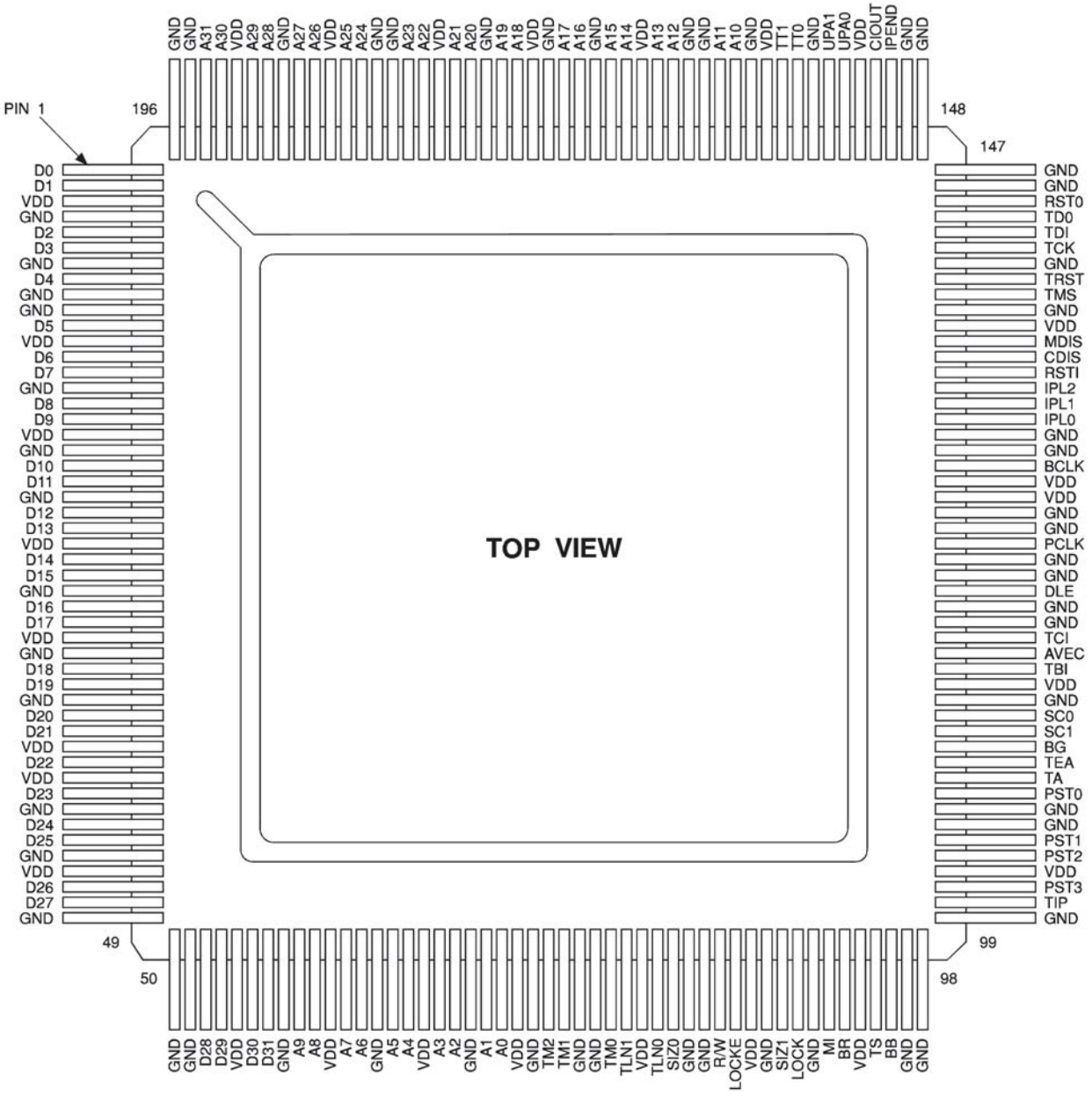


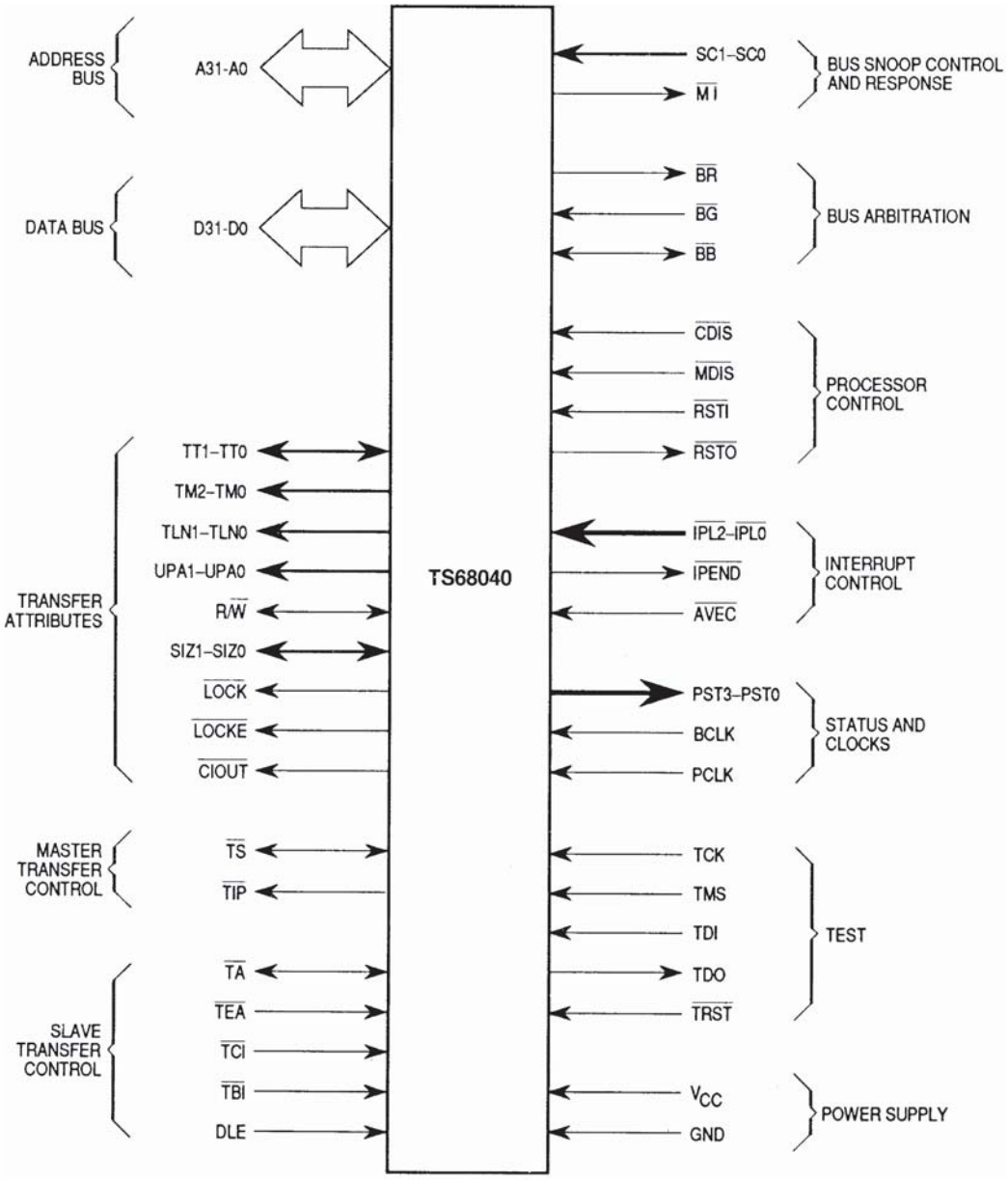
Table 2. Power Supply Affectation to CQFP Body

	GND	**V_{CC}**
PLL		127
Internal Logic	4, 9, 10, 19, 32, 45, 73, 88, 113, 119, 121, 122, 124, 125, 129, 130, 141, 159, 172	3, 18, 31, 40, 46, 60, 72, 87, 114, 126, 137, 158, 173, 186
Output Drivers	7, 15, 22, 28, 35, 42, 49, 50, 51, 57, 63, 69, 76, 77, 83, 84, 91, 97, 98, 99, 105, 106, 146, 147, 148, 149, 155, 162, 163, 169, 176, 182, 183, 189, 195, 196	12, 25, 38, 54, 66, 80, 94, 102, 152, 166, 179, 192

Signal Description

Figure 4 and Table 3 describe the signals on the TS68040 and indicate signal functions. The test signals, $\overline{TRST}$, TMS, TCK, TDI, and TDO, comply with subset P-1149.1 of the IEEE testability bus standard.

Figure 4. Functional Signal Groups



The precise case outlines are described at the end of the specification (See “Package Mechanical Data” on page 43.) and into MIL-STD-1835.

Electrical Characteristics

Absolute Maximum Ratings Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

Table 4. Absolute Maximum Ratings

Symbol	Parameter	Condition	Min	Max	Unit
V_{CC}	Supply Voltage Range		-0.3	7.0	V
V_I	Input Voltage Range		-0.3	7.0	V
P_D	Power Dissipation	Large buffers enabled		7.7	W
		Small buffers enabled		6.3	W
T_C	Operating Temperature		-55	T_J	°C
T_{stg}	Storage Temperature Range		-65	+150	°C
T_J	Junction Temperature(1)			+125	°C
T_{lead}	Lead Temperature	Max.10 sec soldering		+300	°C

Note: 1. This device is not tested at TC = +125°C. Testing is performed by setting the junction temperature Tj = +125°C and allowing the case and ambient temperatures to rise and fall as necessary so as not to exceed the maximum junction temperature.

Table 5. Recommended Conditions of Use
Unless otherwise stated, all voltages are referenced to the reference terminal

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage Range		+4.75		+5.25	V
V_{IL}	Logic Low Level Input Voltage Range		GND - 0.3		0.8	V
V_{IH}	Logic High Level Input Voltage Range		+2.0		V_{CC} + 0.3	V
V_{OH}	High Level Output Voltage		2.4			V
V_{OL}	Low Level Output Voltage				0.5	V
f_c	Clock Frequency	-25 MHz Version		25		MHz
		-33 MHz Version		33		MHz
T_C	Case Operating Temperature Range(1)		-55		T_{Jmax}	°C
T_J	Maximum Operating Junction Temperature				+125	°C

Note: 1. This device is not tested at TC = +125°C. Testing is performed by setting the junction temperature T_J = +125°C and allowing the case and ambient temperatures to rise and fall as necessary so as not to exceed the maximum junction temperature.

To calculate the specific power dissipation of a specific design, the termination method of each signal must be considered. For example, a signal output that is not connected would not dissipate any additional power if it were configured in the large buffer rather than the small buffer mode.

Relationships Between Thermal Resistances and Temperatures

Since the maximum operating junction temperature has been specified to be 125°C. The maximum case temperature, TC, in °C can be obtained from:

$$T_C = T_J - P_D \cdot \Phi_{JC} \quad (2)$$

where:

T_C = Maximum case temperature

T_J = Maximum junction temperature

P_D = Maximum power dissipation of the device

Φ_{JC} = Thermal resistance between the junction of the die and the case

In general, the ambient temperature, T_A, in °C is a function of the following formula:

$$T_A = T_J - P_D \cdot \Phi_{JC} - P_D \cdot \Phi_{CA} \quad (3)$$

Where the thermal resistance from case to ambient, Φ_{CA}, is the only user-dependent parameter once a buffer output configuration has been determined. As seen from equation (3), reducing the case to ambient thermal resistance increases the maximum operating ambient temperature. Therefore, by utilizing such methods as heat sinks and ambient air cooling to minimize the Φ_{CA}, a higher ambient operating temperature and/or a lower junction temperature can be achieved.

However, an easier approach to thermal evaluation uses the following formulas:

$$T_A = T_J - P_D \cdot \Phi_{JA} \quad (4)$$

or alternatively,

$$T_J = T_A - P_D \cdot \Phi_{JA} \quad (5)$$

where:

Φ_{JA} = thermal resistance from the junction to the ambient ($\Phi_{JC} + \Phi_{CA}$).

This total thermal resistance of a package, Φ_{JA}, is a combination of its two components, Φ_{JC} and Φ_{CA}. These components represent the barrier to heat flow from the semiconductor junction to the package (case) surface (Φ_{JC}) and from the case to the outside ambient (Φ_{JC}). Although Φ_{JC} is device related and cannot be influenced by the user, Φ_{CA} is user dependent. Thus, good thermal management by the user can significantly reduce Φ_{CA} achieving either a lower semiconductor junction temperature or a higher ambient operating temperature.

Thermal Management Techniques

To attain a reasonable maximum ambient operating temperature, a user must reduce the barrier to heat flow from the semiconductor junction to the outside ambient (Φ_{JA}). The only way to accomplish this is to significantly reduce Φ_{CA} by applying such thermal management techniques as heat sinks and ambient air cooling.

The following paragraphs discuss some results of a thermal study of the TS68040 device without using any thermal management techniques; using only air-flow cooling, using only a heat sink, and using heat sink combined with air-flow cooling.

Thermal Characteristics in Still Air

A sample size of three TS68040 packages was tested in free-air cooling with no heat sink. Measurements showed that the average Φ_{JA} was 22.8°C/W with a standard deviation of 0.44°C/W. The test was performed with 3W of power being dissipated from within the package. The test determined that Φ_{JA} will decrease slightly for the increasing power dissipation range possible. Therefore, since the variance in Φ_{JA} within the possible power dissipation range is negligible, it can be assumed for calculation purposes that Φ_{JA} is valid at all power levels. Using the formulas introduced previously, Table 7 shows the results of a maximum power dissipation of 3 and 5W with no heat sink or air-flow (refer to Table 6 to calculate other power dissipation values).

Table 7. Thermal Parameters With No Heat Sink or Air-flow

Defined Parameters			Measured	Calculated		
P_D	T_J	Φ_{JC}	Φ_{JA}	$\Phi_{CA} = \Phi_{JA} - \Phi_{JC}$	$T_C = T_J - P_D * \Phi_{JC}$	$T_A = T_J - P_D * \Phi_{JA}$
3 Watts	125°C	1°C/W	21.8°C/W	20.8°C/W	122°C	59.6°C
5 Watts	125°C	1°C/W	21.8°C/W	20.8°C/W	120°C	16°C

As seen by looking at the ambient temperature results, most users will want to implement some type of thermal management to obtain a more reasonable maximum ambient temperature.

Thermal Characteristics in Forced Air

A sample size of three TS68040 packages was tested in forced air cooling in a wind tunnel with no heat sink. This test was performed with 3W of power being dissipated from within the package. As previously mentioned, since the variance in ΦJA within the possible power range is negligible, it can be assumed for calculation purposes that Φ_{JA} is constant at all power levels. Using the previous formulas, Table 8 shows the results of the maximum power dissipation at 3 and 5W with air-flow and no heat sink (refer to Table 6 to calculate other power dissipation values).

Table 8. Thermal Parameters With Forced Air Flow and No Heat Sink

Thermal Mgmt. Technique	Defined Parameters			Measured	Calculated		
Air-flow velocity	P_D	T_J	Φ_{JC}	Φ_{JA}	Φ_{CA}	T_C	T_A
100 LFM	3W	125°C	1°C/W	11.7°C/W	10.7°C/W	122°C	89.9°C
250 LFM	3W	125°C	1°C/W	10°C/W	9°C/W	122°C	95°C
500 LFM	3W	125°C	1°C/W	8.9°C/W	7.9°C/W	122°C	98.3°C
750 LFM	3W	125°C	1°C/W	8.5°C/W	7.5°C/W	122°C	99.5°C
1000 LFM	3W	125°C	1°C/W	8.3°C/W	7.3°C/W	122°C	100.1°C
100 LFM	5W	125°C	1°C/W	11.7°C/W	10.7°C/W	120°C	66.5°C
250 LFM	5W	125°C	1°C/W	10°C/W	9°C/W,	120°C	75°C
500 LFM	5W	125°C	1°C/W	8.9°C/W	7.9°C/W	120°C	80.5°C
750 LFM	5W	125°C	1°C/W	8.5°C/W	7.5°C/W	120°C	82.5°C
1000 LFM	5W	125°C	1°C/W	8.3°C/W	7.3°C/W	120°C	83.5°C

By reviewing the maximum ambient operating temperatures, it can be seen that by using the all-small-buffer configuration of the TS68040 with a relatively small amount of air flow (100 LFM), a 0-70°C ambient operating temperature can be achieved. However, depending on the output buffer configuration and available forced-air cooling, additional thermal management techniques may be required.

Thermal Characteristics with a Heat Sink

In choosing a heat sink the designer must consider many factors: heat sink size and composition, method of attachment, and choice of a wet or dry connection. The following paragraphs discuss the relationship of these decisions to the thermal performance of the design noticed during experimentation.

The heat sink size is one of the most significant parameters to consider in the selection of a heat sink. Obviously a larger heat sink will provide better cooling. However, it is less obvious that the most benefit of the larger heat sink of the pin fin type used in the experimentation would be at still air conditions. Under forced-air conditions as low as 100 LFM, the difference between the ΦCA becomes very small (0.4°C/W or less). This difference continues to decrease as the forced air flow increases. The particular heat sink used in our testing fit the perimeter package surface area available within the capacitor pads on the TS68040 (1.48" x 1.48") and showed a nice compromise between height and thermal performance needs. The heat sink base perimeter area was 1.24" x 1.30" and its height was 0.49". It was a pin-fin-type (i.e. bed of nails) design composed of Al alloy. The heat sink is shown in Figure 5 can be obtained through Thermalloy Inc. by referencing part number 2338B.

Figure 5. Heat Sink Example

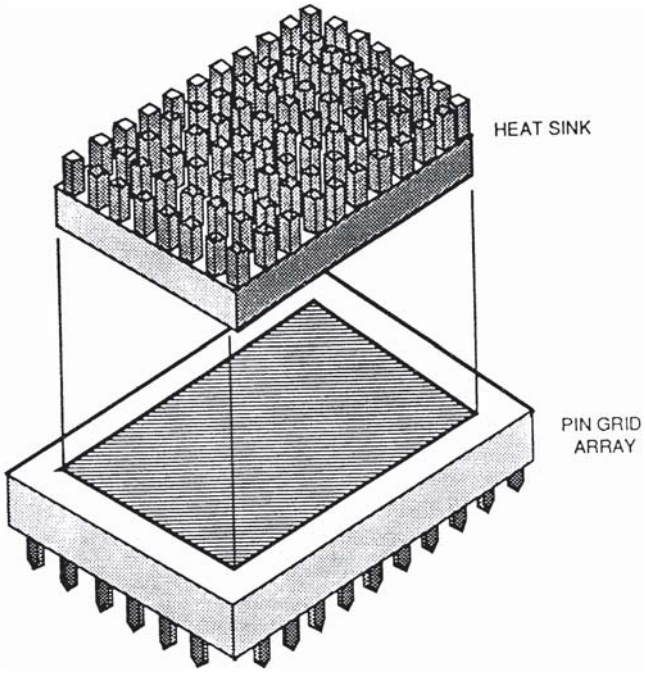


Table 9. Thermal Parameters With Heat Sink and No Air Flow

Thermal Mgmt. Technique	Defined Parameters			Measured	Calculated		
Heat Sink	P_D	T_J	Φ_{JC}	Φ_{JA}	Φ_{CA}	T_C	T_A
2338B	3W	125°C	1°C/W	14°C/W	13°C/W	122°C	83°C
2338B	5W	125°C	1°C/W	14°C/W	13°C/W	120°C	55°C

Thermal Characteristics with a Heat Sink and Forced Air

A sample size of three TS68040 packages was tested in forced-air cooling in a wind tunnel with a heat sink. This test was performed with 3W of power being dissipated from within the package. As mentioned previously, the variance in Φ_{JA} within the possible power range is negligible; it can be assumed for calculation purposes that Φ_{JA} is valid at all power levels. Table 10 shows the results, assuming a maximum power dissipation at 3 and 5W with air flow and heat sink thermal management (refer to Table 6 to calculate other power dissipation values).

Table 10. Thermal Parameters with Heat Sink and Air Flow

Thermal Mgmt. Technique		Defined Parameters			Measured	Calculated		
Air-flow	Heat sink	P_D	T_J	Φ_{JC}	Φ_{JA}	Φ_{CA}	T_C	T_A
100 LFM	2338B	3W	125°C	1°C/W	3.1°C/W	2.1°C/W	122°C	115.7°C
250 LFM	2338B	3W	125°C	1°C/W	2.2°C/W	1.2°C/W	122°C	118.4°C
500 LFM	2338B	3W	125°C	1°C/W	1.7°C/W	0.7°C/W	122°C	119.9°C
750 LFM	2338B	3W	125°C	1°C/W	1.5°C/W	0.5°C/W	122°C	120.5°C
1000 LFM	2338B	3W	125°C	1°C/W	1.4°C/W	0.4°C/W	122°C	120.8°C
100 LFM	2338B	5W	125°C	1°C/W	3.1°C/W	2.1°C/W	120°C	109.5°C
250 LFM	2338B	5W	125°C	1°C/W	2.2°C/W	1.2°C/W	120°C	114°C
500 LFM	2338B	5W	125°C	1°C/W	1.7°C/W	0.7°C/W	120°C	116.5°C
750 LFM	2338B	5W	125°C	1°C/W	1.5°C/W	0.5°C/W	120°C	117.5°C
1000 LFM	2338B	5W	125°C	1°C/W	1.4°C/W	0.4°C/W	120°C	118°C

Thermal Testing Summary

Testing proved that a heat sink in combination with a relatively small amount of air-flow (100 LFM or less) will easily realize a 0-70°C ambient operating temperature for the TS68040 with almost any configuration of the output buffers. A heat sink alone may be capable of providing all necessary cooling, depending on the particular heat sink height/size restraints, the maximum ambient operating temperature required, and the output buffer configuration chosen. Also forced air cooling alone may attain a 0-70°C ambient operating temperature. However this factor is highly dependent on the output buffer configuration chosen and the available forced air for cooling. Figure 7 is a summary of the test results of the relationship between Φ_{JA} and air-flow for the TS68040.

Figure 7. Relationship of Φ_{JA} Air-Flow for PGA

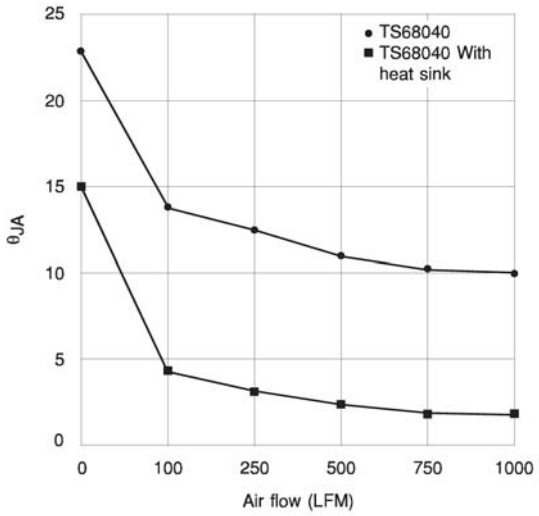


Table 11. Characteristics Guaranteed

Package	Symbol	Parameter	Value	Unit
PGA 179	θ_{J-A}	Thermal Resistance Junction-to-ambient	See Figure 7	°C/W
	θ_{J-C}	Thermal Resistance Junction-to-case	1	°C/W
CQFP 196	θ_{J-A}	Thermal Resistance Junction-to-ambient	TBD	°C/W
	θ_{J-C}	Thermal Resistance Junction-to-case	1	°C/W

Mechanical and Environment

The microcircuits shall meet all mechanical environmental requirements of either MIL-STD-883 for class B devices or for Atmel standard screening.

Marking

The document where are defined the marking are identified in the related reference documents. Each microcircuit are legible and permanently marked with the following information as minimum:

- Atmel Logo
- Manufacturer's Part Number
- Class B Identification
- Date-code Of Inspection Lot
- ESD Identifier If Available
- Country Of Manufacturing

Quality Conformance Inspection

DESC/MIL-STD-883

Is in accordance with MIL-M-38535 and method 5005 of MIL-STD-883. Group A and B inspections are performed on each production lot. Groups C and D inspection are performed on a periodical basis.

Electrical Characteristics

General Requirements

All static and dynamic electrical characteristics specified for inspection purposes and the relevant measurement conditions are given below:

- Table 12: Static electrical characteristics for the electrical variants.
- Table 13: Dynamic electrical characteristics for TS68040 (25 MHz, 33 MHz).

For static characteristics (Table 12), test methods refer to IEC 748-2 method number, where existing.

For dynamic characteristics (Table 13), test methods refer to clause “Static Characteristics” on page 18 of this specification.

Indication of “min.” or “max.” in the column «test temperature» means minimum or maximum operating temperature as defined in sub-clause Table 5 here above.

Static Characteristics

Table 12. Electrical Characteristics
$-55°C \leq T_C \leq T_{Jmax}$; $4.75V \leq V_{CC} \leq 5.25V$ unless otherwise specified(1)(2)(3)(4)

Symbol	Characteristic	Min	Max	Unit
V_{IH}	Input High Voltage	2	V_{CC}	V
V_{IL}	Input Low Voltage	GND	0.8	V
V_U	Undershoot		- 0.8	V
I_{in}	Input Leakage Current at 0.5/2.4V — $\overline{AVEC}$, BCLK $\overline{BG}$, $\overline{CDIS}$, $\overline{IPLn}$, $\overline{MDIS}$, PCLK, $\overline{RSTI}$, SCn, $\overline{TBI}$, $\overline{TCI}$, TCK, $\overline{TEA}$	-20	20	µA
I_{TSI}	Hi-z (Off-state) Leakage Current at 0.5/2.4V — An, $\overline{BB}$, $\overline{CIOUT}$, Dn, $\overline{LOCK}$, $\overline{LOCKE}$, R/$\overline{W}$, SIZn, $\overline{TA}$, TDO, $\overline{TIP}$, TLNn, TMn, $\overline{TS}$, TTn, UPAn	-20	20	µA
I_{IL}	Signal Low Input Current V_{IL} = 0.8V — TMS, TDI, $\overline{TRST}$	-1.1	-0.18	mA
I_{IH}	Signal High Input Current V_{IH} = 2.0V — TMS, TDI, $\overline{TRST}$	-0.94	-0.16	mA
V_{OH}	Output High Voltage Larger Buffers - I_{OH} = 35 mA Small Buffers - I_{OH} = 5 mA	2.4		V

Table 12. Electrical Characteristics (Continued)
$-55°C \leq T_C \leq T_{Jmax}$; $4.75V \leq V_{CC} \leq 5.25V$ unless otherwise specified[1][2][3][4]

Symbol	Characteristic	Min	Max	Unit
V_{OL}	Output Low Voltage Larger buffers - I_{OL} = 35 mA Small buffers - I_{OL} = 5 mA		0.5	V
P_D	Power Dissipation (T_J = 125°C) Larger Buffers Enabled Small Buffers Enabled		7.7 6.3	W
C_{in}	Capacitance - Note 4 V_{in} = 0V, f = 1 MHz		25	pF

Notes:
1. All testing to be performed using worst-case test conditions unless otherwise specified.
2. Maximum operating junction temperature (T_J) = +125°. Minimum case operating temperature (T_C) = -55°. This device is not tested at T_C = +125°. Testing is performed by setting the junction temperature T_J = +125°and allowing the case and ambient temperatures to rise and fall as necessary so as not to exceed the maximum junction temperature.
3. Capacitance is periodically sampled rather than 100% tested.
4. Power dissipation may vary in between limits depending on the application.

Dynamic Characteristics

Table 13. Clock AC Timing Specifications (see Figure 8)
$-55°C \leq T_C \leq T_{Jmax}$; $4.75V \leq V_{CC} \leq 5.25V$ unless otherwise specified[1][2][3][4]

Num	Characteristic	25 MHz		33 MHz		Unit
		Min	Max	Min	Max	
Frequency of Operation		20	25	20	33	MHz
1	PCLK Cycle Time	20	25	15	25	ns
2	PCLK Rise Time[4]		1.7		1.7	ns
3	PCLK Fall Time[4]		1.6		1.6	ns
4	PCLK Duty Cycle Measured at 1.5V[4]	47.5	52.5	46.67	53.33	%
4a	PCLK Pulse Width High Measured at 1.5V[3][4]	9.5	10.5	7	8	ns
4b	PCLK Pulse Width Low Measured at 1.5V[3][4]	9.5	10.5	7	8	ns
5	BCLK Cycle Time	40	50	30	60	ns
6, 7	BCLK Rise and Fall Time		4		3	ns
8	BCLK Duty Cycle Measured at 1.5V[4]	40	60	40	60	%
8a	BCLK Pulse Width High Measured at 1.5V[4]	16	24	12	18	ns
8b	BCLK Pulse Width Low Measured at 1.5V[4]	16	24	12	18	ns
9	PCLK, BCLK Frequency Stability[4]		1000		1000	ppm
10	PCLK to BCLK Skew		9		n/a	ns

Notes:
1. All testing to be performed using worst-case test conditions unless otherwise specified.
2. Maximum operating junction temperature (T_J) = +125°. Minimum case operating temperature (T_C) = -55°. This device is not tested at T_C = +125°. Testing is performed by setting the junction temperature T_J = +125°and allowing the case and ambient temperatures to rise and fall as necessary so as not to exceed the maximum junction temperature.
3. Specification value at maximum frequency of operation.
4. If not tested, shall be guaranteed to the limits specified.

Figure 11. DLE Timing Burst Access

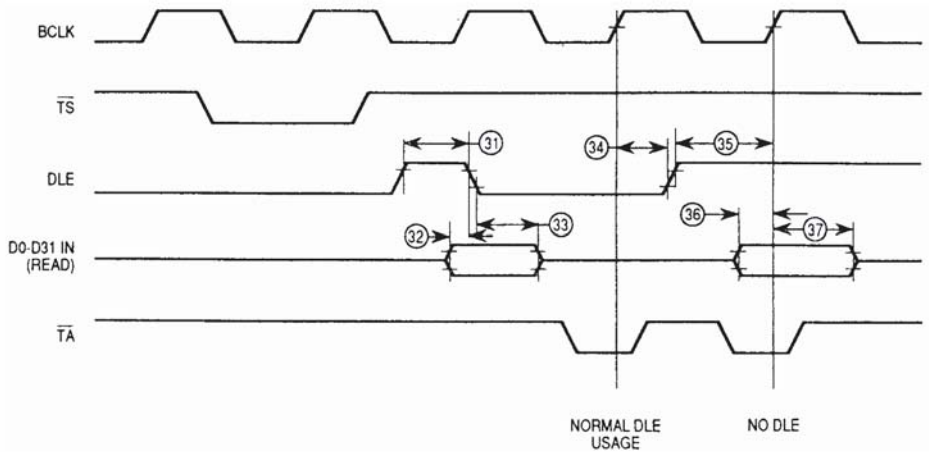


Figure 12. Bus Arbitration Timing

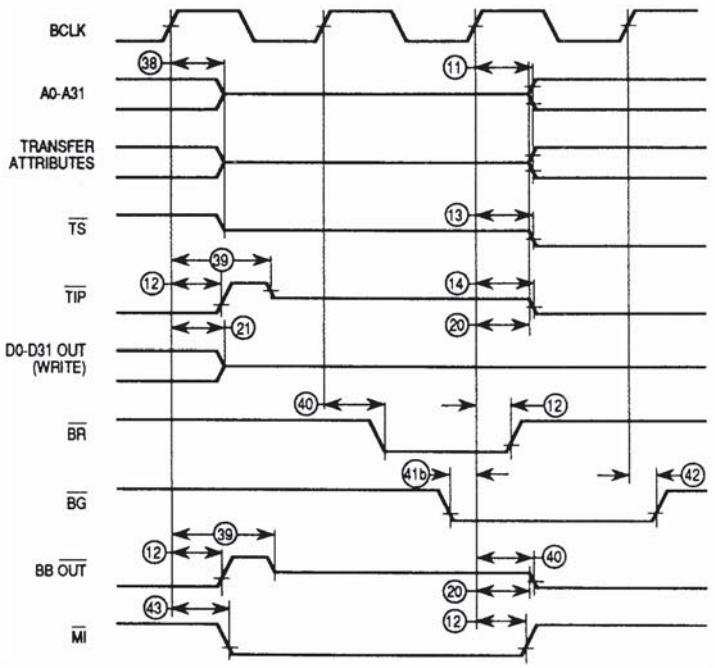


Table 19. Addressing Modes

Addressing Modes	Syntax
Register Direct	
Date Register Direct	Dn
Address Register Direct	An
Register Indirect	
Address Register Indirect	(An)
Address Register Indirect With Postincrement	(An)
Address Register Indirect With Predecrement	(An)
Address Register Indirect With Displacement	(d_{16}, An)
Register Indirect With Index	
Address Register Indirect With Index (8-bit Displacement)	(d_8, An, Xn)
Address Register Indirect With Index (Base Displacement)	(bd, An, Xn)
Memory Indirect	
Memory Indirect Postincrement	([bd, An], Xn, od)
Memory Indirect Preindexed	([bd, An, Xn], od)
Program Counter Indirect With Displacement	(d_{16}, PC)
Program Counter Indirect With Index	
PC Indirect With Index (8-bit Displacement)	(d_8, PC, Xn)
PC Indirect With Index (Base Displacement	(bd, PC, Xn)
Program Counter Memory Indirect	
PC Memory Indirect Postindexed	([bd, PC], Xn, od)
PC Memory Indirect Preindexed	([bd, PC, Xn], od)
Absolute	
Absolute Short	xxx.W
Absolute Long	xxx.L
Immediate	# (data)

Note:

DN = Data register, D0-D7

AN = Address register, A0-A7

d_8, d_{16} = A twos-complement or sign-extended displacement; added as part of the effective address calculation; size is 8 (d_8) or 16 (d_{16}) bits; when omitted, assemblers use a value of zero.

Xn = Address or data register used as an index register; form is Xn, SIZE*SCALE, where SIZE is W or L (indicates index register size) and SCALE is 1, 2, 4 or 8 (index register os multiplied by SCALE); use of SIZE and or SCALE is optional.

bd = A twos-complement base displacement; when present, size can be 16 or 32 bits.

od = Outer displacement added as part of effective address calculation after any memory indirection; use is optional with a size of 16 or 32 bits.

PC = Program counter.

(data) = Immediate value of 8, 16 or 32 bits.

( ) = Effective address.

[ ] = Used as indirect address to long-word address.

The instruction provided by the TS68040 are listed in Table 20. The instruction set has been tailored to support high-level languages and is optimized for those instructions most commonly executed (however, all instructions listed are fully supported). Many instructions operate on bytes, words, and long words, and most instructions can use any of the addressing modes of Table 19.

Table 20. Instruction Set Summary

Mnemonic	Description
ABCD	Add Decimal With Extend
ADD	Add
ADDA	Add Address
ADDI	Add Immediate
ADDQ	Add Quick
ADDX	Add With Extend
AND	Logical AND
ANDI	Logical AND Immediate
ASL, ASR	Arithmetic Shift Left And Right
Bcc	Branch Conditionally
BCHG	Test Bit And Change
BCLR	Test Bit And Clear
BFCHG	Test Bit Field And Change
BFCLR	Test Bit Field And Clear
BFEXTS	Signed Bit Field Extract
BFEXTU	Unsigned Bit Field Extract
BFFFO	Bit Field Find First One
BFINS	Bit Field Insert
BFSET	Test Bit Field And Set
BFTST	Test Bit Field
BKPT	Breakpoint
BRA	Branch
BSET	Test Bit And Set
BSR	Branch To Subroutine
BTST	Test Bit
CAS	Compare And Swap Operands
CAS2	Compare And Swap Dual Operands
CHK	Check Register Against Bounds
CHK2	Check Register Against Upper And Lower Bounds
CINV(1)	Invalidate Cache Entries
CLR	Clear
CMP	Compare
CMPA	Compare Address
CMPI	Compare Immediate
CMPM	Compare Memory To Memory
CMP2	Compare Register Against Upper And Lower Bounds
CPUSH(1)	Push Then Invalidate Cache Entries
DB_{CC}	Test Condition, Decrement And Branch
DIVS, DIVSL	Signed Divide
DIVU, DIVUL	Unsigned Divide
EOR	Logical Exclusive OR
EORI	Logical Exclusive OR Immediate
EXG	Exchange Registers
EXT, EXTB	Sign Extend

Table 20. Instruction Set Summary (Continued)

Mnemonic	Description
SBCD	Substract Decimal With Extend
Scc	Set Conditionally
STOP	Stop
SUB	Subtract
SUBA	Subtract Address
SUBI	Subtract Immediate
SUBQ	Subtract Quick
SUBX	Subtract With Extend
SWAP	Swap Register Words
TAS	Test Operand And Set
TRAP	Trap
TRAPcc	Trap Conditionally
TRAPV	Trap On Overflow
TST	Trap Operand
UNLK	Unlink
UNPK	Unpack BCD

Note: 1. TS6840 additions or alterations to the TS68030 and TS68881/TS68882 instructions sets.

Table 21. Floating-point instructions

Mnemonic	Description
FABS(1)	Floating-point Absolute Value
FADD(1)	Floating-point Add
FBcc	Branch On Floating-point Condition
FCMP	Floating-point Compare
FDBcc	Floating-point Decrement And Branch
FDIV(1)	Floating-point Divide
FMOVE(1)	Move Floating-point Register
FMOVEM	Move Multiple Floating-point Registers
FMUL(1)	Floating-point Multiply
FNEG(1)	Floating-point Negate
FRESTORE	Restore Floating-point Internal State
FSAVE	Save Floating-point Internal State
FScc	Set According To Floating-point Condition
FSQRT(1)	Floating-point Square Root
FSUB(1)	Floating-point Substract
FTRAPcc	Trap On Floating-point Condition
FTST	Floating-point Test

Note: 1. TS6840 additions or alterations to the TS68030 and TS68881/TS68882 instructions sets.

The TS68040 floating-point instructions, a commonly used subset of the TS68882 instruction set, are implemented in hardware. The remaining unimplemented instructions are less frequently used and are efficiently emulated in software, maintaining compatibility with the TS68881/TS68882 floating-point coprocessors.

The TS68040 instruction set includes MOVE16, a new user instruction that allows high-speed transfers of 16-byte blocks between external devices such as memory to memory or coprocessor to memory.

Instruction and Data Caches

Studies have shown that typical programs spend much of their execution time in a few main routines or tight loops. Earlier members of the TS68000 Family took advantage of this locality of reference phenomenon to varying degrees. The TS68040 takes further advantage of cache technology with its two, independent, on-chip, physical address space caches, one for instructions and one for data. The caches reduce the processor's external bus activity and increase CPU throughput by lowering the effective memory access time. For a typical system design, the large caches of the TS68040 yield a very high hit rate, providing a substantial increase in system performance. Additionally, the caches are automatically burstfilled from the external bus whenever a cache miss occurs.

The autonomous nature of the caches allows instruction-stream fetches, data-stream fetches, and a third external access to occur simultaneously with instruction execution. For example, if the TS68040 requires both an instruction-stream access and an external peripheral access and if the instruction is resident in the on-chip cache, the peripheral access proceeds unimpeded rather than being queued behind the instruction fetch. If a data operand is also required and if it is resident in the data cache, it can also be accessed without hindering either the instruction access from its cache or the peripheral access external to the chip. The parallelism inherent in the TS68040 also allows multiple instructions that do not require any external accesses to execute concurrently while the processor is performing an external access for a previous instruction.

Cache Organization

The instruction and data caches are four-way set-associative with 64 sets of four, 16-byte lines for a total cache storage of 4K bytes each. As shown in Figure 21, each 16-byte line contains an address tag and state information. State information for each entry consists of a valid flag for the entire line in both instruction and data caches and write status for each long word in the data cache. The write status in the data cache signifies whether or not the long-word data is dirty (meaning that the data in the cache has been modified but has not been written back to external memory) for data in copyback pages.

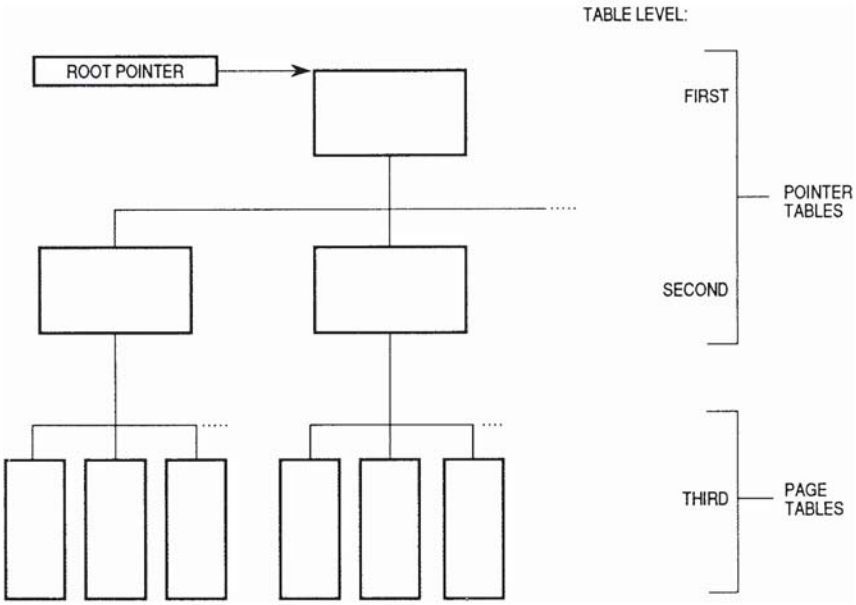
Address Translation Cache

An integral part of the translation function previously described is the dual cache memory that stores recently used logical-to-physical address translation information (page descriptors) for instruction and date accesses. These caches are 64-entry, four-way, set associative. Each ATC compare the logical address of the incoming access against its entries. If one of the entries matches, there is a hit, and the ATC sends the physical address to the bus controller, which then starts the external bus cycle (provided there was no hit in the corresponding cache for the access).

Translation Tables

The translation tables of the TS68040 have a three level tree structure and reside in main memory. Since only a portion of the complete tree needs to exist at any one time, the tree structure minimizes the amount of memory necessary to set up the tables for most programs. As shown in Figure 20, either the user root pointer or the supervisor root pointer points to the first level table, depending on the values of the function code for an access. Table entries at the second level of the tree (pointer tables) contain pointers to the third level (page tables). Entries in the page tables contain either page descriptors or indirect pointers to page descriptors. The mechanism for performing table search operations uses portions of the logical address (as indices) at each level of the search. All addresses in the translation table entries are physical addresses.

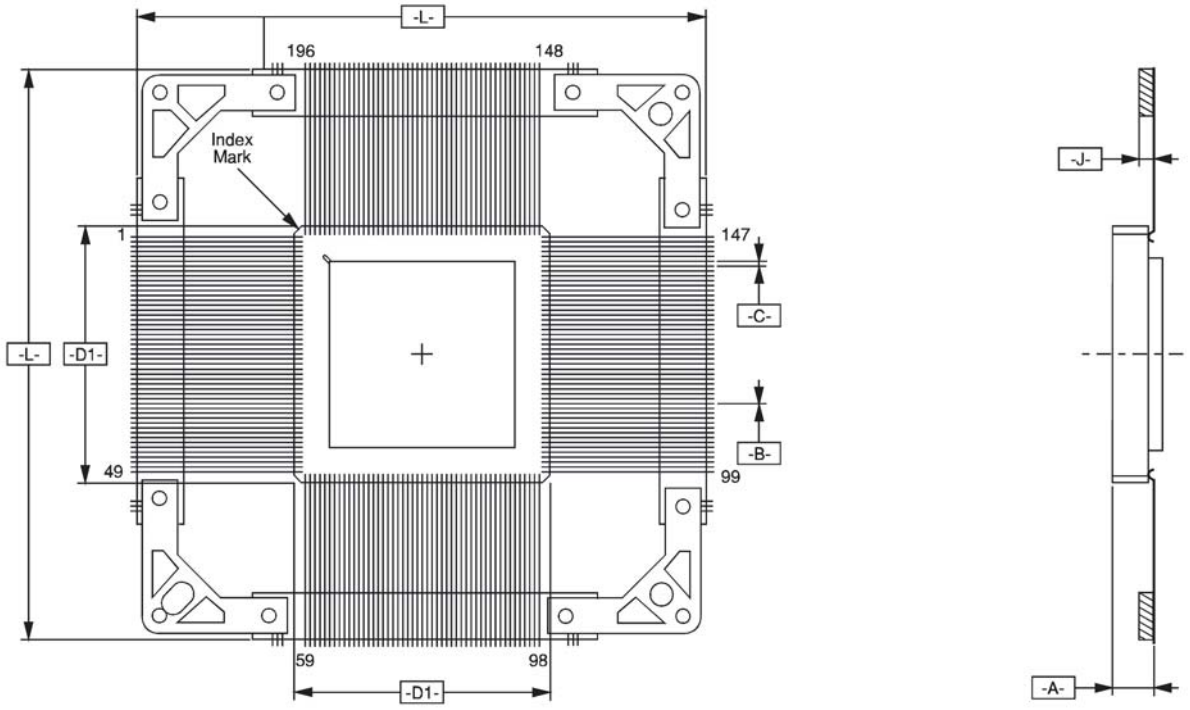
Figure 22. Translation Table Structure



There are two variations of table searches for both 4K and 8K page sizes: normal searches and indirect searches. An indirect search differs in that the entry in the third level page table contains a pointer to a page descriptor rather than the page descriptor itself.

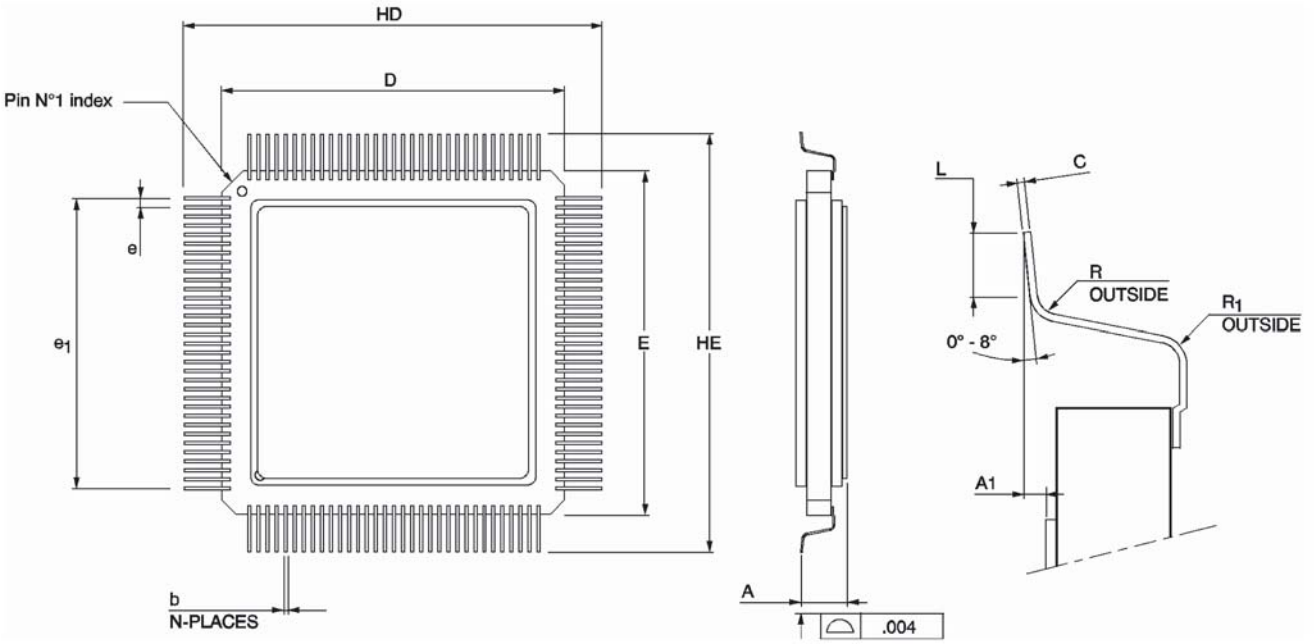
Entries in the translation tables contain control and status information on addition to the physical address information. Control bits specify write protection, limit access to supervisor only, and determine cachability of data in each memory page. Each page descriptor also has two user-programmable bits that appear on the UPA0 and UPA1 signals during an external access for use as address modifier bits.

196 pins – Tie Bar CQFP
Cavity Up (on request)



Dim	Millimeters	Inches
A	3.30 max	0.130 max
B	0.23 +0.05 0.23 -0.038	0.009 +0.002 0.009 -0.015
C	0.635 typ.	.025 typ.
D1	33.91 ± 0.25	1.335 ± 0.01
J	0.89 ± 0.13	0.035 ± 0.005
L	63.5 ± 0.51	2.5 ± 0.02

196 pins – Gullwing
CQFP cavity up



* Reduce pin count shown for clarity, 49 pins per side

Symbol	Millimeters	Inches
A	4.19 max	0.165 max
A1	0.673 ± 0.2	.0265 ±.008
b	0.23 +0.05 0.23 -0.038	.009 +.002 .009 -.0015
c	0.127 +0.05 0.127 -0.025	.005 +.002 .005 -.001
D/E	33.91 ±0.25	1.335 ±.01
e	.635 BSC	.025 BSC
e1	30.48 ±0.13	1.2 ±.005
HD/HE	38.8 ±0.18	1.528 ±.007
L	0.813 ±0.2	.032 ±.008
N	196	196
R	0.55 ±0.25	.022 ±.01
R1	0.23 min	.009 min

Standard Product

Commercial Atmel Part Number	Norms	Package	Temperature Range (°C)	Frequency (MHz)	Drawing Number
TS68040VR25A	Atmel standard	PGA 179	T_C = -40/+T_J = +110	25	Atmel datasheet
TS68040VR33A	Atmel standard	PGA 179	T_C = -40/+T_J = +110	33	Atmel datasheet
TS68040MR25A	Atmel standard	PGA 179	T_C = -55/+T_J = +125	25	Atmel datasheet
TS68040MR33A	Atmel standard	PGA 179	T_C = -55/+T_J = +125	33	Atmel datasheet
TS68040VF25A	Atmel standard	CQFP 196	T_C = -40/+T_J = +110	25	Atmel datasheet
TS68040VF33A	Atmel standard	CQFP 196	T_C = -40/+T_J = +110	33	Atmel datasheet
TS68040MF25A	Atmel standard	CQFP 196	T_C = -55/+T_J = +125	25	Atmel datasheet
TS68040MF33A	Atmel standard	CQFP 196	T_C = -55/+T_J = +125	33	Atmel datasheet

Note: FT: available on request.

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