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## Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

## Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | 68000 |
| Number of Cores/Bus Width | 1 Core, 32-Bit |
| Speed | 25MHz |
| Co-Processors/DSP | - |
| RAM Controllers | - |
| Graphics Acceleration | No |
| Display & Interface Controllers | - |
| Ethernet | - |
| SATA | - |
| USB | - |
| Voltage - I/O | 5.0V |
| Operating Temperature | -40°C ~ 110°C (TC) |
| Security Features | - |
| Package / Case | 196-BCQFP |
| Supplier Device Package | 196-CQFP (34x34) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/ts68040vf25a |

## Introduction

The TS68040 is an enhanced, 32-bit, HCMOS microprocessor that combines the integer unit processing capabilities of the TS68030 microprocessor with independent 4K bytes data and instruction caches and an on-chip FPU. The TS68040 maintains the 32-bit registers available with the entire TS68000 Family as well as the 32-bit address and data paths, rich instruction set, and versatile addressing modes. Instruction execution proceeds in parallel with accesses to the internal caches, MMU operations, and bus controller activity. Additionally, the integer unit is optimized for high-level language environments.

The TS68040 FPU is user-object-code compatible with the TS68882 floating-point coprocessor and conforms to the ANSI/IEEE Standard 754 for binary floating-point arithmetic. The FPU has been optimized to execute the most commonly used subset of the TS68882 instruction set, and includes additional instruction formats for single and double-precision rounding of results. Floating-point instructions in the FPU execute concurrently with integer instructions in the integer unit.

The MMUs support multiprocessing, virtual memory systems by translating logical addresses to physical addresses using translation tables stored in memory. The MMUs store recently used address mappings in two separate ATCs-on-chip. When an ATC contains the physical address for a bus cycle requested by the processor, a translation table search is avoided and the physical address is supplied immediately, incurring no delay for address translation. Each MMU has two transparent translation registers available that define a one-to-one mapping for address space segments ranging in size from 16M bytes to 4G bytes each.

Each MMU provides read-only and supervisor-only protections on a page basis. Also, processes can be given isolated address spaces by assigning each a unique table structure and updating the root pointer upon a task swap. Isolated address spaces protect the integrity of independent processes.

The instruction and data caches operate independently from the rest of the machine, storing information for fast access by the execution units. Each cache resides on its own internal address bus and internal data bus, allowing simultaneous access to both. The data cache provides write through or copyback write modes that can be configured on a page-by-page basis.

The TS68040 bus controller supports a high-speed, non multiplexed, synchronous external bus interface, which allows the following transfer sizes: byte, word (2 bytes), long word (4 bytes), and line (16 bytes). Line accesses are performed using burst transfers for both reads and writes to provide high data transfer rates.

## Signal Description

Figure 4 and Table 3 describe the signals on the TS68040 and indicate signal functions. The test signals, $\overline{TRST}$, TMS, TCK, TDI, and TDO, comply with subset P-1149.1 of the IEEE testability bus standard.

**Figure 4.** Functional Signal Groups

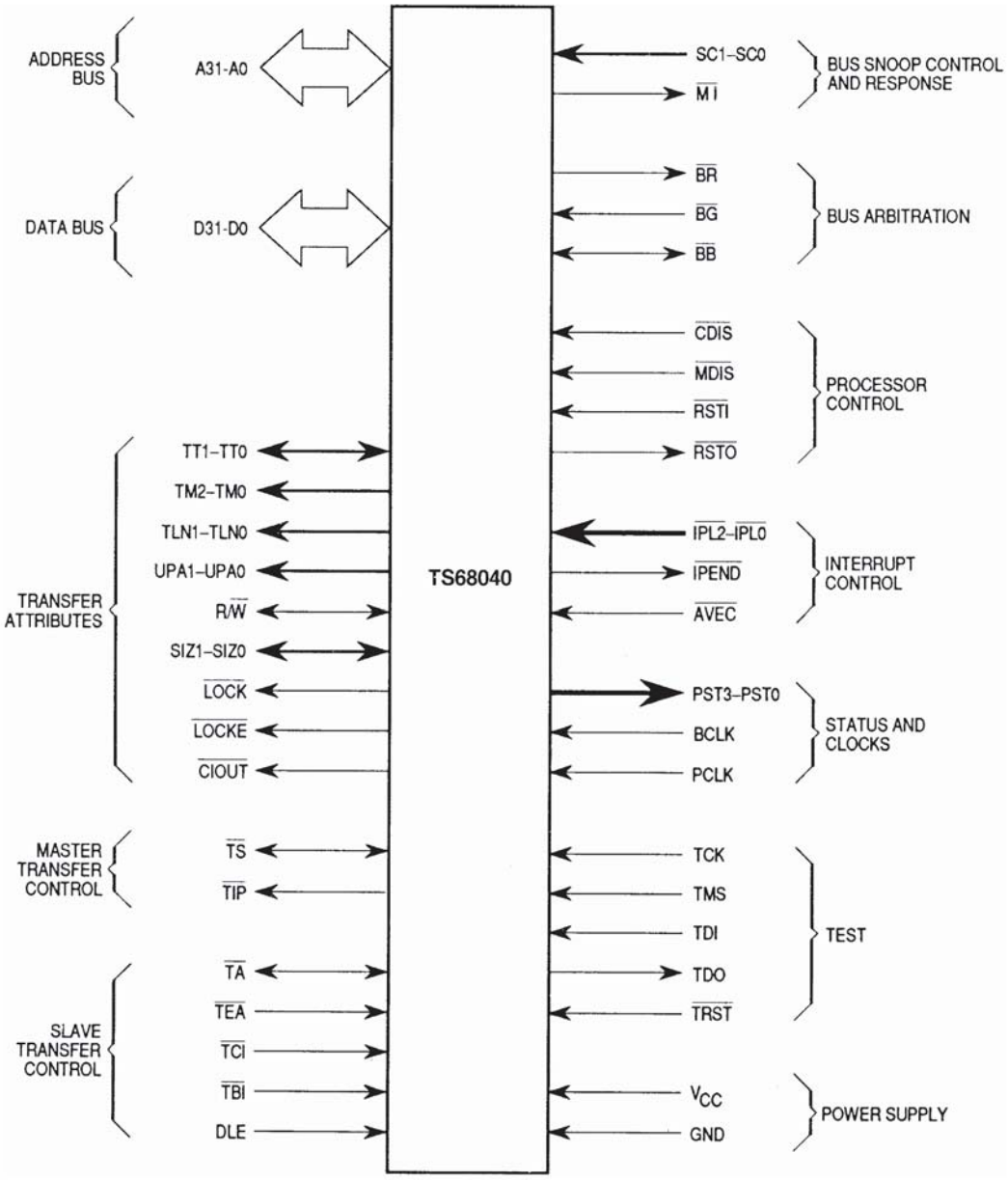


**Table 3.** Signal Index (Continued)

| Signal Name | Mnemonic | Function |
|---|---|---|
| Bus Clock | BCLK | Clock input used to derive all bus signal timing |
| Processor Clock | PCLK | Clock input used for internal logic timing. The PCLK frequency is exactly 2X the BCLK frequency |
| Test Clock | TCK | Clock signal for the IEEE P1149.1 test access port (TAP) |
| Test Mode Select | TMS | Selects the principle operations of the test-support circuitry |
| Test Data Input | TDI | Serial data input for the TAP |
| Test Data Output | TDO | Serial data output for the TAP |
| Test Reset | $\overline{\text{TRST}}$ | Provides an asynchronous reset of the TAP controller |
| Power Supply | $V_{CC}$ | Power supply |
| Ground | GND | Ground connection |

## Scope

This drawing describes the specific requirements for the microprocessor TS68040 - 25 MHz and 33 MHz, in compliance with MIL-STD-883 class B or Atmel standard screening.

## Applicable Documents

### MIL-STD-883

1. MIL-STD-883: test methods and procedures for electronics.
2. MIL-I-38535: general specifications for microcircuits.
3. DESC 5962-93143.

## Requirements

### General

The microcircuits are in accordance with the applicable document and as specified herein.

### Design and Construction

**Terminal Connections**

See Figure 2 and Figure 3.

**Lead Material and Finish**

Lead material and finish shall be as specified in MIL-STD-883 (see enclosed “MIL-STD-883 C and Internal Standard” on page 46).

**Package**

The macro circuits are packaged in hermetically sealed ceramic packages which conform to case outlines of MIL-STD-1835-or as follow:

- CMGA 10-179-PAK pin grid array, but see “179 pins – PGA” on page 43.
- Similar to CQCC1-F196C-U6 ceramic uniform lead chip carrier package with ceramic nonconductive tie-bar but use Atmel’s internal drawing, see “196 pins – Tie Bar CQFP Cavity Up (on request)” on page 44.
- Gullwing shape CQFP see “196 pins – Gullwing CQFP cavity up” on page 45.

The precise case outlines are described at the end of the specification (See “Package Mechanical Data” on page 43.) and into MIL-STD-1835.

## Electrical Characteristics

**Absolute Maximum Ratings** Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

**Table 4.** Absolute Maximum Ratings

| Symbol | Parameter | Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage Range | | -0.3 | 7.0 | V |
| $V_I$ | Input Voltage Range | | -0.3 | 7.0 | V |
| $P_D$ | Power Dissipation | Large buffers enabled | | 7.7 | W |
| | | Small buffers enabled | | 6.3 | W |
| $T_C$ | Operating Temperature | | -55 | $T_J$ | °C |
| $T_{stg}$ | Storage Temperature Range | | -65 | +150 | °C |
| $T_J$ | Junction Temperature(1) | | | +125 | °C |
| $T_{lead}$ | Lead Temperature | Max.10 sec soldering | | +300 | °C |

Note: 1. This device is not tested at TC = +125°C. Testing is performed by setting the junction temperature Tj = +125°C and allowing the case and ambient temperatures to rise and fall as necessary so as not to exceed the maximum junction temperature.

**Table 5.** Recommended Conditions of Use
Unless otherwise stated, all voltages are referenced to the reference terminal

| Symbol | Parameter | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage Range | | +4.75 | | +5.25 | V |
| $V_{IL}$ | Logic Low Level Input Voltage Range | | GND - 0.3 | | 0.8 | V |
| $V_{IH}$ | Logic High Level Input Voltage Range | | +2.0 | | $V_{CC}$ + 0.3 | V |
| $V_{OH}$ | High Level Output Voltage | | 2.4 | | | V |
| $V_{OL}$ | Low Level Output Voltage | | | | 0.5 | V |
| $f_c$ | Clock Frequency | -25 MHz Version | | 25 | | MHz |
| | | -33 MHz Version | | 33 | | MHz |
| $T_C$ | Case Operating Temperature Range(1) | | -55 | | $T_{Jmax}$ | °C |
| $T_J$ | Maximum Operating Junction Temperature | | | | +125 | °C |

Note: 1. This device is not tested at TC = +125°C. Testing is performed by setting the junction temperature $T_J$ = +125°C and allowing the case and ambient temperatures to rise and fall as necessary so as not to exceed the maximum junction temperature.

To calculate the specific power dissipation of a specific design, the termination method of each signal must be considered. For example, a signal output that is not connected would not dissipate any additional power if it were configured in the large buffer rather than the small buffer mode.

**Relationships Between Thermal Resistances and Temperatures**

Since the maximum operating junction temperature has been specified to be 125°C. The maximum case temperature, TC, in °C can be obtained from:

$$T_C = T_J - P_D \cdot \Phi_{JC} \quad (2)$$

where:

$T_C$ = Maximum case temperature

$T_J$ = Maximum junction temperature

$P_D$ = Maximum power dissipation of the device

$\Phi_{JC}$ = Thermal resistance between the junction of the die and the case

In general, the ambient temperature, $T_A$, in °C is a function of the following formula:

$$T_A = T_J - P_D \cdot \Phi_{JC} - P_D \cdot \Phi_{CA} \quad (3)$$

Where the thermal resistance from case to ambient, $\Phi_{CA}$, is the only user-dependent parameter once a buffer output configuration has been determined. As seen from equation (3), reducing the case to ambient thermal resistance increases the maximum operating ambient temperature. Therefore, by utilizing such methods as heat sinks and ambient air cooling to minimize the $\Phi_{CA}$, a higher ambient operating temperature and/or a lower junction temperature can be achieved.

However, an easier approach to thermal evaluation uses the following formulas:

$$T_A = T_J - P_D \cdot \Phi_{JA} \quad (4)$$

or alternatively,

$$T_J = T_A - P_D \cdot \Phi_{JA} \quad (5)$$

where:

$\Phi_{JA}$ = thermal resistance from the junction to the ambient ($\Phi_{JC} + \Phi_{CA}$).

This total thermal resistance of a package, $\Phi_{JA}$, is a combination of its two components, $\Phi_{JC}$ and $\Phi_{CA}$. These components represent the barrier to heat flow from the semiconductor junction to the package (case) surface ($\Phi_{JC}$) and from the case to the outside ambient ($\Phi_{JC}$). Although $\Phi_{JC}$ is device related and cannot be influenced by the user, $\Phi_{CA}$ is user dependent. Thus, good thermal management by the user can significantly reduce $\Phi_{CA}$ achieving either a lower semiconductor junction temperature or a higher ambient operating temperature.

**Thermal Management Techniques**

To attain a reasonable maximum ambient operating temperature, a user must reduce the barrier to heat flow from the semiconductor junction to the outside ambient ($\Phi_{JA}$). The only way to accomplish this is to significantly reduce $\Phi_{CA}$ by applying such thermal management techniques as heat sinks and ambient air cooling.

The following paragraphs discuss some results of a thermal study of the TS68040 device without using any thermal management techniques; using only air-flow cooling, using only a heat sink, and using heat sink combined with air-flow cooling.

### Thermal Characteristics in Still Air

A sample size of three TS68040 packages was tested in free-air cooling with no heat sink. Measurements showed that the average $\Phi_{JA}$ was 22.8°C/W with a standard deviation of 0.44°C/W. The test was performed with 3W of power being dissipated from within the package. The test determined that $\Phi_{JA}$ will decrease slightly for the increasing power dissipation range possible. Therefore, since the variance in $\Phi_{JA}$ within the possible power dissipation range is negligible, it can be assumed for calculation purposes that $\Phi_{JA}$ is valid at all power levels. Using the formulas introduced previously, Table 7 shows the results of a maximum power dissipation of 3 and 5W with no heat sink or air-flow (refer to Table 6 to calculate other power dissipation values).

**Table 7.** Thermal Parameters With No Heat Sink or Air-flow

| Defined Parameters | | | Measured | Calculated | | |
|---|---|---|---|---|---|---|
| $P_D$ | $T_J$ | $\Phi_{JC}$ | $\Phi_{JA}$ | $\Phi_{CA} = \Phi_{JA} - \Phi_{JC}$ | $T_C = T_J - P_D * \Phi_{JC}$ | $T_A = T_J - P_D * \Phi_{JA}$ |
| 3 Watts | 125°C | 1°C/W | 21.8°C/W | 20.8°C/W | 122°C | 59.6°C |
| 5 Watts | 125°C | 1°C/W | 21.8°C/W | 20.8°C/W | 120°C | 16°C |

As seen by looking at the ambient temperature results, most users will want to implement some type of thermal management to obtain a more reasonable maximum ambient temperature.

### Thermal Characteristics in Forced Air

A sample size of three TS68040 packages was tested in forced air cooling in a wind tunnel with no heat sink. This test was performed with 3W of power being dissipated from within the package. As previously mentioned, since the variance in ΦJA within the possible power range is negligible, it can be assumed for calculation purposes that $\Phi_{JA}$ is constant at all power levels. Using the previous formulas, Table 8 shows the results of the maximum power dissipation at 3 and 5W with air-flow and no heat sink (refer to Table 6 to calculate other power dissipation values).

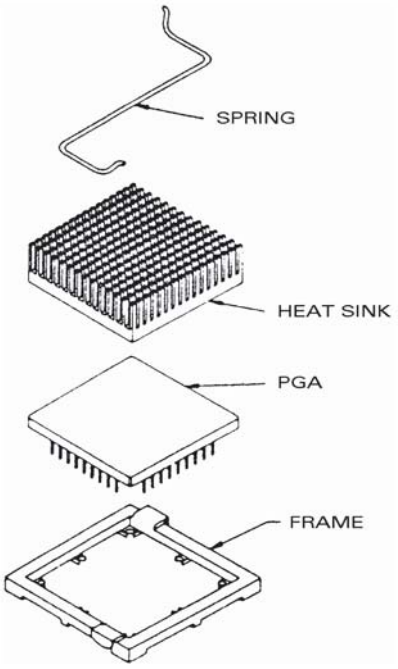
**Table 8.** Thermal Parameters With Forced Air Flow and No Heat Sink

| Thermal Mgmt. Technique | Defined Parameters | | | Measured | Calculated | | |
|---|---|---|---|---|---|---|---|
| Air-flow velocity | $P_D$ | $T_J$ | $\Phi_{JC}$ | $\Phi_{JA}$ | $\Phi_{CA}$ | $T_C$ | $T_A$ |
| 100 LFM | 3W | 125°C | 1°C/W | 11.7°C/W | 10.7°C/W | 122°C | 89.9°C |
| 250 LFM | 3W | 125°C | 1°C/W | 10°C/W | 9°C/W | 122°C | 95°C |
| 500 LFM | 3W | 125°C | 1°C/W | 8.9°C/W | 7.9°C/W | 122°C | 98.3°C |
| 750 LFM | 3W | 125°C | 1°C/W | 8.5°C/W | 7.5°C/W | 122°C | 99.5°C |
| 1000 LFM | 3W | 125°C | 1°C/W | 8.3°C/W | 7.3°C/W | 122°C | 100.1°C |
| 100 LFM | 5W | 125°C | 1°C/W | 11.7°C/W | 10.7°C/W | 120°C | 66.5°C |
| 250 LFM | 5W | 125°C | 1°C/W | 10°C/W | 9°C/W, | 120°C | 75°C |
| 500 LFM | 5W | 125°C | 1°C/W | 8.9°C/W | 7.9°C/W | 120°C | 80.5°C |
| 750 LFM | 5W | 125°C | 1°C/W | 8.5°C/W | 7.5°C/W | 120°C | 82.5°C |
| 1000 LFM | 5W | 125°C | 1°C/W | 8.3°C/W | 7.3°C/W | 120°C | 83.5°C |

All pin fin heat sinks tested were made from extrusion Al products. The planar face of the heat sink mating to the package should have a good degree of planarity; if it has any curvature, the curvature should be convex at the central region of the heat sink surface to provide intimate physical contact to the PGA surface. All heat sinks tested met this criteria. Nonplanar, concave curvature the central regions of the heat sink will result in poor thermal contact to the package. A specification needs to be determined for the planarity of the surface as part of any heat sink design.

Although there are several ways to attach a heat sink to the package, it was easiest to use a demountable heat sink attach called “E-Z attach for PGA packages” developed by Thermalloy (see Figure 6). The heat sink is clamped to the package with the help of a steel spring to a plastic frame (or plastic shoes Besides the height of the heat sink and plastic frame, no additional height added to the package. The interface between the ceramic package and the heat sink was evaluated for both dry and wet (i.e., thermal grease) interfaces in still air. The thermal grease reduced the $\Phi_{CA}$ quite significantly (about 2.5 °C/W) in still air. Therefore, it was used in all other testing done with the heat sink. According to other testing, attachment with thermal grease provided about the same thermal performance as if a thermal epoxy were used.

**Figure 6.** Heat Sink with Attachment




A sample size of one TS68040 package was tested in still air with the heat sink and attachment method previously described. This test was performed with 3W of power being dissipated from within the package. Since the variance in $\Phi_{JA}$ within the possible power range is negligible, it can be assumed for calculation purposes that $\Phi_{JA}$ is constant at all power levels. Table 9 shows the result assuming a maximum power dissipation of the part at 3 and 5W (refer to Table 6 to calculate other power dissipation values).

**Figure 8.** Clock Input Timing

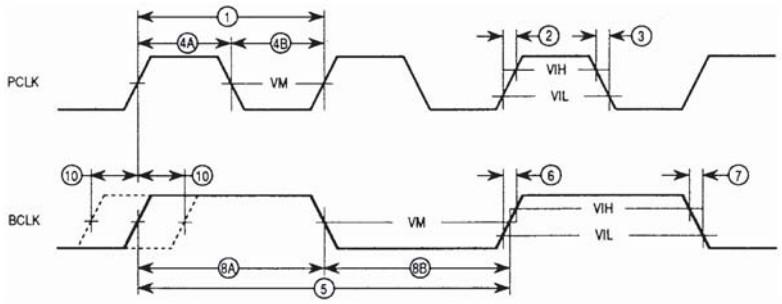



**Table 14.** Output AC Timing Specifications[1] (Figure 9 to Figure 15)

These output specifications are only for 25 MHz. They must be scaled for lower operating frequencies. Refer to TS6804DH/AD for further information. -55°C ≤$T_C$ ≤$T_{Jmax}$; 4.75V ≤$V_{CC}$ ≤5.25V unless otherwise specified.[2][3][4]

| | | 25 MHz | | | | 33 MHz | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Large Buffer[1] | | Small Buffer[1] | | Large Buffer[1] | | Small Buffer[1] | | |
| Num | Characteristic | Min | Max | Min | Max | Min | Max | Min | Max | Unit |
| 11 | BCLK to address $\overline{\text{CIOUT}}$, $\overline{\text{LOCK}}$, $\overline{\text{LOCKE}}$, R/$\overline{\text{W}}$, SIZn, TLN, TMn, UPAn valid[5] | 9 | 21 | 9 | 30 | 6.50 | 18 | 6.50 | 25 | ns |
| 12 | BCLK to output invalid (output hold) | 9 | | 9 | | 6.50 | | 6.50 | | ns |
| 13 | BCLK to $\overline{\text{TS}}$ valid | 9 | 21 | 9 | 30 | 6.50 | 18 | 6.50 | 25 | ns |
| 14 | BCLK to $\overline{\text{TIP}}$ valid | 9 | 21 | 9 | 30 | 6.50 | 18 | 6.50 | 25 | ns |
| 18 | BCLK to data-out valid[6] | 9 | 23 | 9 | 32 | 6.50 | 20 | 6.50 | 27 | ns |
| 19 | BCLK to data-out invalid (output hold)[6] | 9 | | 9 | | 6.50 | | 6.50 | | ns |
| 20 | BCLK to output low impedance[5][6] | 9 | | 9 | | 6.50 | | 6.50 | | ns |
| 21 | BCLK to data-out high impedance | 9 | 20 | 9 | 20 | 6.50 | 17 | 6.50 | 17 | ns |
| 26 | BCLK to multiplexed address valid[5] | 19 | 31 | 19 | 40 | 14 | 26 | 14 | 33 | ns |
| 27 | BCLK to multiplexed address driven[5] | 19 | | 19 | | 14 | | 14 | | ns |
| 28 | BCLK to multiplexed address high impedance[5][6] | 9 | 18 | 9 | 18 | 6.50 | 15 | 6.50 | 15 | ns |
| 29 | BCLK to multiplexed data driven[6] | 19 | | 19 | | 14 | 20 | 14 | 20 | ns |
| 30 | BCLK to multiplexed data valid[6] | 19 | 33 | 19 | 42 | 14 | 28 | 14 | 35 | ns |
| 38 | BCLK to address $\overline{\text{CIOUT}}$, $\overline{\text{LOCK}}$, $\overline{\text{LOCKE}}$, R/$\overline{\text{W}}$, SIZn, $\overline{\text{TS}}$, TLNn, TMn, TTn, UPAn high impedance[5] | 9 | 18 | 9 | 18 | 6.50 | 15 | 6.50 | 15 | ns |
| 39 | BCLK to $\overline{\text{BB}}$, $\overline{\text{TA}}$, $\overline{\text{TIP}}$ high impedance | 19 | 28 | 19 | 28 | 14 | 23 | 14 | 23 | ns |
| 40 | BCLK to $\overline{\text{BR}}$, $\overline{\text{BB}}$ valid | 9 | 21 | 9 | 30 | 6.50 | 18 | 6.50 | 25 | ns |
| 43 | BCLK to $\overline{\text{MI}}$ valid | 9 | 21 | 9 | 30 | 6.50 | 18 | 6.50 | 25 | ns |
| 48 | BCLK to $\overline{\text{TA}}$ valid | 9 | 21 | 9 | 30 | 6.50 | 18 | 6.50 | 25 | ns |
| 50 | BCLK to $\overline{\text{IPEND}}$, PSTn, $\overline{\text{RSTO}}$ valid | 9 | 21 | 9 | 30 | 6.50 | 18 | 6.50 | 25 | ns |

**Table 15.** Input AC Timing Specifications (Figure 9 to Figure 15) (Continued)
-55°C ≤$T_C$ ≤$T_{Jmax}$; 4.75V ≤$V_{CC}$ ≤5.25V unless otherwise specified[1][2][3][4]

| Num | Characteristic | 25 MHz | | 33 MHz | | Unit |
|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | |
| 44c | TTn Valid to BCLK (Setup) | 6 | | 8.5 | | ns |
| 44d | R/$\overline{W}$ Valid to BCLK (Setup) | 6 | | 5 | | ns |
| 44e | SCn Valid to BCLK (Setup) | 10 | | 11 | | ns |
| 45 | BCLK to Address SIZn, TTn, R/$\overline{W}$, SCn Invalid (Hold) | 2 | | 2 | | ns |
| 46 | $\overline{TS}$ Valid to BCLK (Setup) | 5 | | 9 | | ns |
| 47 | BCLK to $\overline{TS}$ Invalid (Hold) | 2 | | 2 | | ns |
| 49 | BCLK to $\overline{BB}$ High Impedance (68040 Assumes Bus Mastership) | | 9 | | 9 | ns |
| 51 | $\overline{RSTI}$ Valid to BCLK | 5 | | 4 | | ns |
| 52 | BCLK to $\overline{RSTI}$ Invalid | 2 | | 2 | | ns |
| 53 | Mode Select Setup to $\overline{RSTI}$ Negated[4] | 20 | | 20 | | ns |
| 54 | $\overline{RSTI}$ Negated to Mode Selects Invalid[4] | 2 | | 2 | | ns |

Notes:
1. All testing to be performed using worst-case test conditions unless otherwise specified.
2. The following pins are active low: $\overline{AVEC}$, $\overline{BG}$, $\overline{BS}$, $\overline{BR}$, $\overline{CDIS}$, $\overline{CIOUT}$, $\overline{IPEND}$, $\overline{IPLO}$, $\overline{IPL1}$, $\overline{IPL2}$, $\overline{LOCK}$, $\overline{LOCKE}$, $\overline{MDIS}$, $\overline{MI}$, $\overline{RST0}$, $\overline{RSTI}$, $\overline{TA}$, $\overline{TBI}$, $\overline{TCI}$, $\overline{TEA}$, $\overline{TIP}$, $\overline{TRST}$, $\overline{TS}$ and $\overline{W}$ of R/$\overline{W}$.
3. Maximum operating junction temperature ($T_J$) = +125°. Minimum case operating temperature ($T_C$) = -55°. This device is not tested at $T_C$ = +125°. Testing is performed by setting the junction temperature $T_J$ = +125°and allowing the case and ambient temperatures to rise and fall as necessary so as not to exceed the maximum junction temperature.
4. The levels on $\overline{CDIS}$, $\overline{MDIS}$, and the $\overline{IPL2}$-$\overline{IPL0}$ signals enable or disable the multiplexed bus mode, data latch enable mode, and driver impedance selection respectively.

**Figure 13.** Snoop Hit Timing

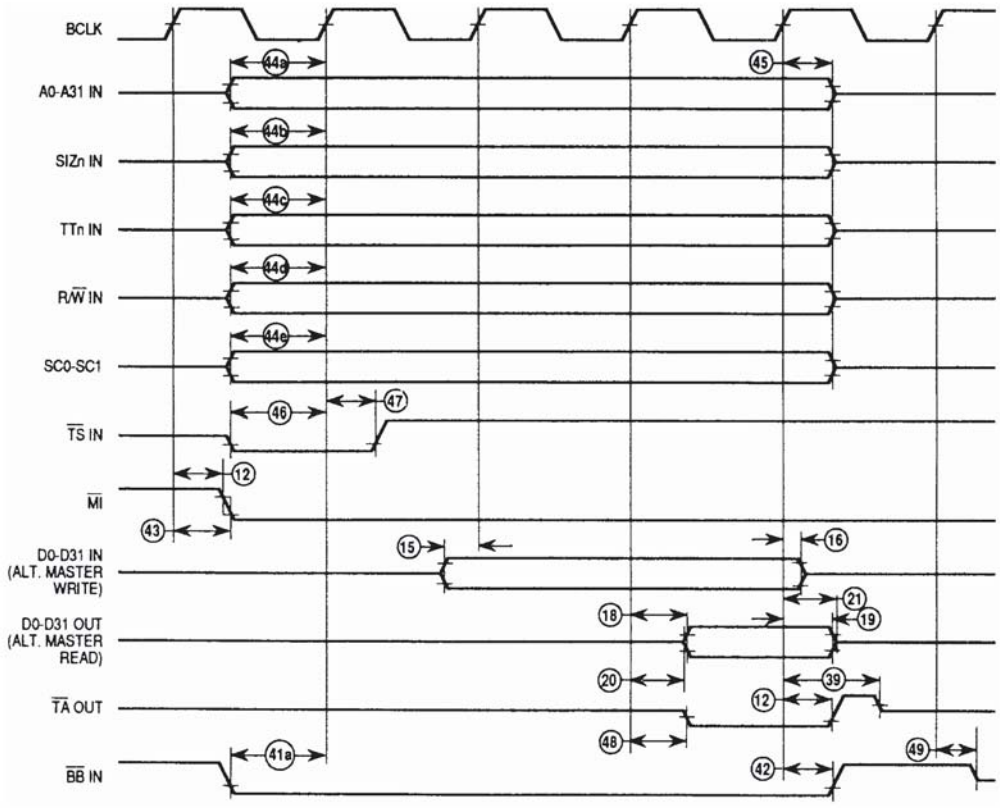


**Figure 14.** Snoop Miss Timing

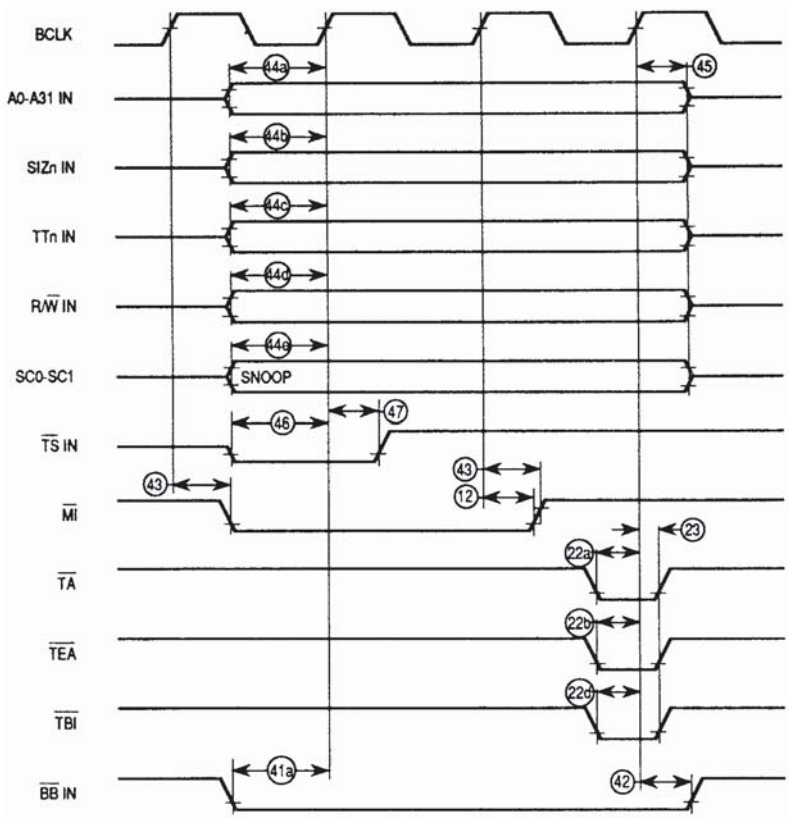
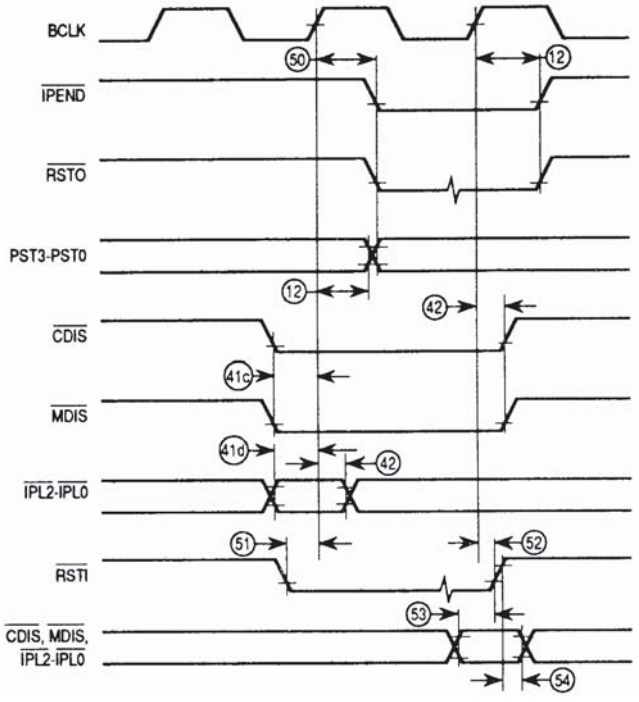



**Figure 15.** Other Signal Timing



registers may be used for word and long-word operations, and all of the 16 general-purpose registers (D0-D7, A0-A7 in Figure 20) may be used as index registers.

The eight, 80-bit, floating-point data registers (FP0-FP7) are analogous to the integer data registers (D0-D7) of all TS68000 Family processors. Floating-point data registers always contain extended-precision numbers. All external operands, regardless of the data format, are converted to extended-precision values before being used in any floating-point calculation or stored in a floating-point data register.

The program counter (PC) usually contains the address of the instruction being executed by the TS68040. During instruction execution and exception processing, the processor automatically increments the contents of the PC or places a new value in the PC, as appropriate. The status register (SR in the supervisor programming model) contains the condition codes that reflect the results of a previous operation and can be used for conditional instruction execution in a program. The lower byte of the SR is accessible in user mode as the condition code register (CCR). Access to the upper byte of the SR is restricted to the supervisor mode.

As part of exception processing, the vector number of the exception provides an index into the exception vector table. The base address of the exception vector table is stored in the vector base register (VBR). The displacement of an exception vector is added to the value in the VBR when the TS68040 accesses the vector table during exception processing.

Alternate function code registers, SFC and DFC (source and destination), contain 3-bit function codes. Function codes can be considered extensions of the 32-bit linear address. Function codes are automatically generated by the processor to select address spaces for data and program accesses at the user and supervisor modes. The alternate function code registers are used by certain instructions to explicitly specify the function codes for various operations. The cache control register (CACR) controls enabling of the on-chip instruction and data caches of the TS68040.

The supervisor root pointer (SRP) and user root pointer (URP) registers point to the root of the address translation table tree to be used for supervisor mode and user mode accesses. The URP is used if FC2 of the logical address is zero, and the SRP is used if FC2 is one.

The translation control register (TC) enables logical-to-physical address translation and selects either 4K or 8K page sizes. As shown in Figure 20, there are four transparent translation registers - ITT0 and ITT1 for instruction accesses and DTT0 and DTT1 for data accesses. These registers allow portions of the logical address space to be transparently mapped and accessed without the use of resident descriptors in an ATC. The MMU status register (MMUSR) contains status information from the execution of a PTEST instruction. The PTEST instruction searches the translation tables for the logical address as specified by this instruction’s effective address field and the DFC.

The 32-bit floating-point control register (FPCR) contains an exception enable byte that enables disables traps for each class of floating-point exceptions and a mode byte that sets the user-selectable modes. The FPCR can be read or written to by the user and is cleared by a hardware reset or a restore operation of the null state. When cleared, the FPCR provides the IEEE 754 standard defaults. The floating-point status register (FPSR) contains a condition code byte, quotient bits, an exception status byte, and an accrued exception byte. All bits in the FPSR can be read or written by the user. Execution of most floating-point instructions modifies this register.

**Table 19.** Addressing Modes

| Addressing Modes | Syntax |
|---|---|
| Register Direct | |
| Date Register Direct | Dn |
| Address Register Direct | An |
| Register Indirect | |
| Address Register Indirect | (An) |
| Address Register Indirect With Postincrement | (An) |
| Address Register Indirect With Predecrement | (An) |
| Address Register Indirect With Displacement | ($d_{16}$, An) |
| Register Indirect With Index | |
| Address Register Indirect With Index (8-bit Displacement) | ($d_8$, An, Xn) |
| Address Register Indirect With Index (Base Displacement) | (bd, An, Xn) |
| Memory Indirect | |
| Memory Indirect Postincrement | ([bd, An], Xn, od) |
| Memory Indirect Preindexed | ([bd, An, Xn], od) |
| Program Counter Indirect With Displacement | ($d_{16}$, PC) |
| Program Counter Indirect With Index | |
| PC Indirect With Index (8-bit Displacement) | ($d_8$, PC, Xn) |
| PC Indirect With Index (Base Displacement | (bd, PC, Xn) |
| Program Counter Memory Indirect | |
| PC Memory Indirect Postindexed | ([bd, PC], Xn, od) |
| PC Memory Indirect Preindexed | ([bd, PC, Xn], od) |
| Absolute | |
| Absolute Short | xxx.W |
| Absolute Long | xxx.L |
| Immediate | # (data) |

Note:

DN = Data register, D0-D7

AN = Address register, A0-A7

$d_8$, $d_{16}$ = A twos-complement or sign-extended displacement; added as part of the effective address calculation; size is 8 ($d_8$) or 16 ($d_{16}$) bits; when omitted, assemblers use a value of zero.

Xn = Address or data register used as an index register; form is Xn, SIZE*SCALE, where SIZE is W or L (indicates index register size) and SCALE is 1, 2, 4 or 8 (index register os multiplied by SCALE); use of SIZE and or SCALE is optional.

bd = A twos-complement base displacement; when present, size can be 16 or 32 bits.

od = Outer displacement added as part of effective address calculation after any memory indirection; use is optional with a size of 16 or 32 bits.

PC = Program counter.

(data) = Immediate value of 8, 16 or 32 bits.

( ) = Effective address.

[ ] = Used as indirect address to long-word address.

## Instruction and Data Caches

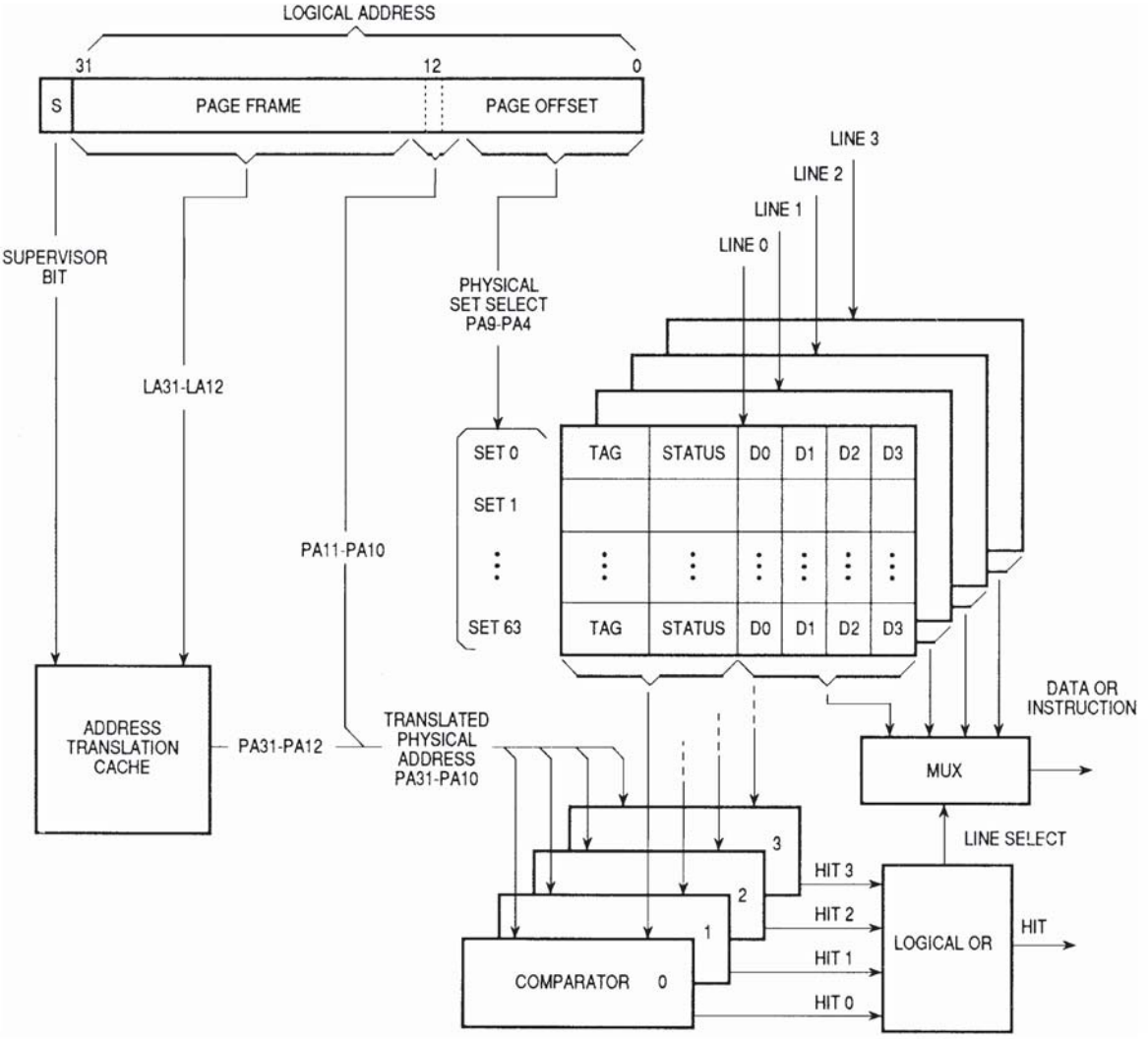
Studies have shown that typical programs spend much of their execution time in a few main routines or tight loops. Earlier members of the TS68000 Family took advantage of this locality of reference phenomenon to varying degrees. The TS68040 takes further advantage of cache technology with its two, independent, on-chip, physical address space caches, one for instructions and one for data. The caches reduce the processor's external bus activity and increase CPU throughput by lowering the effective memory access time. For a typical system design, the large caches of the TS68040 yield a very high hit rate, providing a substantial increase in system performance. Additionally, the caches are automatically burstfilled from the external bus whenever a cache miss occurs.

The autonomous nature of the caches allows instruction-stream fetches, data-stream fetches, and a third external access to occur simultaneously with instruction execution. For example, if the TS68040 requires both an instruction-stream access and an external peripheral access and if the instruction is resident in the on-chip cache, the peripheral access proceeds unimpeded rather than being queued behind the instruction fetch. If a data operand is also required and if it is resident in the data cache, it can also be accessed without hindering either the instruction access from its cache or the peripheral access external to the chip. The parallelism inherent in the TS68040 also allows multiple instructions that do not require any external accesses to execute concurrently while the processor is performing an external access for a previous instruction.

### Cache Organization

The instruction and data caches are four-way set-associative with 64 sets of four, 16-byte lines for a total cache storage of 4K bytes each. As shown in Figure 21, each 16-byte line contains an address tag and state information. State information for each entry consists of a valid flag for the entire line in both instruction and data caches and write status for each long word in the data cache. The write status in the data cache signifies whether or not the long-word data is dirty (meaning that the data in the cache has been modified but has not been written back to external memory) for data in copyback pages.

**Figure 21.** Cache Organization Overview




The caches are accessed by physical addresses from the on-chip MMUs. The translation of the upper bits of the logical address occurs concurrently with the accesses into the set array in the cache by the lower address bits. The output of the ATC is compared with the tag field in the cache to determine if one of the lines in the selected set matches the translated physical address. If the tag matches and the entry is valid, then the cache has a hit.

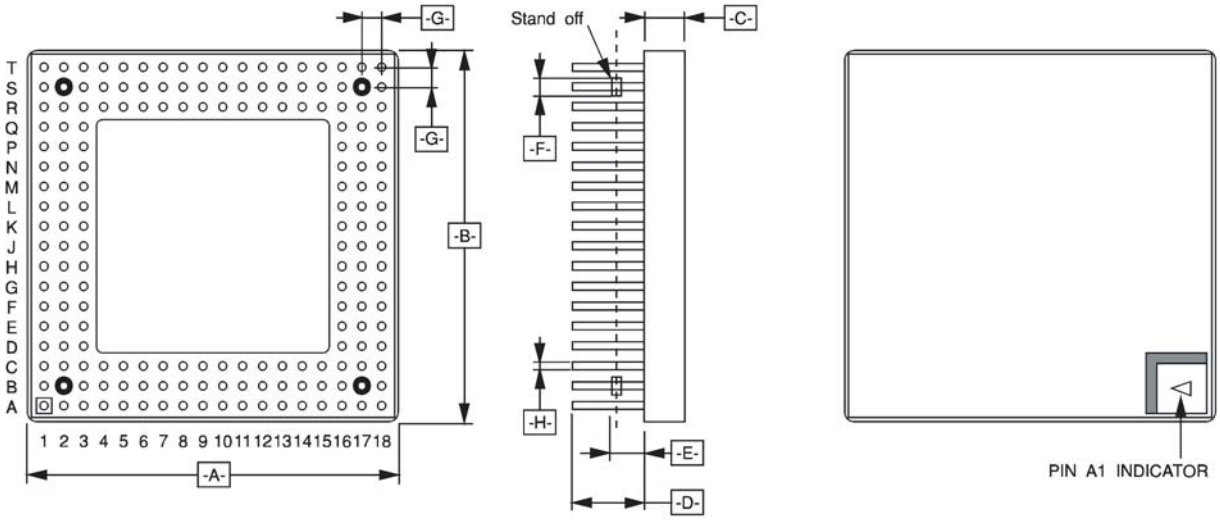
If the cache hits and the access is a read, the appropriate long word from the cache line is multiplexed onto the appropriate internal bus. If the cache hits and the access is a write, the data, regardless of size, is written to the appropriate portion of the corresponding longword entry in the cache.

When a data cache miss occurs and a previously valid cache line is needed to cache the new line, any dirty data in the old line will be internally buffered and copied back to memory after the new cache line has been loaded.

Pushing of dirty data can be forced by the CPUSH instruction.

# Package Mechanical Data

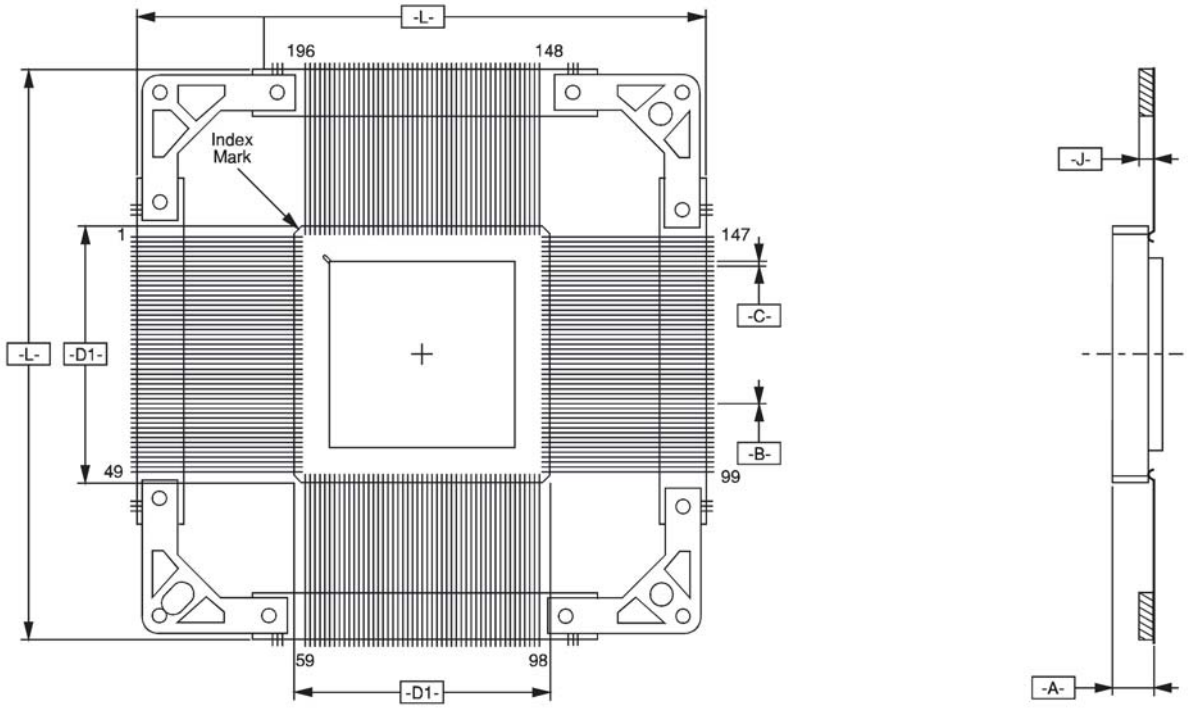
## 179 pins – PGA




| Dim | Millimeters | | Inches | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| A | 46.863 | 47.625 | 1.845 | 1.875 |
| B | 46.863 | 47.625 | 1.845 | 1.875 |
| C | 2.3876 | 1.875 | 0.094 | 0.116 |
| D | 4.318 | 4.826 | 0.170 | 0.190 |
| E | 1.143 | 1.4 | 0.045 | 0.055 |
| F | 1.143 | 1.4 | 0.045 | 0.055 |
| G | 2.54 BSC | | 0.100 BSC | |
| H(1) | 0.432 | 0.483 | 0.017 | 0.019 |

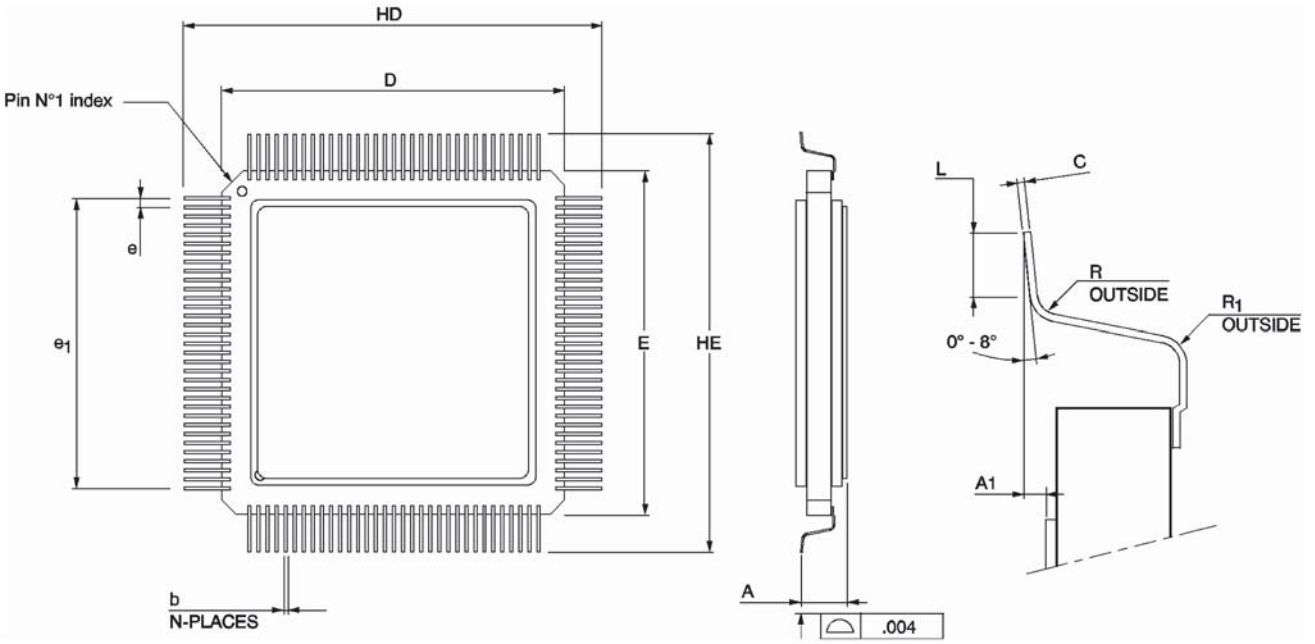
Note: 1. For untinned leads (gold)

## 196 pins – Tie Bar CQFP
## Cavity Up (on request)




| Dim | Millimeters | Inches |
|---|---|---|
| A | 3.30 max | 0.130 max |
| B | 0.23 +0.05<br>0.23 -0.038 | 0.009 +0.002<br>0.009 -0.015 |
| C | 0.635 typ. | .025 typ. |
| D1 | 33.91 ± 0.25 | 1.335 ± 0.01 |
| J | 0.89 ± 0.13 | 0.035 ± 0.005 |
| L | 63.5 ± 0.51 | 2.5 ± 0.02 |

## 196 pins – Gullwing
## CQFP cavity up

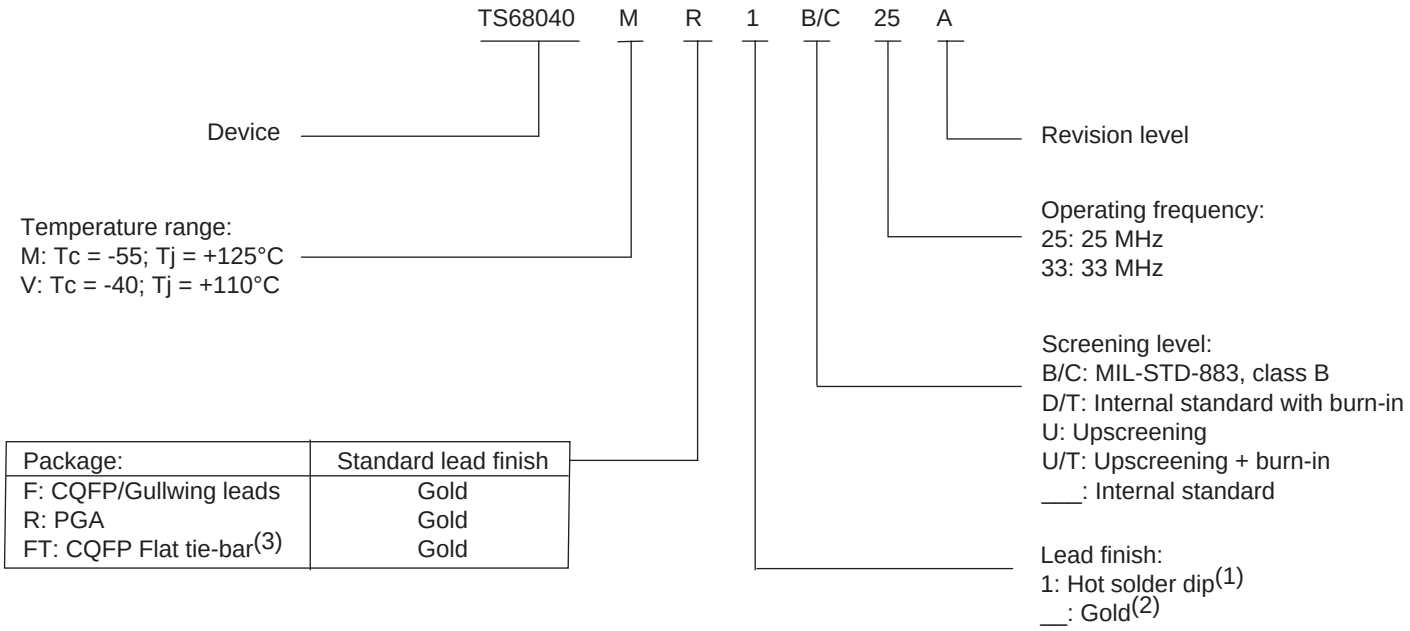



* Reduce pin count shown for clarity, 49 pins per side

| Symbol | Millimeters | Inches |
|---|---|---|
| A | 4.19 max | 0.165 max |
| A1 | 0.673 ± 0.2 | .0265 ±.008 |
| b | 0.23 +0.05<br>0.23 -0.038 | .009 +.002<br>.009 -.0015 |
| c | 0.127 +0.05<br>0.127 -0.025 | .005 +.002<br>.005 -.001 |
| D/E | 33.91 ±0.25 | 1.335 ±.01 |
| e | .635 BSC | .025 BSC |
| e1 | 30.48 ±0.13 | 1.2 ±.005 |
| HD/HE | 38.8 ±0.18 | 1.528 ±.007 |
| L | 0.813 ±0.2 | .032 ±.008 |
| N | 196 | 196 |
| R | 0.55 ±0.25 | .022 ±.01 |
| R1 | 0.23 min | .009 min |

# Ordering Information

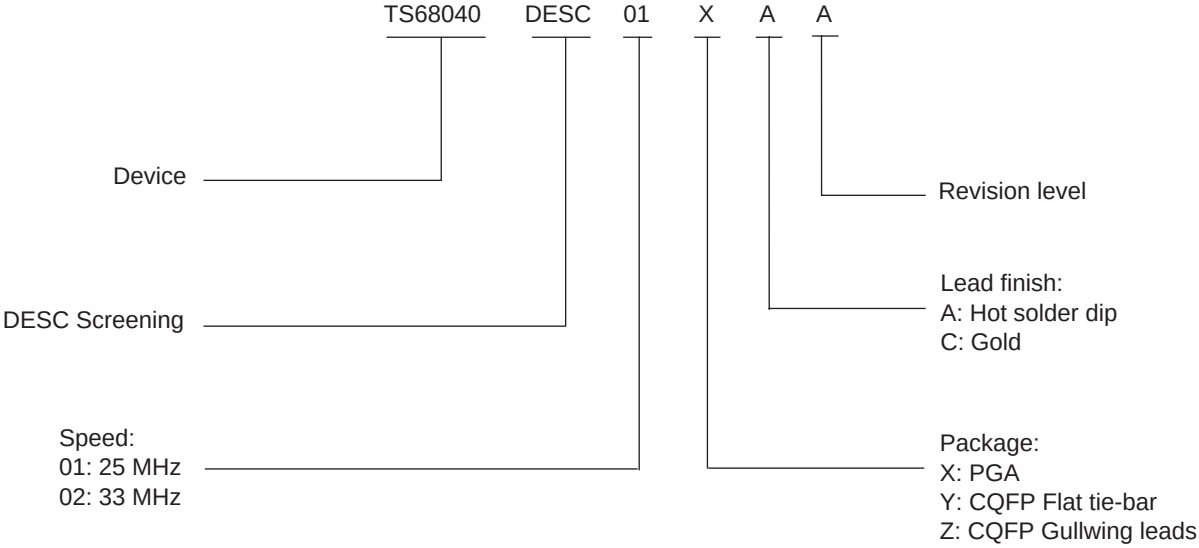
## MIL-STD-883 C and Internal Standard




| Package: | Standard lead finish |
|---|---|
| F: CQFP/Gullwing leads | Gold |
| R: PGA | Gold |
| FT: CQFP Flat tie-bar(3) | Gold |

Notes: 1. On request.
2. Standard process.
3. Non request for small quantity.

## DESC Drawing 5962-93143



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