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Understanding Embedded - Microprocessors

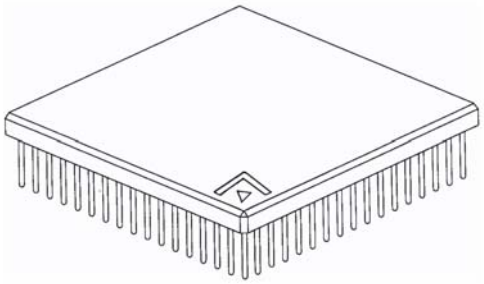
Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	68000
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	25MHz
Co-Processors/DSP	-
RAM Controllers	-
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	5.0V
Operating Temperature	-40°C ~ 110°C (TC)
Security Features	-
Package / Case	179-PGA
Supplier Device Package	179-PGA (47.24x47.24)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/ts68040vr25a

R suffix
PGA 179
Ceramic Pin Grid Array
Cavity Down



F suffix
CQFP 196
Gullwing Shape Lead
Ceramic Quad Fla Pack

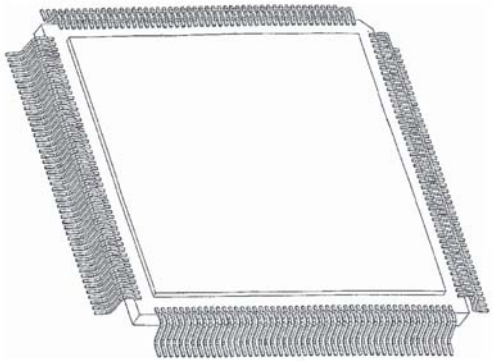
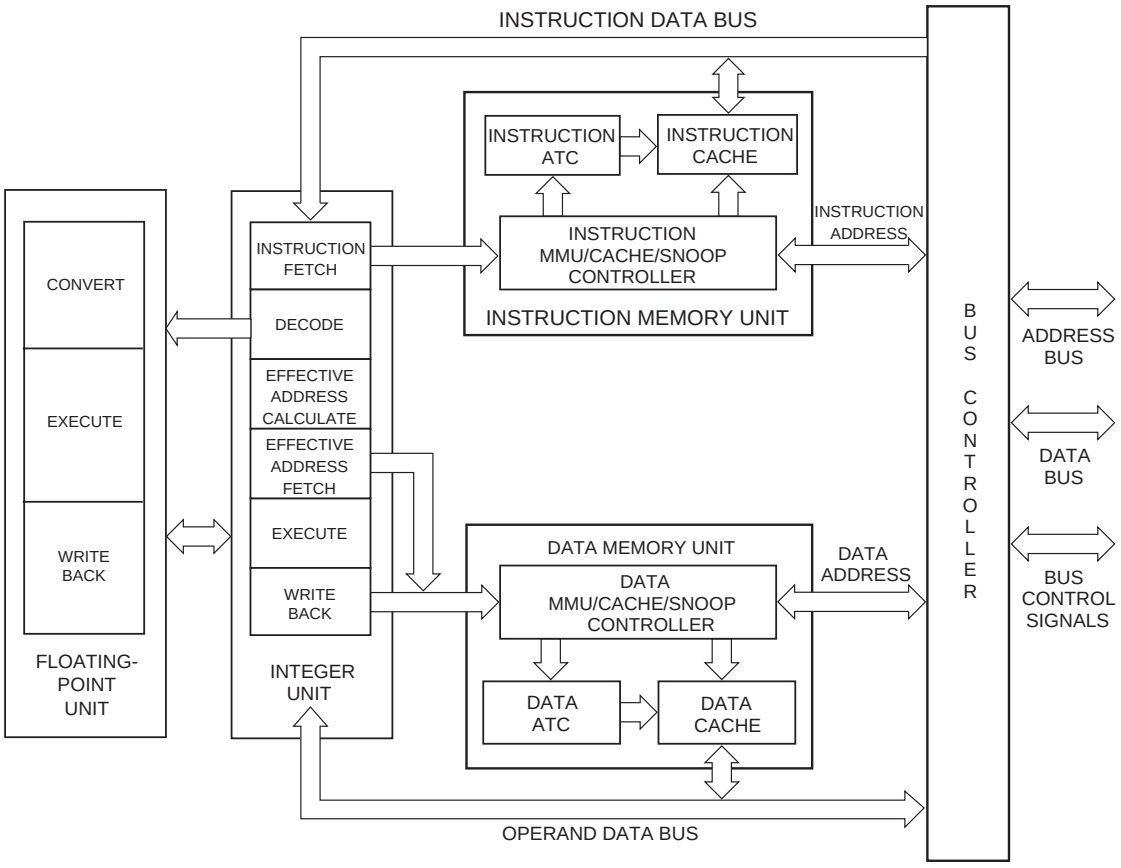


Figure 1. Block Diagram



Pin Assignments

PGA 179

Figure 2. Bottom View

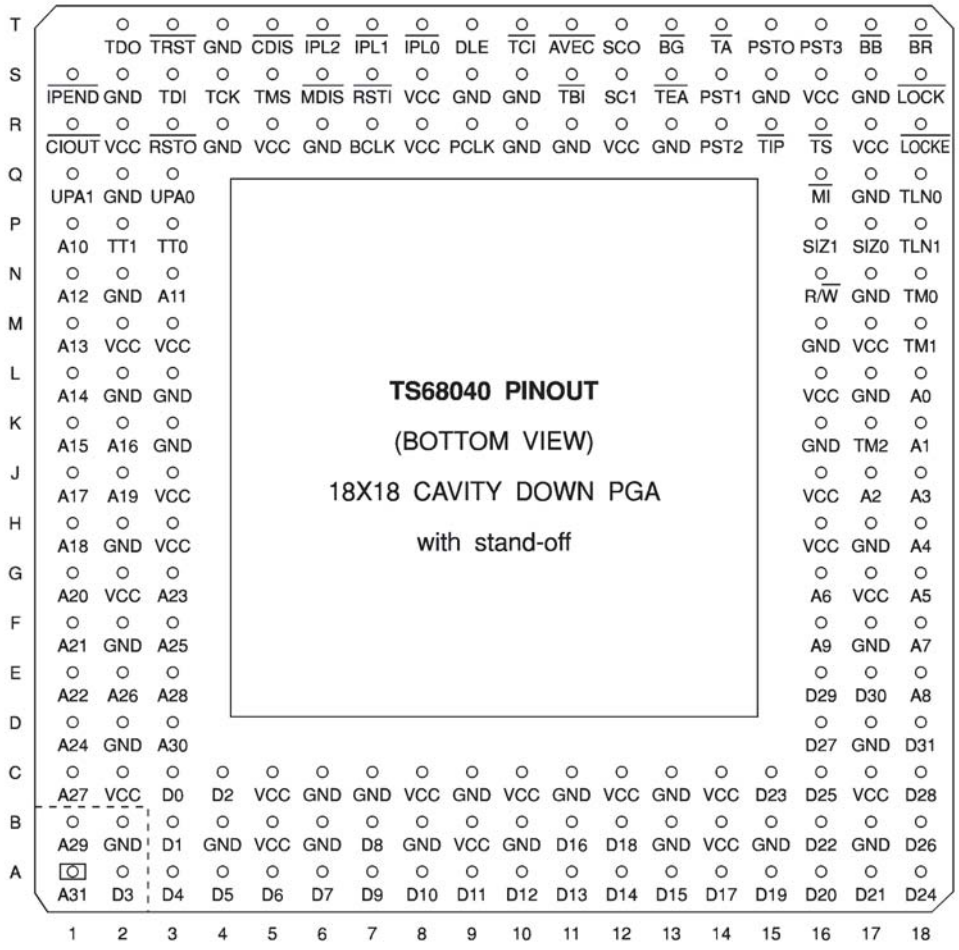


Table 1. Power Supply Affectation to PGA Body

	GND	V_{CC}
PLL		S8
Internal Logic	C6, C7, C9, C11,C13, K3, K16, L3, M16, R4, R11, R13, S10, T4, S9, R6, R10	C5, C8, C10, C12, C14, H3, H16, J3, J16, L16, M3, R5, R12, R8
Output Drivers	B2, B4, B6, B8, B10, B13, B15, B17, D2, D17, F2, F17, H2, H17, L2, L17, N2, N17, Q2, Q17, S2, S15, S17	B5, B9, B14, C2, C17, G2, G17, M2, M17, R2, R17, S16

CQFP 196

Figure 3. Pin Assignments

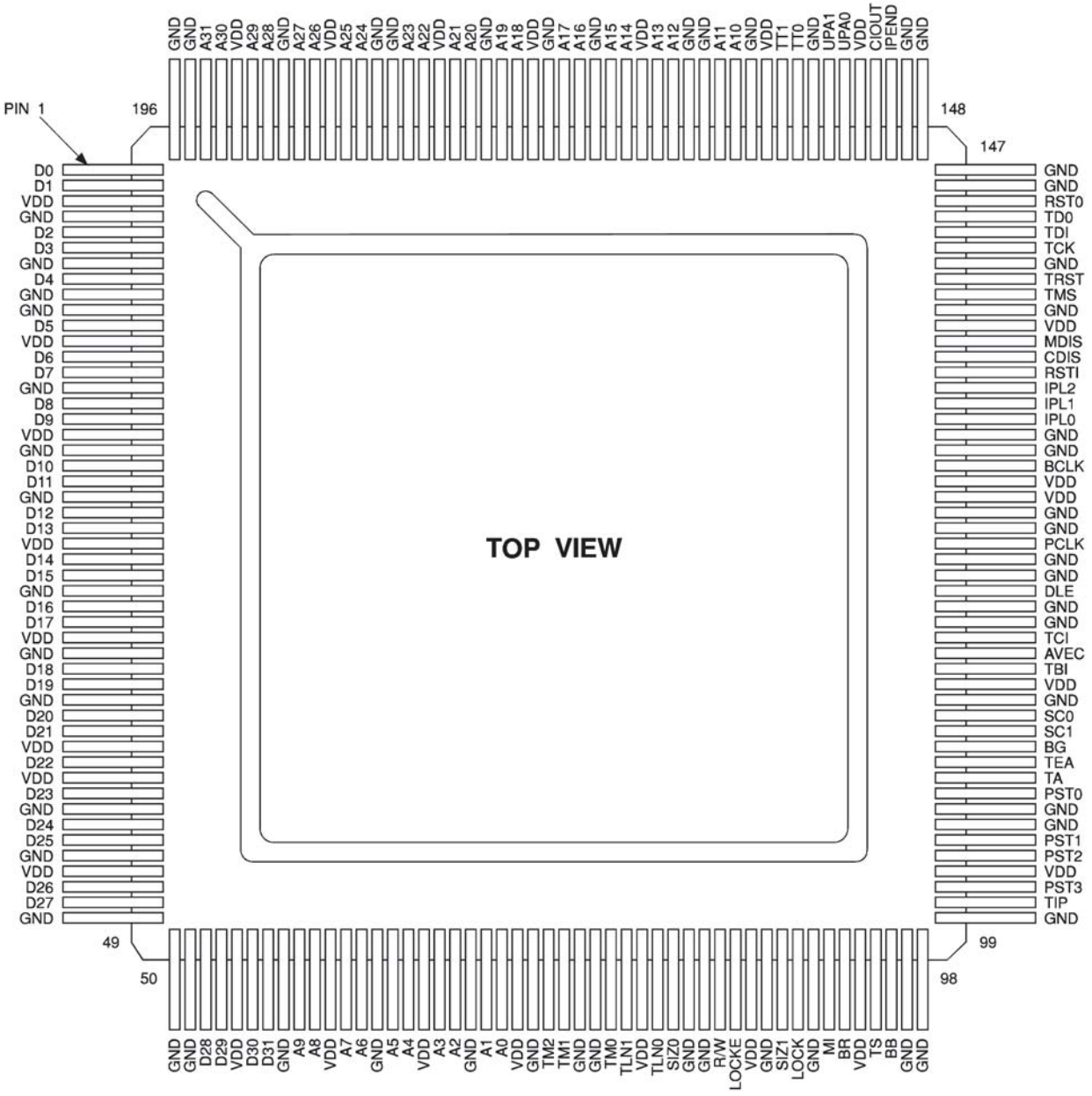


Table 2. Power Supply Affectation to CQFP Body

	GND	**V_{CC}**
PLL		127
Internal Logic	4, 9, 10, 19, 32, 45, 73, 88, 113, 119, 121, 122, 124, 125, 129, 130, 141, 159, 172	3, 18, 31, 40, 46, 60, 72, 87, 114, 126, 137, 158, 173, 186
Output Drivers	7, 15, 22, 28, 35, 42, 49, 50, 51, 57, 63, 69, 76, 77, 83, 84, 91, 97, 98, 99, 105, 106, 146, 147, 148, 149, 155, 162, 163, 169, 176, 182, 183, 189, 195, 196	12, 25, 38, 54, 66, 80, 94, 102, 152, 166, 179, 192

Signal Description

Figure 4 and Table 3 describe the signals on the TS68040 and indicate signal functions. The test signals, $\overline{TRST}$, TMS, TCK, TDI, and TDO, comply with subset P-1149.1 of the IEEE testability bus standard.

Figure 4. Functional Signal Groups

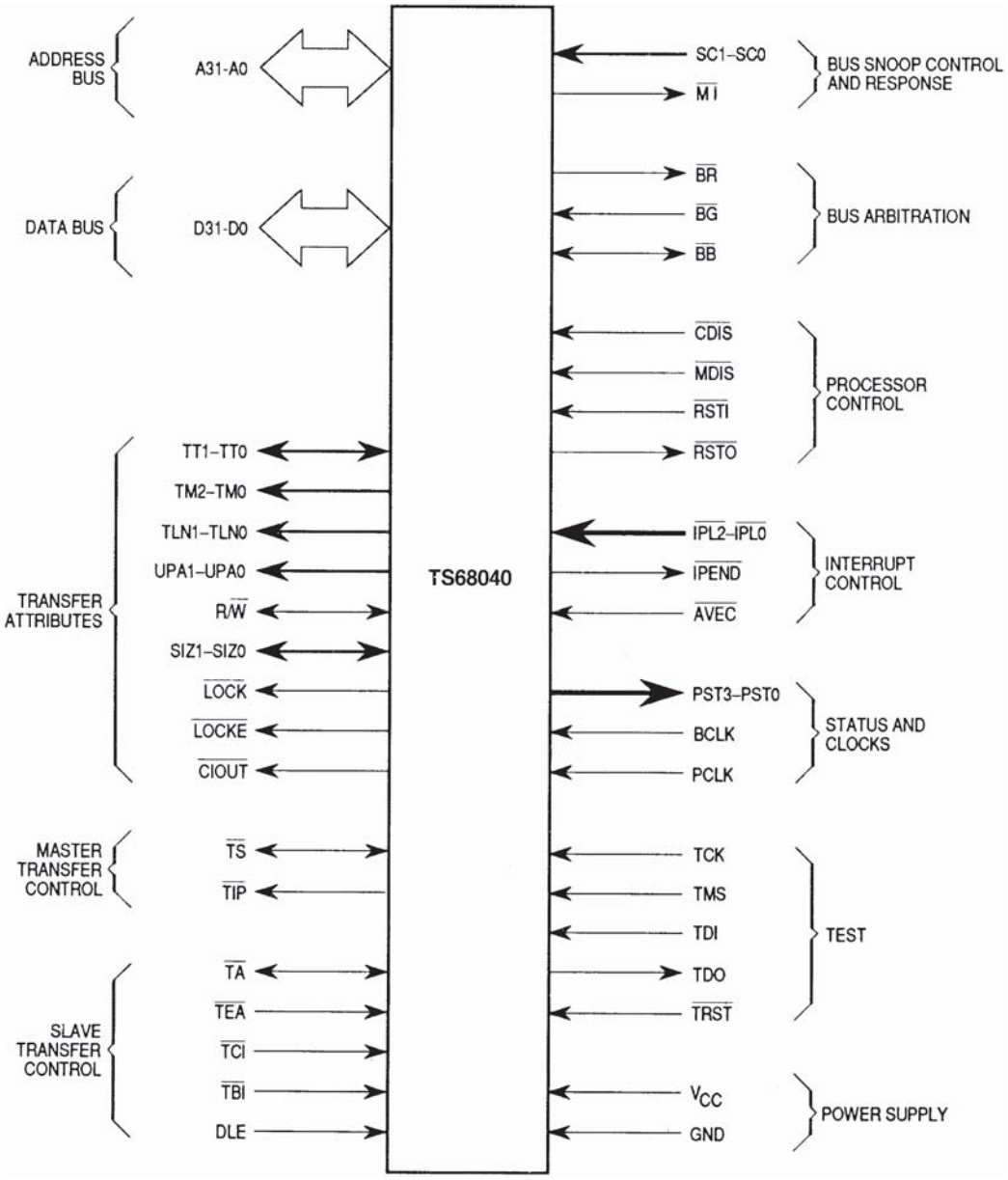


Table 3. Signal Index (Continued)

Signal Name	Mnemonic	Function
Bus Clock	BCLK	Clock input used to derive all bus signal timing
Processor Clock	PCLK	Clock input used for internal logic timing. The PCLK frequency is exactly 2X the BCLK frequency
Test Clock	TCK	Clock signal for the IEEE P1149.1 test access port (TAP)
Test Mode Select	TMS	Selects the principle operations of the test-support circuitry
Test Data Input	TDI	Serial data input for the TAP
Test Data Output	TDO	Serial data output for the TAP
Test Reset	$\overline{\text{TRST}}$	Provides an asynchronous reset of the TAP controller
Power Supply	V_{CC}	Power supply
Ground	GND	Ground connection

Scope

This drawing describes the specific requirements for the microprocessor TS68040 - 25 MHz and 33 MHz, in compliance with MIL-STD-883 class B or Atmel standard screening.

Applicable Documents

MIL-STD-883

1. MIL-STD-883: test methods and procedures for electronics.
2. MIL-I-38535: general specifications for microcircuits.
3. DESC 5962-93143.

Requirements

General

The microcircuits are in accordance with the applicable document and as specified herein.

Design and Construction

Terminal Connections

See Figure 2 and Figure 3.

Lead Material and Finish

Lead material and finish shall be as specified in MIL-STD-883 (see enclosed “MIL-STD-883 C and Internal Standard” on page 46).

Package

The macro circuits are packaged in hermetically sealed ceramic packages which conform to case outlines of MIL-STD-1835-or as follow:

- CMGA 10-179-PAK pin grid array, but see “179 pins – PGA” on page 43.
- Similar to CQCC1-F196C-U6 ceramic uniform lead chip carrier package with ceramic nonconductive tie-bar but use Atmel’s internal drawing, see “196 pins – Tie Bar CQFP Cavity Up (on request)” on page 44.
- Gullwing shape CQFP see “196 pins – Gullwing CQFP cavity up” on page 45.

The precise case outlines are described at the end of the specification (See “Package Mechanical Data” on page 43.) and into MIL-STD-1835.

Electrical Characteristics

Absolute Maximum Ratings Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

Table 4. Absolute Maximum Ratings

Symbol	Parameter	Condition	Min	Max	Unit
V_{CC}	Supply Voltage Range		-0.3	7.0	V
V_I	Input Voltage Range		-0.3	7.0	V
P_D	Power Dissipation	Large buffers enabled		7.7	W
		Small buffers enabled		6.3	W
T_C	Operating Temperature		-55	T_J	°C
T_{stg}	Storage Temperature Range		-65	+150	°C
T_J	Junction Temperature(1)			+125	°C
T_{lead}	Lead Temperature	Max.10 sec soldering		+300	°C

Note: 1. This device is not tested at TC = +125°C. Testing is performed by setting the junction temperature Tj = +125°C and allowing the case and ambient temperatures to rise and fall as necessary so as not to exceed the maximum junction temperature.

Table 5. Recommended Conditions of Use
Unless otherwise stated, all voltages are referenced to the reference terminal

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage Range		+4.75		+5.25	V
V_{IL}	Logic Low Level Input Voltage Range		GND - 0.3		0.8	V
V_{IH}	Logic High Level Input Voltage Range		+2.0		V_{CC} + 0.3	V
V_{OH}	High Level Output Voltage		2.4			V
V_{OL}	Low Level Output Voltage				0.5	V
f_c	Clock Frequency	-25 MHz Version		25		MHz
		-33 MHz Version		33		MHz
T_C	Case Operating Temperature Range(1)		-55		T_{Jmax}	°C
T_J	Maximum Operating Junction Temperature				+125	°C

Note: 1. This device is not tested at TC = +125°C. Testing is performed by setting the junction temperature T_J = +125°C and allowing the case and ambient temperatures to rise and fall as necessary so as not to exceed the maximum junction temperature.

To calculate the specific power dissipation of a specific design, the termination method of each signal must be considered. For example, a signal output that is not connected would not dissipate any additional power if it were configured in the large buffer rather than the small buffer mode.

Relationships Between Thermal Resistances and Temperatures

Since the maximum operating junction temperature has been specified to be 125°C. The maximum case temperature, TC, in °C can be obtained from:

$$T_C = T_J - P_D \cdot \Phi_{JC} \quad (2)$$

where:

T_C = Maximum case temperature

T_J = Maximum junction temperature

P_D = Maximum power dissipation of the device

Φ_{JC} = Thermal resistance between the junction of the die and the case

In general, the ambient temperature, T_A, in °C is a function of the following formula:

$$T_A = T_J - P_D \cdot \Phi_{JC} - P_D \cdot \Phi_{CA} \quad (3)$$

Where the thermal resistance from case to ambient, Φ_{CA}, is the only user-dependent parameter once a buffer output configuration has been determined. As seen from equation (3), reducing the case to ambient thermal resistance increases the maximum operating ambient temperature. Therefore, by utilizing such methods as heat sinks and ambient air cooling to minimize the Φ_{CA}, a higher ambient operating temperature and/or a lower junction temperature can be achieved.

However, an easier approach to thermal evaluation uses the following formulas:

$$T_A = T_J - P_D \cdot \Phi_{JA} \quad (4)$$

or alternatively,

$$T_J = T_A - P_D \cdot \Phi_{JA} \quad (5)$$

where:

Φ_{JA} = thermal resistance from the junction to the ambient ($\Phi_{JC} + \Phi_{CA}$).

This total thermal resistance of a package, Φ_{JA}, is a combination of its two components, Φ_{JC} and Φ_{CA}. These components represent the barrier to heat flow from the semiconductor junction to the package (case) surface (Φ_{JC}) and from the case to the outside ambient (Φ_{JC}). Although Φ_{JC} is device related and cannot be influenced by the user, Φ_{CA} is user dependent. Thus, good thermal management by the user can significantly reduce Φ_{CA} achieving either a lower semiconductor junction temperature or a higher ambient operating temperature.

Thermal Management Techniques

To attain a reasonable maximum ambient operating temperature, a user must reduce the barrier to heat flow from the semiconductor junction to the outside ambient (Φ_{JA}). The only way to accomplish this is to significantly reduce Φ_{CA} by applying such thermal management techniques as heat sinks and ambient air cooling.

The following paragraphs discuss some results of a thermal study of the TS68040 device without using any thermal management techniques; using only air-flow cooling, using only a heat sink, and using heat sink combined with air-flow cooling.

Table 9. Thermal Parameters With Heat Sink and No Air Flow

Thermal Mgmt. Technique	Defined Parameters			Measured	Calculated		
Heat Sink	P_D	T_J	Φ_{JC}	Φ_{JA}	Φ_{CA}	T_C	T_A
2338B	3W	125°C	1°C/W	14°C/W	13°C/W	122°C	83°C
2338B	5W	125°C	1°C/W	14°C/W	13°C/W	120°C	55°C

Thermal Characteristics with a Heat Sink and Forced Air

A sample size of three TS68040 packages was tested in forced-air cooling in a wind tunnel with a heat sink. This test was performed with 3W of power being dissipated from within the package. As mentioned previously, the variance in Φ_{JA} within the possible power range is negligible; it can be assumed for calculation purposes that Φ_{JA} is valid at all power levels. Table 10 shows the results, assuming a maximum power dissipation at 3 and 5W with air flow and heat sink thermal management (refer to Table 6 to calculate other power dissipation values).

Table 10. Thermal Parameters with Heat Sink and Air Flow

Thermal Mgmt. Technique		Defined Parameters			Measured	Calculated		
Air-flow	Heat sink	P_D	T_J	Φ_{JC}	Φ_{JA}	Φ_{CA}	T_C	T_A
100 LFM	2338B	3W	125°C	1°C/W	3.1°C/W	2.1°C/W	122°C	115.7°C
250 LFM	2338B	3W	125°C	1°C/W	2.2°C/W	1.2°C/W	122°C	118.4°C
500 LFM	2338B	3W	125°C	1°C/W	1.7°C/W	0.7°C/W	122°C	119.9°C
750 LFM	2338B	3W	125°C	1°C/W	1.5°C/W	0.5°C/W	122°C	120.5°C
1000 LFM	2338B	3W	125°C	1°C/W	1.4°C/W	0.4°C/W	122°C	120.8°C
100 LFM	2338B	5W	125°C	1°C/W	3.1°C/W	2.1°C/W	120°C	109.5°C
250 LFM	2338B	5W	125°C	1°C/W	2.2°C/W	1.2°C/W	120°C	114°C
500 LFM	2338B	5W	125°C	1°C/W	1.7°C/W	0.7°C/W	120°C	116.5°C
750 LFM	2338B	5W	125°C	1°C/W	1.5°C/W	0.5°C/W	120°C	117.5°C
1000 LFM	2338B	5W	125°C	1°C/W	1.4°C/W	0.4°C/W	120°C	118°C

Thermal Testing Summary

Testing proved that a heat sink in combination with a relatively small amount of air-flow (100 LFM or less) will easily realize a 0-70°C ambient operating temperature for the TS68040 with almost any configuration of the output buffers. A heat sink alone may be capable of providing all necessary cooling, depending on the particular heat sink height/size restraints, the maximum ambient operating temperature required, and the output buffer configuration chosen. Also forced air cooling alone may attain a 0-70°C ambient operating temperature. However this factor is highly dependent on the output buffer configuration chosen and the available forced air for cooling. Figure 7 is a summary of the test results of the relationship between Φ_{JA} and air-flow for the TS68040.

Figure 7. Relationship of Φ_{JA} Air-Flow for PGA

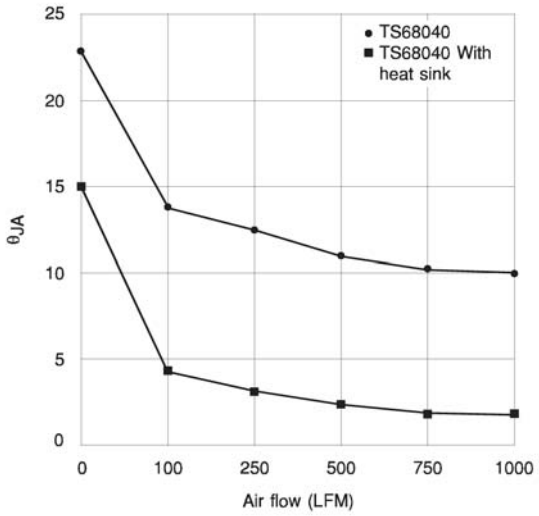


Table 11. Characteristics Guaranteed

Package	Symbol	Parameter	Value	Unit
PGA 179	θ_{J-A}	Thermal Resistance Junction-to-ambient	See Figure 7	°C/W
	θ_{J-C}	Thermal Resistance Junction-to-case	1	°C/W
CQFP 196	θ_{J-A}	Thermal Resistance Junction-to-ambient	TBD	°C/W
	θ_{J-C}	Thermal Resistance Junction-to-case	1	°C/W

Mechanical and Environment

The microcircuits shall meet all mechanical environmental requirements of either MIL-STD-883 for class B devices or for Atmel standard screening.

Marking

The document where are defined the marking are identified in the related reference documents. Each microcircuit are legible and permanently marked with the following information as minimum:

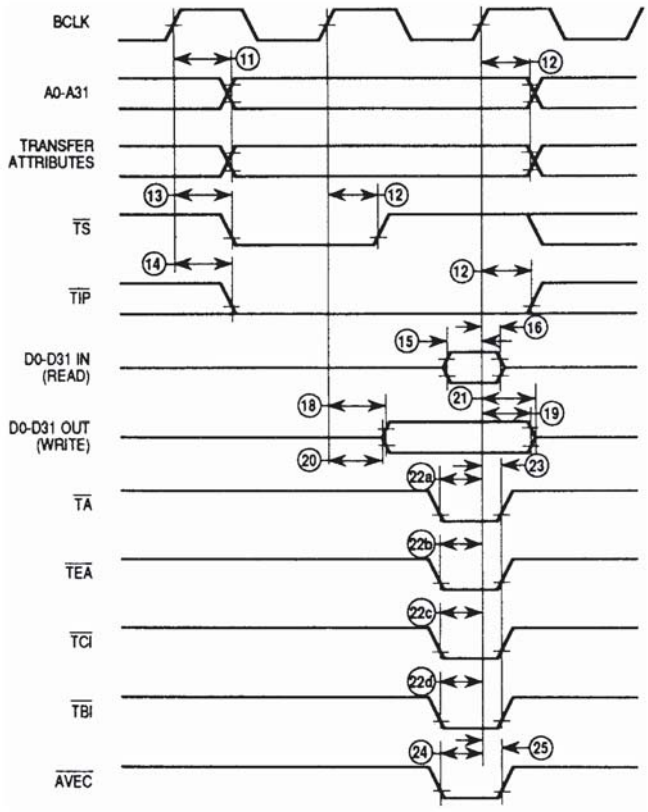
- Atmel Logo
- Manufacturer's Part Number
- Class B Identification
- Date-code Of Inspection Lot
- ESD Identifier If Available
- Country Of Manufacturing

Notes:
1. Output timing is specified for a valid signal measured at the pin. Large buffer timing is specified driving a 50Ω transmission line with a length characterized by a 2.5 ns one-way propagation delay, terminated through 50Ω to 2.5V. Large buffer output impedance is typically 3Ω, resulting in incident wave switching for this environment. Small buffer timing is specified driving an unterminated 30Ω transmission line with a length characterized by a 2.5 ns one-way propagation delay. Small buffer output impedance is typically 30Ω; the small buffer specifications include approximately 5 ns for the signal to propagate the length of the transmission line and back.
2. All testing to be performed using worst-case test conditions unless otherwise specified.
3. The following pins are active low: $\overline{AVEC}$, $\overline{BG}$, $\overline{BS}$, $\overline{BR}$, $\overline{CDIS}$, $\overline{CIOUT}$, $\overline{IPEND}$, $\overline{IPLO}$, $\overline{IPL1}$, $\overline{IPL2}$, $\overline{LOCK}$, $\overline{LOCKE}$, $\overline{MDIS}$, $\overline{MI}$, $\overline{RST0}$, $\overline{RSTI}$, $\overline{TA}$, $\overline{TBI}$, $\overline{TCI}$, $\overline{TEA}$, $\overline{TIP}$, $\overline{TRST}$, $\overline{TS}$ and $\overline{W}$ of R/$\overline{W}$.
4. Maximum operating junction temperature (T_J) = +125°. Minimum case operating temperature (T_C) = -55°. This device is not tested at T_C = +125°. Testing is performed by setting the junction temperature T_J = +125°and allowing the case and ambient temperatures to rise and fall as necessary so as not to exceed the maximum junction temperature.
5. Timing specifications 11, 20 and 38 for address bus output timing apply when normal bus operation is selected. Specifications 26, 27 and 28 should be used when the multiplexed bus mode of operation is enabled.
6. Timing specifications 18 and 19 for data bus output timing apply when normal bus operation is selected. Specifications 28 and 29 should be used when the multiplexed bus mode of operation is enabled.

Table 15. Input AC Timing Specifications (Figure 9 to Figure 15)
-55°C ≤T_C ≤T_{Jmax}; 4.75V ≤V_{CC} ≤5.25V unless otherwise specified(1)(2)(3)(4)

Num	Characteristic	25 MHz		33 MHz		Unit
		Min.	Max.	Min.	Max.	
15	Data-in Valid to BCLK (Setup)	5		4		ns
16	BCLK to Data-in Invalid (Hold)	4		4		ns
17	BCLK to Data-in High Impedance (Read Followed By Write)		49		36.5	ns
22a	$\overline{TA}$ Valid to BCLK (Setup)	10		10		ns
22b	$\overline{TEA}$ Valid to BCLK (Setup)	10		10		ns
22c	$\overline{TCI}$ Valid to BCLK (Setup)	10		10		ns
22d	$\overline{TBI}$ Valid to BCLK (Setup)	11		10		ns
23	BCLK to $\overline{TA}$, $\overline{TEA}$, $\overline{TCI}$, $\overline{TBI}$ Invalid (Hold)	2		2		ns
24	$\overline{AVEC}$ Valid to BCLK (Setup)	5		5		ns
25	BCLK to $\overline{AVEC}$ Invalid (Hold)	2		2		ns
31	DLE Width High	8		8		ns
32	Data-in Valid to DLE (Setup)	2		2		ns
33	DLE to Data-in Invalid (Hold)	8		8		ns
34	BCLK to DLE Hold	3		3		ns
35	DLE High to BCLK	16		12		ns
36	Data-in Valid to BCLK (DLE Mode Setup)	5		5		ns
37	BCLK Data-in Invalid (DLE Mode Hold)	4		4		ns
41a	$\overline{BB}$ Valid to BCLK (Setup)	7		7		ns
41b	$\overline{BG}$ Valid to BCLK (Setup)	8		7		ns
41c	$\overline{CDIS}$, $\overline{MDIS}$ Valid to BCLK (Setup)	10		8		ns
41d	$\overline{IPLn}$ Valid to BCLK (Setup)	4		3		ns
42	BCLK to $\overline{BB}$, $\overline{BG}$, $\overline{CDIS}$, $\overline{IPLn}$, $\overline{MDIS}$ Invalid (Hold)	2		2		ns
44a	Address Valid to BCLK (Setup)	8		7		ns
44b	SIZn Valid BCLK (Setup)	12		8		ns

Figure 9. Read/Write Timing



Note: Transfer attribute signals UPAN, SIZN, TTN, TMN, TLNN, R/$\overline{W}$, $\overline{LOCK}$, $\overline{LOCKE}$, $\overline{CIOUT}$

Table 16. JTAG Timing Application (Figure 16 to Figure 19)
-55°C ≤T_C ≤$T_J$max; 4.75V ≤V_{CC} ≤5.25V unless otherwise specified(1)(2)

Num	Characteristic	Min	Max	Unit
	TCK Frequency	0	10	MHz
1	TCK Cycle Time	100		ns
2	TCK Clock Pulse Width Measured at 1.5V	40		ns
3	TCK Rise and Fall Times	0	10	ns
4	$\overline{TRST}$ Setup Time to TCK Falling Edge	40		ns
5	$\overline{TRST}$ Assert Time	100		ns
6	Boundary Scan Input Data Setup Time	50		ns
7	Boundary Scan Input Data Hold Time	50		ns
8	TCK to Output Data Valid	0	50	ns
9	TCK to Output High Impedance	0	50	ns
10	TMS, TDI Data Setup Time	20		ns
11	TMS, TDI Data Hold Time	5		ns
12	TCK to TDO Data Valid	0	20	ns
13	TCK to TDO High Impedance	0	20	ns

Notes: 1. All testing to be performed using worst-case test conditions unless otherwise specified.
2. Maximum operating junction temperature (T_J) = +125°. Minimum case operating temperature (T_C) = -55°. This device is not tested at T_C = +125°. Testing is performed by setting the junction temperature T_J = +125° and allowing the case and ambient temperatures to rise and fall as necessary so as not to exceed the maximum junction temperature.

Table 17. Boundary Scan Instruction Codes

Bit 2	Bit 1	Bit 0	Instruction Selected	Test Data Register Accessed
0	0	0	Extest	Boundary Scan
0	0	1	Highz	Bypass
0	1	0	Sample/Preload	Boundary Scan
0	1	1	DRVCTLT	Boundary Scan
1	0	0	Shutdown	Bypass
1	0	1	Private	Bypass
1	1	0	DRVCTLS	Boundary Scan
1	1	1	Bypass	Bypass

Switching Test Circuit and Waveforms

Figure 10. Address and Data Bus Timing — Multiplexed Bus Mode

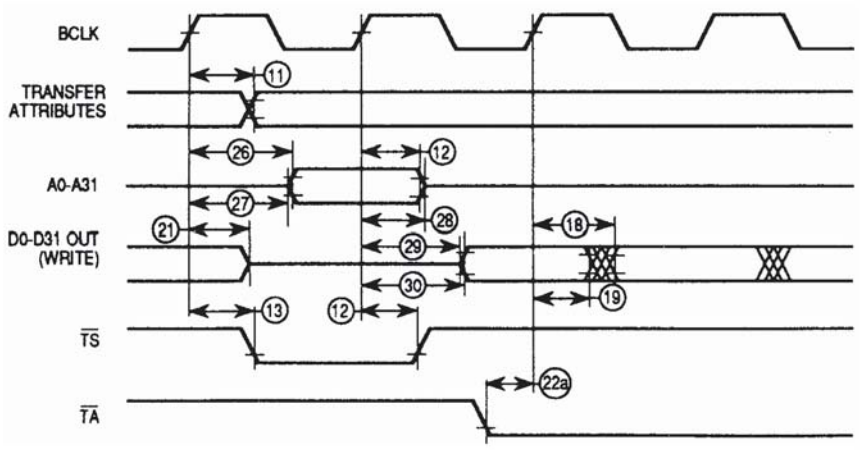


Figure 16. Clock Input Timing Diagram

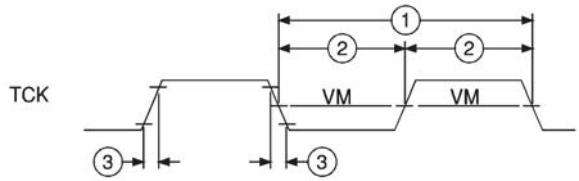


Figure 17. $\overline{\text{TRST}}$ Timing Diagram

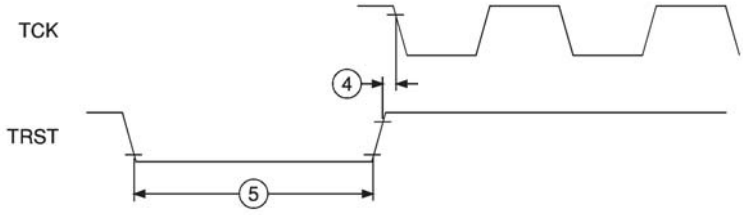
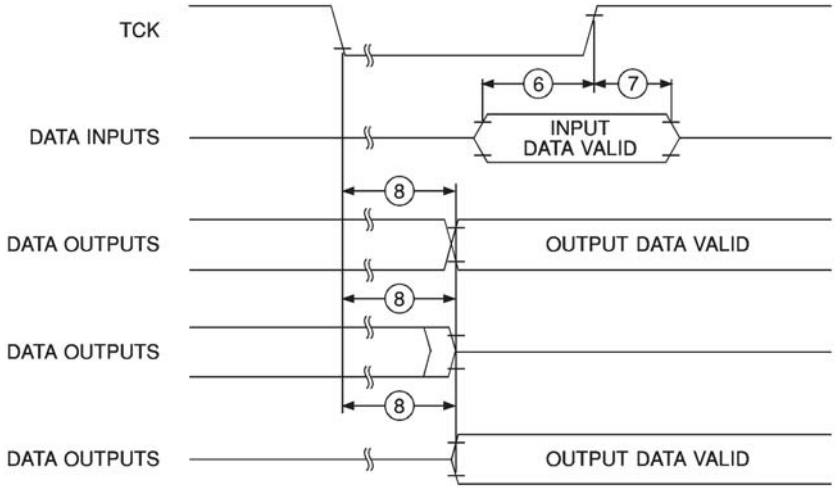


Figure 18. Boundary Scan Timing Diagram



For the subset of the FPU instructions that generate exception traps, the 32-bit floating-point instruction address register (FPIAR) is loaded with the logical address of an instruction before the instruction is executed. This address can then be used by a floating-point exception handler to locate a floating-point instruction that has caused an exception. The move floating-point data register (FMOVE) instruction (to from the FPCR, FPSR, or FPIAR) and the move multiple data registers (FMOVEN) instruction cannot generate floating-point exceptions; therefore, these instructions do not modify the FPIAR. Thus, the FMOVE and FMOVEM instructions can be used to read the FPIAR in the trap handler without changing the previous value.

Figure 20. Programming Model

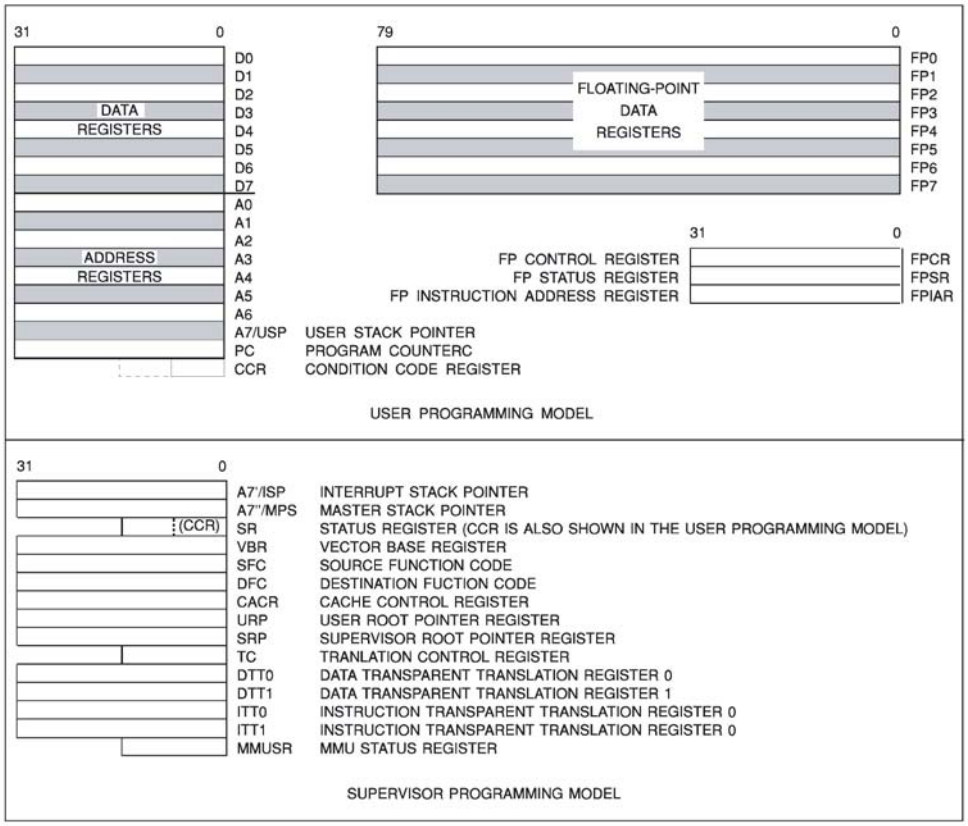


Table 19. Addressing Modes

Addressing Modes	Syntax
Register Direct	
Date Register Direct	Dn
Address Register Direct	An
Register Indirect	
Address Register Indirect	(An)
Address Register Indirect With Postincrement	(An)
Address Register Indirect With Predecrement	(An)
Address Register Indirect With Displacement	(d_{16}, An)
Register Indirect With Index	
Address Register Indirect With Index (8-bit Displacement)	(d_8, An, Xn)
Address Register Indirect With Index (Base Displacement)	(bd, An, Xn)
Memory Indirect	
Memory Indirect Postincrement	([bd, An], Xn, od)
Memory Indirect Preindexed	([bd, An, Xn], od)
Program Counter Indirect With Displacement	(d_{16}, PC)
Program Counter Indirect With Index	
PC Indirect With Index (8-bit Displacement)	(d_8, PC, Xn)
PC Indirect With Index (Base Displacement	(bd, PC, Xn)
Program Counter Memory Indirect	
PC Memory Indirect Postindexed	([bd, PC], Xn, od)
PC Memory Indirect Preindexed	([bd, PC, Xn], od)
Absolute	
Absolute Short	xxx.W
Absolute Long	xxx.L
Immediate	# (data)

Note:

DN = Data register, D0-D7

AN = Address register, A0-A7

d_8, d_{16} = A twos-complement or sign-extended displacement; added as part of the effective address calculation; size is 8 (d_8) or 16 (d_{16}) bits; when omitted, assemblers use a value of zero.

Xn = Address or data register used as an index register; form is Xn, SIZE*SCALE, where SIZE is W or L (indicates index register size) and SCALE is 1, 2, 4 or 8 (index register os multiplied by SCALE); use of SIZE and or SCALE is optional.

bd = A twos-complement base displacement; when present, size can be 16 or 32 bits.

od = Outer displacement added as part of effective address calculation after any memory indirection; use is optional with a size of 16 or 32 bits.

PC = Program counter.

(data) = Immediate value of 8, 16 or 32 bits.

( ) = Effective address.

[ ] = Used as indirect address to long-word address.

The instruction provided by the TS68040 are listed in Table 20. The instruction set has been tailored to support high-level languages and is optimized for those instructions most commonly executed (however, all instructions listed are fully supported). Many instructions operate on bytes, words, and long words, and most instructions can use any of the addressing modes of Table 19.

Table 20. Instruction Set Summary

Mnemonic	Description
ABCD	Add Decimal With Extend
ADD	Add
ADDA	Add Address
ADDI	Add Immediate
ADDQ	Add Quick
ADDX	Add With Extend
AND	Logical AND
ANDI	Logical AND Immediate
ASL, ASR	Arithmetic Shift Left And Right
Bcc	Branch Conditionally
BCHG	Test Bit And Change
BCLR	Test Bit And Clear
BFCHG	Test Bit Field And Change
BFCLR	Test Bit Field And Clear
BFEXTS	Signed Bit Field Extract
BFEXTU	Unsigned Bit Field Extract
BFFFO	Bit Field Find First One
BFINS	Bit Field Insert
BFSET	Test Bit Field And Set
BFTST	Test Bit Field
BKPT	Breakpoint
BRA	Branch
BSET	Test Bit And Set
BSR	Branch To Subroutine
BTST	Test Bit
CAS	Compare And Swap Operands
CAS2	Compare And Swap Dual Operands
CHK	Check Register Against Bounds
CHK2	Check Register Against Upper And Lower Bounds
CINV(1)	Invalidate Cache Entries
CLR	Clear
CMP	Compare
CMPA	Compare Address
CMPI	Compare Immediate
CMPM	Compare Memory To Memory
CMP2	Compare Register Against Upper And Lower Bounds
CPUSH(1)	Push Then Invalidate Cache Entries
DB_{CC}	Test Condition, Decrement And Branch
DIVS, DIVSL	Signed Divide
DIVU, DIVUL	Unsigned Divide
EOR	Logical Exclusive OR
EORI	Logical Exclusive OR Immediate
EXG	Exchange Registers
EXT, EXTB	Sign Extend

Table 20. Instruction Set Summary (Continued)

Mnemonic	Description
SBCD	Substract Decimal With Extend
Scc	Set Conditionally
STOP	Stop
SUB	Subtract
SUBA	Subtract Address
SUBI	Subtract Immediate
SUBQ	Subtract Quick
SUBX	Subtract With Extend
SWAP	Swap Register Words
TAS	Test Operand And Set
TRAP	Trap
TRAPcc	Trap Conditionally
TRAPV	Trap On Overflow
TST	Trap Operand
UNLK	Unlink
UNPK	Unpack BCD

Note: 1. TS6840 additions or alterations to the TS68030 and TS68881/TS68882 instructions sets.

Table 21. Floating-point instructions

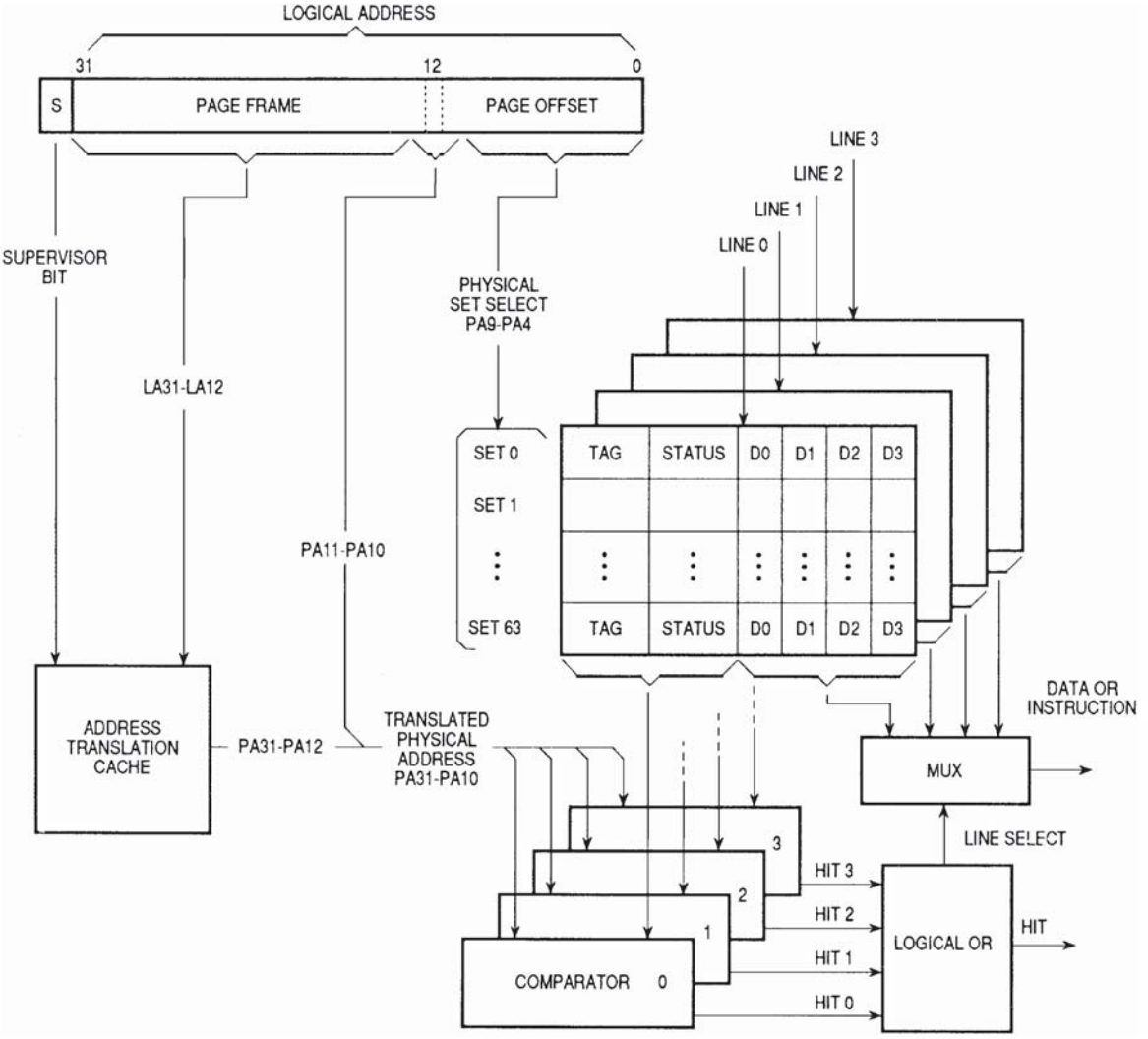
Mnemonic	Description
FABS(1)	Floating-point Absolute Value
FADD(1)	Floating-point Add
FBcc	Branch On Floating-point Condition
FCMP	Floating-point Compare
FDBcc	Floating-point Decrement And Branch
FDIV(1)	Floating-point Divide
FMOVE(1)	Move Floating-point Register
FMOVEM	Move Multiple Floating-point Registers
FMUL(1)	Floating-point Multiply
FNEG(1)	Floating-point Negate
FRESTORE	Restore Floating-point Internal State
FSAVE	Save Floating-point Internal State
FScc	Set According To Floating-point Condition
FSQRT(1)	Floating-point Square Root
FSUB(1)	Floating-point Substract
FTRAPcc	Trap On Floating-point Condition
FTST	Floating-point Test

Note: 1. TS6840 additions or alterations to the TS68030 and TS68881/TS68882 instructions sets.

The TS68040 floating-point instructions, a commonly used subset of the TS68882 instruction set, are implemented in hardware. The remaining unimplemented instructions are less frequently used and are efficiently emulated in software, maintaining compatibility with the TS68881/TS68882 floating-point coprocessors.

The TS68040 instruction set includes MOVE16, a new user instruction that allows high-speed transfers of 16-byte blocks between external devices such as memory to memory or coprocessor to memory.

Figure 21. Cache Organization Overview



The caches are accessed by physical addresses from the on-chip MMUs. The translation of the upper bits of the logical address occurs concurrently with the accesses into the set array in the cache by the lower address bits. The output of the ATC is compared with the tag field in the cache to determine if one of the lines in the selected set matches the translated physical address. If the tag matches and the entry is valid, then the cache has a hit.

If the cache hits and the access is a read, the appropriate long word from the cache line is multiplexed onto the appropriate internal bus. If the cache hits and the access is a write, the data, regardless of size, is written to the appropriate portion of the corresponding longword entry in the cache.

When a data cache miss occurs and a previously valid cache line is needed to cache the new line, any dirty data in the old line will be internally buffered and copied back to memory after the new cache line has been loaded.

Pushing of dirty data can be forced by the CPUSH instruction.

Cachability of data in each memory page is controlled by two bits in the page descriptor for each page. Cachable pages may be either write through or copyback, with no write-allocate for misses to write through pages. Non-cachable pages may also be specified as non-cachable I/O, forcing accesses to these pages to occur in order of instruction execution.

Cache Coherency

The TS68040 has the ability to snoop the external bus during accesses by other bus masters to maintain coherency between the TS68040's caches and external memory systems. External write cycles are snooped by both the instruction cache and data cache; whereas, external read cycles are snooped only by the data cache. In addition, external cycles can be flagged on the bus as snoopable or non snoopable. When an external cycle is marked as snoopable, the bus snooper checks the caches for a coherency conflict based on the state of the corresponding cache line and the type of external cycle.

Although the internal execution units and the bus snooper circuit all have access to the on-chip caches, the snooper has priority over the execution units to allow the snooper to resolve coherency discrepancies immediately.

Cache Instructions

The TS68040 supports the following instructions for cache maintenance. Both instructions may selectively operate on the data or instruction cache.

CINV: Invalidates a single line, all lines in a physical page, or the entire cache.

CPUSH: Pushes selected dirty data cache lines to memory, then invalidates all selected lines.

Operand Transfer Mechanisms

The TS68040 external synchronous bus supports multiple masters and overlaps arbitration with data transfers. The bus is optimized to perform high-speed transfers to and from an external cache or memory. The data and address buses are each 32 bits wide.

Transfer Types

The TS68040 provides two signals (TT1-TT0) that define four types of bus transfers: normal access, MOVE16 access, alternate access, and interrupt acknowledge access. Normal accesses identify normal memory references: MOVE16 accesses are memory accesses by a MOVE16 instruction; and alternate accesses identify accesses to the undefined address spaces (function code values of 0, 3, 4, 7). The interrupt acknowledge access is used to fetch an interrupt vector during interrupt exception processing.

Burst Transfer Operation

During burst read write to cache transfers, the values on the address and transfer type signals do not change; they are the address of the first requested item of the cache line. When the TS68040 request a burst read transfer of a cache line, the address bus indicates the address of the long word in the line needed first, but the memory system is expected to provide data in the following order (modulo 4): 0, 1, 2, 3 (long-word offsets). The first address needed may not be from offset 0; nevertheless, all four long words must be transferred. Burst writes occur in a similar manner.

Bus Snooping

Bus snooping ensures that data in main memory is consistent with data in the on-chip caches. If an alternate bus master is performing a read transfer on the bus and snooping is enabled, and if the snoop logic determines that the on-chip data cache has dirty data (data valid but not consistent with memory) for this transfer, the memory is prevented from responding to the read request, and the TS68040 supplies the data directly to the master. If the alternate master is performing a write transfer on the bus and snooping is enabled, and if the snooper determines that one of the on-chip caches has a valid line for this request, then the snooper may either invalidate or update the line as selected by the snoop control signals.

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