Welcome to E-XFL.COM

Understanding Embedded - Microprocessors

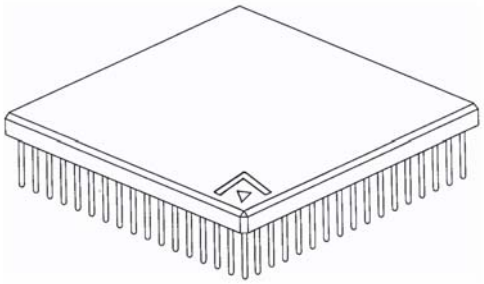
Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	68000
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	25MHz
Co-Processors/DSP	-
RAM Controllers	-
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	5.0V
Operating Temperature	-40°C ~ 110°C (TC)
Security Features	-
Package / Case	179-PGA
Supplier Device Package	179-PGA (47.24x47.24)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/ts68040vr33a

R suffix
PGA 179
Ceramic Pin Grid Array
Cavity Down



F suffix
CQFP 196
Gullwing Shape Lead
Ceramic Quad Fla Pack

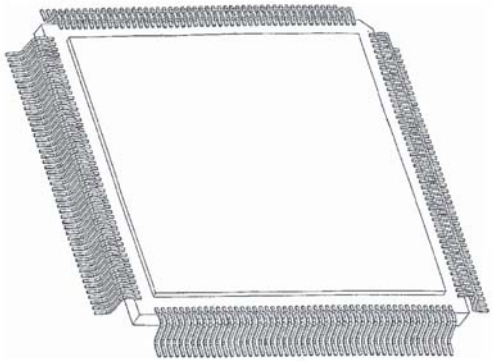
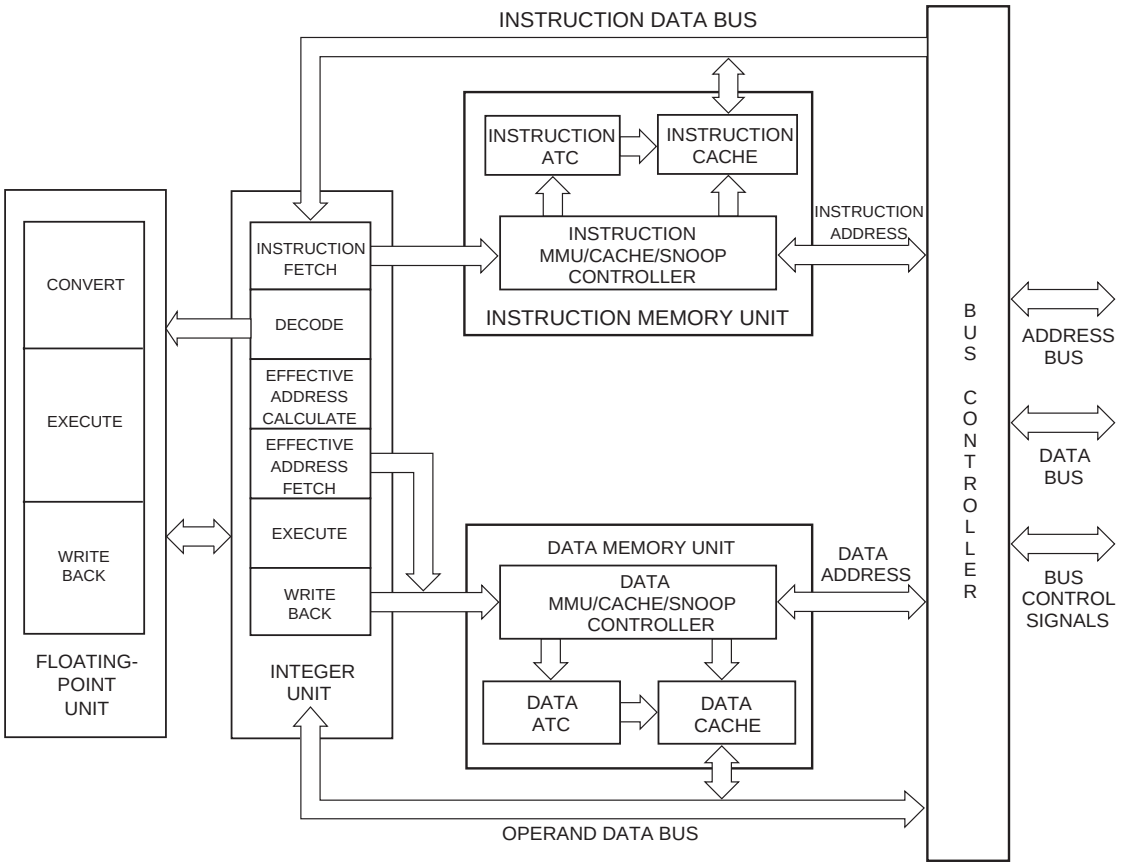


Figure 1. Block Diagram



Introduction

The TS68040 is an enhanced, 32-bit, HCMOS microprocessor that combines the integer unit processing capabilities of the TS68030 microprocessor with independent 4K bytes data and instruction caches and an on-chip FPU. The TS68040 maintains the 32-bit registers available with the entire TS68000 Family as well as the 32-bit address and data paths, rich instruction set, and versatile addressing modes. Instruction execution proceeds in parallel with accesses to the internal caches, MMU operations, and bus controller activity. Additionally, the integer unit is optimized for high-level language environments.

The TS68040 FPU is user-object-code compatible with the TS68882 floating-point coprocessor and conforms to the ANSI/IEEE Standard 754 for binary floating-point arithmetic. The FPU has been optimized to execute the most commonly used subset of the TS68882 instruction set, and includes additional instruction formats for single and double-precision rounding of results. Floating-point instructions in the FPU execute concurrently with integer instructions in the integer unit.

The MMUs support multiprocessing, virtual memory systems by translating logical addresses to physical addresses using translation tables stored in memory. The MMUs store recently used address mappings in two separate ATCs-on-chip. When an ATC contains the physical address for a bus cycle requested by the processor, a translation table search is avoided and the physical address is supplied immediately, incurring no delay for address translation. Each MMU has two transparent translation registers available that define a one-to-one mapping for address space segments ranging in size from 16M bytes to 4G bytes each.

Each MMU provides read-only and supervisor-only protections on a page basis. Also, processes can be given isolated address spaces by assigning each a unique table structure and updating the root pointer upon a task swap. Isolated address spaces protect the integrity of independent processes.

The instruction and data caches operate independently from the rest of the machine, storing information for fast access by the execution units. Each cache resides on its own internal address bus and internal data bus, allowing simultaneous access to both. The data cache provides write through or copyback write modes that can be configured on a page-by-page basis.

The TS68040 bus controller supports a high-speed, non multiplexed, synchronous external bus interface, which allows the following transfer sizes: byte, word (2 bytes), long word (4 bytes), and line (16 bytes). Line accesses are performed using burst transfers for both reads and writes to provide high data transfer rates.

Pin Assignments

PGA 179

Figure 2. Bottom View

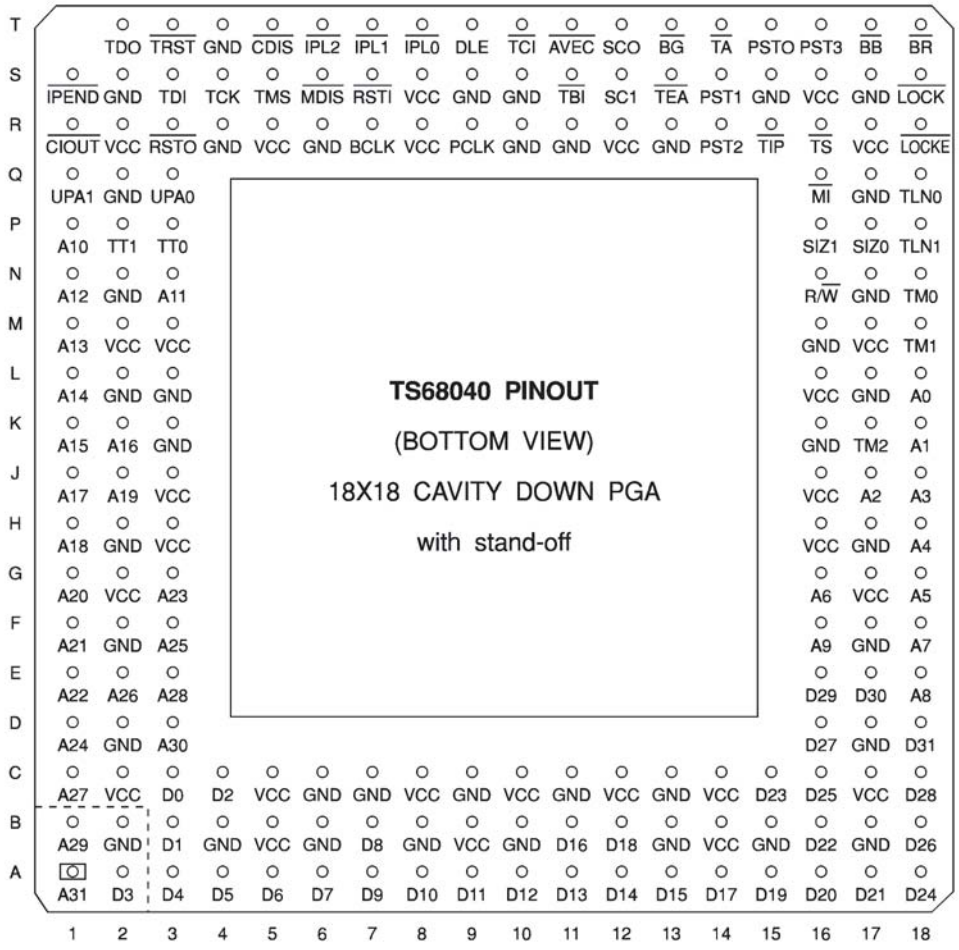


Table 1. Power Supply Affectation to PGA Body

	GND	V_{CC}
PLL		S8
Internal Logic	C6, C7, C9, C11,C13, K3, K16, L3, M16, R4, R11, R13, S10, T4, S9, R6, R10	C5, C8, C10, C12, C14, H3, H16, J3, J16, L16, M3, R5, R12, R8
Output Drivers	B2, B4, B6, B8, B10, B13, B15, B17, D2, D17, F2, F17, H2, H17, L2, L17, N2, N17, Q2, Q17, S2, S15, S17	B5, B9, B14, C2, C17, G2, G17, M2, M17, R2, R17, S16

Output Buffer Mode

The 68040 is capable of resetting to enable for a combination of either large buffers or small buffers on the outputs of the miscellaneous control signals, data bus, and address bus/transfer attribute pins. The large buffers offer quicker output times, which allow for an easier logic design. However, they do so by driving about 11 times as much current as the small buffers (refer to TS68040 Electrical specifications for current output). The designer should consider whether the quicker timings present enough advantage to justify the additional consideration to the individual signal terminations, the die power consumption, and the required cooling for the device. Since the TS68040 can be powered-up in one of eight output buffer modes upon reset, the actual maximum power consumption for TS68040 rated at a particular maximum operating frequency is dependent upon the power up mode. Therefore, the TS68040 is rated at a maximum power dissipation for either the large buffers or small buffers at a particular frequency (refer to TS68040 Electrical specifications). This allows the possibility of some of the thermal management to be controlled upon reset. The following equation provides a rough method to calculate the maximum power consumption for a chosen output buffer mode:

$$P_D = P_{DSB} + (P_{DLB} - P_{DSB}) \cdot (PINS_{LB}/PINS_{CLB}) \qquad (1)$$

where:

P_D = Max. power dissipation for output buffer mode selected

P_{DSB} = Max. power dissipation for small buffer mode (all outputs)

P_{DLB} = Max. power dissipation for large buffer mode (all outputs)

$PINS_{LB}$ = Number of pins large buffer mode

$PINS_{CLB}$ = Number of pins capable of the large buffer mode

Table 6 shows the simplified relationship on the maximum power dissipation for eight possible configurations of output buffer modes.

Table 6. Maximum Power Dissipation for Output Buffer Mode Configurations

Output Configuration			Maximum Power Dissipation
Data Bus	**Address Bus and Transfer Attrib.**	**Misc. Control Signals**	**PD**
Small Buffer	Small Buffer	Small Buffer	P_{DSB}
Small Buffer	Small Buffer	Large Buffer	$P_{DSB} + (P_{DLB} - P_{DSB}) \cdot 13\%$
Small Buffer	Large Buffer	Small Buffer	$P_{DSB} + (P_{DLB} - P_{DSB}) \cdot 52\%$
Small Buffer	Large Buffer	Large Buffer	$P_{DSB} + (P_{DLB} - P_{DSB}) \cdot 65\%$
Large Buffer	Small Buffer	Small Buffer	$P_{DSB} + (P_{DLB} - P_{DSB}) \cdot 35\%$
Large Buffer	Small Buffer	Large Buffer	$P_{DSB} + (P_{DLB} - P_{DSB}) \cdot 48\%$
Large Buffer	Large Buffer	Small Buffer	$P_{DSB} + (P_{DLB} - P_{DSB}) \cdot 87\%$
Large Buffer	Large Buffer	Large Buffer	$P_{DSB} + (P_{DLB} - P_{DSB}) \cdot 100\%$

Thermal Characteristics in Still Air

A sample size of three TS68040 packages was tested in free-air cooling with no heat sink. Measurements showed that the average Φ_{JA} was 22.8°C/W with a standard deviation of 0.44°C/W. The test was performed with 3W of power being dissipated from within the package. The test determined that Φ_{JA} will decrease slightly for the increasing power dissipation range possible. Therefore, since the variance in Φ_{JA} within the possible power dissipation range is negligible, it can be assumed for calculation purposes that Φ_{JA} is valid at all power levels. Using the formulas introduced previously, Table 7 shows the results of a maximum power dissipation of 3 and 5W with no heat sink or air-flow (refer to Table 6 to calculate other power dissipation values).

Table 7. Thermal Parameters With No Heat Sink or Air-flow

Defined Parameters			Measured	Calculated		
P_D	T_J	Φ_{JC}	Φ_{JA}	$\Phi_{CA} = \Phi_{JA} - \Phi_{JC}$	$T_C = T_J - P_D * \Phi_{JC}$	$T_A = T_J - P_D * \Phi_{JA}$
3 Watts	125°C	1°C/W	21.8°C/W	20.8°C/W	122°C	59.6°C
5 Watts	125°C	1°C/W	21.8°C/W	20.8°C/W	120°C	16°C

As seen by looking at the ambient temperature results, most users will want to implement some type of thermal management to obtain a more reasonable maximum ambient temperature.

Thermal Characteristics in Forced Air

A sample size of three TS68040 packages was tested in forced air cooling in a wind tunnel with no heat sink. This test was performed with 3W of power being dissipated from within the package. As previously mentioned, since the variance in ΦJA within the possible power range is negligible, it can be assumed for calculation purposes that Φ_{JA} is constant at all power levels. Using the previous formulas, Table 8 shows the results of the maximum power dissipation at 3 and 5W with air-flow and no heat sink (refer to Table 6 to calculate other power dissipation values).

Table 8. Thermal Parameters With Forced Air Flow and No Heat Sink

Thermal Mgmt. Technique	Defined Parameters			Measured	Calculated		
Air-flow velocity	P_D	T_J	Φ_{JC}	Φ_{JA}	Φ_{CA}	T_C	T_A
100 LFM	3W	125°C	1°C/W	11.7°C/W	10.7°C/W	122°C	89.9°C
250 LFM	3W	125°C	1°C/W	10°C/W	9°C/W	122°C	95°C
500 LFM	3W	125°C	1°C/W	8.9°C/W	7.9°C/W	122°C	98.3°C
750 LFM	3W	125°C	1°C/W	8.5°C/W	7.5°C/W	122°C	99.5°C
1000 LFM	3W	125°C	1°C/W	8.3°C/W	7.3°C/W	122°C	100.1°C
100 LFM	5W	125°C	1°C/W	11.7°C/W	10.7°C/W	120°C	66.5°C
250 LFM	5W	125°C	1°C/W	10°C/W	9°C/W,	120°C	75°C
500 LFM	5W	125°C	1°C/W	8.9°C/W	7.9°C/W	120°C	80.5°C
750 LFM	5W	125°C	1°C/W	8.5°C/W	7.5°C/W	120°C	82.5°C
1000 LFM	5W	125°C	1°C/W	8.3°C/W	7.3°C/W	120°C	83.5°C

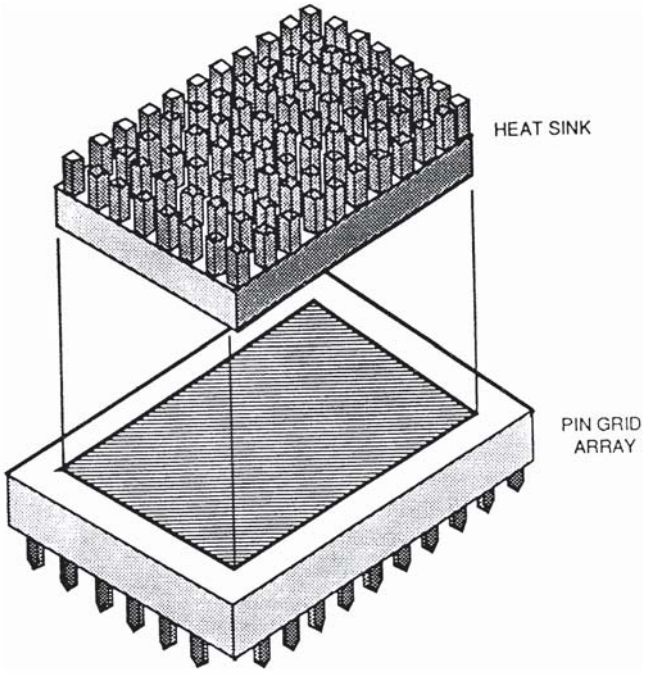
By reviewing the maximum ambient operating temperatures, it can be seen that by using the all-small-buffer configuration of the TS68040 with a relatively small amount of air flow (100 LFM), a 0-70°C ambient operating temperature can be achieved. However, depending on the output buffer configuration and available forced-air cooling, additional thermal management techniques may be required.

Thermal Characteristics with a Heat Sink

In choosing a heat sink the designer must consider many factors: heat sink size and composition, method of attachment, and choice of a wet or dry connection. The following paragraphs discuss the relationship of these decisions to the thermal performance of the design noticed during experimentation.

The heat sink size is one of the most significant parameters to consider in the selection of a heat sink. Obviously a larger heat sink will provide better cooling. However, it is less obvious that the most benefit of the larger heat sink of the pin fin type used in the experimentation would be at still air conditions. Under forced-air conditions as low as 100 LFM, the difference between the ΦCA becomes very small (0.4°C/W or less). This difference continues to decrease as the forced air flow increases. The particular heat sink used in our testing fit the perimeter package surface area available within the capacitor pads on the TS68040 (1.48" x 1.48") and showed a nice compromise between height and thermal performance needs. The heat sink base perimeter area was 1.24" x 1.30" and its height was 0.49". It was a pin-fin-type (i.e. bed of nails) design composed of Al alloy. The heat sink is shown in Figure 5 can be obtained through Thermalloy Inc. by referencing part number 2338B.

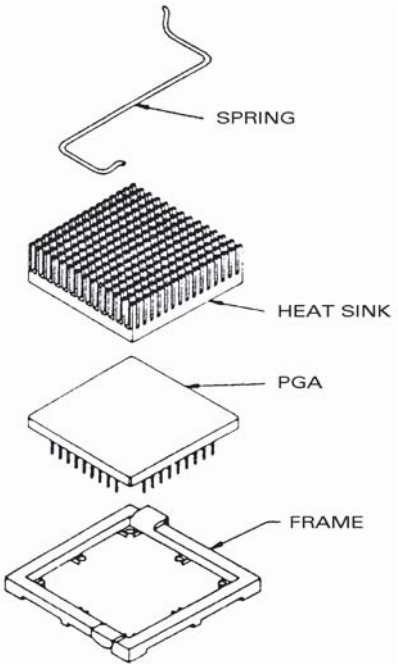
Figure 5. Heat Sink Example



All pin fin heat sinks tested were made from extrusion Al products. The planar face of the heat sink mating to the package should have a good degree of planarity; if it has any curvature, the curvature should be convex at the central region of the heat sink surface to provide intimate physical contact to the PGA surface. All heat sinks tested met this criteria. Nonplanar, concave curvature the central regions of the heat sink will result in poor thermal contact to the package. A specification needs to be determined for the planarity of the surface as part of any heat sink design.

Although there are several ways to attach a heat sink to the package, it was easiest to use a demountable heat sink attach called “E-Z attach for PGA packages” developed by Thermalloy (see Figure 6). The heat sink is clamped to the package with the help of a steel spring to a plastic frame (or plastic shoes Besides the height of the heat sink and plastic frame, no additional height added to the package. The interface between the ceramic package and the heat sink was evaluated for both dry and wet (i.e., thermal grease) interfaces in still air. The thermal grease reduced the Φ_{CA} quite significantly (about 2.5 °C/W) in still air. Therefore, it was used in all other testing done with the heat sink. According to other testing, attachment with thermal grease provided about the same thermal performance as if a thermal epoxy were used.

Figure 6. Heat Sink with Attachment



A sample size of one TS68040 package was tested in still air with the heat sink and attachment method previously described. This test was performed with 3W of power being dissipated from within the package. Since the variance in Φ_{JA} within the possible power range is negligible, it can be assumed for calculation purposes that Φ_{JA} is constant at all power levels. Table 9 shows the result assuming a maximum power dissipation of the part at 3 and 5W (refer to Table 6 to calculate other power dissipation values).

Table 9. Thermal Parameters With Heat Sink and No Air Flow

Thermal Mgmt. Technique	Defined Parameters			Measured	Calculated		
Heat Sink	P_D	T_J	Φ_{JC}	Φ_{JA}	Φ_{CA}	T_C	T_A
2338B	3W	125°C	1°C/W	14°C/W	13°C/W	122°C	83°C
2338B	5W	125°C	1°C/W	14°C/W	13°C/W	120°C	55°C

Thermal Characteristics with a Heat Sink and Forced Air

A sample size of three TS68040 packages was tested in forced-air cooling in a wind tunnel with a heat sink. This test was performed with 3W of power being dissipated from within the package. As mentioned previously, the variance in Φ_{JA} within the possible power range is negligible; it can be assumed for calculation purposes that Φ_{JA} is valid at all power levels. Table 10 shows the results, assuming a maximum power dissipation at 3 and 5W with air flow and heat sink thermal management (refer to Table 6 to calculate other power dissipation values).

Table 10. Thermal Parameters with Heat Sink and Air Flow

Thermal Mgmt. Technique		Defined Parameters			Measured	Calculated		
Air-flow	Heat sink	P_D	T_J	Φ_{JC}	Φ_{JA}	Φ_{CA}	T_C	T_A
100 LFM	2338B	3W	125°C	1°C/W	3.1°C/W	2.1°C/W	122°C	115.7°C
250 LFM	2338B	3W	125°C	1°C/W	2.2°C/W	1.2°C/W	122°C	118.4°C
500 LFM	2338B	3W	125°C	1°C/W	1.7°C/W	0.7°C/W	122°C	119.9°C
750 LFM	2338B	3W	125°C	1°C/W	1.5°C/W	0.5°C/W	122°C	120.5°C
1000 LFM	2338B	3W	125°C	1°C/W	1.4°C/W	0.4°C/W	122°C	120.8°C
100 LFM	2338B	5W	125°C	1°C/W	3.1°C/W	2.1°C/W	120°C	109.5°C
250 LFM	2338B	5W	125°C	1°C/W	2.2°C/W	1.2°C/W	120°C	114°C
500 LFM	2338B	5W	125°C	1°C/W	1.7°C/W	0.7°C/W	120°C	116.5°C
750 LFM	2338B	5W	125°C	1°C/W	1.5°C/W	0.5°C/W	120°C	117.5°C
1000 LFM	2338B	5W	125°C	1°C/W	1.4°C/W	0.4°C/W	120°C	118°C

Thermal Testing Summary

Testing proved that a heat sink in combination with a relatively small amount of air-flow (100 LFM or less) will easily realize a 0-70°C ambient operating temperature for the TS68040 with almost any configuration of the output buffers. A heat sink alone may be capable of providing all necessary cooling, depending on the particular heat sink height/size restraints, the maximum ambient operating temperature required, and the output buffer configuration chosen. Also forced air cooling alone may attain a 0-70°C ambient operating temperature. However this factor is highly dependent on the output buffer configuration chosen and the available forced air for cooling. Figure 7 is a summary of the test results of the relationship between Φ_{JA} and air-flow for the TS68040.

Figure 7. Relationship of Φ_{JA} Air-Flow for PGA

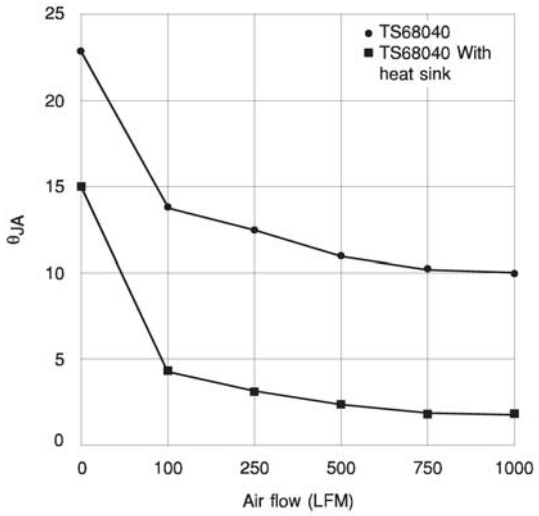


Table 11. Characteristics Guaranteed

Package	Symbol	Parameter	Value	Unit
PGA 179	θ_{J-A}	Thermal Resistance Junction-to-ambient	See Figure 7	°C/W
	θ_{J-C}	Thermal Resistance Junction-to-case	1	°C/W
CQFP 196	θ_{J-A}	Thermal Resistance Junction-to-ambient	TBD	°C/W
	θ_{J-C}	Thermal Resistance Junction-to-case	1	°C/W

Mechanical and Environment

The microcircuits shall meet all mechanical environmental requirements of either MIL-STD-883 for class B devices or for Atmel standard screening.

Marking

The document where are defined the marking are identified in the related reference documents. Each microcircuit are legible and permanently marked with the following information as minimum:

- Atmel Logo
- Manufacturer's Part Number
- Class B Identification
- Date-code Of Inspection Lot
- ESD Identifier If Available
- Country Of Manufacturing

Quality Conformance Inspection

DESC/MIL-STD-883

Is in accordance with MIL-M-38535 and method 5005 of MIL-STD-883. Group A and B inspections are performed on each production lot. Groups C and D inspection are performed on a periodical basis.

Electrical Characteristics

General Requirements

All static and dynamic electrical characteristics specified for inspection purposes and the relevant measurement conditions are given below:

- Table 12: Static electrical characteristics for the electrical variants.
- Table 13: Dynamic electrical characteristics for TS68040 (25 MHz, 33 MHz).

For static characteristics (Table 12), test methods refer to IEC 748-2 method number, where existing.

For dynamic characteristics (Table 13), test methods refer to clause “Static Characteristics” on page 18 of this specification.

Indication of “min.” or “max.” in the column «test temperature» means minimum or maximum operating temperature as defined in sub-clause Table 5 here above.

Static Characteristics

Table 12. Electrical Characteristics
$-55°C \leq T_C \leq T_{Jmax}$; $4.75V \leq V_{CC} \leq 5.25V$ unless otherwise specified(1)(2)(3)(4)

Symbol	Characteristic	Min	Max	Unit
V_{IH}	Input High Voltage	2	V_{CC}	V
V_{IL}	Input Low Voltage	GND	0.8	V
V_U	Undershoot		- 0.8	V
I_{in}	Input Leakage Current at 0.5/2.4V — $\overline{AVEC}$, BCLK $\overline{BG}$, $\overline{CDIS}$, $\overline{IPLn}$, $\overline{MDIS}$, PCLK, $\overline{RSTI}$, SCn, $\overline{TBI}$, $\overline{TCI}$, TCK, $\overline{TEA}$	-20	20	µA
I_{TSI}	Hi-z (Off-state) Leakage Current at 0.5/2.4V — An, $\overline{BB}$, $\overline{CIOUT}$, Dn, $\overline{LOCK}$, $\overline{LOCKE}$, R/$\overline{W}$, SIZn, $\overline{TA}$, TDO, $\overline{TIP}$, TLNn, TMn, $\overline{TS}$, TTn, UPAn	-20	20	µA
I_{IL}	Signal Low Input Current V_{IL} = 0.8V — TMS, TDI, $\overline{TRST}$	-1.1	-0.18	mA
I_{IH}	Signal High Input Current V_{IH} = 2.0V — TMS, TDI, $\overline{TRST}$	-0.94	-0.16	mA
V_{OH}	Output High Voltage Larger Buffers - I_{OH} = 35 mA Small Buffers - I_{OH} = 5 mA	2.4		V

Notes:
1. Output timing is specified for a valid signal measured at the pin. Large buffer timing is specified driving a 50Ω transmission line with a length characterized by a 2.5 ns one-way propagation delay, terminated through 50Ω to 2.5V. Large buffer output impedance is typically 3Ω, resulting in incident wave switching for this environment. Small buffer timing is specified driving an unterminated 30Ω transmission line with a length characterized by a 2.5 ns one-way propagation delay. Small buffer output impedance is typically 30Ω; the small buffer specifications include approximately 5 ns for the signal to propagate the length of the transmission line and back.
2. All testing to be performed using worst-case test conditions unless otherwise specified.
3. The following pins are active low: $\overline{AVEC}$, $\overline{BG}$, $\overline{BS}$, $\overline{BR}$, $\overline{CDIS}$, $\overline{CIOUT}$, $\overline{IPEND}$, $\overline{IPLO}$, $\overline{IPL1}$, $\overline{IPL2}$, $\overline{LOCK}$, $\overline{LOCKE}$, $\overline{MDIS}$, $\overline{MI}$, $\overline{RST0}$, $\overline{RSTI}$, $\overline{TA}$, $\overline{TBI}$, $\overline{TCI}$, $\overline{TEA}$, $\overline{TIP}$, $\overline{TRST}$, $\overline{TS}$ and $\overline{W}$ of R/$\overline{W}$.
4. Maximum operating junction temperature (T_J) = +125°. Minimum case operating temperature (T_C) = -55°. This device is not tested at T_C = +125°. Testing is performed by setting the junction temperature T_J = +125°and allowing the case and ambient temperatures to rise and fall as necessary so as not to exceed the maximum junction temperature.
5. Timing specifications 11, 20 and 38 for address bus output timing apply when normal bus operation is selected. Specifications 26, 27 and 28 should be used when the multiplexed bus mode of operation is enabled.
6. Timing specifications 18 and 19 for data bus output timing apply when normal bus operation is selected. Specifications 28 and 29 should be used when the multiplexed bus mode of operation is enabled.

Table 15. Input AC Timing Specifications (Figure 9 to Figure 15)
-55°C ≤T_C ≤T_{Jmax}; 4.75V ≤V_{CC} ≤5.25V unless otherwise specified(1)(2)(3)(4)

Num	Characteristic	25 MHz		33 MHz		Unit
		Min.	Max.	Min.	Max.	
15	Data-in Valid to BCLK (Setup)	5		4		ns
16	BCLK to Data-in Invalid (Hold)	4		4		ns
17	BCLK to Data-in High Impedance (Read Followed By Write)		49		36.5	ns
22a	$\overline{TA}$ Valid to BCLK (Setup)	10		10		ns
22b	$\overline{TEA}$ Valid to BCLK (Setup)	10		10		ns
22c	$\overline{TCI}$ Valid to BCLK (Setup)	10		10		ns
22d	$\overline{TBI}$ Valid to BCLK (Setup)	11		10		ns
23	BCLK to $\overline{TA}$, $\overline{TEA}$, $\overline{TCI}$, $\overline{TBI}$ Invalid (Hold)	2		2		ns
24	$\overline{AVEC}$ Valid to BCLK (Setup)	5		5		ns
25	BCLK to $\overline{AVEC}$ Invalid (Hold)	2		2		ns
31	DLE Width High	8		8		ns
32	Data-in Valid to DLE (Setup)	2		2		ns
33	DLE to Data-in Invalid (Hold)	8		8		ns
34	BCLK to DLE Hold	3		3		ns
35	DLE High to BCLK	16		12		ns
36	Data-in Valid to BCLK (DLE Mode Setup)	5		5		ns
37	BCLK Data-in Invalid (DLE Mode Hold)	4		4		ns
41a	$\overline{BB}$ Valid to BCLK (Setup)	7		7		ns
41b	$\overline{BG}$ Valid to BCLK (Setup)	8		7		ns
41c	$\overline{CDIS}$, $\overline{MDIS}$ Valid to BCLK (Setup)	10		8		ns
41d	$\overline{IPLn}$ Valid to BCLK (Setup)	4		3		ns
42	BCLK to $\overline{BB}$, $\overline{BG}$, $\overline{CDIS}$, $\overline{IPLn}$, $\overline{MDIS}$ Invalid (Hold)	2		2		ns
44a	Address Valid to BCLK (Setup)	8		7		ns
44b	SIZn Valid BCLK (Setup)	12		8		ns

Table 15. Input AC Timing Specifications (Figure 9 to Figure 15) (Continued)
-55°C ≤T_C ≤T_{Jmax}; 4.75V ≤V_{CC} ≤5.25V unless otherwise specified[1][2][3][4]

Num	Characteristic	25 MHz		33 MHz		Unit
		Min.	Max.	Min.	Max.	
44c	TTn Valid to BCLK (Setup)	6		8.5		ns
44d	R/$\overline{W}$ Valid to BCLK (Setup)	6		5		ns
44e	SCn Valid to BCLK (Setup)	10		11		ns
45	BCLK to Address SIZn, TTn, R/$\overline{W}$, SCn Invalid (Hold)	2		2		ns
46	$\overline{TS}$ Valid to BCLK (Setup)	5		9		ns
47	BCLK to $\overline{TS}$ Invalid (Hold)	2		2		ns
49	BCLK to $\overline{BB}$ High Impedance (68040 Assumes Bus Mastership)		9		9	ns
51	$\overline{RSTI}$ Valid to BCLK	5		4		ns
52	BCLK to $\overline{RSTI}$ Invalid	2		2		ns
53	Mode Select Setup to $\overline{RSTI}$ Negated[4]	20		20		ns
54	$\overline{RSTI}$ Negated to Mode Selects Invalid[4]	2		2		ns

Notes:
1. All testing to be performed using worst-case test conditions unless otherwise specified.
2. The following pins are active low: $\overline{AVEC}$, $\overline{BG}$, $\overline{BS}$, $\overline{BR}$, $\overline{CDIS}$, $\overline{CIOUT}$, $\overline{IPEND}$, $\overline{IPLO}$, $\overline{IPL1}$, $\overline{IPL2}$, $\overline{LOCK}$, $\overline{LOCKE}$, $\overline{MDIS}$, $\overline{MI}$, $\overline{RST0}$, $\overline{RSTI}$, $\overline{TA}$, $\overline{TBI}$, $\overline{TCI}$, $\overline{TEA}$, $\overline{TIP}$, $\overline{TRST}$, $\overline{TS}$ and $\overline{W}$ of R/$\overline{W}$.
3. Maximum operating junction temperature (T_J) = +125°. Minimum case operating temperature (T_C) = -55°. This device is not tested at T_C = +125°. Testing is performed by setting the junction temperature T_J = +125°and allowing the case and ambient temperatures to rise and fall as necessary so as not to exceed the maximum junction temperature.
4. The levels on $\overline{CDIS}$, $\overline{MDIS}$, and the $\overline{IPL2}$-$\overline{IPL0}$ signals enable or disable the multiplexed bus mode, data latch enable mode, and driver impedance selection respectively.

Figure 16. Clock Input Timing Diagram

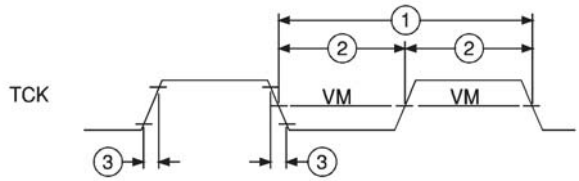


Figure 17. $\overline{\text{TRST}}$ Timing Diagram

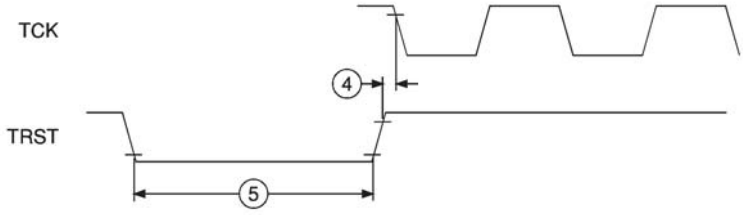


Figure 18. Boundary Scan Timing Diagram

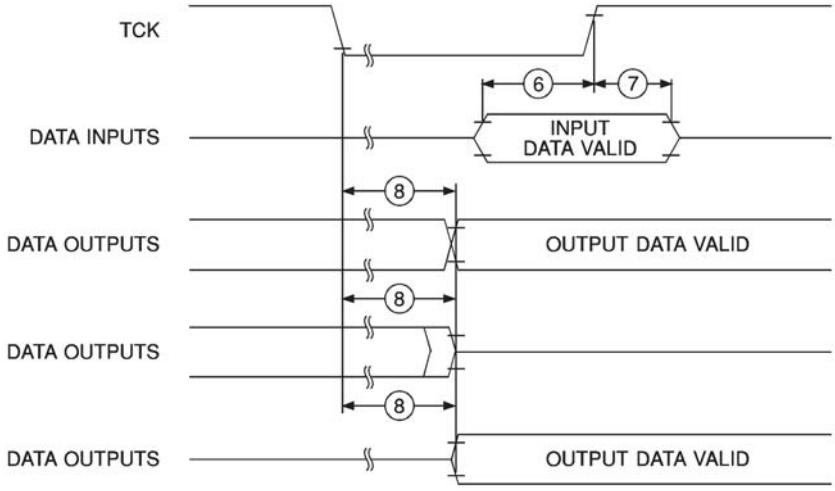
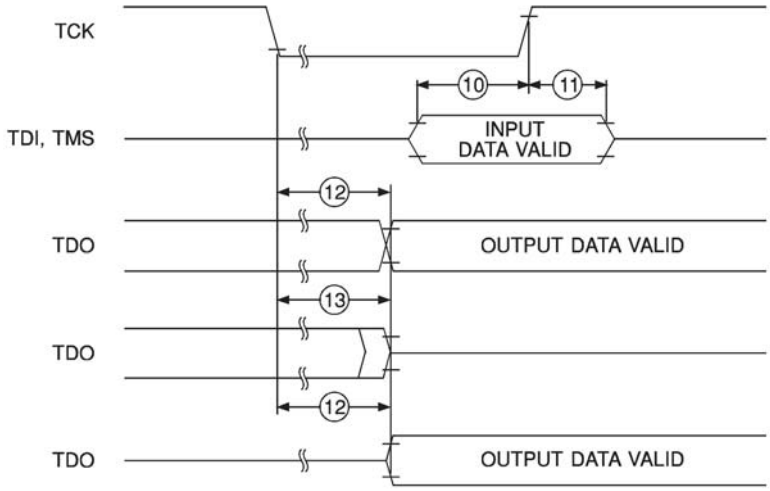


Figure 19. Test Access Port Timing Diagram



Functional Description

Programming Model

The TS68040 integrates the functions of the integer unit, MMU, and FPU. As shown in Figure 20, the registers depicted in the programming model provide access and control for the three units. The registers are partitioned into two levels of privilege: user and supervisor. User programs, executing in the user mode, can only use the resources of the user model. System software, executing in the supervisor mode, has unrestricted access to all processor resources.

The integer portion of the user programming model, consisting of 16, general-purpose, 32-bit registers and two control registers, is the same as the user programming model of the TS68030. The TS68040 user programming model also incorporates the TS68882 programming model consisting of eight, floating-point, 80-bit data registers, a floating-point control register, a floating-point status register, and a floating-point instruction address register.

The supervisor programming model is used exclusively by TS68040 system programmers to implement operating system functions, I/O control, and memory management subsystems. This supervisor/user distinction in the TS68000 architecture was carefully planned so that all application software can be written to execute in the nonprivileged user mode and migrate to the TS68040 from any TS68000 platform without modification. Since system software is usually modified by system designers when porting to a new design, the control features are properly placed in the supervisor programming model. For example, the transparent translation registers of the TS68040 can only be read or written by the supervisor software; the programming resources of user application programs are unaffected by the existence of the transparent translation registers

Registers D0-D7 are data registers containing operands for bit and bit field (1- to 32-bit), byte (8-bit), word (16-bit), long-word (32-bit), and quad-word (64-bit) operations. Registers A0-A6 and the stack pointer registers (user, interrupt, and master) are address registers that may be used as software stack pointers or base address registers. Register A7 is the user stack pointer in user mode, and is either the interrupt or master stack pointer (A7’ or A7’’) in supervisor mode. In supervisor mode, the active stack pointer (interrupt or master) is selected based on a bit in the status register (SR). The address

Table 20. Instruction Set Summary (Continued)

Mnemonic	Description
SBCD	Substract Decimal With Extend
Scc	Set Conditionally
STOP	Stop
SUB	Subtract
SUBA	Subtract Address
SUBI	Subtract Immediate
SUBQ	Subtract Quick
SUBX	Subtract With Extend
SWAP	Swap Register Words
TAS	Test Operand And Set
TRAP	Trap
TRAPcc	Trap Conditionally
TRAPV	Trap On Overflow
TST	Trap Operand
UNLK	Unlink
UNPK	Unpack BCD

Note: 1. TS6840 additions or alterations to the TS68030 and TS68881/TS68882 instructions sets.

Table 21. Floating-point instructions

Mnemonic	Description
FABS(1)	Floating-point Absolute Value
FADD(1)	Floating-point Add
FBcc	Branch On Floating-point Condition
FCMP	Floating-point Compare
FDBcc	Floating-point Decrement And Branch
FDIV(1)	Floating-point Divide
FMOVE(1)	Move Floating-point Register
FMOVEM	Move Multiple Floating-point Registers
FMUL(1)	Floating-point Multiply
FNEG(1)	Floating-point Negate
FRESTORE	Restore Floating-point Internal State
FSAVE	Save Floating-point Internal State
FScc	Set According To Floating-point Condition
FSQRT(1)	Floating-point Square Root
FSUB(1)	Floating-point Substract
FTRAPcc	Trap On Floating-point Condition
FTST	Floating-point Test

Note: 1. TS6840 additions or alterations to the TS68030 and TS68881/TS68882 instructions sets.

The TS68040 floating-point instructions, a commonly used subset of the TS68882 instruction set, are implemented in hardware. The remaining unimplemented instructions are less frequently used and are efficiently emulated in software, maintaining compatibility with the TS68881/TS68882 floating-point coprocessors.

The TS68040 instruction set includes MOVE16, a new user instruction that allows high-speed transfers of 16-byte blocks between external devices such as memory to memory or coprocessor to memory.

Instruction and Data Caches

Studies have shown that typical programs spend much of their execution time in a few main routines or tight loops. Earlier members of the TS68000 Family took advantage of this locality of reference phenomenon to varying degrees. The TS68040 takes further advantage of cache technology with its two, independent, on-chip, physical address space caches, one for instructions and one for data. The caches reduce the processor's external bus activity and increase CPU throughput by lowering the effective memory access time. For a typical system design, the large caches of the TS68040 yield a very high hit rate, providing a substantial increase in system performance. Additionally, the caches are automatically burstfilled from the external bus whenever a cache miss occurs.

The autonomous nature of the caches allows instruction-stream fetches, data-stream fetches, and a third external access to occur simultaneously with instruction execution. For example, if the TS68040 requires both an instruction-stream access and an external peripheral access and if the instruction is resident in the on-chip cache, the peripheral access proceeds unimpeded rather than being queued behind the instruction fetch. If a data operand is also required and if it is resident in the data cache, it can also be accessed without hindering either the instruction access from its cache or the peripheral access external to the chip. The parallelism inherent in the TS68040 also allows multiple instructions that do not require any external accesses to execute concurrently while the processor is performing an external access for a previous instruction.

Cache Organization

The instruction and data caches are four-way set-associative with 64 sets of four, 16-byte lines for a total cache storage of 4K bytes each. As shown in Figure 21, each 16-byte line contains an address tag and state information. State information for each entry consists of a valid flag for the entire line in both instruction and data caches and write status for each long word in the data cache. The write status in the data cache signifies whether or not the long-word data is dirty (meaning that the data in the cache has been modified but has not been written back to external memory) for data in copyback pages.

A global bit can be set in each page descriptor to prevent flushing of the ATC entry for that page by some PFLUSH instruction variants, allowing system ATC entries to remain resident during task swaps. If these special PFLUSH instructions are not used, this bit can be user defined. The MMUs automatically maintain access history information for the pages by updating the used (U) and modified (M) status bits.

MMU Instructions

The MMU instructions supported by the TS68040 are as follows:

PFLUSH: Allows flushing of either selected ATC entries by function code and logical address or the entire ATCs.

PTEST: Takes an address and function code and searches the translation tables for the corresponding entry, which is then loaded into the ATC. The results of the search are available in the MMU status register and are often useful in determining the cause of a fault.

All of the TS68040 MMU instructions are privileged and can only be executed from the supervisor mode.

Transparent Translation

Four transparent translation registers, two each for instruction and data accesses, have been provided on the TS68040 MMU to allow portions of the logical address space to be transparently mapped and accessed without the need for corresponding entries resident in the ATC. Each register can be used to define a range of logical addresses from 16M bytes to 4G bytes with a base address and a mask. All addresses within these ranges are not mapped, and are optionally protected against user or supervisor accesses and write accesses. Logical addresses in these areas become the physical addresses for memory access. The transparent translation feature allows rapid movement of large blocks of data in memory or I/O space without disturbing the context of the on-chip ATCs or incurring delays associated with translation table searches.

Preparation For Delivery

Packaging

Microcircuits are prepared for delivery in accordance with MIL-M-38510 or Atmel standard.

Certificate of Compliance

Atmel offers a certificate of compliances with each shipment of parts, affirming the products are in compliance either with MIL-STD-883 or Atmel standard and guarantying the parameters not tested at temperature extremes for the entire temperature range.

Handling

MOS devices must be handled with certain precautions to avoid damage due to accumulation of static charge. Input protection devices have been designed in the chip to minimize the effect of this static buildup. However, the following handling practices are recommended:

a) Devices should be handled on benches with conductive and grounded surfaces.

b) Ground test equipment, tools and operator.

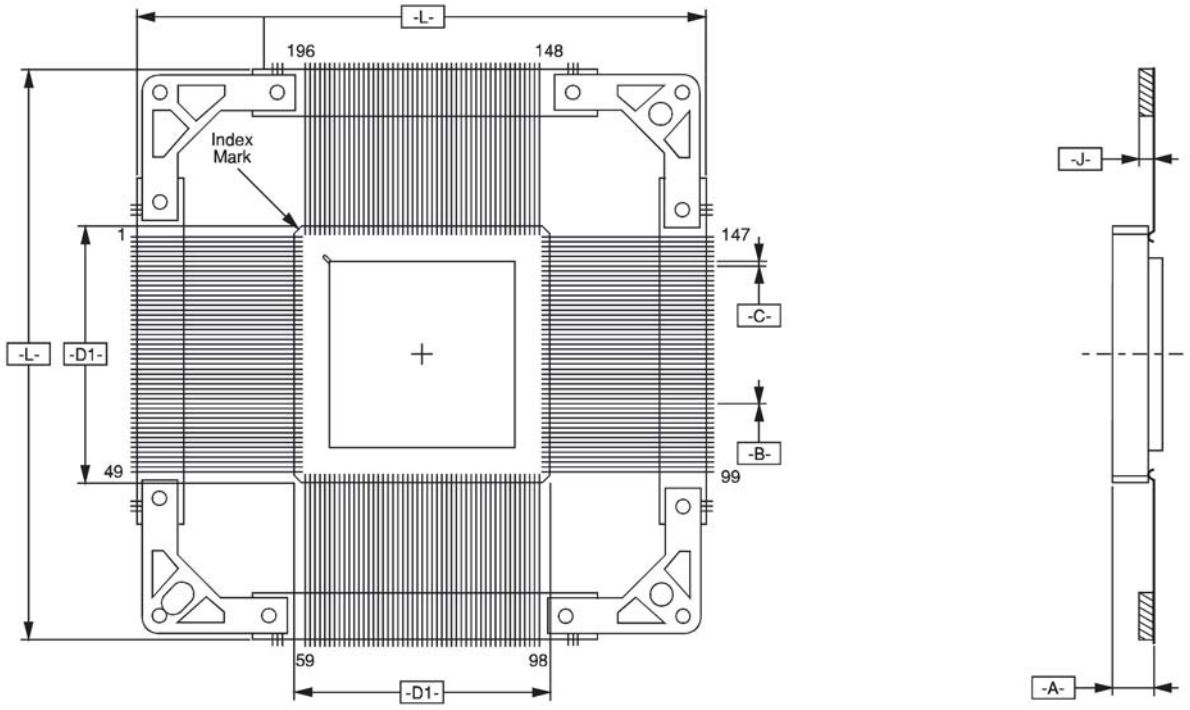
c) Do not handle devices by the leads.

d) Store devices in conductive foam or carriers.

e) Avoid use of plastic, rubber, or silk in MOS areas.

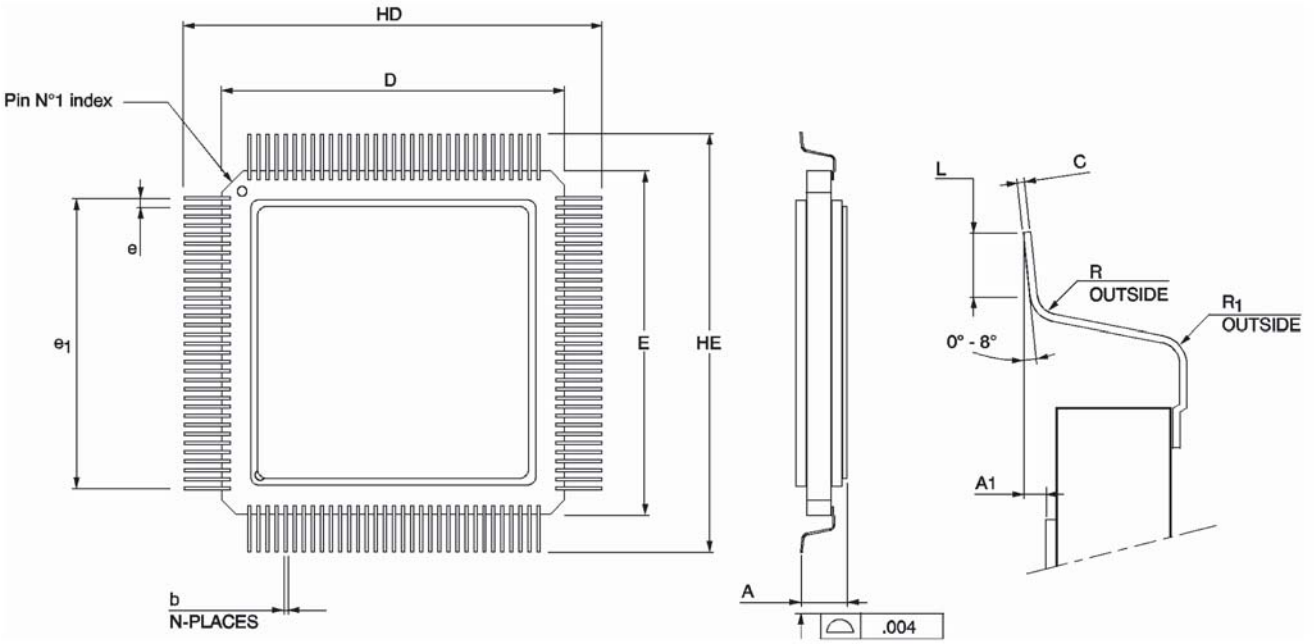
f) Maintain relative humidity above 50 percent if practical.

196 pins – Tie Bar CQFP
Cavity Up (on request)



Dim	Millimeters	Inches
A	3.30 max	0.130 max
B	0.23 +0.05 0.23 -0.038	0.009 +0.002 0.009 -0.015
C	0.635 typ.	.025 typ.
D1	33.91 ± 0.25	1.335 ± 0.01
J	0.89 ± 0.13	0.035 ± 0.005
L	63.5 ± 0.51	2.5 ± 0.02

196 pins – Gullwing
CQFP cavity up

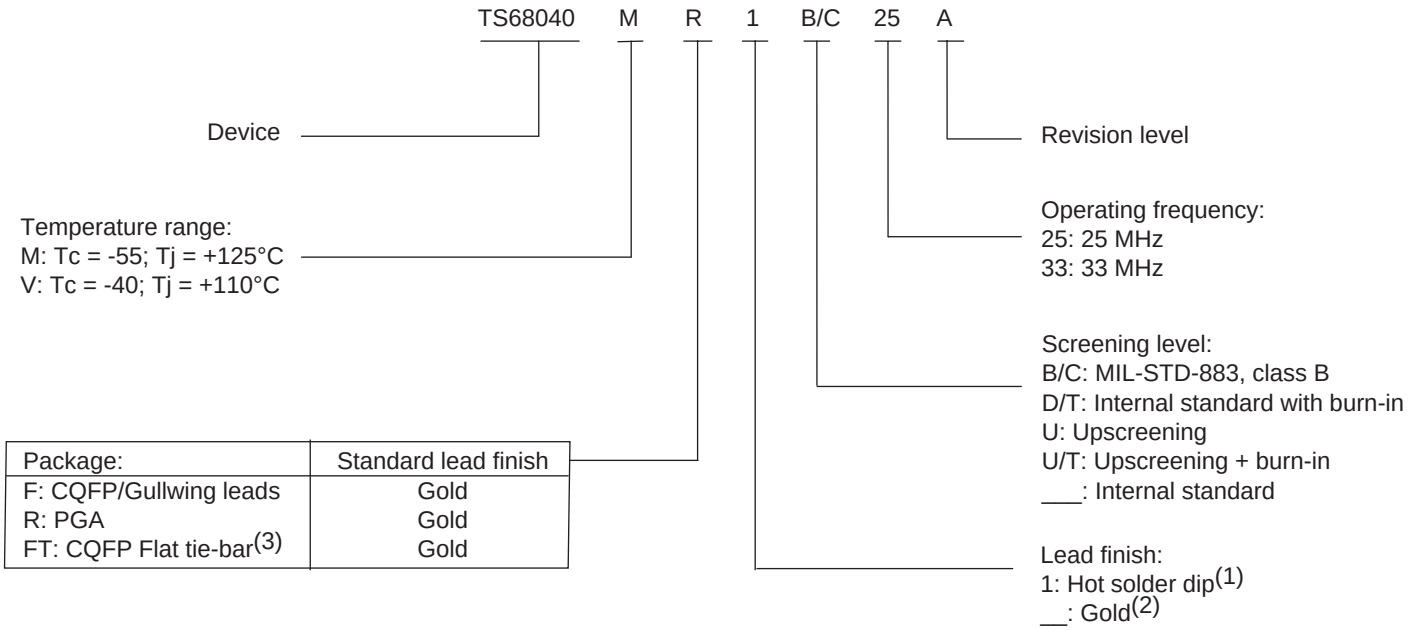


* Reduce pin count shown for clarity, 49 pins per side

Symbol	Millimeters	Inches
A	4.19 max	0.165 max
A1	0.673 ± 0.2	.0265 ±.008
b	0.23 +0.05 0.23 -0.038	.009 +.002 .009 -.0015
c	0.127 +0.05 0.127 -0.025	.005 +.002 .005 -.001
D/E	33.91 ±0.25	1.335 ±.01
e	.635 BSC	.025 BSC
e1	30.48 ±0.13	1.2 ±.005
HD/HE	38.8 ±0.18	1.528 ±.007
L	0.813 ±0.2	.032 ±.008
N	196	196
R	0.55 ±0.25	.022 ±.01
R1	0.23 min	.009 min

Ordering Information

MIL-STD-883 C and Internal Standard



Package:	Standard lead finish
F: CQFP/Gullwing leads	Gold
R: PGA	Gold
FT: CQFP Flat tie-bar(3)	Gold

Notes: 1. On request.
2. Standard process.
3. Non request for small quantity.

DESC Drawing 5962-93143