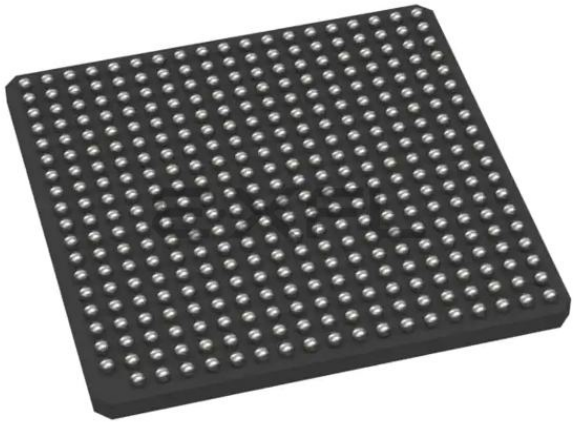

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC G4
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.267GHz
Co-Processors/DSP	Multimedia; SIMD
RAM Controllers	-
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	1.5V, 1.8V, 2.5V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	360-BCBGA, FCCBGA
Supplier Device Package	360-FCCBGA (25x25)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmc7448hx1267nd

Figure 2 shows the undershoot and overshoot voltage on the MPC7448.

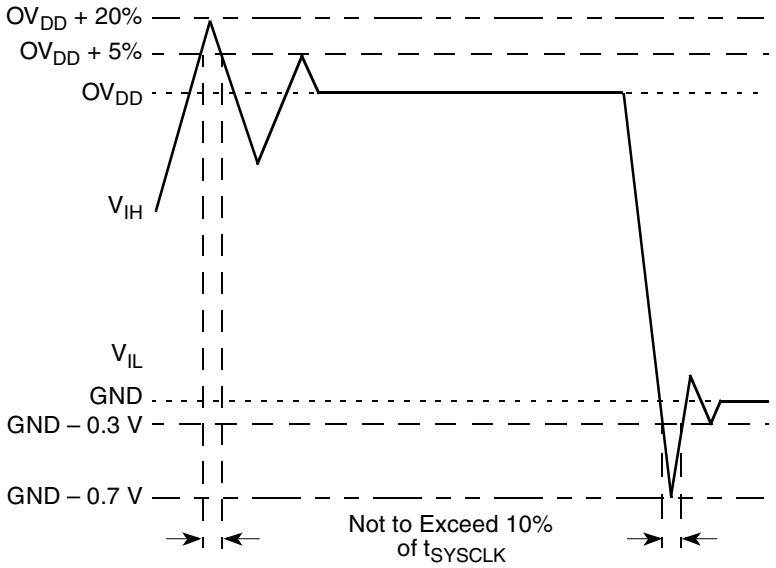


Figure 2. Overshoot/Undershoot Voltage

The MPC7448 provides several I/O voltages to support both compatibility with existing systems and migration to future systems. The MPC7448 core voltage must always be provided at the nominal voltage (see Table 4). The input voltage threshold for each bus is selected by sampling the state of the voltage select pins at the negation of the signal $\overline{\text{HRESET}}$. The output voltage will swing from GND to the maximum voltage applied to the OV_{DD} power pins. Table 3 provides the input threshold voltage settings. Because these settings may change in future products, it is recommended that BVSEL[0:1] be configured using resistor options, jumpers, or some other flexible means, with the capability to reconfigure the termination of this signal in the future, if necessary.

Table 3. Input Threshold Voltage Setting

BVSEL0	BVSEL1	I/O Voltage Mode[1]	Notes
0	0	1.8 V	2, 3
0	1	2.5 V	2, 4
1	0	1.5 V	2
1	1	2.5 V	4

Notes:

1. **Caution:** The I/O voltage mode selected must agree with the OV_{DD} voltages supplied. See Table 4.
2. If used, pull-down resistors should be less than 250 Ω.
3. The pin configuration used to select 1.8V mode on the MPC7448 is not compatible with the pin configuration used to select 1.8V mode on the MPC7447A and earlier devices.
4. The pin configuration used to select 2.5V mode on the MPC7448 is fully compatible with the pin configuration used to select 2.5V mode on the MPC7447A and earlier devices.

Table 6. DC Electrical Specifications (continued)

At recommended operating conditions. See Table 4.

Characteristic		Nominal Bus Voltage [1]	Symbol	Min	Max	Unit	Notes
High-impedance (off-state) leakage current: $V_{in} = OV_{DD}$ V_{in} = GND		—	I_{TSI}	—	 50 – 50	µA	2, 3, 4
Output high voltage @ I_{OH} = –5 mA		1.5	V_{OH}	OV_{DD} – 0.45	—	V	
		1.8		OV_{DD} – 0.45	—		
		2.5		1.8	—		
Output low voltage @ I_{OL} = 5 mA		1.5	V_{OL}	—	0.45	V	
		1.8		—	0.45		
		2.5		—	0.6		
Capacitance, V_{in} = 0 V, f = 1 MHz	All inputs		C_{in}	—	8.0	pF	5

Notes:

1. Nominal voltages; see Table 4 for recommended operating conditions.
2. All I/O signals are referenced to OV_{DD}.
3. Excludes test signals and IEEE Std. 1149.1 boundary scan (JTAG) signals
4. The leakage is measured for nominal OV_{DD} and V_{DD}, or both OV_{DD} and V_{DD} must vary in the same direction (for example, both OV_{DD} and V_{DD} vary by either +5% or –5%).
5. Capacitance is periodically sampled rather than 100% tested.
6. These pins have internal pull-up resistors.

Table 7 provides the power consumption for the MPC7448 part numbers described by this document; see Section 11.1, “Part Numbers Fully Addressed by This Document,” for information regarding which part numbers are described by this document. Freescale also offers MPC7448 part numbers that meet lower power consumption specifications by adhering to lower core voltage and core frequency specifications. For more information on these devices, including references to the MPC7448 Hardware Specification Addenda that describe these devices, see Section 11.2, “Part Numbers Not Fully Addressed by This Document.”

The power consumptions provided in Table 7 represent the power consumption of each speed grade when operated at the rated maximum core frequency (see Table 8). Freescale sorts devices by power as well as by core frequency, and power limits for each speed grade are independent of each other. Each device is tested at its maximum core frequency only. (Note that Deep Sleep Mode power consumption is independent of clock frequency.) Operating a device at a frequency lower than its rated maximum is fully supported provided the clock frequencies are within the specifications given in Table 8, and a device operated below its rated maximum will have lower power consumption. However, inferences should not be made about a device’s power consumption based on the power specifications of another (lower) speed grade. For example, a 1700 MHz device operated at 1420 MHz may not exhibit the same power consumption as a 1420 MHz device operated at 1420 MHz.

For all MPC7448 devices, the following guidelines on the use of these parameters for system design are suggested. The Full-Power Mode–Typical value represents the sustained power consumption of the device

when running a typical benchmark at temperatures in a typical system. The Full-Power Mode–Thermal value is intended to represent the sustained power consumption of the device when running a typical code sequence at high temperature and is recommended to be used as the basis for designing a thermal solution; see Section 9.7, "Power and Thermal Management Information" for more information on thermal solutions. The Full-Power Mode–Maximum value is recommended to be used for power supply design because this represents the maximum peak power draw of the device that a power supply must be capable of sourcing without voltage droop. For information on power consumption when dynamic frequency switching is enabled, see Section 9.7.5, "Dynamic Frequency Switching (DFS)."

Table 7. Power Consumption for MPC7448 at Maximum Rated Frequency

	Die Junction Temperature (T_j)	Maximum Processor Core Frequency (Speed Grade, MHz)				Unit	Notes
		1000 MHz	1420 MHz	1600 MHz	1700 MHz		
Full-Power Mode							
Typical	65 •C	15.0	19.0	20.0	21.0	W	1, 2
Thermal	105 •C	18.6	23.3	24.4	25.6	W	1, 5
Maximum	105 •C	21.6	27.1	28.4	29.8	W	1, 3
Nap Mode							
Typical	105 •C	11.1	11.8	13.0	13.0	W	1, 6
Sleep Mode							
Typical	105 •C	10.8	11.4	12.5	12.5	W	1, 6
Deep Sleep Mode (PLL Disabled)							
Typical	105 •C	10.4	11.0	12.0	12.0	W	1, 6

Notes:

1. These values specify the power consumption for the core power supply (V_{DD}) at nominal voltage and apply to all valid processor bus frequencies and configurations. The values do not include I/O supply power (OV_{DD}) or PLL supply power (AV_{DD}). OV_{DD} power is system dependent but is typically < 5% of V_{DD} power. Worst case power consumption for AV_{DD} < 13 mW. Freescale also offers MPC7448 part numbers that meet lower power consumption specifications; for more information on these devices, see Section 11.2, "Part Numbers Not Fully Addressed by This Document."
2. Typical power consumption is an average value measured with the processor operating at its rated maximum processor core frequency (except for Deep Sleep Mode), at nominal recommended V_{DD} (see Table 4) and 65°C while running the Dhrystone 2.1 benchmark and achieving 2.3 Dhrystone MIPs/MHz. This parameter is not 100% tested but periodically sampled.b
3. Maximum power consumption is the average measured with the processor operating at its rated maximum processor core frequency, at nominal V_{DD} and maximum operating junction temperature (see Table 4) while running an entirely cache-resident, contrived sequence of instructions to keep all the execution units maximally busy.
4. Doze mode is not a user-definable state; it is an intermediate state between full-power and either nap or sleep mode. As a result, power consumption for this mode is not tested.
5. Thermal power consumption is an average value measured at the nominal recommended V_{DD} (see Table 4) and 105 °C while running the Dhrystone 2.1 benchmark and achieving 2.3 Dhrystone MIPs/MHz. This parameter is not 100% tested but periodically sampled.
6. Typical power consumption for these modes is measured at the nominal recommended V_{DD} (see Table 4) and 105 °C in the mode described. This parameter is not 100% tested but is periodically sampled.

Table 9. Processor Bus AC Timing Specifications[1] (continued)

At recommended operating conditions. See Table 4.

Parameter	Symbol [2]	All Speed Grades		Unit	Notes
		Min	Max		
SYSCLK to output high impedance (all except $\overline{TS}$, $\overline{ARTRY}$, $\overline{SHD0}$, $\overline{SHD1}$)	t_{KHOZ}	—	1.8	ns	5
SYSCLK to $\overline{TS}$ high impedance after precharge	t_{KHTSPZ}	—	1	t_{SYSCLK}	3, 4, 5
Maximum delay to $\overline{ARTRY}$/$\overline{SHD0}$/$\overline{SHD1}$ precharge	t_{KHARP}	—	1	t_{SYSCLK}	3, 5, 6, 7
SYSCLK to $\overline{ARTRY}$/$\overline{SHD0}$/$\overline{SHD1}$ high impedance after precharge	t_{KHARPZ}	—	2	t_{SYSCLK}	3, 5, 6, 7

Notes:

1. All input specifications are measured from the midpoint of the signal in question to the midpoint of the rising edge of the input SYSCLK. All output specifications are measured from the midpoint of the rising edge of SYSCLK to the midpoint of the signal in question. All output timings assume a purely resistive 50-Ω load (see Figure 4). Input and output timings are measured at the pin; time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. The symbology used for timing specifications herein follows the pattern of $t_{(signal)(state)(reference)(state)}$ for inputs and $t_{(reference)(state)(signal)(state)}$ for outputs. For example, t_{IVKH} symbolizes the time input signals (I) reach the valid state (V) relative to the SYSCLK reference (K) going to the high (H) state or input setup time. And t_{KHOV} symbolizes the time from SYSCLK(K) going high (H) until outputs (O) are valid (V) or output valid time. Input hold time can be read as the time that the input signal (I) went invalid (X) with respect to the rising clock edge (KH) (note the position of the reference and its state for inputs) and output hold time can be read as the time from the rising edge (KH) until the output went invalid (OX).
3. t_{sysclk} is the period of the external clock (SYSCLK) in ns. The numbers given in the table must be multiplied by the period of SYSCLK to compute the actual time duration (in ns) of the parameter in question.
4. According to the bus protocol, $\overline{TS}$ is driven only by the currently active bus master. It is asserted low and precharged high before returning to high impedance, as shown in Figure 6. The nominal precharge width for $\overline{TS}$ is t_{SYSCLK}, that is, one clock period. Since no master can assert $\overline{TS}$ on the following clock edge, there is no concern regarding contention with the precharge. Output valid and output hold timing is tested for the signal asserted. Output valid time is tested for precharge.The high-impedance behavior is guaranteed by design.
5. Guaranteed by design and not tested
6. According to the bus protocol, $\overline{ARTRY}$ can be driven by multiple bus masters through the clock period immediately following $\overline{AACK}$. Bus contention is not an issue because any master asserting $\overline{ARTRY}$ will be driving it low. Any master asserting it low in the first clock following $\overline{AACK}$ will then go to high impedance for a fraction of a cycle, then negated for up to an entire cycle (crossing a bus cycle boundary) before being three-stated again. The nominal precharge width for $\overline{ARTRY}$ is 1.0 t_{SYSCLK}; that is, it should be high impedance as shown in Figure 6 before the first opportunity for another master to assert $\overline{ARTRY}$. Output valid and output hold timing is tested for the signal asserted.The high-impedance behavior is guaranteed by design.
7. According to the MPX bus protocol, $\overline{SHD0}$ and $\overline{SHD1}$ can be driven by multiple bus masters beginning two cycles after $\overline{TS}$. Timing is the same as $\overline{ARTRY}$, that is, the signal is high impedance for a fraction of a cycle, then negated for up to an entire cycle (crossing a bus cycle boundary) before being three-stated again. The nominal precharge width for $\overline{SHD0}$ and $\overline{SHD1}$ is 1.0 t_{SYSCLK}. The edges of the precharge vary depending on the programmed ratio of core to bus (PLL configurations).
8. $\overline{BMODE}$[0:1] and BVSEL[0:1] are mode select inputs. $\overline{BMODE}$[0:1] are sampled before and after $\overline{HRESET}$ negation. BVSEL[0:1] are sampled before $\overline{HRESET}$ negation. These parameters represent the input setup and hold times for each sample. These values are guaranteed by design and not tested. $\overline{BMODE}$[0:1] must remain stable after the second sample; BVSEL[0:1] must remain stable after the first (and only) sample. See Figure 5 for sample timing.

Figure 4 provides the AC test load for the MPC7448.

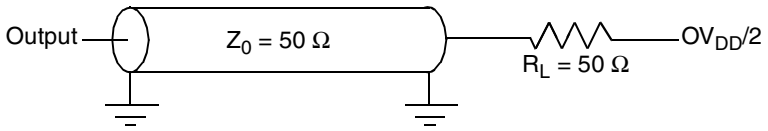


Figure 4. AC Test Load

Figure 5 provides the $\overline{\text{BMODE}}$[0:1] input timing diagram for the MPC7448. These mode select inputs are sampled once before and once after $\overline{\text{HRESET}}$ negation.

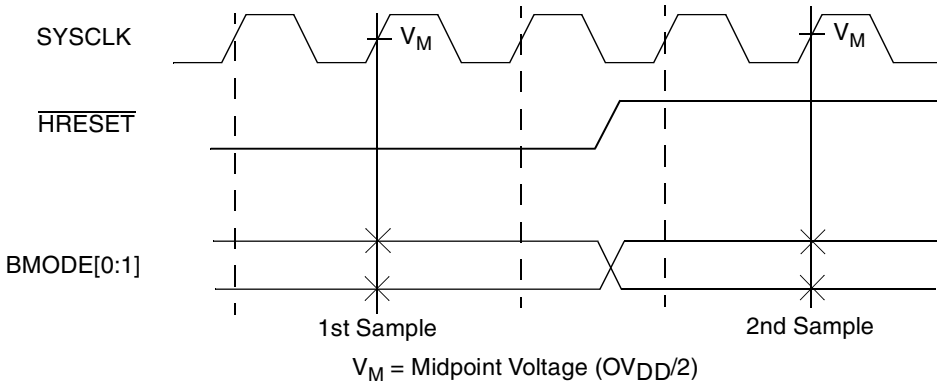


Figure 5. $\overline{\text{BMODE}}$[0:1] Input Sample Timing Diagram

5.2.3 IEEE Std. 1149.1 AC Timing Specifications

Table 10 provides the IEEE Std. 1149.1 (JTAG) AC timing specifications as defined in Figure 8 through Figure 11.

Table 10. JTAG AC Timing Specifications (Independent of SYSCLK)[1]

At recommended operating conditions. See Table 4.

Parameter	Symbol	Min	Max	Unit	Notes
TCK frequency of operation	f_{TCLK}	0	33.3	MHz	
TCK cycle time	t_{TCLK}	30	—	ns	
TCK clock pulse width measured at 1.4 V	t_{JHJL}	15	—	ns	
TCK rise and fall times	t_{JR} and t_{JF}	—	2	ns	
$\overline{\text{TRST}}$ assert time	t_{TRST}	25	—	ns	2
Input setup times: Boundary-scan data TMS, TDI	 t_{DVJH} t_{IVJH}	 4 0	 — —	ns	3
Input hold times: Boundary-scan data TMS, TDI	 t_{DXJH} t_{IXJH}	 20 25	 — —	ns	3
Valid times: Boundary-scan data TDO	 t_{JLDV} t_{JLOV}	 4 4	 20 25	ns	4
Output hold times: Boundary-scan data TDO	 t_{JLDX} t_{JLOX}	 30 30	 — —	ns	4
TCK to output high impedance: Boundary-scan data TDO	 t_{JLDZ} t_{JLOZ}	 3 3	 19 9	ns	4, 5

Notes:

1. All outputs are measured from the midpoint voltage of the falling/rising edge of TCLK to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load (see Figure 7). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. $\overline{\text{TRST}}$ is an asynchronous level sensitive signal. The time is for test purposes only.
3. Non-JTAG signal input timing with respect to TCK.
4. Non-JTAG signal output timing with respect to TCK.
5. Guaranteed by design and characterization.

Figure 11 provides the test access port timing diagram.

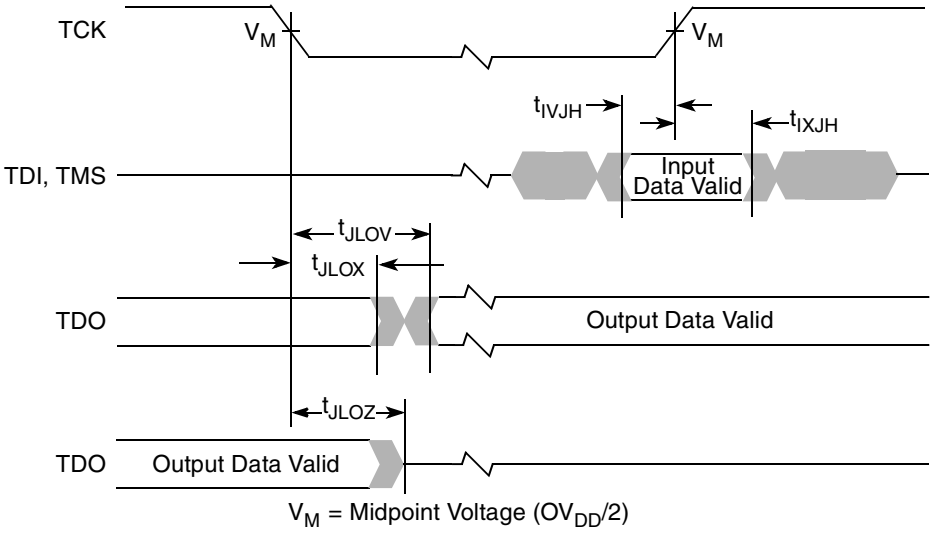


Figure 11. Test Access Port Timing Diagram

5.3 Voltage and Frequency Derating

Voltage and frequency derating is no longer supported for part numbers described by this document beginning with datecode 0613. (See Section 11, “Part Numbering and Marking,” for information on date code markings.) It is supported by some MPC7448 part numbers which target low-power applications; see Section 11.2, “Part Numbers Not Fully Addressed by This Document” and the referenced MPC7448 Hardware Specification Addenda for more information on these low-power devices. For those devices which previously supported this feature, information has been archived in the *Chip Errata for the MPC7448* (document order no. MPC7448CE).

7 Pinout Listings

Table 11 provides the pinout listing for the MPC7448, 360 HCTE package. The pinouts of the MPC7448 and MPC7447A are compatible, but the requirements regarding the use of the additional power and ground pins have changed. The MPC7448 requires these pins be connected to the appropriate power or ground plane to achieve high core frequencies; see Section 9.3, “Connection Recommendations,” for additional information. As a result, these pins should be connected in all new designs.

Additionally, the MPC7448 may be populated on a board designed for a MPC7447 (or MPC7445 or MPC7441), provided the core voltage can be made to match the requirements in Table 4 and all pins defined as ‘no connect’ for the MPC7447 are unterminated, as required by the *MPC7457 RISC Microprocessor Hardware Specifications*. The MPC7448 uses pins previously marked ‘no connect’ for the temperature diode pins and for additional power and ground connections. The additional power and ground pins are required to achieve high core frequencies and core frequency will be limited if they are not connected; see Section 9.3, “Connection Recommendations,” for additional information. Because these ‘no connect’ pins in the MPC7447 360 pin package are not driven in functional mode, an MPC7447 can be populated in an MPC7448 board.

NOTE

Caution must be exercised when performing boundary scan test operations on a board designed for an MPC7448, but populated with an MPC7447 or earlier device. This is because in the MPC7447 it is possible to drive the latches associated with the former ‘no connect’ pins in the MPC7447, potentially causing contention on those pins. To prevent this, ensure that these pins are not connected on the board or, if they are connected, ensure that the states of internal MPC7447 latches do not cause these pins to be driven during board testing.

For the MPC7448, pins that were defined as the TEST[0:4] factory test signal group on the MPC7447A and earlier devices have been assigned new functions. For most of these, the termination recommendations for the TEST[0:4] pins of the MPC7447A are compatible with the MPC7448 and will allow correct operation with no performance loss. The exception is BVSEL1 (TEST3 on the MPC7447A and earlier devices), which may require a different termination depending which I/O voltage mode is desired; see Table 3 for more information.

NOTE

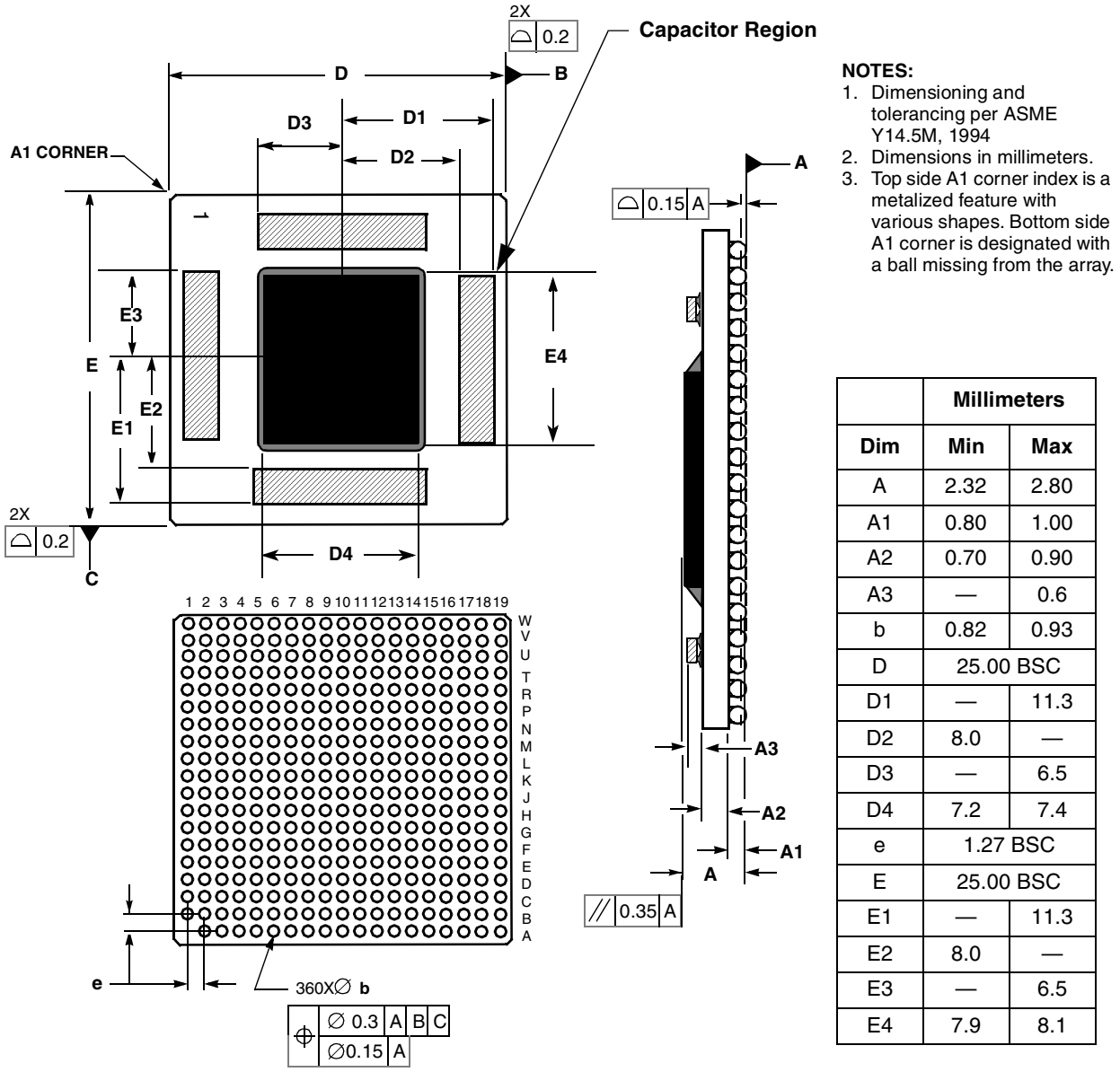
This pinout is not compatible with the MPC750, MPC7400, or MPC7410 360 BGA package.

Table 11. Pinout Listing for the MPC7448, 360 HCTE Package

Signal Name	Pin Number	Active	I/O	Notes
A[0:35]	E11, H1, C11, G3, F10, L2, D11, D1, C10, G2, D12, L3, G4, T2, F4, V1, J4, R2, K5, W2, J2, K4, N4, J3, M5, P5, N3, T1, V2, U1, N5, W1, B12, C4, G10, B11	High	I/O	2
$\overline{\text{AACK}}$	R1	Low	Input	
AP[0:4]	C1, E3, H6, F5, G7	High	I/O	2
$\overline{\text{ARTRY}}$	N2	Low	I/O	3
AV_{DD}	A8	—	Input	
$\overline{\text{BG}}$	M1	Low	Input	
$\overline{\text{BMODE0}}$	G9	Low	Input	4
$\overline{\text{BMODE1}}$	F8	Low	Input	5
$\overline{\text{BR}}$	D2	Low	Output	
BVSEL0	B7	High	Input	1, 6
BVSEL1	E10	High	Input	1, 20
$\overline{\text{CI}}$	J1	Low	Output	
$\overline{\text{CKSTP\_IN}}$	A3	Low	Input	
$\overline{\text{CKSTP\_OUT}}$	B1	Low	Output	
CLK_OUT	H2	High	Output	
D[0:63]	R15, W15, T14, V16, W16, T15, U15, P14, V13, W13, T13, P13, U14, W14, R12, T12, W12, V12, N11, N10, R11, U11, W11, T11, R10, N9, P10, U10, R9, W10, U9, V9, W5, U6, T5, U5, W7, R6, P7, V6, P17, R19, V18, R18, V19, T19, U19, W19, U18, W17, W18, T16, T18, T17, W3, V17, U4, U8, U7, R7, P6, R8, W8, T8	High	I/O	
$\overline{\text{DBG}}$	M2	Low	Input	
$\overline{\text{DFS2}}$	A12	Low	Input	20, 21
$\overline{\text{DFS4}}$	B6	Low	Input	12, 20, 21
DP[0:7]	T3, W4, T4, W9, M6, V3, N8, W6	High	I/O	
$\overline{\text{DRDY}}$	R3	Low	Output	7
DTI[0:3]	G1, K1, P1, N1	High	Input	8
EXT_QUAL	A11	High	Input	9
$\overline{\text{GBL}}$	E2	Low	I/O	
GND	B5, C3, D6, D13, E17, F3, G17, H4, H7, H9, H11, H13, J6, J8, J10, J12, K7, K3, K9, K11, K13, L6, L8, L10, L12, M4, M7, M9, M11, M13, N7, P3, P9, P12, R5, R14, R17, T7, T10, U3, U13, U17, V5, V8, V11, V15	—	—	
GND	A17, A19, B13, B16, B18, E12, E19, F13, F16, F18, G19, H18, J14, L14, M15, M17, M19, N14, N16, P15, P19	—	—	15
GND_SENSE	G12, N13	—	—	19
$\overline{\text{HIT}}$	B2	Low	Output	7
$\overline{\text{HRESET}}$	D8	Low	Input	
$\overline{\text{INT}}$	D4	Low	Input	
L1_TSTCLK	G8	High	Input	9
L2_TSTCLK	B3	High	Input	10

8.2 Mechanical Dimensions for the MPC7448, 360 HCTE BGA

Figure 13 provides the mechanical dimensions and bottom surface nomenclature for the MPC7448, 360 HCTE BGA package.



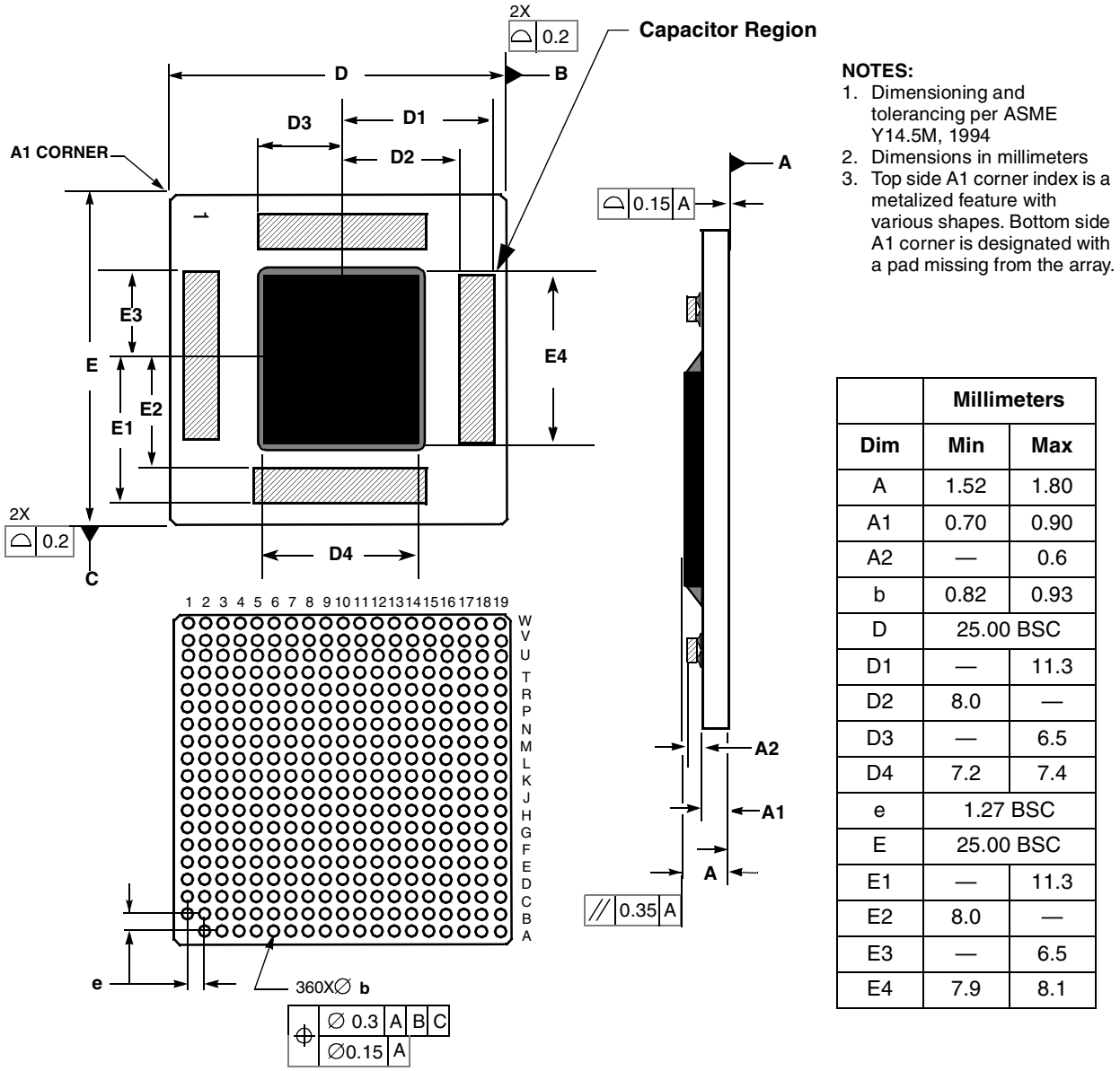
NOTES:
1. Dimensioning and tolerancing per ASME Y14.5M, 1994
2. Dimensions in millimeters.
3. Top side A1 corner index is a metalized feature with various shapes. Bottom side A1 corner is designated with a ball missing from the array.

	Millimeters	
Dim	Min	Max
A	2.32	2.80
A1	0.80	1.00
A2	0.70	0.90
A3	—	0.6
b	0.82	0.93
D	25.00 BSC	
D1	—	11.3
D2	8.0	—
D3	—	6.5
D4	7.2	7.4
e	1.27 BSC	
E	25.00 BSC	
E1	—	11.3
E2	8.0	—
E3	—	6.5
E4	7.9	8.1

Figure 13. Mechanical Dimensions and Bottom Surface Nomenclature for the MPC7448, 360 HCTE BGA Package

8.4 Mechanical Dimensions for the MPC7448, 360 HCTE LGA

Figure 13 provides the mechanical dimensions and bottom surface nomenclature for the MPC7448, 360 HCTE LGA package.



NOTES:
1. Dimensioning and tolerancing per ASME Y14.5M, 1994
2. Dimensions in millimeters
3. Top side A1 corner index is a metalized feature with various shapes. Bottom side A1 corner is designated with a pad missing from the array.

	Millimeters	
Dim	Min	Max
A	1.52	1.80
A1	0.70	0.90
A2	—	0.6
b	0.82	0.93
D	25.00 BSC	
D1	—	11.3
D2	8.0	—
D3	—	6.5
D4	7.2	7.4
e	1.27 BSC	
E	25.00 BSC	
E1	—	11.3
E2	8.0	—
E3	—	6.5
E4	7.9	8.1

Figure 14. Mechanical Dimensions and Bottom Surface Nomenclature for the MPC7448, 360 HCTE LGA Package

Table 12. MPC7448 Microprocessor PLL Configuration Example (continued)

PLL_CFG[0:5]	Example Core and VCO Frequency in MHz										
	Bus-to-Core Multiplier [5]	Core-to-VCO Multiplier [5]	Bus (SYSCLK) Frequency								
			33.3 MHz	50 MHz	66.6 MHz	75 MHz	83 MHz	100 MHz	133 MHz	167 MHz	200 MHz
100110	11x	1x			733	825	913	1100	1467		
000000	11.5x	1x			766	863	955	1150	1533		
101110	12x	1x		600	800	900	996	1200	1600		
111110	12.5x	1x		625	833	938	1038	1250	1667		
010110	13x	1x		650	865	975	1079	1300			
111000	13.5x	1x		675	900	1013	1121	1350			
110010	14x	1x		700	933	1050	1162	1400			
000110	15x	1x		750	1000	1125	1245	1500			
110110	16x	1x		800	1066	1200	1328	1600			
000010	17x	1x		850	1132	1275	1417	1700			
001010	18x	1x	600	900	1200	1350	1500				
001110	20x	1x	667	1000	1332	1500	1666				
010010	21x	1x	700	1050	1399	1575					
011010	24x	1x	800	1200	1600						
111010	28x	1x	933	1400							
001100	PLL bypass		PLL off, SYSCLK clocks core circuitry directly								
111100	PLL off		PLL off, no core clocking occurs								

Notes:

1. PLL_CFG[0:5] settings not listed are reserved.
2. The sample bus-to-core frequencies shown are for reference only. Some PLL configurations may select bus, core, or VCO frequencies which are not useful, not supported, or not tested for by the MPC7448; see Section 5.2.1, "Clock AC Specifications," for valid SYSCLK, core, and VCO frequencies.
3. In PLL-bypass mode, the SYSCLK input signal clocks the internal processor directly and the PLL is disabled. However, the bus interface unit requires a 2x clock to function. Therefore, an additional signal, EXT_QUAL, must be driven at half the frequency of SYSCLK and offset in phase to meet the required input setup t_{IVKH} and hold time t_{IXKH} (see Table 9). The result will be that the processor bus frequency will be one-half SYSCLK, while the internal processor is clocked at SYSCLK frequency. This mode is intended for factory use and emulator tool use only.
   Note: The AC timing specifications given in this document do not apply in PLL-bypass mode.
4. In PLL-off mode, no clocking occurs inside the MPC7448 regardless of the SYSCLK input.
5. Applicable when DFS modes are disabled. These multipliers change when operating in a DFS mode. See Section 9.7.5, "Dynamic Frequency Switching (DFS)" for more information.
6. Bus-to-core multipliers less than 5x require that assertion of AACK be delayed by one or two bus cycles to allow the processor to generate a response to a snooped transaction. See the *MPC7450 RISC Microprocessor Reference Manual* for more information.

9.2.4 Decoupling Recommendations

Due to the MPC7448 dynamic power management feature, large address and data buses, and high operating frequencies, the MPC7448 can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the MPC7448 system, and the MPC7448 itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer use sufficient decoupling capacitors, typically one capacitor for every V_{DD} pin, and a similar amount for the OV_{DD} pins, placed as close as possible to the power pins of the MPC7448. It is also recommended that these decoupling capacitors receive their power from separate V_{DD}, OV_{DD}, and GND power planes in the PCB, using short traces to minimize inductance.

These capacitors should have a value of 0.01 or 0.1 µF. Only ceramic surface mount technology (SMT) capacitors should be used to minimize lead inductance. Orientations where connections are made along the length of the part, such as 0204, are preferable but not mandatory. Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993) and contrary to previous recommendations for decoupling Freescale microprocessors, multiple small capacitors of equal value are recommended over using multiple values of capacitance.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V_{DD} and OV_{DD} planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low equivalent series resistance (ESR) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors are 100–330 µF (AVX TPS tantalum or Sanyo OSCON).

9.3 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. Unless otherwise noted, unused active low inputs should be tied to OV_{DD} and unused active high inputs should be connected to GND. All NC (no connect) signals must remain unconnected.

Power and ground connections must be made to all external V_{DD}, OV_{DD}, and GND pins in the MPC7448. For backward compatibility with the MPC7447, MPC7445, and MP7441, or for migrating a system originally designed for one of these devices to the MPC7448, the new power and ground signals (formerly NC, see Table 11) may be left unconnected if the core frequency is 1 GHz or less. Operation above 1 GHz requires that these additional power and ground signals be connected, and it is strongly recommended that all new designs include the additional connections. See also Section 7, “Pinout Listings,” for additional information.

The MPC7448 provides VDD_SENSE, OVDD_SENSE, and GND_SENSE pins. These pins connect directly to the power/ground planes in the device package and are intended to allow an external device to measure the voltage present on the V_{DD}, OV_{DD} and GND planes in the device package. The most common use for these signals is as a feedback signal to a power supply regulator to allow it to compensate for board losses and supply the correct voltage at the device. (Note that all voltage parameters are specified at the pins of the device.) If not used for this purpose, it is recommended that these signals be connected to test points that can be used in the event that an accurate measurement of the voltage at the device is needed during system debug. Otherwise, these signals should be connected to the appropriate power/ground planes on the circuit board or left unconnected.

9.7.1 Internal Package Conduction Resistance

For the exposed-die packaging technology described in Table 5, the intrinsic conduction thermal resistance paths are as follows:

- The die junction-to-case thermal resistance (the case is actually the top of the exposed silicon die)
- The die junction-to-board thermal resistance

Figure 24 depicts the primary heat transfer path for a package with an attached heat sink mounted to a printed-circuit board.

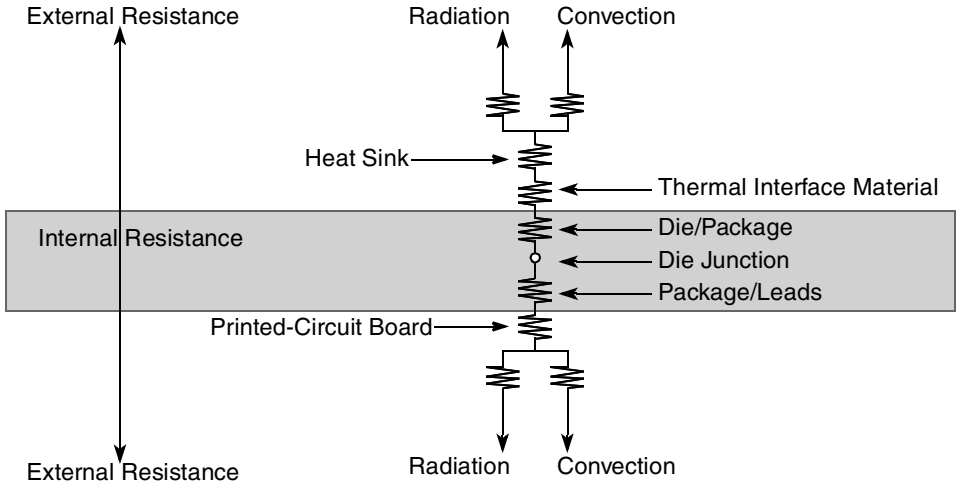


Figure 24. C4 Package with Heat Sink Mounted to a Printed-Circuit Board

Heat generated on the active side of the chip is conducted through the silicon, through the heat sink attach material (or thermal interface material), and, finally, to the heat sink, where it is removed by forced-air convection.

Because the silicon thermal resistance is quite small, the temperature drop in the silicon may be neglected for a first-order analysis. Thus, the thermal interface material and the heat sink conduction/convective thermal resistances are the dominant terms.

9.7.2 Thermal Interface Materials

A thermal interface material is recommended at the package lid-to-heat sink interface to minimize the thermal contact resistance. For those applications where the heat sink is attached by spring clip mechanism, Figure 25 shows the thermal performance of three thin-sheet thermal-interface materials (silicone, graphite/oil, fluoroether oil), a bare joint, and a joint with thermal grease as a function of contact pressure. As shown, the performance of these thermal interface materials improves with increasing contact pressure. The use of thermal grease significantly reduces the interface thermal resistance. That is, the bare joint results in a thermal resistance approximately seven times greater than the thermal grease joint.

Often, heat sinks are attached to the package by means of a spring clip to holes in the printed-circuit board (see Figure 22). Therefore, synthetic grease offers the best thermal performance due to the low interface pressure and is recommended due to the high power dissipation of the MPC7448. Of course, the selection

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Laird Technologies - Thermal (formerly Thermagon Inc.) 4707 Detroit Ave. Cleveland, OH 44102 Internet: www.lairdtech.com	888-246-905

The following section provides a heat sink selection example using one of the commercially available heat sinks.

9.7.3 Heat Sink Selection Example

For preliminary heat sink sizing, the die-junction temperature can be expressed as follows:

$$T_j = T_i + T_r + (R_{\theta JC} + R_{\theta int} + R_{\theta sa}) \times P_d$$

where:

T_j is the die-junction temperature
T_i is the inlet cabinet ambient temperature
T_r is the air temperature rise within the computer cabinet
$R_{\theta JC}$ is the junction-to-case thermal resistance
$R_{\theta int}$ is the adhesive or interface material thermal resistance
$R_{\theta sa}$ is the heat sink base-to-ambient thermal resistance
P_d is the power dissipated by the device

During operation, the die-junction temperatures (T_j) should be maintained less than the value specified in Table 4. The temperature of air cooling the component greatly depends on the ambient inlet air temperature and the air temperature rise within the electronic cabinet. An electronic cabinet inlet-air temperature (T_i) may range from 30□ to 40□C. The air temperature rise within a cabinet (T_r) may be in the range of 5□ to 10□C. The thermal resistance of the thermal interface material ($R_{\theta int}$) is typically about 1.1 □C/W. For example, assuming a T_i of 30□C, a T_r of 5□C, an HCTE package $R_{\theta JC}$ = 0.1, and a power consumption (P_d) of 25.6 W, the following expression for T_j is obtained:

Die-junction temperature: $T_j = 30□C + 5□C + (0.1□C/W + 1.1□C/W + \theta_{sa}) \times 25.6$

For this example, a $R_{\theta sa}$value of 1.53 □C/W or less is required to maintain the die junction temperature below the maximum value of Table 4.

Though the die junction-to-ambient and the heat sink-to-ambient thermal resistances are a common figure-of-merit used for comparing the thermal performance of various microelectronic packaging technologies, one should exercise caution when only using this metric in determining thermal management because no single parameter can adequately describe three-dimensional heat flow. The final die-junction operating temperature is not only a function of the component-level thermal resistance, but the system-level design and its operating conditions. In addition to the component's power consumption, a number of factors affect the final operating die-junction temperature—airflow, board population (local heat flux of adjacent components), heat sink efficiency, heat sink attach, heat sink placement, next-level interconnect technology, system air temperature rise, altitude, and so on.

Due to the complexity and variety of system-level boundary conditions for today's microelectronic equipment, the combined effects of the heat transfer mechanisms (radiation, convection, and conduction) may vary widely. For these reasons, we recommend using conjugate heat transfer models for the board as well as system-level designs.

For system thermal modeling, the MPC7448 thermal model is shown in Figure 26. Four volumes represent this device. Two of the volumes, solder ball-air and substrate, are modeled using the package outline size of the package. The other two, die and bump-underfill, have the same size as the die. The silicon die should be modeled $8.0 \times 7.3 \times 0.86$ mm^3 with the heat source applied as a uniform source at the bottom of the volume. The bump and underfill layer is modeled as $8.0 \times 7.3 \times 0.07$ mm^{3}collapsed in the z-direction with a thermal conductivity of 5.0 W/(m • K) in the z-direction. The substrate volume is $25 \times 25 \times 1.14$ mm^3 and has 9.9 W/(m • K) isotropic conductivity in the xy-plane and 2.95 W/(m • K) in the direction of the z-axis. The solder ball and air layer are modeled with the same horizontal dimensions as the substrate and is 0.8 mm thick. For the LGA package the solder and air layer is 0.1 mm thick, but the material properties are the same. It can also be modeled as a collapsed volume using orthotropic material properties: 0.034 W/(m • K) in the xy-plane direction and 11.2 W/(m • K) in the direction of the z-axis.

Conductivity	Value	Unit
Die ($8.0 \times 7.3 \times 0.86$ mm^3)		
Silicon	Temperature-dependent	W/(m • K)
Bump and Underfill ($8.0 \times 7.3 \times 0.07$ mm^3)		
k_z	5.0	W/(m • K)
Substrate ($25 \times 25 \times 1.14$ mm^3)		
k_x	9.9	W/(m • K)
k_y	9.9	
k_z	2.95	
Solder Ball and Air ($25 \times 25 \times 0.8$ mm^3)		
k_x	0.034	W/(m • K)
k_y	0.034	
k_z	11.2	

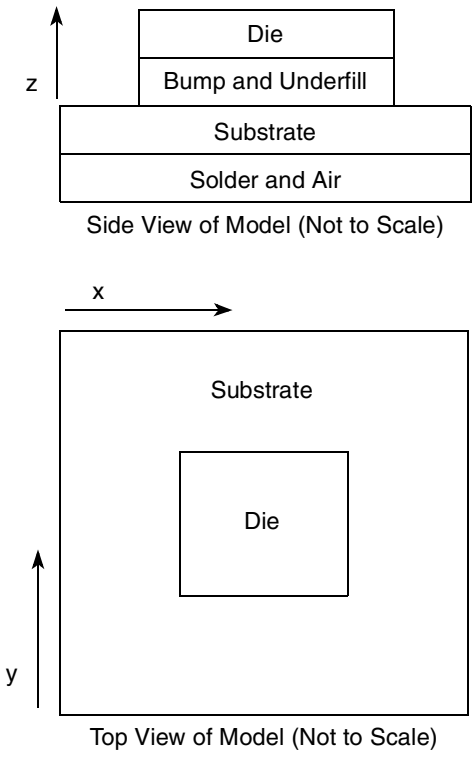


Figure 26. Recommended Thermal Model of MPC7448

Solving for T, the equation becomes:

$$nT = \frac{V_H - V_L}{1.986 \times 10^{-4}}$$

9.7.5 Dynamic Frequency Switching (DFS)

The DFS feature in the MPC7448 adds the ability to divide the processor-to-system bus ratio by two or four during normal functional operation. Divide-by-two mode is enabled by setting the HID1[DFS2] bit in software or by asserting the $\overline{\text{DFS2}}$ pin via hardware. The MPC7448 can be returned for full speed by clearing HID1[DFS2] or negating $\overline{\text{DFS2}}$. Similarly, divide-by-four mode is enabled by setting HID1[DFS4] in software or by asserting the $\overline{\text{DFS4}}$ pin. In all cases, the frequency change occurs in 1 clock cycle and no idle waiting period is required to switch between modes. Note that asserting either $\overline{\text{DFS2}}$ or $\overline{\text{DFS4}}$ overrides software control of DFS, and that asserting both $\overline{\text{DFS2}}$ and $\overline{\text{DFS4}}$ disables DFS completely, including software control. Additional information regarding DFS can be found in the *MPC7450 RISC Microprocessor Family Reference Manual.* Note that minimum core frequency requirements must be observed when enabling DFS, and the resulting core frequency must meet the requirements for f_{core_DFS} given in Table 8.

9.7.5.1 Power Consumption with DFS Enabled

Power consumption with DFS enabled can be approximated using the following formula:

$$P_{DFS} = \left[\frac{f_{DFS}}{f}\ (P - P_{DS})\right] + P_{DS}$$

Where:

P_{DFS} = Power consumption with DFS enabled
f_{DFS} = Core frequency with DFS enabled
f = Core frequency prior to enabling DFS
P = Power consumption prior to enabling DFS (see Table 7)
P_{DS} = Deep sleep mode power consumption (see Table 7)

The above is an approximation only. Power consumption with DFS enabled is not tested or guaranteed.

9.7.5.2 Bus-to-Core Multiplier Constraints with DFS

DFS is not available for all bus-to-core multipliers as configured by PLL_CFG[0:5] during hard reset. The complete listing is shown in Table 16. Shaded cells represent DFS modes that are not available for a particular PLL_CFG[0:5] setting. Should software or hardware attempt to transition to a multiplier that is not supported, the device will remain at its current multiplier. For example, if a transition from DFS-disabled to an unsupported divide-by-2 or divide-by-4 setting is attempted, the bus-to-core multiplier will remain at the setting configured by the PLL_CFG[0:5] pins. In the case of an attempted transition from a supported divide-by-2 mode to an unsupported divide-by-4 mode, the device will remain in divide-by-2 mode. In all cases, the HID1[PC0-5] bits will correctly reflect the current bus-to-core frequency multiplier.

Table 17. Document Revision History (continued)

Revision	Date	Substantive Change(s)
2		Table 6: Added separate input leakage specification for BVSEL0, $\overline{\text{LSSD\_MODE}}$, $\overline{\text{TCK}}$, TDI, TMS, $\overline{\text{TRST}}$ signals to correctly indicate leakage current for signals with internal pull-up resistors. Section 5.1: Added paragraph preceding Table 7 and edited notes in Table 7 to clarify core frequencies at which power consumption is measured. Section 5.3: Removed voltage derating specifications; this feature has been made redundant by new device offerings and is no longer supported. Changed names of “Typical–Nominal” and “Typical–Thermal” power consumption parameters to “Typical” and “Thermal”, respectively. (Name change only–no specifications were changed.) Table 11: Revised Notes 16, 18, and 19 to reflect current recommendations for connection of SENSE pins. Section 9.3: Added paragraph explaining connection recommendations for SENSE pins. (See also Table 11 entry above.) Table 19: Updated table to reflect changes in specifications for MC7448xxnnnnNC devices. Table 9: Changed all instances of TT[0:3] to TT[0:4] Removed mention of these input signals from output valid times and output hold times: • AACK, CKSTP_IN, DT[0:3] Figure 17: Modified diagram slightly to correctly show constraint on SYSCLK ramping is related to V_{DD} voltage, not AV_{DD} voltage. (Diagram clarification only; no change in power sequencing requirements.) Added Table 20 to reflect introduction of extended temperature devices and associated hardware specification addendum.
1		Added 1600 MHz, 1420 MHz, and 1000 MHz devices Section 4: corrected die size Table 2: Revised Note 4 to consider overshoot/undershoot and combined with Note 5. Table 4: Revised operating voltage for 1700 MHz device from ± 50 mV to +20 mV / –50 mV. Table 7: Updated and expanded table to include Typical – Nominal power consumption. Table 11: Added voltage derating information for 1700 MHz devices; this feature is not supported at this time for other speed grades. Added transient specifications for VDD power supply in Section 9.2.3, added Table 15 and Figure 19 and renumbered subsequent tables and figures. Moved Decoupling Recommendations from Section 9.4 to Section 9.2.4 and renumbered subsequent sections. Section 9.2.1: Revised power sequencing requirements. Section 9.7.4: Added thermal diode ideality factor information (previously TBD). Table 17: Expanded table to show HID1 register values when DFS modes are enabled. Section 11.2: updated to include additional N-spec device speed grades Tables 18 and 19: corrected PVR values and added “MC” product code prefix
0		Initial public release.

Table 20. Part Numbers Addressed by MC7448T*xxnnnn*N*x* Series Hardware Specification Addendum (Document Order No. MPC7448ECS02AD)

xx	**7448**	**T**	***xx***	***nnnn***	**N**	***x***

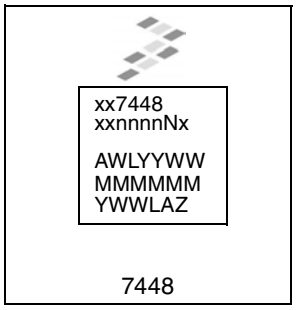
Product Code	Part Identifier	Specification Modifier	Package	Processor Frequency	Application Modifier	Revision Level
MC PPC[1]	7448	T = Extended Temperature Device	HX = HCTE BGA	1400	N: 1.15 V ± 50 mV – 40 to 105 °C	C: 2.1; PVR = 0x8004_0201 D: 2.2; PVR = 0x8004_0202
				1267 Revision C only	N: 1.1 V ± 50 mV – 40 to 105 °C	
				1267 Revision D only	N: 1.05 V ± 50 mV – 40 to 105 °C	
				1000	N: 1.0 V ± 50 mV – 40 to 105 °C	

Notes:

1. The P prefix in a Freescale part number designates a “Pilot Production Prototype” as defined by Freescale SOP 3-13. These parts have only preliminary reliability and characterization data. Before pilot production prototypes can be shipped, written authorization from the customer must be on file in the applicable sales office acknowledging the qualification status and the fact that product changes may still occur as pilot production prototypes are shipped.

11.3 Part Marking

Parts are marked as the example shown in Figure 27.



BGA/LGA

Notes:

AWLYYWW is the test code, where YYWW is the date code (YY = year, WW = work week)
MMMMMM is the M00 (mask) number.
YWWLAZ is the assembly traceability code.

Figure 27. Part Marking for BGA and LGA Device

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