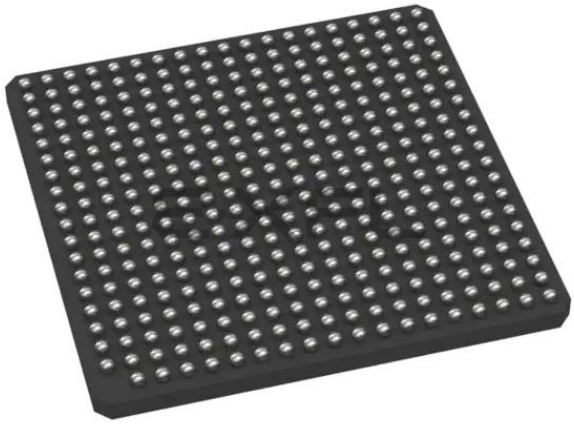

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC G4
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.4GHz
Co-Processors/DSP	Multimedia; SIMD
RAM Controllers	-
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	1.5V, 1.8V, 2.5V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	360-BCBGA, FCCBGA
Supplier Device Package	360-FCCBGA (25x25)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmc7448hx1400nc

2 Features

This section summarizes features of the MPC7448 implementation.

Major features of the MPC7448 are as follows:

- High-performance, superscalar microprocessor
  - Up to four instructions can be fetched from the instruction cache at a time.
  - Up to three instructions plus a branch instruction can be dispatched to the issue queues at a time.
  - Up to 12 instructions can be in the instruction queue (IQ).
  - Up to 16 instructions can be at some stage of execution simultaneously.
  - Single-cycle execution for most instructions
  - One instruction per clock cycle throughput for most instructions
  - Seven-stage pipeline control
- Eleven independent execution units and three register files
  - Branch processing unit (BPU) features static and dynamic branch prediction
    - 128-entry (32-set, four-way set-associative) branch target instruction cache (BTIC), a cache of branch instructions that have been encountered in branch/loop code sequences. If a target instruction is in the BTIC, it is fetched into the instruction queue a cycle sooner than it can be made available from the instruction cache. Typically, a fetch that hits the BTIC provides the first four instructions in the target stream.
    - 2048-entry branch history table (BHT) with 2 bits per entry for four levels of prediction—not taken, strongly not taken, taken, and strongly taken
    - Up to three outstanding speculative branches
    - Branch instructions that do not update the count register (CTR) or link register (LR) are often removed from the instruction stream.
    - Eight-entry link register stack to predict the target address of Branch Conditional to Link Register (**bclr**) instructions
  - Four integer units (IUs) that share 32 GPRs for integer operands
    - Three identical IUs (IU1a, IU1b, and IU1c) can execute all integer instructions except multiply, divide, and move to/from special-purpose register instructions.
    - IU2 executes miscellaneous instructions, including the CR logical operations, integer multiplication and division instructions, and move to/from special-purpose register instructions.
  - Five-stage FPU and 32-entry FPR file
    - Fully IEEE Std. 754™-1985–compliant FPU for both single- and double-precision operations
    - Supports non-IEEE mode for time-critical operations
    - Hardware support for denormalized numbers
    - Thirty-two 64-bit FPRs for single- or double-precision operands

- Efficient data flow
  - Although the VR/LSU interface is 128 bits, the L1/L2 bus interface allows up to 256 bits.
  - The L1 data cache is fully pipelined to provide 128 bits/cycle to or from the VRs.
  - The L2 cache is fully pipelined to provide 32 bytes per clock every other cycle to the L1 caches.
  - As many as 16 out-of-order transactions can be present on the MPX bus.
  - Store merging for multiple store misses to the same line. Only coherency action taken (address-only) for store misses merged to all 32 bytes of a cache block (no data tenure needed).
  - Three-entry finished store queue and five-entry completed store queue between the LSU and the L1 data cache
  - Separate additional queues for efficient buffering of outbound data (such as castouts and write-through stores) from the L1 data cache and L2 cache
- Multiprocessing support features include the following:
  - Hardware-enforced, MESI cache coherency protocols for data cache
  - Load/store with reservation instruction pair for atomic memory references, semaphores, and other multiprocessor operations
- Power and thermal management
  - Dynamic frequency switching (DFS) feature allows processor core frequency to be halved or quartered through software to reduce power consumption.
  - The following three power-saving modes are available to the system:
    - Nap—Instruction fetching is halted. Only the clocks for the time base, decrementer, and JTAG logic remain running. The part goes into the doze state to snoop memory operations on the bus and then back to nap using a $\overline{\text{QREQ}}$/$\overline{\text{QACK}}$ processor-system handshake protocol.
    - Sleep—Power consumption is further reduced by disabling bus snooping, leaving only the PLL in a locked and running state. All internal functional units are disabled.
    - Deep sleep—When the part is in the sleep state, the system can disable the PLL. The system can then disable the SYSCLK source for greater system power savings. Power-on reset procedures for restarting and relocking the PLL must be followed upon exiting the deep sleep state.
  - Instruction cache throttling provides control of instruction fetching to limit device temperature.
  - A new temperature diode that can determine the temperature of the microprocessor
- Performance monitor can be used to help debug system designs and improve software efficiency.
- In-system testability and debugging features through JTAG boundary-scan capability
- Testability
  - LSSD scan design
  - IEEE Std. 1149.1™ JTAG interface

4 General Parameters

The following list summarizes the general parameters of the MPC7448:

Technology	90 nm CMOS SOI, nine-layer metal	
Die size	8.0 mm × 7.3 mm	
Transistor count	90 million	
Logic design	Mixed static and dynamic	
Packages	Surface mount 360 ceramic ball grid array (HCTE)	
	Surface mount 360 ceramic land grid array (HCTE)	
	Surface mount 360 ceramic ball grid array with lead-free spheres (HCTE)	
Core power supply	1.30 V	(1700 MHz device)
	1.25 V	(1600 MHz device)
	1.20 V	(1420 MHz device)
	1.15 V	(1000 MHz device)
I/O power supply	1.5 V, 1.8 V, or 2.5 V	

5 Electrical and Thermal Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC7448.

5.1 DC Electrical Characteristics

The tables in this section describe the MPC7448 DC electrical characteristics. Table 2 provides the absolute maximum ratings. See Section 9.2, “Power Supply Design and Sequencing,” for power sequencing requirements.

Table 2. Absolute Maximum Ratings [1]

Characteristic		Symbol	Maximum Value	Unit	Notes
Core supply voltage		V_{DD}	–0.3 to 1.4	V	2
PLL supply voltage		AV_{DD}	–0.3 to 1.4	V	2
Processor bus supply voltage	I/O Voltage Mode = 1.5 V	OV_{DD}	–0.3 to 1.8	V	3
	I/O Voltage Mode = 1.8 V		–0.3 to 2.2		3
	I/O Voltage Mode = 2.5 V		–0.3 to 3.0		3
Input voltage	Processor bus	V_{in}	–0.3 to OV_{DD} + 0.3	V	4
	JTAG signals	V_{in}	–0.3 to OV_{DD} + 0.3	V	
Storage temperature range		T_{stg}	– 55 to 150	•C	

Notes:

1. Functional and tested operating conditions are given in Table 4. Absolute maximum ratings are stress ratings only and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. See Section 9.2, “Power Supply Design and Sequencing” for power sequencing requirements.
3. Bus must be configured in the corresponding I/O voltage mode; see Table 3.
4. **Caution**: V_{in} must not exceed OV_{DD} by more than 0.3 V at any time including during power-on reset except as allowed by the overshoot specifications. V_{in} may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 2.

5.2 AC Electrical Characteristics

This section provides the AC electrical characteristics for the MPC7448. After fabrication, functional parts are sorted by maximum processor core frequency as shown in Section 5.2.1, “Clock AC Specifications,” and tested for conformance to the AC specifications for that frequency. The processor core frequency, determined by the bus (SYSCLK) frequency and the settings of the PLL_CFG[0:5] signals, can be dynamically modified using dynamic frequency switching (DFS). Parts are sold by maximum processor core frequency; see Section 11, “Part Numbering and Marking,” for information on ordering parts. DFS is described in Section 9.7.5, “Dynamic Frequency Switching (DFS).”

5.2.1 Clock AC Specifications

Table 8 provides the clock AC timing specifications as defined in Figure 3 and represents the tested operating frequencies of the devices. The maximum system bus frequency, f_{SYSCLK}, given in Table 8, is considered a practical maximum in a typical single-processor system. This does not exclude multi-processor systems, but these typically require considerably more design effort to achieve the maximum rated bus frequency. The actual maximum SYSCLK frequency for any application of the MPC7448 will be a function of the AC timings of the microprocessor(s), the AC timings for the system controller, bus loading, circuit board topology, trace lengths, and so forth, and may be less than the value given in Table 8.

Table 9. Processor Bus AC Timing Specifications[1] (continued)

At recommended operating conditions. See Table 4.

Parameter	Symbol [2]	All Speed Grades		Unit	Notes
		Min	Max		
SYSCLK to output high impedance (all except $\overline{TS}$, $\overline{ARTRY}$, $\overline{SHD0}$, $\overline{SHD1}$)	t_{KHOZ}	—	1.8	ns	5
SYSCLK to $\overline{TS}$ high impedance after precharge	t_{KHTSPZ}	—	1	t_{SYSCLK}	3, 4, 5
Maximum delay to $\overline{ARTRY}$/$\overline{SHD0}$/$\overline{SHD1}$ precharge	t_{KHARP}	—	1	t_{SYSCLK}	3, 5, 6, 7
SYSCLK to $\overline{ARTRY}$/$\overline{SHD0}$/$\overline{SHD1}$ high impedance after precharge	t_{KHARPZ}	—	2	t_{SYSCLK}	3, 5, 6, 7

Notes:

1. All input specifications are measured from the midpoint of the signal in question to the midpoint of the rising edge of the input SYSCLK. All output specifications are measured from the midpoint of the rising edge of SYSCLK to the midpoint of the signal in question. All output timings assume a purely resistive 50-Ω load (see Figure 4). Input and output timings are measured at the pin; time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. The symbology used for timing specifications herein follows the pattern of $t_{(signal)(state)(reference)(state)}$ for inputs and $t_{(reference)(state)(signal)(state)}$ for outputs. For example, t_{IVKH} symbolizes the time input signals (I) reach the valid state (V) relative to the SYSCLK reference (K) going to the high (H) state or input setup time. And t_{KHOV} symbolizes the time from SYSCLK(K) going high (H) until outputs (O) are valid (V) or output valid time. Input hold time can be read as the time that the input signal (I) went invalid (X) with respect to the rising clock edge (KH) (note the position of the reference and its state for inputs) and output hold time can be read as the time from the rising edge (KH) until the output went invalid (OX).
3. t_{sysclk} is the period of the external clock (SYSCLK) in ns. The numbers given in the table must be multiplied by the period of SYSCLK to compute the actual time duration (in ns) of the parameter in question.
4. According to the bus protocol, $\overline{TS}$ is driven only by the currently active bus master. It is asserted low and precharged high before returning to high impedance, as shown in Figure 6. The nominal precharge width for $\overline{TS}$ is t_{SYSCLK}, that is, one clock period. Since no master can assert $\overline{TS}$ on the following clock edge, there is no concern regarding contention with the precharge. Output valid and output hold timing is tested for the signal asserted. Output valid time is tested for precharge.The high-impedance behavior is guaranteed by design.
5. Guaranteed by design and not tested
6. According to the bus protocol, $\overline{ARTRY}$ can be driven by multiple bus masters through the clock period immediately following $\overline{AACK}$. Bus contention is not an issue because any master asserting $\overline{ARTRY}$ will be driving it low. Any master asserting it low in the first clock following $\overline{AACK}$ will then go to high impedance for a fraction of a cycle, then negated for up to an entire cycle (crossing a bus cycle boundary) before being three-stated again. The nominal precharge width for $\overline{ARTRY}$ is 1.0 t_{SYSCLK}; that is, it should be high impedance as shown in Figure 6 before the first opportunity for another master to assert $\overline{ARTRY}$. Output valid and output hold timing is tested for the signal asserted.The high-impedance behavior is guaranteed by design.
7. According to the MPX bus protocol, $\overline{SHD0}$ and $\overline{SHD1}$ can be driven by multiple bus masters beginning two cycles after $\overline{TS}$. Timing is the same as $\overline{ARTRY}$, that is, the signal is high impedance for a fraction of a cycle, then negated for up to an entire cycle (crossing a bus cycle boundary) before being three-stated again. The nominal precharge width for $\overline{SHD0}$ and $\overline{SHD1}$ is 1.0 t_{SYSCLK}. The edges of the precharge vary depending on the programmed ratio of core to bus (PLL configurations).
8. $\overline{BMODE}$[0:1] and BVSEL[0:1] are mode select inputs. $\overline{BMODE}$[0:1] are sampled before and after $\overline{HRESET}$ negation. BVSEL[0:1] are sampled before $\overline{HRESET}$ negation. These parameters represent the input setup and hold times for each sample. These values are guaranteed by design and not tested. $\overline{BMODE}$[0:1] must remain stable after the second sample; BVSEL[0:1] must remain stable after the first (and only) sample. See Figure 5 for sample timing.

Figure 6 provides the input/output timing diagram for the MPC7448.

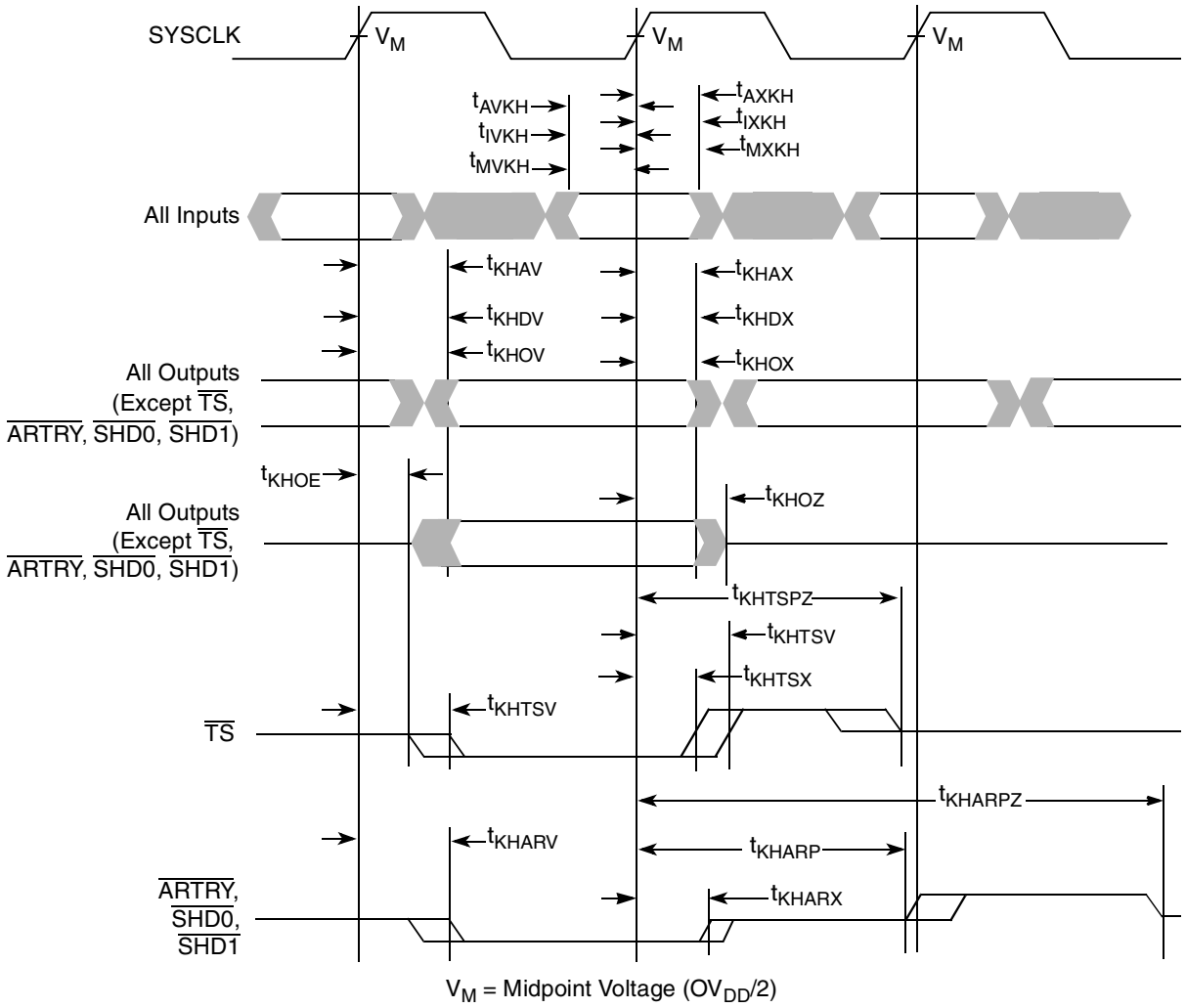


Figure 6. Input/Output Timing Diagram

5.2.3 IEEE Std. 1149.1 AC Timing Specifications

Table 10 provides the IEEE Std. 1149.1 (JTAG) AC timing specifications as defined in Figure 8 through Figure 11.

Table 10. JTAG AC Timing Specifications (Independent of SYSCLK)[1]

At recommended operating conditions. See Table 4.

Parameter	Symbol	Min	Max	Unit	Notes
TCK frequency of operation	f_{TCLK}	0	33.3	MHz	
TCK cycle time	t_{TCLK}	30	—	ns	
TCK clock pulse width measured at 1.4 V	t_{JHJL}	15	—	ns	
TCK rise and fall times	t_{JR} and t_{JF}	—	2	ns	
$\overline{\text{TRST}}$ assert time	t_{TRST}	25	—	ns	2
Input setup times: Boundary-scan data TMS, TDI	 t_{DVJH} t_{IVJH}	 4 0	 — —	ns	3
Input hold times: Boundary-scan data TMS, TDI	 t_{DXJH} t_{IXJH}	 20 25	 — —	ns	3
Valid times: Boundary-scan data TDO	 t_{JLDV} t_{JLOV}	 4 4	 20 25	ns	4
Output hold times: Boundary-scan data TDO	 t_{JLDX} t_{JLOX}	 30 30	 — —	ns	4
TCK to output high impedance: Boundary-scan data TDO	 t_{JLDZ} t_{JLOZ}	 3 3	 19 9	ns	4, 5

Notes:

1. All outputs are measured from the midpoint voltage of the falling/rising edge of TCLK to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load (see Figure 7). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. $\overline{\text{TRST}}$ is an asynchronous level sensitive signal. The time is for test purposes only.
3. Non-JTAG signal input timing with respect to TCK.
4. Non-JTAG signal output timing with respect to TCK.
5. Guaranteed by design and characterization.

Figure 7 provides the AC test load for TDO and the boundary-scan outputs of the MPC7448.

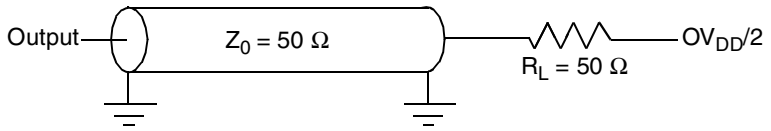


Figure 7. Alternate AC Test Load for the JTAG Interface

Figure 8 provides the JTAG clock input timing diagram.

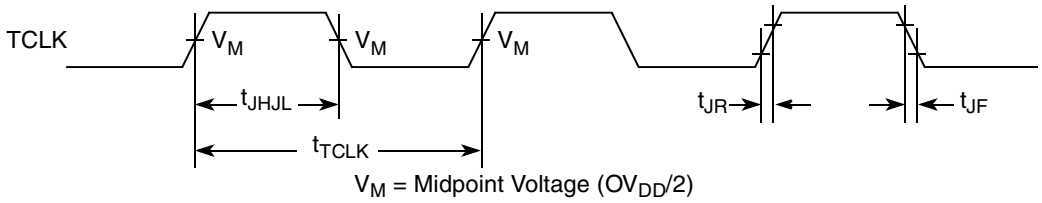


Figure 8. JTAG Clock Input Timing Diagram

Figure 9 provides the $\overline{\text{TRST}}$ timing diagram.

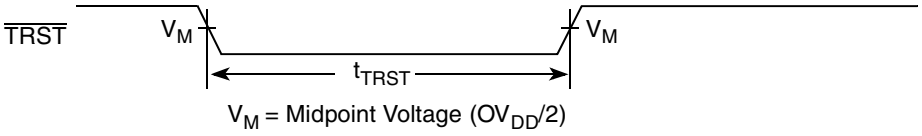


Figure 9. $\overline{\text{TRST}}$ Timing Diagram

Figure 10 provides the boundary-scan timing diagram.

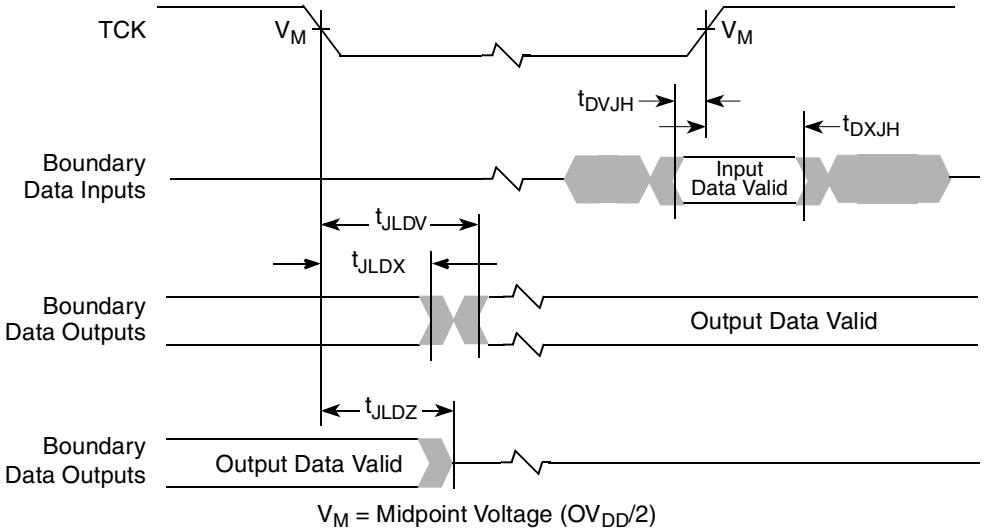


Figure 10. Boundary-Scan Timing Diagram

Table 11. Pinout Listing for the MPC7448, 360 HCTE Package

Signal Name	Pin Number	Active	I/O	Notes
A[0:35]	E11, H1, C11, G3, F10, L2, D11, D1, C10, G2, D12, L3, G4, T2, F4, V1, J4, R2, K5, W2, J2, K4, N4, J3, M5, P5, N3, T1, V2, U1, N5, W1, B12, C4, G10, B11	High	I/O	2
$\overline{\text{AACK}}$	R1	Low	Input	
AP[0:4]	C1, E3, H6, F5, G7	High	I/O	2
$\overline{\text{ARTRY}}$	N2	Low	I/O	3
AV_{DD}	A8	—	Input	
$\overline{\text{BG}}$	M1	Low	Input	
$\overline{\text{BMODE0}}$	G9	Low	Input	4
$\overline{\text{BMODE1}}$	F8	Low	Input	5
$\overline{\text{BR}}$	D2	Low	Output	
BVSEL0	B7	High	Input	1, 6
BVSEL1	E10	High	Input	1, 20
$\overline{\text{CI}}$	J1	Low	Output	
$\overline{\text{CKSTP\_IN}}$	A3	Low	Input	
$\overline{\text{CKSTP\_OUT}}$	B1	Low	Output	
CLK_OUT	H2	High	Output	
D[0:63]	R15, W15, T14, V16, W16, T15, U15, P14, V13, W13, T13, P13, U14, W14, R12, T12, W12, V12, N11, N10, R11, U11, W11, T11, R10, N9, P10, U10, R9, W10, U9, V9, W5, U6, T5, U5, W7, R6, P7, V6, P17, R19, V18, R18, V19, T19, U19, W19, U18, W17, W18, T16, T18, T17, W3, V17, U4, U8, U7, R7, P6, R8, W8, T8	High	I/O	
$\overline{\text{DBG}}$	M2	Low	Input	
$\overline{\text{DFS2}}$	A12	Low	Input	20, 21
$\overline{\text{DFS4}}$	B6	Low	Input	12, 20, 21
DP[0:7]	T3, W4, T4, W9, M6, V3, N8, W6	High	I/O	
$\overline{\text{DRDY}}$	R3	Low	Output	7
DTI[0:3]	G1, K1, P1, N1	High	Input	8
EXT_QUAL	A11	High	Input	9
$\overline{\text{GBL}}$	E2	Low	I/O	
GND	B5, C3, D6, D13, E17, F3, G17, H4, H7, H9, H11, H13, J6, J8, J10, J12, K7, K3, K9, K11, K13, L6, L8, L10, L12, M4, M7, M9, M11, M13, N7, P3, P9, P12, R5, R14, R17, T7, T10, U3, U13, U17, V5, V8, V11, V15	—	—	
GND	A17, A19, B13, B16, B18, E12, E19, F13, F16, F18, G19, H18, J14, L14, M15, M17, M19, N14, N16, P15, P19	—	—	15
GND_SENSE	G12, N13	—	—	19
$\overline{\text{HIT}}$	B2	Low	Output	7
$\overline{\text{HRESET}}$	D8	Low	Input	
$\overline{\text{INT}}$	D4	Low	Input	
L1_TSTCLK	G8	High	Input	9
L2_TSTCLK	B3	High	Input	10

8 Package Description

The following sections provide the package parameters and mechanical dimensions for the HCTE package.

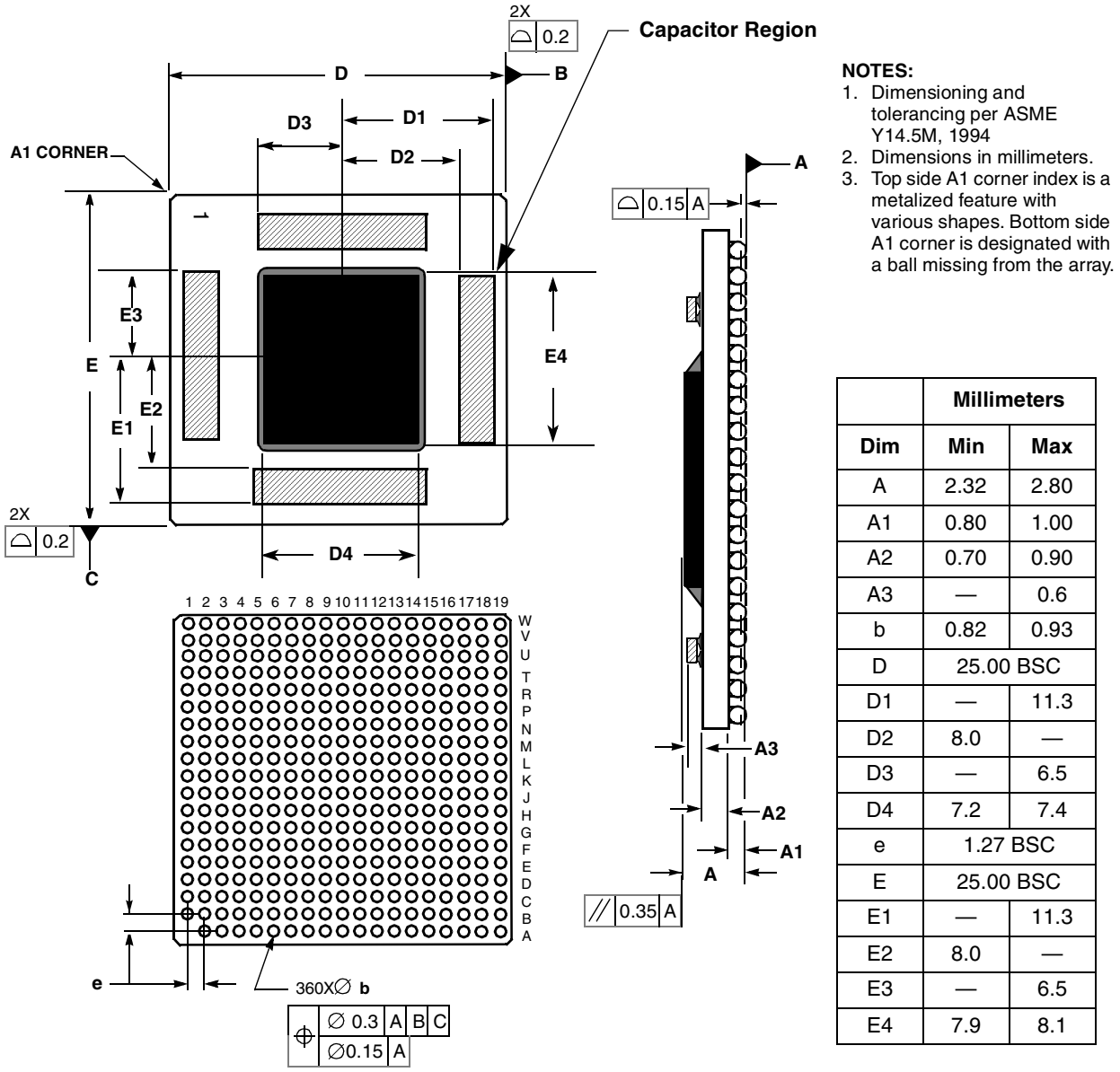
8.1 Package Parameters for the MPC7448, 360 HCTE BGA

The package parameters are as provided in the following list. The package type is 25 × 25 mm, 360-lead high coefficient of thermal expansion ceramic ball grid array (HCTE).

Package outline	25 × 25 mm
Interconnects	360 (19 × 19 ball array – 1)
Pitch	1.27 mm (50 mil)
Minimum module height	2.32 mm
Maximum module height	2.80 mm
Ball diameter	0.89 mm (35 mil)
Coefficient of thermal expansion	12.3 ppm/°C

8.2 Mechanical Dimensions for the MPC7448, 360 HCTE BGA

Figure 13 provides the mechanical dimensions and bottom surface nomenclature for the MPC7448, 360 HCTE BGA package.



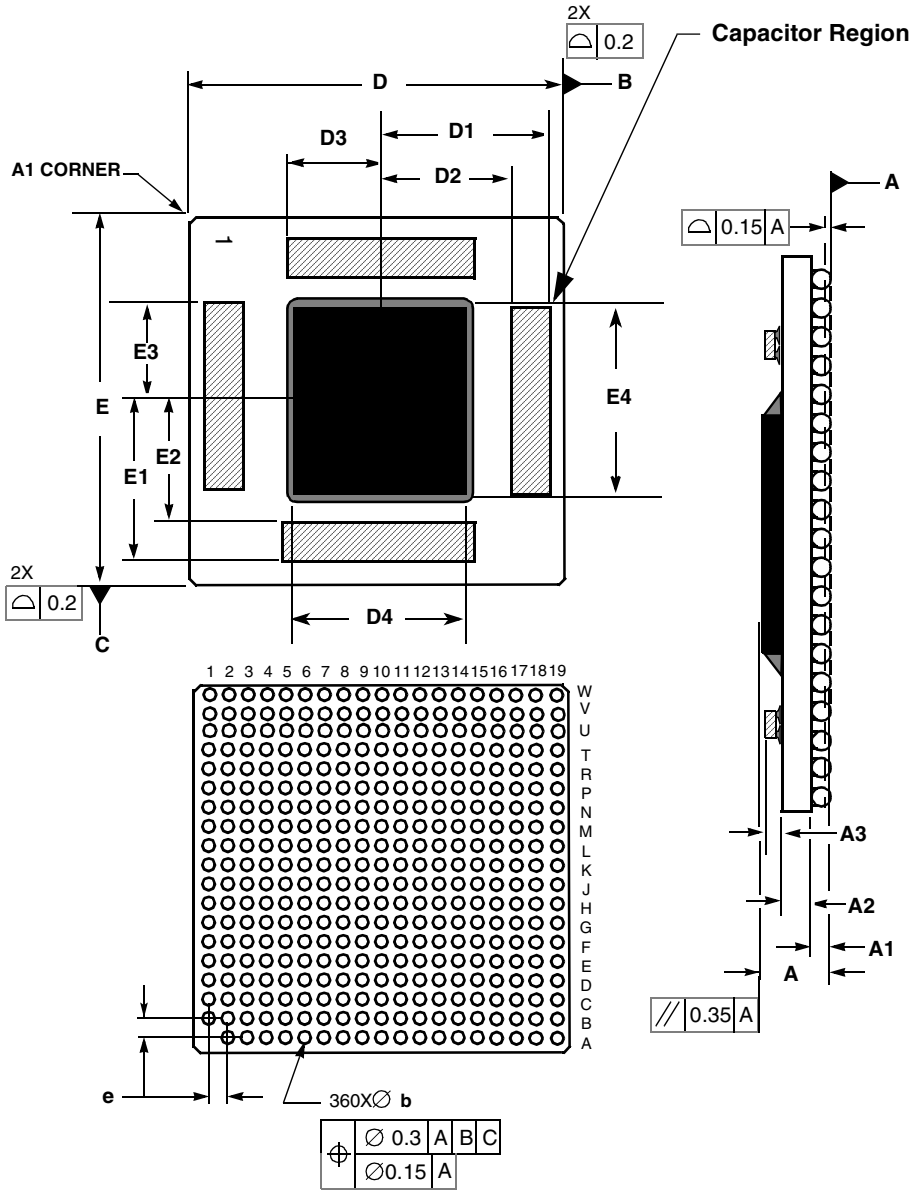
NOTES:
1. Dimensioning and tolerancing per ASME Y14.5M, 1994
2. Dimensions in millimeters.
3. Top side A1 corner index is a metalized feature with various shapes. Bottom side A1 corner is designated with a ball missing from the array.

	Millimeters	
Dim	Min	Max
A	2.32	2.80
A1	0.80	1.00
A2	0.70	0.90
A3	—	0.6
b	0.82	0.93
D	25.00 BSC	
D1	—	11.3
D2	8.0	—
D3	—	6.5
D4	7.2	7.4
e	1.27 BSC	
E	25.00 BSC	
E1	—	11.3
E2	8.0	—
E3	—	6.5
E4	7.9	8.1

Figure 13. Mechanical Dimensions and Bottom Surface Nomenclature for the MPC7448, 360 HCTE BGA Package

8.6 Mechanical Dimensions for the MPC7448, 360 HCTE RoHS-Compliant BGA

Figure 13 provides the mechanical dimensions and bottom surface nomenclature for the MPC7448, 360 HCTE BGA package with RoHS-compliant lead-free spheres.



NOTES:
1. Dimensioning and tolerancing per ASME Y14.5M, 1994
2. Dimensions in millimeters.
3. Top side A1 corner index is a metalized feature with various shapes. Bottom side A1 corner is designated with a ball missing from the array.
4. Dimension A1 represents the collapsed sphere diameter.

	Millimeters	
Dim	**Min**	**Max**
A	1.92	2.40
A1 [4]	0.40	0.60
A2	0.70	0.90
A3	—	0.6
b	0.60	0.90
D	25.00 BSC	
D1	—	11.3
D2	8.0	—
D3	—	6.5
D4	7.2	7.4
e	1.27 BSC	
E	25.00 BSC	
E1	—	11.3
E2	8.0	—
E3	—	6.5
E4	7.9	8.1

Figure 15. Mechanical Dimensions and Bottom Surface Nomenclature for the MPC7448, 360 HCTE RoHS-Compliant BGA Package

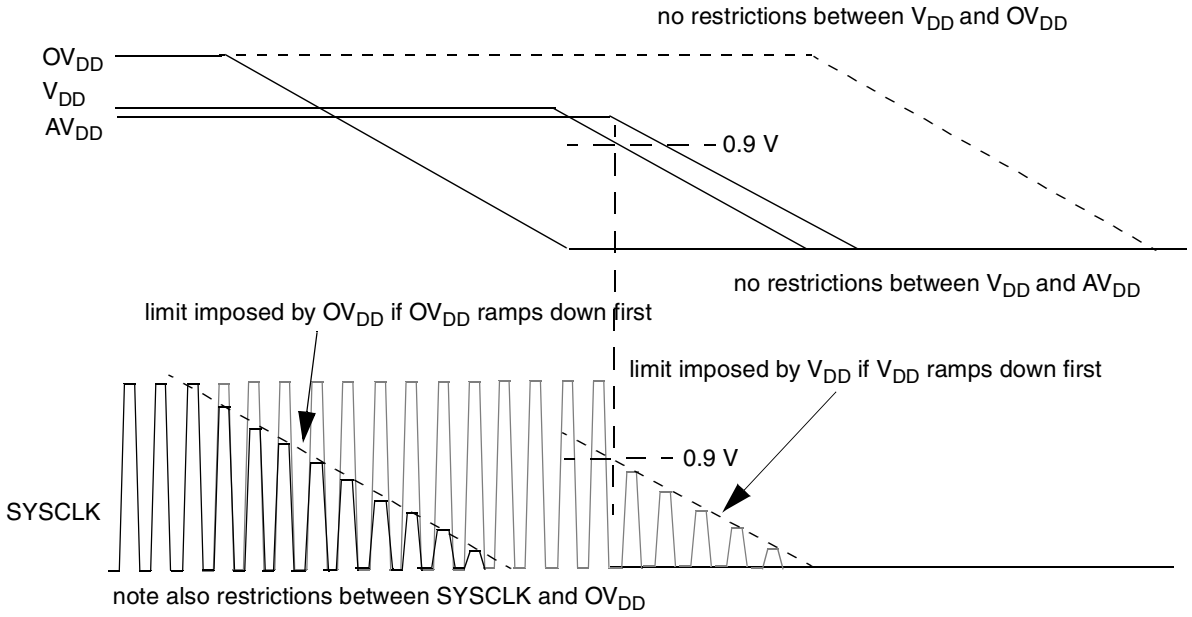


Figure 17. MPC7448 Power Down Sequencing Requirements

There is no requirement regarding AV_{DD} during power down, but it is recommended that AV_{DD} track V_{DD} within the RC time constant of the PLL filter circuit described in Section 9.2.2, "PLL Power Supply Filtering" (nominally 100 µs).

9.2.2 PLL Power Supply Filtering

The AV_{DD} power signal is provided on the MPC7448 to provide power to the clock generation PLL. To ensure stability of the internal clock, the power supplied to the AV_{DD} input signal should be filtered of any noise in the 500-KHz to 10-MHz resonant frequency range of the PLL. The circuit shown in Figure 18 using surface mount capacitors with minimum effective series inductance (ESL) is strongly recommended. In addition to filtering noise from the AV_{DD} input, it also provides the required delay between V_{DD} and AV_{DD} as described in Section 9.2.1, "Power Supply Sequencing."

The circuit should be placed as close as possible to the AV_{DD} pin to minimize noise coupled from nearby circuits. It is often possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of the device footprint.

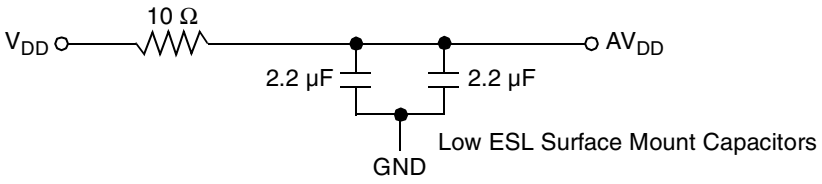


Figure 18. PLL Power Supply Filter Circuit

9.4 Output Buffer DC Impedance

The MPC7448 processor bus drivers are characterized over process, voltage, and temperature. To measure Z_0, an external resistor is connected from the chip pad to OV_{DD} or GND. The value of each resistor is varied until the pad voltage is $OV_{DD}/2$. Figure 20 shows the driver impedance measurement.

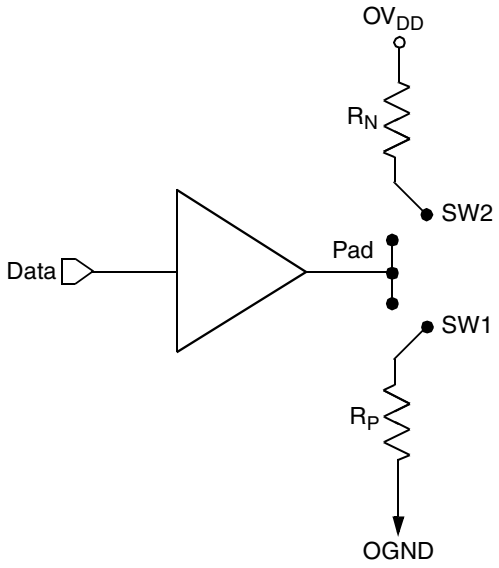


Figure 20. Driver Impedance Measurement

The output impedance is the average of two components—the resistances of the pull-up and pull-down devices. When data is held low, SW2 is closed (SW1 is open), and R_N is trimmed until the voltage at the pad equals $OV_{DD}/2$. R_N then becomes the resistance of the pull-down devices. When data is held high, SW1 is closed (SW2 is open), and R_P is trimmed until the voltage at the pad equals $OV_{DD}/2$. R_P then becomes the resistance of the pull-up devices. R_P and R_N are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N)/2$.

Table 15 summarizes the signal impedance results. The impedance increases with junction temperature and is relatively unaffected by bus voltage.

Table 15. Impedance Characteristics

At recommended operating conditions. See Table 4

Impedance		Processor Bus	Unit
Z_0	Typical	33–42	Ω
	Maximum	31–51	Ω

9.5 Pull-Up/Pull-Down Resistor Requirements

The MPC7448 requires high-resistive (weak: 4.7-KΩ) pull-up resistors on several control pins of the bus interface to maintain the control signals in the negated state after they have been actively negated and released by the MPC7448 or other bus masters. These pins are: $\overline{TS}$, $\overline{ARTRY}$, $\overline{SHDO}$, and $\overline{SHD1}$.

Some pins designated as being factory test pins must be pulled up to OV_{DD} or down to GND to ensure proper device operation. The pins that must be pulled up to OV_{DD} are $\overline{LSSD\_MODE}$ and TEST[0:3]; the pins that must be pulled down to GND are L1_TSTCLK and TEST[4]. The $\overline{CKSTP\_IN}$ signal should

likewise be pulled up through a pull-up resistor (weak or stronger: 4.7–1 KΩ) to prevent erroneous assertions of this signal.

In addition, the MPC7448 has one open-drain style output that requires a pull-up resistor (weak or stronger: 4.7–1 KΩ) if it is used by the system. This pin is $\overline{\text{CKSTP\_OUT}}$.

BVSEL0 and BVSEL1 should not be allowed to float, and should be configured either via pull-up or pull-down resistors or actively driven by external logic. If pull-down resistors are used to configure BVSEL0 or BVSEL1, the resistors should be less than 250 Ω (see Table 11). Because PLL_CFG[0:5] must remain stable during normal operation, strong pull-up and pull-down resistors (1 KΩ or less) are recommended to configure these signals in order to protect against erroneous switching due to ground bounce, power supply noise, or noise coupling.

During inactive periods on the bus, the address and transfer attributes may not be driven by any master and may, therefore, float in the high-impedance state for relatively long periods of time. Because the MPC7448 must continually monitor these signals for snooping, this float condition may cause excessive power draw by the input receivers on the MPC7448 or by other receivers in the system. These signals can be pulled up through weak (10-KΩ) pull-up resistors by the system, address bus driven mode enabled (see the *MPC7450 RISC Microprocessor Family Users' Manual* for more information on this mode), or they may be otherwise driven by the system during inactive periods of the bus to avoid this additional power draw. Preliminary studies have shown the additional power draw by the MPC7448 input receivers to be negligible and, in any event, none of these measures are necessary for proper device operation. The snooped address and transfer attribute inputs are: A[0:35], AP[0:4], TT[0:4], $\overline{\text{CI}}$, $\overline{\text{WT}}$, and $\overline{\text{GBL}}$.

If address or data parity is not used by the system, and respective parity checking is disabled through HID1, the input receivers for those pins are disabled and do not require pull-up resistors, therefore they may be left unconnected by the system. If extended addressing is not used (HID0[XAEN] = 0), A[0:3] are unused and must be pulled low to GND through weak pull-down resistors; additionally, if address parity checking is enabled (HID1[EBA] = 1) and extended addressing is not used, AP[0] must be pulled up to OV_{DD} through a weak pull-up resistor. If the MPC7448 is in 60x bus mode, DTI[0:3] must be pulled low to GND through weak pull-down resistors.

The data bus input receivers are normally turned off when no read operation is in progress and, therefore, do not require pull-up resistors on the bus. Other data bus receivers in the system, however, may require pull-ups or require that those signals be otherwise driven by the system during inactive periods. The data bus signals are D[0:63] and DP[0:7].

9.6 JTAG Configuration Signals

Boundary-scan testing is enabled through the JTAG interface signals. The $\overline{\text{TRST}}$ signal is optional in the IEEE 1149.1 standard specification, but is typically provided on all processors that implement the PowerPC architecture. While it is possible to force the TAP controller to the reset state using only the TCK and TMS signals, more reliable power-on reset performance will be obtained if the $\overline{\text{TRST}}$ signal is asserted during power-on reset. Because the JTAG interface is also used for accessing the common on-chip processor (COP) function, simply tying $\overline{\text{TRST}}$ to $\overline{\text{HRESET}}$ is not practical.

The COP function of these processors allows a remote computer system (typically a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$ in order

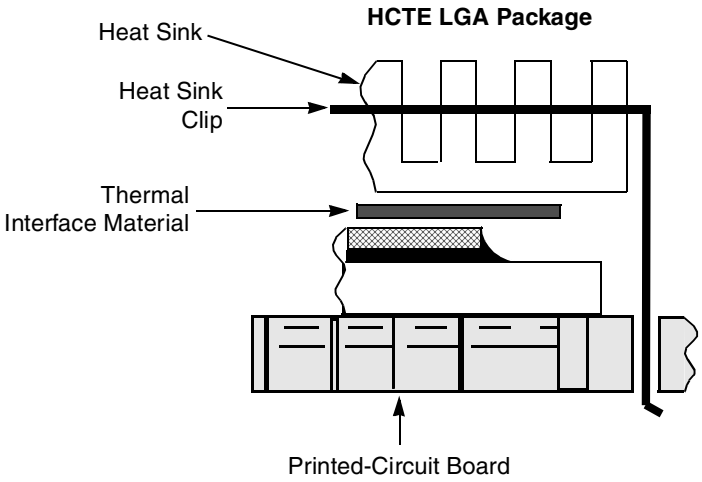


Figure 23. LGA Package Exploded Cross-Sectional View with Several Heat Sink Options

There are several commercially-available heat sinks for the MPC7448 provided by the following vendors:

Aavid Thermalloy 80 Commercial St. Concord, NH 03301 Internet: www.aavidthermalloy.com	603-224-9988
Alpha Novatech 473 Sapena Ct. #12 Santa Clara, CA 95054 Internet: www.alphanovatech.com	408-567-8082
Calgreg Thermal Solutions 60 Alhambra Road, Suite 1 Warwick, RI 02886 Internet: www.calgregthermalsolutions.com	888-732-6100
International Electronic Research Corporation (IERC) 413 North Moss St. Burbank, CA 91502 Internet: www.ctscorp.com	818-842-7277
Tyco Electronics Chip Coolers™ P.O. Box 3668 Harrisburg, PA 17105-3668 Internet: www.tycoelectronics.com	800-522-6752
Wakefield Engineering 33 Bridge St. Pelham, NH 03076 Internet: www.wakefield.com	603-635-2800

Ultimately, the final selection of an appropriate heat sink depends on many factors, such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost.

of any thermal interface material depends on many factors—thermal performance requirements, manufacturability, service temperature, dielectric properties, cost, and so on.

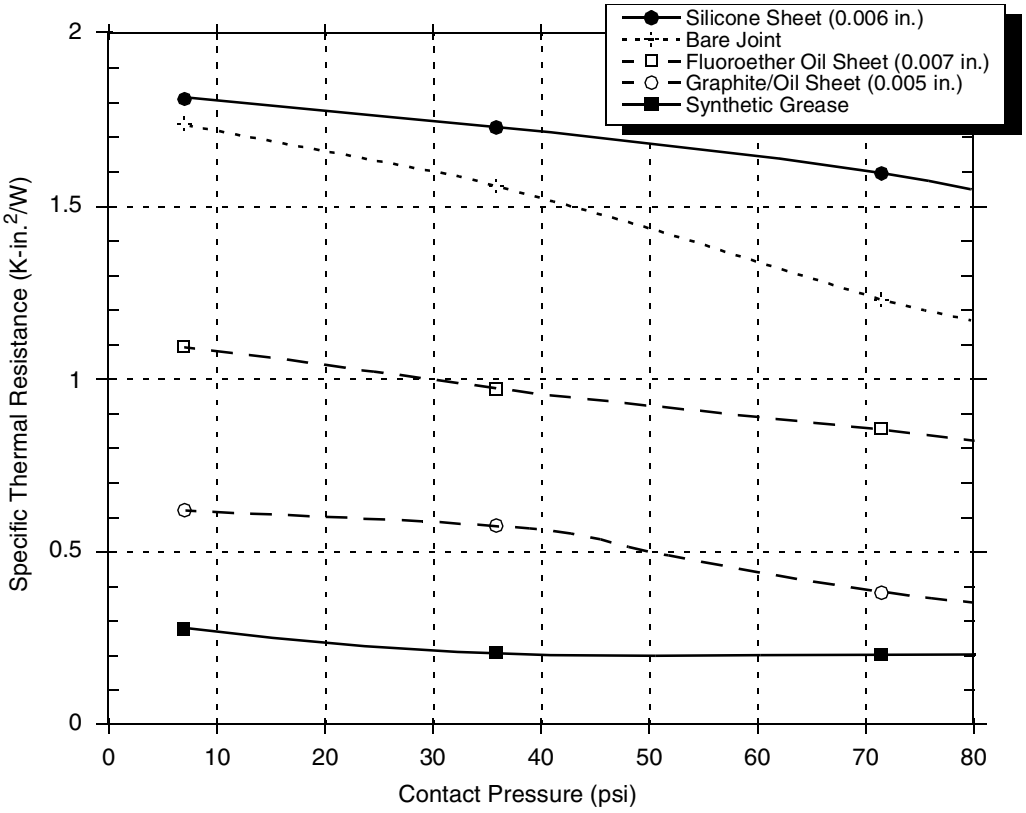


Figure 25. Thermal Performance of Select Thermal Interface Material

The board designer can choose between several types of thermal interfaces. Heat sink adhesive materials should be selected based on high conductivity and mechanical strength to meet equipment shock/vibration requirements. There are several commercially available thermal interfaces and adhesive materials provided by the following vendors:

The Bergquist Company 18930 West 78th St. Chanhassen, MN 55317 Internet: www.bergquistcompany.com	800-347-4572
Chomerics, Inc. 77 Dragon Ct. Woburn, MA 01801 Internet: www.chomerics.com	781-935-4850
Dow-Corning Corporation Corporate Center P.O. Box 994. Midland, MI 48686-0994 Internet: www.dowcorning.com	800-248-2481

Due to the complexity and variety of system-level boundary conditions for today's microelectronic equipment, the combined effects of the heat transfer mechanisms (radiation, convection, and conduction) may vary widely. For these reasons, we recommend using conjugate heat transfer models for the board as well as system-level designs.

For system thermal modeling, the MPC7448 thermal model is shown in Figure 26. Four volumes represent this device. Two of the volumes, solder ball-air and substrate, are modeled using the package outline size of the package. The other two, die and bump-underfill, have the same size as the die. The silicon die should be modeled $8.0 \times 7.3 \times 0.86$ mm^3 with the heat source applied as a uniform source at the bottom of the volume. The bump and underfill layer is modeled as $8.0 \times 7.3 \times 0.07$ mm^{3}collapsed in the z-direction with a thermal conductivity of 5.0 W/(m • K) in the z-direction. The substrate volume is $25 \times 25 \times 1.14$ mm^3 and has 9.9 W/(m • K) isotropic conductivity in the xy-plane and 2.95 W/(m • K) in the direction of the z-axis. The solder ball and air layer are modeled with the same horizontal dimensions as the substrate and is 0.8 mm thick. For the LGA package the solder and air layer is 0.1 mm thick, but the material properties are the same. It can also be modeled as a collapsed volume using orthotropic material properties: 0.034 W/(m • K) in the xy-plane direction and 11.2 W/(m • K) in the direction of the z-axis.

Conductivity	Value	Unit
Die ($8.0 \times 7.3 \times 0.86$ mm^3)		
Silicon	Temperature-dependent	W/(m • K)
Bump and Underfill ($8.0 \times 7.3 \times 0.07$ mm^3)		
k_z	5.0	W/(m • K)
Substrate ($25 \times 25 \times 1.14$ mm^3)		
k_x	9.9	W/(m • K)
k_y	9.9	
k_z	2.95	
Solder Ball and Air ($25 \times 25 \times 0.8$ mm^3)		
k_x	0.034	W/(m • K)
k_y	0.034	
k_z	11.2	

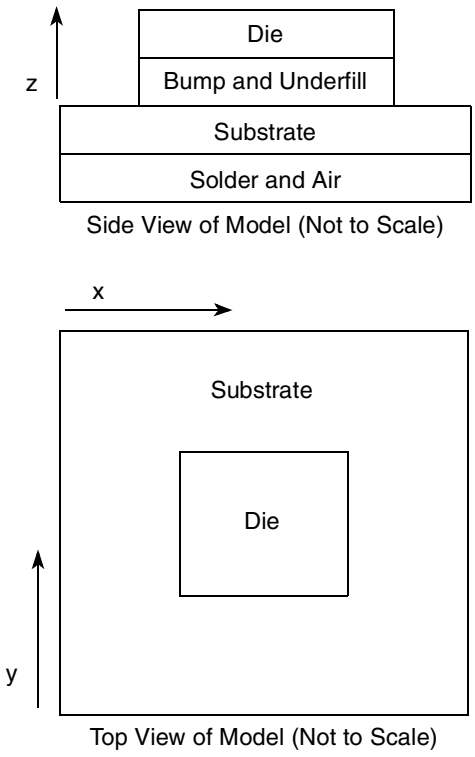


Figure 26. Recommended Thermal Model of MPC7448

11 Part Numbering and Marking

Ordering information for the part numbers fully covered by this specification document is provided in Section 11.1, "Part Numbers Fully Addressed by This Document." Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact a local Freescale sales office. In addition to the processor frequency, the part numbering scheme also includes an application modifier that may specify special application conditions. An optional specification modifier may also apply for parts to indicate a specific change in specifications, such as support for an extended temperature range. Finally, each part number contains a revision level code that refers to the die mask revision number. Section 11.2, "Part Numbers Not Fully Addressed by This Document," lists the part numbers that do not fully conform to the specifications of this document. These special part numbers require an additional document called a hardware specification addendum.

11.1 Part Numbers Fully Addressed by This Document

Table 18 provides the Freescale part numbering nomenclature for the MPC7448 part numbers fully addressed by this document. For information regarding other MPC7448 part numbers, see Section 11.2, "Part Numbers Not Fully Addressed by This Document."

Table 18. Part Numbering Nomenclature

xx	**7448**	***xx***	***nnnn***	**L**	***x***
Product Code	**Part Identifier**	**Package**	**Processor Frequency**	**Application Modifier**	**Revision Level**
MC PPC [1]	7448	HX = HCTE BGA VS = RoHS LGA VU = RoHS BGA	1700	L: 1.3 V +20/–50 mV 0 to 105 °C	C: 2.1; PVR = 0x8004_0201 D: 2.2; PVR = 0x8004_0202
			1600	L: 1.25 V ± 50 mV 0 to 105 °C	
			1420	L: 1.2 V ± 50 mV 0 to 105 °C	
			1000	L: 1.15 V ± 50 mV 0 to 105 °C	

Notes:

1. The P prefix in a Freescale part number designates a "Pilot Production Prototype" as defined by Freescale SOP 3-13. These parts have only preliminary reliability and characterization data. Before pilot production prototypes may be shipped, written authorization from the customer must be on file in the applicable sales office acknowledging the qualification status and the fact that product changes may still occur as pilot production prototypes are shipped.

11.2 Part Numbers Not Fully Addressed by This Document

Parts with application modifiers or revision levels not fully addressed in this specification document are described in separate hardware specification addenda which supplement and supersede this document. As such parts are released, these specifications will be listed in this section.

Table 19. Part Numbers Addressed by MC7448*xxnnnn*N*x* Series Hardware Specification Addendum (Document Order No. MPC7448ECS01AD)

xx	**7448**	***xx***	***nnnn***	**N**	***x***
Product Code	**Part Identifier**	**Package**	**Processor Frequency**	**Application Modifier**	**Revision Level**
MC	7448	HX = HCTE BGA VS = RoHS LGA VU = RoHS BGA	1400	N: 1.15 V ± 50 mV 0 to 105 °C (date code 0613 and later) [2]	C: 2.1; PVR = 0x8004_0201 D: 2.2; PVR = 0x8004_0202
MC PPC[1]			1400	N: 1.1 V ± 50 mV 0 to 105 °C (date code 0612 and prior) [2]	
MC PPC[1]			1267 Revision C only	N: 1.1 V ± 50 mV 0 to 105 °C	
MC PPC[1]			1267 Revision D only	N: 1.05 V ± 50 mV 0 to 105 °C	
MC PPC[1]			1250	N: 1.1 V ± 50 mV 0 to 105 °C	
MC PPC[1]			1000 867 800 667 600	N: 1.0 V ± 50 mV 0 to 105 °C	

Notes:

1. The P prefix in a Freescale part number designates a “Pilot Production Prototype” as defined by Freescale SOP 3-13. These parts have only preliminary reliability and characterization data. Before pilot production prototypes can be shipped, written authorization from the customer must be on file in the applicable sales office acknowledging the qualification status and the fact that product changes may still occur as pilot production prototypes are shipped.
2. Core voltage for 1400 MHz devices currently in production (date code of 0613 and later) is 1.15 V ± 50 mV; all such devices have the MC product code. The 1400 MHz devices with date code of 0612 and prior specified core voltage of 1.1 V ± 50 mV; this includes all 1400 MHz devices with the PPC product code. See Section 11.3, “Part Marking,” for information on part marking.