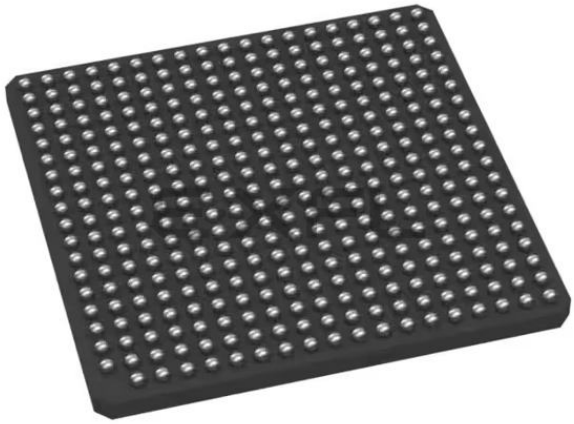

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## Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

## Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | PowerPC G4 |
| Number of Cores/Bus Width | 1 Core, 32-Bit |
| Speed | 1.267GHz |
| Co-Processors/DSP | Multimedia; SIMD |
| RAM Controllers | - |
| Graphics Acceleration | No |
| Display & Interface Controllers | - |
| Ethernet | - |
| SATA | - |
| USB | - |
| Voltage - I/O | 1.5V, 1.8V, 2.5V |
| Operating Temperature | 0°C ~ 105°C (TA) |
| Security Features | - |
| Package / Case | 360-CLGA, FCCLGA |
| Supplier Device Package | 360-FCCLGA (25x25) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/kmc7448vs1267nd |

# 2 Features

This section summarizes features of the MPC7448 implementation.

Major features of the MPC7448 are as follows:

- High-performance, superscalar microprocessor
  - Up to four instructions can be fetched from the instruction cache at a time.
  - Up to three instructions plus a branch instruction can be dispatched to the issue queues at a time.
  - Up to 12 instructions can be in the instruction queue (IQ).
  - Up to 16 instructions can be at some stage of execution simultaneously.
  - Single-cycle execution for most instructions
  - One instruction per clock cycle throughput for most instructions
  - Seven-stage pipeline control
- Eleven independent execution units and three register files
  - Branch processing unit (BPU) features static and dynamic branch prediction
    - 128-entry (32-set, four-way set-associative) branch target instruction cache (BTIC), a cache of branch instructions that have been encountered in branch/loop code sequences. If a target instruction is in the BTIC, it is fetched into the instruction queue a cycle sooner than it can be made available from the instruction cache. Typically, a fetch that hits the BTIC provides the first four instructions in the target stream.
    - 2048-entry branch history table (BHT) with 2 bits per entry for four levels of prediction—not taken, strongly not taken, taken, and strongly taken
    - Up to three outstanding speculative branches
    - Branch instructions that do not update the count register (CTR) or link register (LR) are often removed from the instruction stream.
    - Eight-entry link register stack to predict the target address of Branch Conditional to Link Register (**bclr**) instructions
  - Four integer units (IUs) that share 32 GPRs for integer operands
    - Three identical IUs (IU1a, IU1b, and IU1c) can execute all integer instructions except multiply, divide, and move to/from special-purpose register instructions.
    - IU2 executes miscellaneous instructions, including the CR logical operations, integer multiplication and division instructions, and move to/from special-purpose register instructions.
  - Five-stage FPU and 32-entry FPR file
    - Fully IEEE Std. 754™-1985–compliant FPU for both single- and double-precision operations
    - Supports non-IEEE mode for time-critical operations
    - Hardware support for denormalized numbers
    - Thirty-two 64-bit FPRs for single- or double-precision operands

- Four vector units and 32-entry vector register file (VRs)
  - Vector permute unit (VPU)
  - Vector integer unit 1 (VIU1) handles short-latency AltiVec™ integer instructions, such as vector add instructions (for example, **vaddsbs**, **vaddshs**, and **vaddsws**).
  - Vector integer unit 2 (VIU2) handles longer-latency AltiVec integer instructions, such as vector multiply add instructions (for example, **vmhaddshs**, **vmhraddshs**, and **vmladduhm**).
  - Vector floating-point unit (VFPU)
- Three-stage load/store unit (LSU)
  - Supports integer, floating-point, and vector instruction load/store traffic
  - Four-entry vector touch queue (VTQ) supports all four architected AltiVec data stream operations
  - Three-cycle GPR and AltiVec load latency (byte, half word, word, vector) with one-cycle throughput
  - Four-cycle FPR load latency (single, double) with one-cycle throughput
  - No additional delay for misaligned access within double-word boundary
  - A dedicated adder calculates effective addresses (EAs).
  - Supports store gathering
  - Performs alignment, normalization, and precision conversion for floating-point data
  - Executes cache control and TLB instructions
  - Performs alignment, zero padding, and sign extension for integer data
  - Supports hits under misses (multiple outstanding misses)
  - Supports both big- and little-endian modes, including misaligned little-endian accesses

- Three issue queues, FIQ, VIQ, and GIQ, can accept as many as one, two, and three instructions, respectively, in a cycle. Instruction dispatch requires the following:
  - Instructions can only be dispatched from the three lowest IQ entries—IQ0, IQ1, and IQ2.
  - A maximum of three instructions can be dispatched to the issue queues per clock cycle.
  - Space must be available in the CQ for an instruction to dispatch (this includes instructions that are assigned a space in the CQ but not in an issue queue).
- Rename buffers
  - 16 GPR rename buffers
  - 16 FPR rename buffers
  - 16 VR rename buffers
- Dispatch unit
  - Decode/dispatch stage fully decodes each instruction
- Completion unit
  - Retires an instruction from the 16-entry completion queue (CQ) when all instructions ahead of it have been completed, the instruction has finished executing, and no exceptions are pending
  - Guarantees sequential programming model (precise exception model)

Figure 2 shows the undershoot and overshoot voltage on the MPC7448.

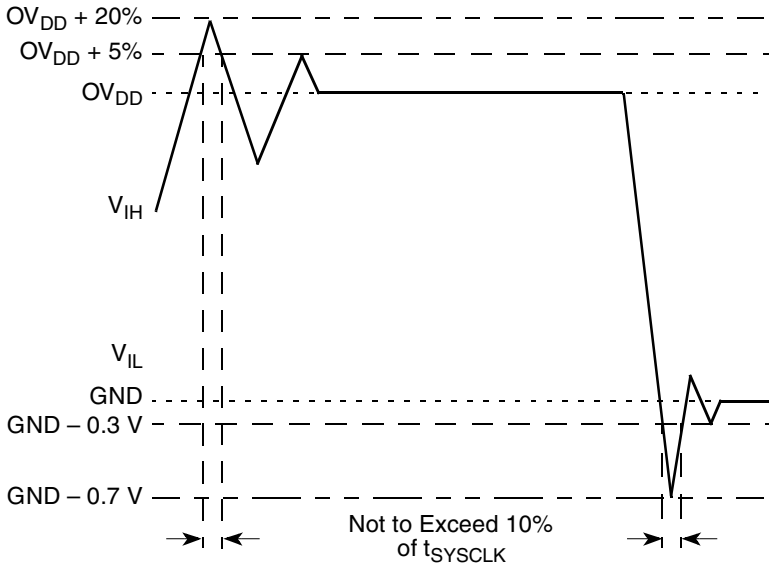



**Figure 2. Overshoot/Undershoot Voltage**

The MPC7448 provides several I/O voltages to support both compatibility with existing systems and migration to future systems. The MPC7448 core voltage must always be provided at the nominal voltage (see Table 4). The input voltage threshold for each bus is selected by sampling the state of the voltage select pins at the negation of the signal $\overline{\text{HRESET}}$. The output voltage will swing from GND to the maximum voltage applied to the $OV_{DD}$ power pins. Table 3 provides the input threshold voltage settings. Because these settings may change in future products, it is recommended that BVSEL[0:1] be configured using resistor options, jumpers, or some other flexible means, with the capability to reconfigure the termination of this signal in the future, if necessary.

**Table 3. Input Threshold Voltage Setting**

| BVSEL0 | BVSEL1 | I/O Voltage Mode[1] | Notes |
|---|---|---|---|
| 0 | 0 | 1.8 V | 2, 3 |
| 0 | 1 | 2.5 V | 2, 4 |
| 1 | 0 | 1.5 V | 2 |
| 1 | 1 | 2.5 V | 4 |

**Notes:**

1. **Caution:** The I/O voltage mode selected must agree with the $OV_{DD}$ voltages supplied. See Table 4.
2. If used, pull-down resistors should be less than 250 Ω.
3. The pin configuration used to select 1.8V mode on the MPC7448 is not compatible with the pin configuration used to select 1.8V mode on the MPC7447A and earlier devices.
4. The pin configuration used to select 2.5V mode on the MPC7448 is fully compatible with the pin configuration used to select 2.5V mode on the MPC7447A and earlier devices.

when running a typical benchmark at temperatures in a typical system. The Full-Power Mode–Thermal value is intended to represent the sustained power consumption of the device when running a typical code sequence at high temperature and is recommended to be used as the basis for designing a thermal solution; see Section 9.7, "Power and Thermal Management Information" for more information on thermal solutions. The Full-Power Mode–Maximum value is recommended to be used for power supply design because this represents the maximum peak power draw of the device that a power supply must be capable of sourcing without voltage droop. For information on power consumption when dynamic frequency switching is enabled, see Section 9.7.5, "Dynamic Frequency Switching (DFS)."

**Table 7. Power Consumption for MPC7448 at Maximum Rated Frequency**

| | Die Junction Temperature ($T_j$) | Maximum Processor Core Frequency (Speed Grade, MHz) | | | | Unit | Notes |
|---|---|---|---|---|---|---|---|
| | | 1000 MHz | 1420 MHz | 1600 MHz | 1700 MHz | | |
| **Full-Power Mode** | | | | | | | |
| **Typical** | 65 •C | 15.0 | 19.0 | 20.0 | 21.0 | W | 1, 2 |
| **Thermal** | 105 •C | 18.6 | 23.3 | 24.4 | 25.6 | W | 1, 5 |
| **Maximum** | 105 •C | 21.6 | 27.1 | 28.4 | 29.8 | W | 1, 3 |
| **Nap Mode** | | | | | | | |
| **Typical** | 105 •C | 11.1 | 11.8 | 13.0 | 13.0 | W | 1, 6 |
| **Sleep Mode** | | | | | | | |
| **Typical** | 105 •C | 10.8 | 11.4 | 12.5 | 12.5 | W | 1, 6 |
| **Deep Sleep Mode (PLL Disabled)** | | | | | | | |
| **Typical** | 105 •C | 10.4 | 11.0 | 12.0 | 12.0 | W | 1, 6 |

**Notes:**

1. These values specify the power consumption for the core power supply ($V_{DD}$) at nominal voltage and apply to all valid processor bus frequencies and configurations. The values do not include I/O supply power ($OV_{DD}$) or PLL supply power ($AV_{DD}$). $OV_{DD}$ power is system dependent but is typically < 5% of $V_{DD}$ power. Worst case power consumption for $AV_{DD}$ < 13 mW. Freescale also offers MPC7448 part numbers that meet lower power consumption specifications; for more information on these devices, see Section 11.2, "Part Numbers Not Fully Addressed by This Document."
2. Typical power consumption is an average value measured with the processor operating at its rated maximum processor core frequency (except for Deep Sleep Mode), at nominal recommended $V_{DD}$ (see Table 4) and 65°C while running the Dhrystone 2.1 benchmark and achieving 2.3 Dhrystone MIPs/MHz. This parameter is not 100% tested but periodically sampled.b
3. Maximum power consumption is the average measured with the processor operating at its rated maximum processor core frequency, at nominal $V_{DD}$ and maximum operating junction temperature (see Table 4) while running an entirely cache-resident, contrived sequence of instructions to keep all the execution units maximally busy.
4. Doze mode is not a user-definable state; it is an intermediate state between full-power and either nap or sleep mode. As a result, power consumption for this mode is not tested.
5. Thermal power consumption is an average value measured at the nominal recommended $V_{DD}$ (see Table 4) and 105 °C while running the Dhrystone 2.1 benchmark and achieving 2.3 Dhrystone MIPs/MHz. This parameter is not 100% tested but periodically sampled.
6. Typical power consumption for these modes is measured at the nominal recommended $V_{DD}$ (see Table 4) and 105 °C in the mode described. This parameter is not 100% tested but is periodically sampled.

Figure 3 provides the SYSCLK input timing diagram.

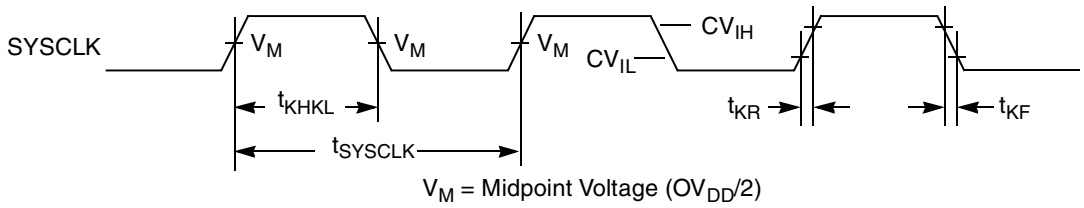



**Figure 3. SYSCLK Input Timing Diagram**

## 5.2.2 Processor Bus AC Specifications

Table 9 provides the processor bus AC timing specifications for the MPC7448 as defined in Figure 4 and Figure 5.

**Table 9. Processor Bus AC Timing Specifications[1]**

At recommended operating conditions. See Table 4.

| Parameter | Symbol [2] | All Speed Grades | | Unit | Notes |
|---|---|---|---|---|---|
| | | Min | Max | | |
| Input setup times: | | | | ns | |
| A[0:35], AP[0:4] | $t_{AVKH}$ | 1.5 | — | | — |
| D[0:63], DP[0:7] | $t_{DVKH}$ | 1.5 | — | | — |
| AACK, ARTRY, BG, CKSTP_IN, DBG, DTI[0:3], GBL, TT[0:4], QACK, TA, TBEN, TEA, TS, EXT_QUAL, PMON_IN, SHD[0:1] | $t_{IVKH}$ | 1.5 | — | | — |
| BMODE[0:1], BVSEL[0:1] | $t_{MVKH}$ | 1.5 | — | | 8 |
| Input hold times: | | | | ns | |
| A[0:35], AP[0:4] | $t_{AXKH}$ | 0 | — | | — |
| D[0:63], DP[0:7] | $t_{DXKH}$ | 0 | — | | — |
| AACK, ARTRY, BG, CKSTP_IN, DBG, DTI[0:3], GBL, TT[0:4], QACK, TA, TBEN, TEA, TS, EXT_QUAL, PMON_IN, SHD[0:1] | $t_{IXKH}$ | 0 | — | | — |
| | | | | | — |
| BMODE[0:1], BVSEL[0:1] | $t_{MXKH}$ | 0 | — | | 8 |
| Output valid times: | | | | ns | |
| A[0:35], AP[0:4] | $t_{KHAV}$ | — | 1.8 | | |
| D[0:63], DP[0:7] | $t_{KHDV}$ | — | 1.8 | | |
| BR, CI, DRDY, GBL, HIT, PMON_OUT, QREQ, TBST, TSIZ[0:2], TT[0:4], WT | $t_{KHOV}$ | — | 1.8 | | |
| TS | $t_{KHTSV}$ | — | 1.8 | | |
| ARTRY, SHD[0:1] | $t_{KHARV}$ | — | 1.8 | | |
| Output hold times: | | | | ns | |
| A[0:35], AP[0:4] | $t_{KHAX}$ | 0.5 | — | | |
| D[0:63], DP[0:7] | $t_{KHDX}$ | 0.5 | — | | |
| BR, CI, DRDY, GBL, HIT, PMON_OUT, QREQ, TBST, TSIZ[0:2], TT[0:4], WT | $t_{KHOX}$ | 0.5 | — | | |
| TS | $t_{KHTSX}$ | 0.5 | — | | |
| ARTRY, SHD[0:1] | $t_{KHARX}$ | 0.5 | — | | |
| SYSCLK to output enable | $t_{KHOE}$ | 0.5 | — | ns | 5 |

## Table 9. Processor Bus AC Timing Specifications[1] (continued)

At recommended operating conditions. See Table 4.

| Parameter | Symbol [2] | All Speed Grades | | Unit | Notes |
|---|---|---|---|---|---|
| | | Min | Max | | |
| SYSCLK to output high impedance (all except $\overline{TS}$, $\overline{ARTRY}$, $\overline{SHD0}$, $\overline{SHD1}$) | $t_{KHOZ}$ | — | 1.8 | ns | 5 |
| SYSCLK to $\overline{TS}$ high impedance after precharge | $t_{KHTSPZ}$ | — | 1 | $t_{SYSCLK}$ | 3, 4, 5 |
| Maximum delay to $\overline{ARTRY}$/$\overline{SHD0}$/$\overline{SHD1}$ precharge | $t_{KHARP}$ | — | 1 | $t_{SYSCLK}$ | 3, 5, 6, 7 |
| SYSCLK to $\overline{ARTRY}$/$\overline{SHD0}$/$\overline{SHD1}$ high impedance after precharge | $t_{KHARPZ}$ | — | 2 | $t_{SYSCLK}$ | 3, 5, 6, 7 |

**Notes:**

1. All input specifications are measured from the midpoint of the signal in question to the midpoint of the rising edge of the input SYSCLK. All output specifications are measured from the midpoint of the rising edge of SYSCLK to the midpoint of the signal in question. All output timings assume a purely resistive 50-Ω load (see Figure 4). Input and output timings are measured at the pin; time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. The symbology used for timing specifications herein follows the pattern of $t_{(signal)(state)(reference)(state)}$ for inputs and $t_{(reference)(state)(signal)(state)}$ for outputs. For example, $t_{IVKH}$ symbolizes the time input signals (I) reach the valid state (V) relative to the SYSCLK reference (K) going to the high (H) state or input setup time. And $t_{KHOV}$ symbolizes the time from SYSCLK(K) going high (H) until outputs (O) are valid (V) or output valid time. Input hold time can be read as the time that the input signal (I) went invalid (X) with respect to the rising clock edge (KH) (note the position of the reference and its state for inputs) and output hold time can be read as the time from the rising edge (KH) until the output went invalid (OX).
3. $t_{sysclk}$ is the period of the external clock (SYSCLK) in ns. The numbers given in the table must be multiplied by the period of SYSCLK to compute the actual time duration (in ns) of the parameter in question.
4. According to the bus protocol, $\overline{TS}$ is driven only by the currently active bus master. It is asserted low and precharged high before returning to high impedance, as shown in Figure 6. The nominal precharge width for $\overline{TS}$ is $t_{SYSCLK}$, that is, one clock period. Since no master can assert $\overline{TS}$ on the following clock edge, there is no concern regarding contention with the precharge. Output valid and output hold timing is tested for the signal asserted. Output valid time is tested for precharge.The high-impedance behavior is guaranteed by design.
5. Guaranteed by design and not tested
6. According to the bus protocol, $\overline{ARTRY}$ can be driven by multiple bus masters through the clock period immediately following $\overline{AACK}$. Bus contention is not an issue because any master asserting $\overline{ARTRY}$ will be driving it low. Any master asserting it low in the first clock following $\overline{AACK}$ will then go to high impedance for a fraction of a cycle, then negated for up to an entire cycle (crossing a bus cycle boundary) before being three-stated again. The nominal precharge width for $\overline{ARTRY}$ is 1.0 $t_{SYSCLK}$; that is, it should be high impedance as shown in Figure 6 before the first opportunity for another master to assert $\overline{ARTRY}$. Output valid and output hold timing is tested for the signal asserted.The high-impedance behavior is guaranteed by design.
7. According to the MPX bus protocol, $\overline{SHD0}$ and $\overline{SHD1}$ can be driven by multiple bus masters beginning two cycles after $\overline{TS}$. Timing is the same as $\overline{ARTRY}$, that is, the signal is high impedance for a fraction of a cycle, then negated for up to an entire cycle (crossing a bus cycle boundary) before being three-stated again. The nominal precharge width for $\overline{SHD0}$ and $\overline{SHD1}$ is 1.0 $t_{SYSCLK}$. The edges of the precharge vary depending on the programmed ratio of core to bus (PLL configurations).
8. $\overline{BMODE}$[0:1] and BVSEL[0:1] are mode select inputs. $\overline{BMODE}$[0:1] are sampled before and after $\overline{HRESET}$ negation. BVSEL[0:1] are sampled before $\overline{HRESET}$ negation. These parameters represent the input setup and hold times for each sample. These values are guaranteed by design and not tested. $\overline{BMODE}$[0:1] must remain stable after the second sample; BVSEL[0:1] must remain stable after the first (and only) sample. See Figure 5 for sample timing.

Figure 7 provides the AC test load for TDO and the boundary-scan outputs of the MPC7448.

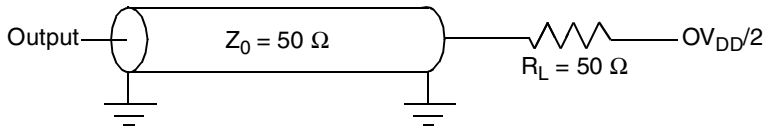



**Figure 7. Alternate AC Test Load for the JTAG Interface**

Figure 8 provides the JTAG clock input timing diagram.

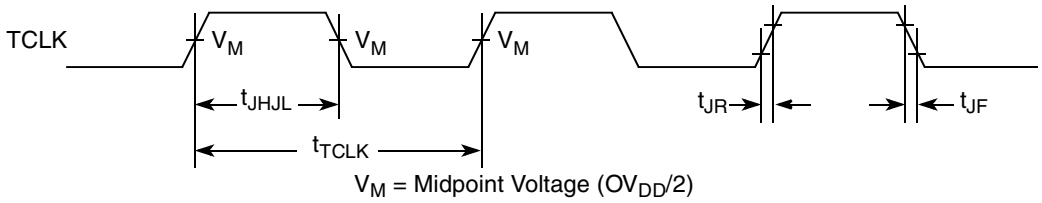



**Figure 8. JTAG Clock Input Timing Diagram**

Figure 9 provides the $\overline{\text{TRST}}$ timing diagram.

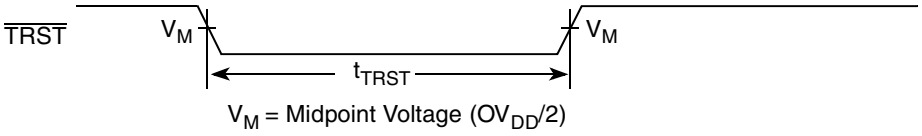



**Figure 9. $\overline{\text{TRST}}$ Timing Diagram**

Figure 10 provides the boundary-scan timing diagram.

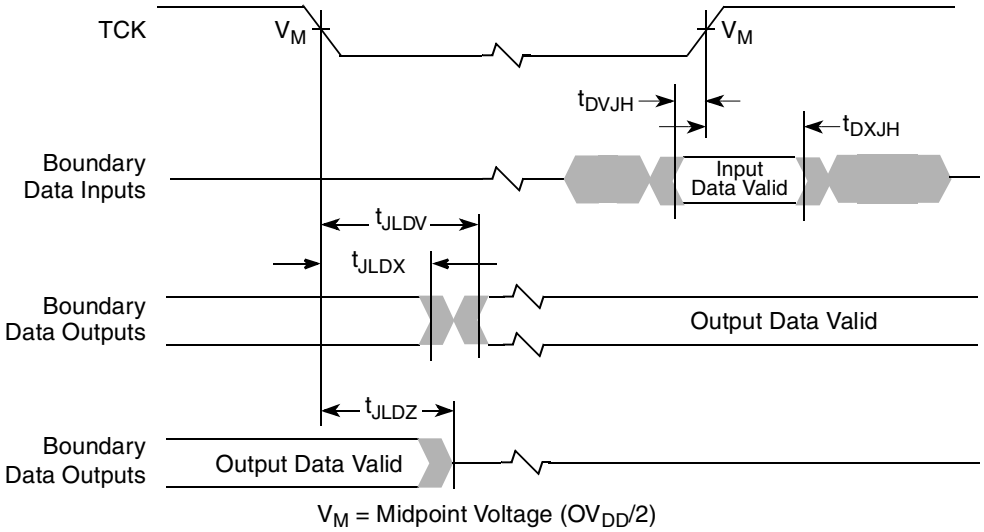
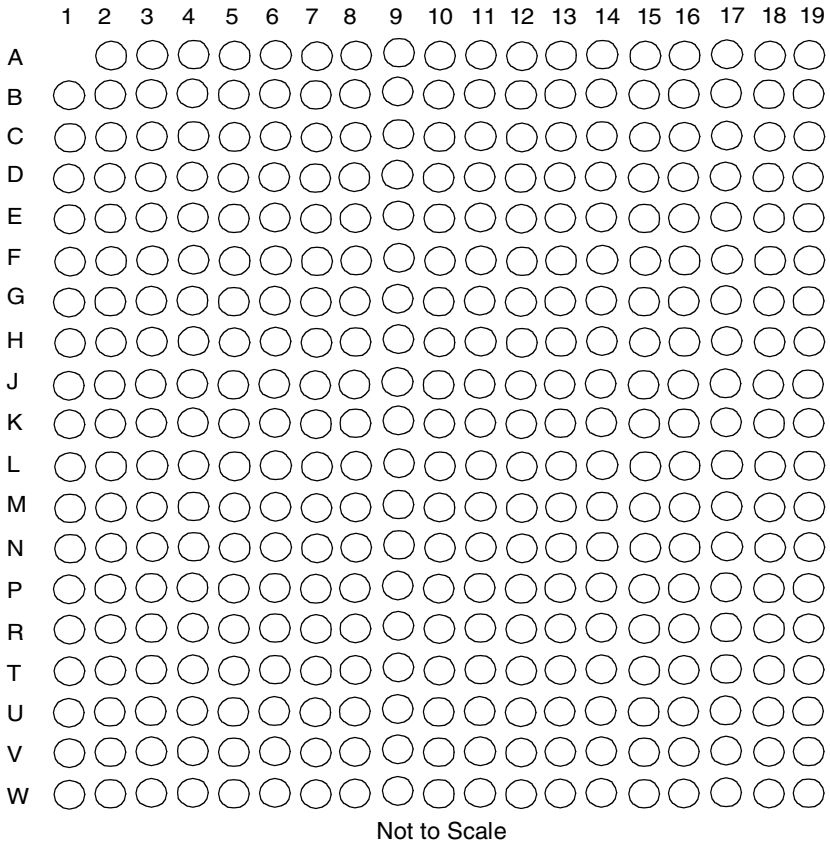



**Figure 10. Boundary-Scan Timing Diagram**

# 6 Pin Assignments

Figure 12 (in Part A) shows the pinout of the MPC7448, 360 high coefficient of thermal expansion ceramic ball grid array (HCTE) package as viewed from the top surface. Part B shows the side profile of the HCTE package to indicate the direction of the top surface view.

**Part A**




**Part B**

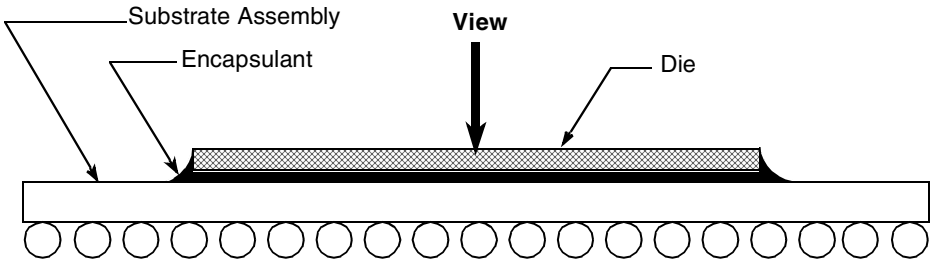



**Figure 12. Pinout of the MPC7448, 360 HCTE Package as Viewed from the Top Surface**

# 7 Pinout Listings

Table 11 provides the pinout listing for the MPC7448, 360 HCTE package. The pinouts of the MPC7448 and MPC7447A are compatible, but the requirements regarding the use of the additional power and ground pins have changed. The MPC7448 requires these pins be connected to the appropriate power or ground plane to achieve high core frequencies; see Section 9.3, “Connection Recommendations,” for additional information. As a result, these pins should be connected in all new designs.

Additionally, the MPC7448 may be populated on a board designed for a MPC7447 (or MPC7445 or MPC7441), provided the core voltage can be made to match the requirements in Table 4 and all pins defined as ‘no connect’ for the MPC7447 are unterminated, as required by the *MPC7457 RISC Microprocessor Hardware Specifications*. The MPC7448 uses pins previously marked ‘no connect’ for the temperature diode pins and for additional power and ground connections. The additional power and ground pins are required to achieve high core frequencies and core frequency will be limited if they are not connected; see Section 9.3, “Connection Recommendations,” for additional information. Because these ‘no connect’ pins in the MPC7447 360 pin package are not driven in functional mode, an MPC7447 can be populated in an MPC7448 board.

**NOTE**

Caution must be exercised when performing boundary scan test operations on a board designed for an MPC7448, but populated with an MPC7447 or earlier device. This is because in the MPC7447 it is possible to drive the latches associated with the former ‘no connect’ pins in the MPC7447, potentially causing contention on those pins. To prevent this, ensure that these pins are not connected on the board or, if they are connected, ensure that the states of internal MPC7447 latches do not cause these pins to be driven during board testing.

For the MPC7448, pins that were defined as the TEST[0:4] factory test signal group on the MPC7447A and earlier devices have been assigned new functions. For most of these, the termination recommendations for the TEST[0:4] pins of the MPC7447A are compatible with the MPC7448 and will allow correct operation with no performance loss. The exception is BVSEL1 (TEST3 on the MPC7447A and earlier devices), which may require a different termination depending which I/O voltage mode is desired; see Table 3 for more information.

**NOTE**

This pinout is not compatible with the MPC750, MPC7400, or MPC7410 360 BGA package.

**Table 11. Pinout Listing for the MPC7448, 360 HCTE Package**

| Signal Name | Pin Number | Active | I/O | Notes |
|---|---|---|---|---|
| A[0:35] | E11, H1, C11, G3, F10, L2, D11, D1, C10, G2, D12, L3, G4, T2, F4, V1, J4, R2, K5, W2, J2, K4, N4, J3, M5, P5, N3, T1, V2, U1, N5, W1, B12, C4, G10, B11 | High | I/O | 2 |
| $\overline{\text{AACK}}$ | R1 | Low | Input | |
| AP[0:4] | C1, E3, H6, F5, G7 | High | I/O | 2 |
| $\overline{\text{ARTRY}}$ | N2 | Low | I/O | 3 |
| $AV_{DD}$ | A8 | — | Input | |
| $\overline{\text{BG}}$ | M1 | Low | Input | |
| $\overline{\text{BMODE0}}$ | G9 | Low | Input | 4 |
| $\overline{\text{BMODE1}}$ | F8 | Low | Input | 5 |
| $\overline{\text{BR}}$ | D2 | Low | Output | |
| BVSEL0 | B7 | High | Input | 1, 6 |
| BVSEL1 | E10 | High | Input | 1, 20 |
| $\overline{\text{CI}}$ | J1 | Low | Output | |
| $\overline{\text{CKSTP\_IN}}$ | A3 | Low | Input | |
| $\overline{\text{CKSTP\_OUT}}$ | B1 | Low | Output | |
| CLK_OUT | H2 | High | Output | |
| D[0:63] | R15, W15, T14, V16, W16, T15, U15, P14, V13, W13, T13, P13, U14, W14, R12, T12, W12, V12, N11, N10, R11, U11, W11, T11, R10, N9, P10, U10, R9, W10, U9, V9, W5, U6, T5, U5, W7, R6, P7, V6, P17, R19, V18, R18, V19, T19, U19, W19, U18, W17, W18, T16, T18, T17, W3, V17, U4, U8, U7, R7, P6, R8, W8, T8 | High | I/O | |
| $\overline{\text{DBG}}$ | M2 | Low | Input | |
| $\overline{\text{DFS2}}$ | A12 | Low | Input | 20, 21 |
| $\overline{\text{DFS4}}$ | B6 | Low | Input | 12, 20, 21 |
| DP[0:7] | T3, W4, T4, W9, M6, V3, N8, W6 | High | I/O | |
| $\overline{\text{DRDY}}$ | R3 | Low | Output | 7 |
| DTI[0:3] | G1, K1, P1, N1 | High | Input | 8 |
| EXT_QUAL | A11 | High | Input | 9 |
| $\overline{\text{GBL}}$ | E2 | Low | I/O | |
| GND | B5, C3, D6, D13, E17, F3, G17, H4, H7, H9, H11, H13, J6, J8, J10, J12, K7, K3, K9, K11, K13, L6, L8, L10, L12, M4, M7, M9, M11, M13, N7, P3, P9, P12, R5, R14, R17, T7, T10, U3, U13, U17, V5, V8, V11, V15 | — | — | |
| GND | A17, A19, B13, B16, B18, E12, E19, F13, F16, F18, G19, H18, J14, L14, M15, M17, M19, N14, N16, P15, P19 | — | — | 15 |
| GND_SENSE | G12, N13 | — | — | 19 |
| $\overline{\text{HIT}}$ | B2 | Low | Output | 7 |
| $\overline{\text{HRESET}}$ | D8 | Low | Input | |
| $\overline{\text{INT}}$ | D4 | Low | Input | |
| L1_TSTCLK | G8 | High | Input | 9 |
| L2_TSTCLK | B3 | High | Input | 10 |

# 8 Package Description

The following sections provide the package parameters and mechanical dimensions for the HCTE package.

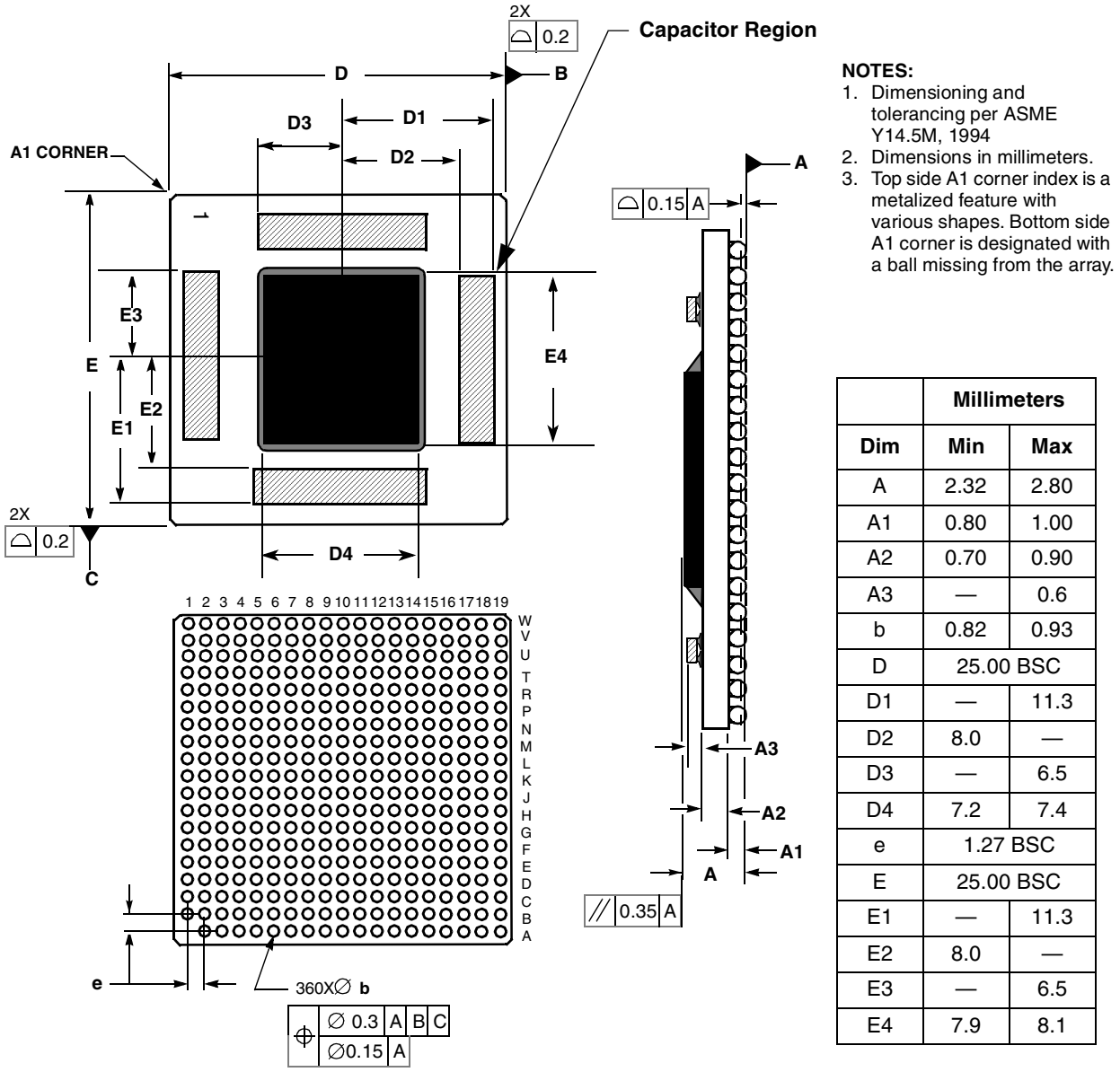
## 8.1 Package Parameters for the MPC7448, 360 HCTE BGA

The package parameters are as provided in the following list. The package type is 25 × 25 mm, 360-lead high coefficient of thermal expansion ceramic ball grid array (HCTE).

| | |
|---|---|
| Package outline | 25 × 25 mm |
| Interconnects | 360 (19 × 19 ball array – 1) |
| Pitch | 1.27 mm (50 mil) |
| Minimum module height | 2.32 mm |
| Maximum module height | 2.80 mm |
| Ball diameter | 0.89 mm (35 mil) |
| Coefficient of thermal expansion | 12.3 ppm/°C |

## 8.2 Mechanical Dimensions for the MPC7448, 360 HCTE BGA

Figure 13 provides the mechanical dimensions and bottom surface nomenclature for the MPC7448, 360 HCTE BGA package.




**NOTES:**
1. Dimensioning and tolerancing per ASME Y14.5M, 1994
2. Dimensions in millimeters.
3. Top side A1 corner index is a metalized feature with various shapes. Bottom side A1 corner is designated with a ball missing from the array.

| | Millimeters | |
|---|---|---|
| Dim | Min | Max |
| A | 2.32 | 2.80 |
| A1 | 0.80 | 1.00 |
| A2 | 0.70 | 0.90 |
| A3 | — | 0.6 |
| b | 0.82 | 0.93 |
| D | 25.00 BSC | |
| D1 | — | 11.3 |
| D2 | 8.0 | — |
| D3 | — | 6.5 |
| D4 | 7.2 | 7.4 |
| e | 1.27 BSC | |
| E | 25.00 BSC | |
| E1 | — | 11.3 |
| E2 | 8.0 | — |
| E3 | — | 6.5 |
| E4 | 7.9 | 8.1 |

**Figure 13. Mechanical Dimensions and Bottom Surface Nomenclature for the MPC7448, 360 HCTE BGA Package**

# 9 System Design Information

This section provides system and thermal design requirements and recommendations for successful application of the MPC7448.

## 9.1 Clocks

The following sections provide more detailed information regarding the clocking of the MPC7448.

### 9.1.1 PLL Configuration

The MPC7448 PLL is configured by the PLL_CFG[0:5] signals. For a given SYSCLK (bus) frequency, the PLL configuration signals set the internal CPU and VCO frequency of operation. The PLL configuration for the MPC7448 is shown in Table 12. In this example, shaded cells represent settings that, for a given SYSCLK frequency, result in core and/or VCO frequencies that do not comply with Table 8. When enabled, dynamic frequency switching (DFS) also affects the core frequency by halving or quartering the bus-to-core multiplier; see Section 9.7.5, "Dynamic Frequency Switching (DFS)," for more information. Note that when DFS is enabled the resulting core frequency must meet the adjusted minimum core frequency requirements ($f_{core\_DFS}$) described in Table 8. Note that the PLL_CFG[5] is currently used for factory test only and should be tied low, and that the MPC7448 PLL configuration settings are compatible with the MPC7447A PLL configuration settings when PLL_CFG[5] = 0.

**Table 12. MPC7448 Microprocessor PLL Configuration Example**

| PLL_CFG[0:5] | Example Core and VCO Frequency in MHz | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | Bus-to-Core Multiplier [5] | Core-to-VCO Multiplier [5] | Bus (SYSCLK) Frequency | | | | | | | |
| | | | 33.3 MHz | 50 MHz | 66.6 MHz | 75 MHz | 83 MHz | 100 MHz | 133 MHz | 167 MHz | 200 MHz |
| 010000 | 2x [6] | 1x | | | | | | | | | |
| 100000 | 3x [6] | 1x | | | | | | | | | 600 |
| 101000 | 4x [6] | 1x | | | | | | | | 667 | 800 |
| 101100 | 5x | 1x | | | | | | | 667 | 835 | 1000 |
| 100100 | 5.5x | 1x | | | | | | | 733 | 919 | 1100 |
| 110100 | 6x | 1x | | | | | | 600 | 800 | 1002 | 1200 |
| 010100 | 6.5x | 1x | | | | | | 650 | 866 | 1086 | 1300 |
| 001000 | 7x | 1x | | | | | | 700 | 931 | 1169 | 1400 |
| 000100 | 7.5x | 1x | | | | | 623 | 750 | 1000 | 1253 | 1500 |
| 110000 | 8x | 1x | | | | 600 | 664 | 800 | 1064 | 1336 | 1600 |
| 011000 | 8.5x | 1x | | | | 638 | 706 | 850 | 1131 | 1417 | 1700 |
| 011110 | 9x | 1x | | | 600 | 675 | 747 | 900 | 1197 | 1500 | |
| 011100 | 9.5x | 1x | | | 633 | 712 | 789 | 950 | 1264 | 1583 | |
| 101010 | 10x | 1x | | | 667 | 750 | 830 | 1000 | 1333 | 1667 | |
| 100010 | 10.5x | 1x | | | 700 | 938 | 872 | 1050 | 1397 | | |

## 9.4 Output Buffer DC Impedance

The MPC7448 processor bus drivers are characterized over process, voltage, and temperature. To measure $Z_0$, an external resistor is connected from the chip pad to $OV_{DD}$ or GND. The value of each resistor is varied until the pad voltage is $OV_{DD}/2$. Figure 20 shows the driver impedance measurement.

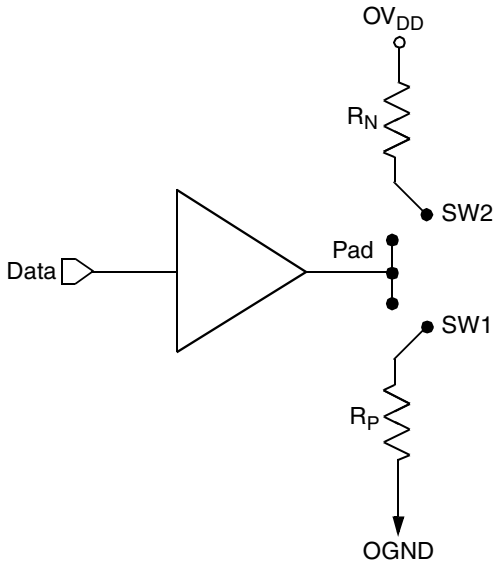



**Figure 20. Driver Impedance Measurement**

The output impedance is the average of two components—the resistances of the pull-up and pull-down devices. When data is held low, SW2 is closed (SW1 is open), and $R_N$ is trimmed until the voltage at the pad equals $OV_{DD}/2$. $R_N$ then becomes the resistance of the pull-down devices. When data is held high, SW1 is closed (SW2 is open), and $R_P$ is trimmed until the voltage at the pad equals $OV_{DD}/2$. $R_P$ then becomes the resistance of the pull-up devices. $R_P$ and $R_N$ are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N)/2$.

Table 15 summarizes the signal impedance results. The impedance increases with junction temperature and is relatively unaffected by bus voltage.

**Table 15. Impedance Characteristics**

At recommended operating conditions. See Table 4

| Impedance | | Processor Bus | Unit |
|---|---|---|---|
| $Z_0$ | Typical | 33–42 | Ω |
| | Maximum | 31–51 | Ω |

## 9.5 Pull-Up/Pull-Down Resistor Requirements

The MPC7448 requires high-resistive (weak: 4.7-KΩ) pull-up resistors on several control pins of the bus interface to maintain the control signals in the negated state after they have been actively negated and released by the MPC7448 or other bus masters. These pins are: $\overline{TS}$, $\overline{ARTRY}$, $\overline{SHDO}$, and $\overline{SHD1}$.

Some pins designated as being factory test pins must be pulled up to $OV_{DD}$ or down to GND to ensure proper device operation. The pins that must be pulled up to $OV_{DD}$ are $\overline{LSSD\_MODE}$ and TEST[0:3]; the pins that must be pulled down to GND are L1_TSTCLK and TEST[4]. The $\overline{CKSTP\_IN}$ signal should

to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must be merged into these signals with logic.

The arrangement shown in Figure 21 allows the COP port to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$, while ensuring that the target can drive $\overline{\text{HRESET}}$ as well. If the JTAG interface and COP header will not be used, $\overline{\text{TRST}}$ should be tied to $\overline{\text{HRESET}}$ through a 0-Ω isolation resistor so that it is asserted when the system reset signal ($\overline{\text{HRESET}}$) is asserted, ensuring that the JTAG scan chain is initialized during power-on. Although Freescale recommends that the COP header be designed into the system as shown in Figure 21, if this is not possible, the isolation resistor will allow future access to $\overline{\text{TRST}}$ in the case where a JTAG interface may need to be wired onto the system in debug situations.

The COP header shown in Figure 21 adds many benefits—breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features are possible through this interface—and can be as inexpensive as an unpopulated footprint for a header to be added when needed.

The COP interface has a standard header for connection to the target system, based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header). The connector typically has pin 14 removed as a connector key.

There is no standardized way to number the COP header shown in Figure 21; consequently, many different pin numbers have been observed from emulator vendors. Some are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom, while still others number the pins counter clockwise from pin 1 (as with an IC). Regardless of the numbering, the signal placement recommended in Figure 21 is common to all known emulators.

The $\overline{\text{QACK}}$ signal shown in Figure 21 is usually connected to the bridge chip or other system control logic in a system and is an input to the MPC7448 informing it that it can go into the quiescent state. Under normal operation this occurs during a low-power mode selection. In order for COP to work, the MPC7448 must see this signal asserted (pulled down). While shown on the COP header, not all emulator products drive this signal. If the product does not, a pull-down resistor can be populated to assert this signal. Additionally, some emulator products implement open-drain type outputs and can only drive $\overline{\text{QACK}}$ asserted; for these tools, a pull-up resistor can be implemented to ensure this signal is negated when it is not being driven by the tool. Note that the pull-up and pull-down resistors on the $\overline{\text{QACK}}$ signal are mutually exclusive and it is never necessary to populate both in a system. To preserve correct power-down operation, $\overline{\text{QACK}}$ should be merged through logic so that it also can be driven by the bridge or system logic.

### 9.7.1 Internal Package Conduction Resistance

For the exposed-die packaging technology described in Table 5, the intrinsic conduction thermal resistance paths are as follows:

- The die junction-to-case thermal resistance (the case is actually the top of the exposed silicon die)
- The die junction-to-board thermal resistance

Figure 24 depicts the primary heat transfer path for a package with an attached heat sink mounted to a printed-circuit board.

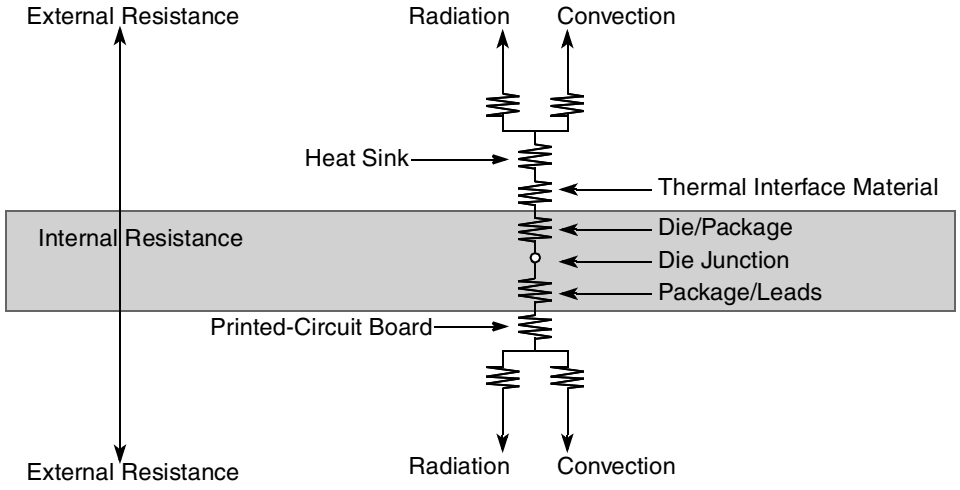



**Figure 24. C4 Package with Heat Sink Mounted to a Printed-Circuit Board**

Heat generated on the active side of the chip is conducted through the silicon, through the heat sink attach material (or thermal interface material), and, finally, to the heat sink, where it is removed by forced-air convection.

Because the silicon thermal resistance is quite small, the temperature drop in the silicon may be neglected for a first-order analysis. Thus, the thermal interface material and the heat sink conduction/convective thermal resistances are the dominant terms.

### 9.7.2 Thermal Interface Materials

A thermal interface material is recommended at the package lid-to-heat sink interface to minimize the thermal contact resistance. For those applications where the heat sink is attached by spring clip mechanism, Figure 25 shows the thermal performance of three thin-sheet thermal-interface materials (silicone, graphite/oil, fluoroether oil), a bare joint, and a joint with thermal grease as a function of contact pressure. As shown, the performance of these thermal interface materials improves with increasing contact pressure. The use of thermal grease significantly reduces the interface thermal resistance. That is, the bare joint results in a thermal resistance approximately seven times greater than the thermal grease joint.

Often, heat sinks are attached to the package by means of a spring clip to holes in the printed-circuit board (see Figure 22). Therefore, synthetic grease offers the best thermal performance due to the low interface pressure and is recommended due to the high power dissipation of the MPC7448. Of course, the selection

| | |
|---|---|
| Shin-Etsu MicroSi, Inc.<br>10028 S. 51st St.<br>Phoenix, AZ 85044<br>Internet: www.microsi.com | 888-642-7674 |
| Laird Technologies - Thermal<br>(formerly Thermagon Inc.)<br>4707 Detroit Ave.<br>Cleveland, OH 44102<br>Internet: www.lairdtech.com | 888-246-905 |

The following section provides a heat sink selection example using one of the commercially available heat sinks.

### 9.7.3 Heat Sink Selection Example

For preliminary heat sink sizing, the die-junction temperature can be expressed as follows:

$$T_j = T_i + T_r + (R_{\theta JC} + R_{\theta int} + R_{\theta sa}) \times P_d$$

where:

$T_j$ is the die-junction temperature
$T_i$ is the inlet cabinet ambient temperature
$T_r$ is the air temperature rise within the computer cabinet
$R_{\theta JC}$ is the junction-to-case thermal resistance
$R_{\theta int}$ is the adhesive or interface material thermal resistance
$R_{\theta sa}$ is the heat sink base-to-ambient thermal resistance
$P_d$ is the power dissipated by the device

During operation, the die-junction temperatures ($T_j$) should be maintained less than the value specified in Table 4. The temperature of air cooling the component greatly depends on the ambient inlet air temperature and the air temperature rise within the electronic cabinet. An electronic cabinet inlet-air temperature ($T_i$) may range from 30□ to 40□C. The air temperature rise within a cabinet ($T_r$) may be in the range of 5□ to 10□C. The thermal resistance of the thermal interface material ($R_{\theta int}$) is typically about 1.1 □C/W. For example, assuming a $T_i$ of 30□C, a $T_r$ of 5□C, an HCTE package $R_{\theta JC}$ = 0.1, and a power consumption ($P_d$) of 25.6 W, the following expression for $T_j$ is obtained:

Die-junction temperature: $T_j = 30□C + 5□C + (0.1□C/W + 1.1□C/W + \theta_{sa}) \times 25.6$

For this example, a $R_{\theta sa}$value of 1.53 □C/W or less is required to maintain the die junction temperature below the maximum value of Table 4.

Though the die junction-to-ambient and the heat sink-to-ambient thermal resistances are a common figure-of-merit used for comparing the thermal performance of various microelectronic packaging technologies, one should exercise caution when only using this metric in determining thermal management because no single parameter can adequately describe three-dimensional heat flow. The final die-junction operating temperature is not only a function of the component-level thermal resistance, but the system-level design and its operating conditions. In addition to the component's power consumption, a number of factors affect the final operating die-junction temperature—airflow, board population (local heat flux of adjacent components), heat sink efficiency, heat sink attach, heat sink placement, next-level interconnect technology, system air temperature rise, altitude, and so on.

Due to the complexity and variety of system-level boundary conditions for today's microelectronic equipment, the combined effects of the heat transfer mechanisms (radiation, convection, and conduction) may vary widely. For these reasons, we recommend using conjugate heat transfer models for the board as well as system-level designs.

For system thermal modeling, the MPC7448 thermal model is shown in Figure 26. Four volumes represent this device. Two of the volumes, solder ball-air and substrate, are modeled using the package outline size of the package. The other two, die and bump-underfill, have the same size as the die. The silicon die should be modeled $8.0 \times 7.3 \times 0.86$ mm$^3$ with the heat source applied as a uniform source at the bottom of the volume. The bump and underfill layer is modeled as $8.0 \times 7.3 \times 0.07$ mm$^3$collapsed in the z-direction with a thermal conductivity of 5.0 W/(m • K) in the z-direction. The substrate volume is $25 \times 25 \times 1.14$ mm$^3$ and has 9.9 W/(m • K) isotropic conductivity in the xy-plane and 2.95 W/(m • K) in the direction of the z-axis. The solder ball and air layer are modeled with the same horizontal dimensions as the substrate and is 0.8 mm thick. For the LGA package the solder and air layer is 0.1 mm thick, but the material properties are the same. It can also be modeled as a collapsed volume using orthotropic material properties: 0.034 W/(m • K) in the xy-plane direction and 11.2 W/(m • K) in the direction of the z-axis.

| Conductivity | Value | Unit |
|---|---|---|
| **Die ($8.0 \times 7.3 \times 0.86$ mm$^3$)** | | |
| Silicon | Temperature-dependent | W/(m • K) |
| **Bump and Underfill ($8.0 \times 7.3 \times 0.07$ mm$^3$)** | | |
| $k_z$ | 5.0 | W/(m • K) |
| **Substrate ($25 \times 25 \times 1.14$ mm$^3$)** | | |
| $k_x$ | 9.9 | W/(m • K) |
| $k_y$ | 9.9 | |
| $k_z$ | 2.95 | |
| **Solder Ball and Air ($25 \times 25 \times 0.8$ mm$^3$)** | | |
| $k_x$ | 0.034 | W/(m • K) |
| $k_y$ | 0.034 | |
| $k_z$ | 11.2 | |

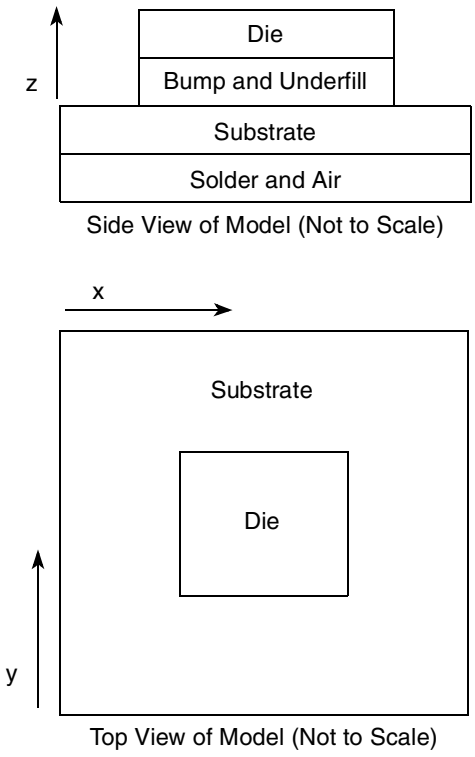



**Figure 26. Recommended Thermal Model of MPC7448**

Solving for T, the equation becomes:

$$nT = \frac{V_H - V_L}{1.986 \times 10^{-4}}$$

### 9.7.5 Dynamic Frequency Switching (DFS)

The DFS feature in the MPC7448 adds the ability to divide the processor-to-system bus ratio by two or four during normal functional operation. Divide-by-two mode is enabled by setting the HID1[DFS2] bit in software or by asserting the $\overline{\text{DFS2}}$ pin via hardware. The MPC7448 can be returned for full speed by clearing HID1[DFS2] or negating $\overline{\text{DFS2}}$. Similarly, divide-by-four mode is enabled by setting HID1[DFS4] in software or by asserting the $\overline{\text{DFS4}}$ pin. In all cases, the frequency change occurs in 1 clock cycle and no idle waiting period is required to switch between modes. Note that asserting either $\overline{\text{DFS2}}$ or $\overline{\text{DFS4}}$ overrides software control of DFS, and that asserting both $\overline{\text{DFS2}}$ and $\overline{\text{DFS4}}$ disables DFS completely, including software control. Additional information regarding DFS can be found in the *MPC7450 RISC Microprocessor Family Reference Manual.* Note that minimum core frequency requirements must be observed when enabling DFS, and the resulting core frequency must meet the requirements for $f_{core\_DFS}$ given in Table 8.

#### 9.7.5.1 Power Consumption with DFS Enabled

Power consumption with DFS enabled can be approximated using the following formula:

$$P_{DFS} = \left[\frac{f_{DFS}}{f}\ (P - P_{DS})\right] + P_{DS}$$

Where:

$P_{DFS}$ = Power consumption with DFS enabled
$f_{DFS}$ = Core frequency with DFS enabled
f = Core frequency prior to enabling DFS
P = Power consumption prior to enabling DFS (see Table 7)
$P_{DS}$ = Deep sleep mode power consumption (see Table 7)

The above is an approximation only. Power consumption with DFS enabled is not tested or guaranteed.

#### 9.7.5.2 Bus-to-Core Multiplier Constraints with DFS

DFS is not available for all bus-to-core multipliers as configured by PLL_CFG[0:5] during hard reset. The complete listing is shown in Table 16. Shaded cells represent DFS modes that are not available for a particular PLL_CFG[0:5] setting. Should software or hardware attempt to transition to a multiplier that is not supported, the device will remain at its current multiplier. For example, if a transition from DFS-disabled to an unsupported divide-by-2 or divide-by-4 setting is attempted, the bus-to-core multiplier will remain at the setting configured by the PLL_CFG[0:5] pins. In the case of an attempted transition from a supported divide-by-2 mode to an unsupported divide-by-4 mode, the device will remain in divide-by-2 mode. In all cases, the HID1[PC0-5] bits will correctly reflect the current bus-to-core frequency multiplier.

**Table 16. Valid Divide Ratio Configurations (continued)**

| DFS mode disabled | | DFS divide-by-2 mode enabled (HID1[DFS2] = 1 or $\overline{\text{DFS2}}$ = 0) | | DFS divide-by-4 mode enabled (HID1[DFS4] = 1 or $\overline{\text{DFS4}}$ = 0) | |
|---|---|---|---|---|---|
| Bus-to-Core Multiplier Configured by PLL_CFG[0:5] (see Table 12) | HID1[PC0-5] [3] | Bus-to-Core Multiplier | HID1[PC0-5] [3] | Bus-to-Core Multiplier | HID1[PC0-5] [3] |
| 24x | 011010 | 12x | 101110 | 6x | 110100 |
| 28x | 111010 | 14x | 110010 | 7x | 001000 |

**Notes:**
1. DFS mode is not supported for this combination of DFS mode and PLL_CFG[0:5] setting. As a result, the processor will ignore these settings and remain at the previous multiplier, as reflected by the HID1[PC0-PC5] bits.
2. Though supported by the MPC7448 clock circuitry, multipliers of *n*.25x and *n*.75x cannot be expressed as valid PLL configuration codes. As a result, the values displayed in HID1[PC0-PC5] are rounded down to the nearest valid PLL configuration code. However, the actual bus-to-core multiplier is as stated in this table.
3. Note that in the HID1 register of the MPC7448, the PC0, PC1, PC2, PC3, PC4, and PC5 bits are bits 15, 16, 17, 18, 19, and 14 (respectively). See the *MPC7450 RISC Microprocessor Reference Manual* for more information.
4. Special considerations regarding snooped transactions must be observed for bus-to-core multipliers less than 5x. See the *MPC7450 RISC Microprocessor Reference Manual* for more information.

### 9.7.5.3 Minimum Core Frequency Requirements with DFS

In many systems, enabling DFS can result in very low processor core frequencies. However, care must be taken to ensure that the resulting processor core frequency is within the limits specified in Table 8. Proper operation of the device is not guaranteed at core frequencies below the specified minimum $f_{core}$.

# 10 Document Revision History

Table 17 provides a revision history for this hardware specification.

**Table 17. Document Revision History**

| Revision | Date | Substantive Change(s) |
|---|---|---|
| 4 | 3/2007 | Table 19: Added 800 MHz processor frequency. |
| 3 | 10/2006 | Section 9.7, “Power and Thermal Management Information”: Updated contact information.<br>Table 18, Table 20, and Table 19: Added Revision D PVR.<br>Table 19: Added 600 processor frequency, additional product codes, date codes for 1400 processor frequency, and footnotes 1 and 2.<br>Table 20: Added PPC product code and footnote 1.<br>Table 19 and Table 20: Added Revision D information for 1267 processor frequency. |