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Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC G4
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.7GHz
Co-Processors/DSP	Multimedia; SIMD
RAM Controllers	-
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	1.5V, 1.8V, 2.5V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	360-CLGA, FCCLGA
Supplier Device Package	360-FCCLGA (25x25)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmc7448vs1700lc

Table 6. DC Electrical Specifications (continued)

 At recommended operating conditions. See [Table 4](#).

Characteristic		Nominal Bus Voltage ¹	Symbol	Min	Max	Unit	Notes
High-impedance (off-state) leakage current: $V_{in} = OV_{DD}$ $V_{in} = GND$		—	I_{TSI}	—	50 – 50	μA	2, 3, 4
Output high voltage @ $I_{OH} = -5$ mA		1.5	V_{OH}	$OV_{DD} - 0.45$	—	V	
		1.8		$OV_{DD} - 0.45$	—		
		2.5		1.8	—		
Output low voltage @ $I_{OL} = 5$ mA		1.5	V_{OL}	—	0.45	V	
		1.8		—	0.45		
		2.5		—	0.6		
Capacitance, $V_{in} = 0$ V, $f = 1$ MHz	All inputs		C_{in}	—	8.0	pF	5

Notes:

1. Nominal voltages; see [Table 4](#) for recommended operating conditions.
2. All I/O signals are referenced to OV_{DD} .
3. Excludes test signals and IEEE Std. 1149.1 boundary scan (JTAG) signals
4. The leakage is measured for nominal OV_{DD} and V_{DD} , or both OV_{DD} and V_{DD} must vary in the same direction (for example, both OV_{DD} and V_{DD} vary by either +5% or –5%).
5. Capacitance is periodically sampled rather than 100% tested.
6. These pins have internal pull-up resistors.

[Table 7](#) provides the power consumption for the MPC7448 part numbers described by this document; see [Section 11.1, “Part Numbers Fully Addressed by This Document,”](#) for information regarding which part numbers are described by this document. Freescale also offers MPC7448 part numbers that meet lower power consumption specifications by adhering to lower core voltage and core frequency specifications. For more information on these devices, including references to the MPC7448 Hardware Specification Addenda that describe these devices, see [Section 11.2, “Part Numbers Not Fully Addressed by This Document.”](#)

The power consumptions provided in [Table 7](#) represent the power consumption of each speed grade when operated at the rated maximum core frequency (see [Table 8](#)). Freescale sorts devices by power as well as by core frequency, and power limits for each speed grade are independent of each other. Each device is tested at its maximum core frequency only. (Note that Deep Sleep Mode power consumption is independent of clock frequency.) Operating a device at a frequency lower than its rated maximum is fully supported provided the clock frequencies are within the specifications given in [Table 8](#), and a device operated below its rated maximum will have lower power consumption. However, inferences should not be made about a device’s power consumption based on the power specifications of another (lower) speed grade. For example, a 1700 MHz device operated at 1420 MHz may not exhibit the same power consumption as a 1420 MHz device operated at 1420 MHz.

For all MPC7448 devices, the following guidelines on the use of these parameters for system design are suggested. The Full-Power Mode–Typical value represents the sustained power consumption of the device

Table 8. Clock AC Timing Specifications

 At recommended operating conditions. See [Table 4](#).

Characteristic		Symbol	Maximum Processor Core Frequency (Speed Grade)								Unit	Notes
			1000 MHz		1420 MHz		1600 MHz		1700 MHz			
			Min	Max	Min	Max	Min	Max	Min	Max		
Processor core frequency	DFS mode disabled	f_{core}	600	1000	600	1420	600	1600	600	1700	MHz	1, 8
	DFS mode enabled	f_{core_DF}	300	500	300	710	300	800	300	850		9
VCO frequency		f_{VCO}	600	1000	600	1420	600	800	600	1700	MHz	1, 10
SYSCLK frequency		f_{SYSCLK}	33	200	33	200	33	200	33	200	MHz	1, 2, 8
SYSCLK cycle time		t_{SYSCLK}	5.0	30	5.0	30	5.0	30	5.0	30	ns	2
SYSCLK rise and fall time		t_{KR}, t_{KF}	—	0.5	—	0.5	—	0.5	—	0.5	ns	3
SYSCLK duty cycle measured at $OV_{DD}/2$		t_{KHKL}/t_{SYSCLK}	40	60	40	60	40	60	40	60	%	4
SYSCLK cycle-to-cycle jitter			—	150	—	150	—	150	—	150	ps	5, 6
Internal PLL relock time			—	100	—	100	—	100	—	100	μ s	7

Notes:

- Caution:** The SYSCLK frequency and PLL_CFG[0:5] settings must be chosen such that the resulting SYSCLK (bus) frequency, processor core frequency, and PLL (VCO) frequency do not exceed their respective maximum or minimum operating frequencies. Refer to the PLL_CFG[0:5] signal description in [Section 9.1.1, “PLL Configuration,”](#) for valid PLL_CFG[0:5] settings.
- Actual maximum system bus frequency is system-dependent. See [Section 5.2.1, “Clock AC Specifications.”](#)
- Rise and fall times for the SYSCLK input measured from 0.4 to 1.4 V
- Timing is guaranteed by design and characterization.
- Guaranteed by design
- The SYSCLK driver's closed loop jitter bandwidth should be less than 1.5 MHz at -3 dB.
- Relock timing is guaranteed by design and characterization. PLL-relock time is the maximum amount of time required for PLL lock after a stable V_{DD} and SYSCLK are reached during the power-on reset sequence. This specification also applies when the PLL has been disabled and subsequently re-enabled during sleep mode. Also note that \overline{HRESET} must be held asserted for a minimum of 255 bus clocks after the PLL-relock time during the power-on reset sequence.
- This reflects the maximum and minimum core frequencies when the dynamic frequency switching feature (DFS) is disabled. f_{core_DFS} provides the maximum and minimum core frequencies when operating in a DFS mode.
- This specification supports the Dynamic Frequency Switching (DFS) feature and is applicable only when one of the DFS modes (divide-by-2 or divide-by-4) is enabled. When DFS is disabled, the core frequency must conform to the maximum and minimum frequencies stated for f_{core} .
- Use of the DFS feature does not affect VCO frequency.

Figure 4 provides the AC test load for the MPC7448.

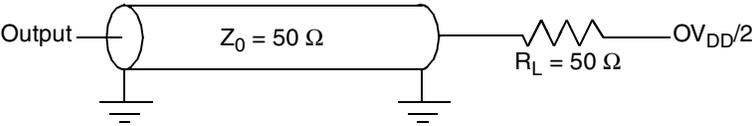


Figure 4. AC Test Load

Figure 5 provides the $\overline{BMODE}[0:1]$ input timing diagram for the MPC7448. These mode select inputs are sampled once before and once after \overline{HRESET} negation.

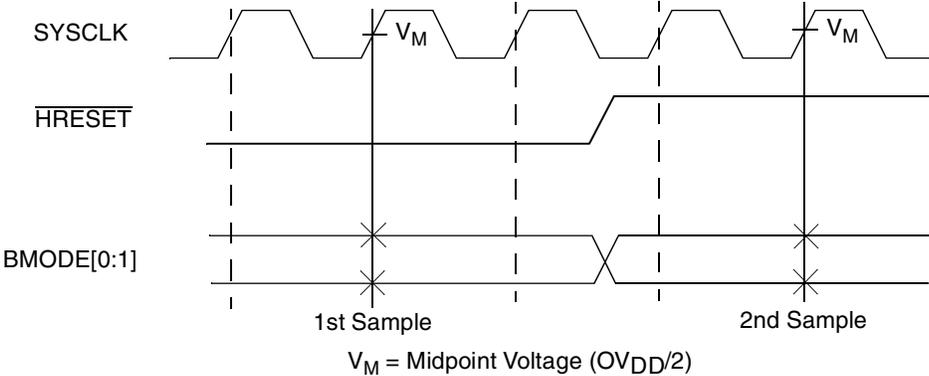


Figure 5. $\overline{BMODE}[0:1]$ Input Sample Timing Diagram

Figure 11 provides the test access port timing diagram.

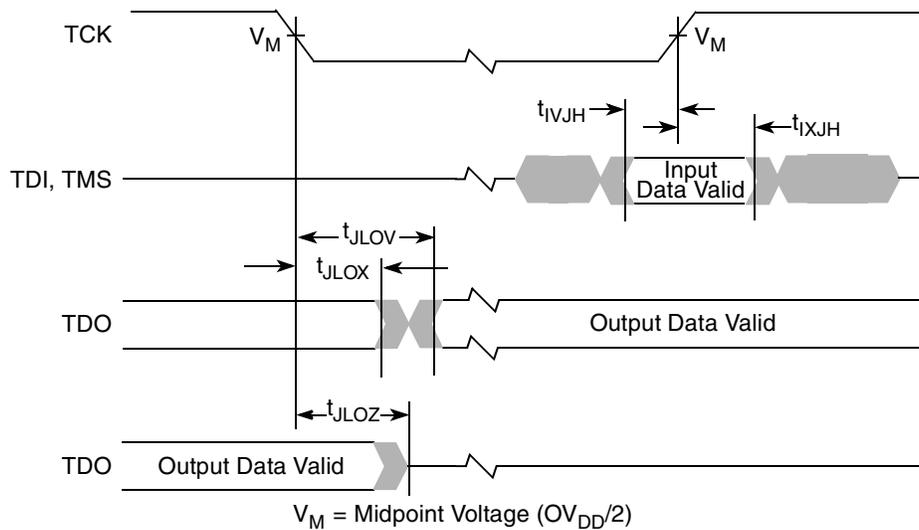


Figure 11. Test Access Port Timing Diagram

5.3 Voltage and Frequency Derating

Voltage and frequency derating is no longer supported for part numbers described by this document beginning with datecode 0613. (See [Section 11, “Part Numbering and Marking,”](#) for information on date code markings.) It is supported by some MPC7448 part numbers which target low-power applications; see [Section 11.2, “Part Numbers Not Fully Addressed by This Document”](#) and the referenced MPC7448 Hardware Specification Addenda for more information on these low-power devices. For those devices which previously supported this feature, information has been archived in the *Chip Errata for the MPC7448* (document order no. MPC7448CE).

7 Pinout Listings

Table 11 provides the pinout listing for the MPC7448, 360 HCTE package. The pinouts of the MPC7448 and MPC7447A are compatible, but the requirements regarding the use of the additional power and ground pins have changed. The MPC7448 requires these pins be connected to the appropriate power or ground plane to achieve high core frequencies; see Section 9.3, “Connection Recommendations,” for additional information. As a result, these pins should be connected in all new designs.

Additionally, the MPC7448 may be populated on a board designed for a MPC7447 (or MPC7445 or MPC7441), provided the core voltage can be made to match the requirements in Table 4 and all pins defined as ‘no connect’ for the MPC7447 are unterminated, as required by the *MPC7457 RISC Microprocessor Hardware Specifications*. The MPC7448 uses pins previously marked ‘no connect’ for the temperature diode pins and for additional power and ground connections. The additional power and ground pins are required to achieve high core frequencies and core frequency will be limited if they are not connected; see Section 9.3, “Connection Recommendations,” for additional information. Because these ‘no connect’ pins in the MPC7447 360 pin package are not driven in functional mode, an MPC7447 can be populated in an MPC7448 board.

NOTE

Caution must be exercised when performing boundary scan test operations on a board designed for an MPC7448, but populated with an MPC7447 or earlier device. This is because in the MPC7447 it is possible to drive the latches associated with the former ‘no connect’ pins in the MPC7447, potentially causing contention on those pins. To prevent this, ensure that these pins are not connected on the board or, if they are connected, ensure that the states of internal MPC7447 latches do not cause these pins to be driven during board testing.

For the MPC7448, pins that were defined as the TEST[0:4] factory test signal group on the MPC7447A and earlier devices have been assigned new functions. For most of these, the termination recommendations for the TEST[0:4] pins of the MPC7447A are compatible with the MPC7448 and will allow correct operation with no performance loss. The exception is BVSEL1 (TEST3 on the MPC7447A and earlier devices), which may require a different termination depending which I/O voltage mode is desired; see Table 3 for more information.

NOTE

This pinout is not compatible with the MPC750, MPC7400, or MPC7410 360 BGA package.

Table 11. Pinout Listing for the MPC7448, 360 HCTE Package (continued)

Signal Name	Pin Number	Active	I/O	Notes
VDD_SENSE	G13, N12	—	—	18

Notes:

1. OV_{DD} supplies power to the processor bus, JTAG, and all control signals, and is configurable. (V_{DD} supplies power to the processor core, and AV_{DD} supplies power to the PLL after filtering from V_{DD}). To program the I/O voltage, see Table 3. If used, the pull-down resistor should be less than 250 Ω . Because these settings may change in future products, it is recommended BVSEL[0:1] be configured using resistor options, jumpers, or some other flexible means, with the capability to reconfigure the termination of this signal in the future if necessary. For actual recommended value of V_{in} or supply voltages see Table 4.
2. Unused address pins must be pulled down to GND and corresponding address parity pins pulled up to OV_{DD} .
3. These pins require weak pull-up resistors (for example, 4.7 K Ω) to maintain the control signals in the negated state after they have been actively negated and released by the MPC7448 and other bus masters.
4. This signal selects between MPX bus mode (asserted) and 60x bus mode (negated) and will be sampled at \overline{HRESET} going high.
5. This signal must be negated during reset, by pull-up resistor to OV_{DD} or negation by $\overline{\overline{HRESET}}$ (inverse of \overline{HRESET}), to ensure proper operation.
6. Internal pull up on die.
7. Not used in 60x bus mode.
8. These signals must be pulled down to GND if unused, or if the MPC7448 is in 60x bus mode.
9. These input signals are for factory use only and must be pulled down to GND for normal machine operation.
10. This test signal is recommended to be tied to \overline{HRESET} ; however, other configurations will not adversely affect performance.
11. These signals are for factory use only and must be left unconnected for normal machine operation. Some pins that were NCs on the MPC7447, MPC7445, and MPC7441 have now been defined for other purposes.
12. These input signals are for factory use only and must be pulled up to OV_{DD} for normal machine operation.
13. This pin can externally cause a performance monitor event. Counting of the event is enabled through software.
14. This signal must be asserted during reset, by pull down to GND or assertion by \overline{HRESET} , to ensure proper operation.
15. These pins were NCs on the MPC7447, MPC7445, and MPC7441. See Section 9.3, "Connection Recommendations," for more information.
16. These pins were OV_{DD} pins on the MPC7447, MPC7445, and MPC7441. These pins are internally connected to OV_{DD} and are intended to allow an external device (such as a power supply) to detect the I/O voltage level present inside the device package. If unused, it is recommended they be connected to test points to facilitate system debug; otherwise, they may be connected directly to OV_{DD} or left unconnected.
17. These pins provide connectivity to the on-chip temperature diode that can be used to determine the die junction temperature of the processor. These pins may be left unterminated if unused.
18. These pins are internally connected to V_{DD} and are intended to allow an external device (such as a power supply) to detect the processor core voltage level present inside the device package. If unused, it is recommended they be connected to test points to facilitate system debug; otherwise, they may be connected directly to V_{DD} or left unconnected.
19. These pins are internally connected to GND and are intended to allow an external device to detect the processor ground voltage level present inside the device package. If unused, it is recommended they be connected to test points to facilitate system debug; otherwise, they may be connected directly to GND or left unconnected.
20. These pins were in the TEST[0:4] factory test pin group on the MPC7447A, MPC7447, MPC7445, and MPC7441. They have been assigned new functions on the MPC7448.
21. These pins can be used to enable the supported dynamic frequency switching (DFS) modes via hardware. If both are pulled down, DFS mode is disabled completely and cannot be enabled via software. If unused, they should be pulled up to OV_{DD} to allow software control of DFS. See the *MPC7450 RISC Microprocessor Family Reference Manual* for more information.
22. This pin is provided to allow operation of the L2 cache at low core voltages and is for factory use only. See the *MPC7450 RISC Microprocessor Family Reference Manual* for more information.

8 Package Description

The following sections provide the package parameters and mechanical dimensions for the HCTE package.

8.1 Package Parameters for the MPC7448, 360 HCTE BGA

The package parameters are as provided in the following list. The package type is 25 × 25 mm, 360-lead high coefficient of thermal expansion ceramic ball grid array (HCTE).

Package outline	25 × 25 mm
Interconnects	360 (19 × 19 ball array – 1)
Pitch	1.27 mm (50 mil)
Minimum module height	2.32 mm
Maximum module height	2.80 mm
Ball diameter	0.89 mm (35 mil)
Coefficient of thermal expansion	12.3 ppm/°C

9 System Design Information

This section provides system and thermal design requirements and recommendations for successful application of the MPC7448.

9.1 Clocks

The following sections provide more detailed information regarding the clocking of the MPC7448.

9.1.1 PLL Configuration

The MPC7448 PLL is configured by the PLL_CFG[0:5] signals. For a given SYSCLK (bus) frequency, the PLL configuration signals set the internal CPU and VCO frequency of operation. The PLL configuration for the MPC7448 is shown in Table 12. In this example, shaded cells represent settings that, for a given SYSCLK frequency, result in core and/or VCO frequencies that do not comply with Table 8. When enabled, dynamic frequency switching (DFS) also affects the core frequency by halving or quartering the bus-to-core multiplier; see Section 9.7.5, “Dynamic Frequency Switching (DFS),” for more information. Note that when DFS is enabled the resulting core frequency must meet the adjusted minimum core frequency requirements ($f_{\text{core_DFS}}$) described in Table 8. Note that the PLL_CFG[5] is currently used for factory test only and should be tied low, and that the MPC7448 PLL configuration settings are compatible with the MPC7447A PLL configuration settings when PLL_CFG[5] = 0.

Table 12. MPC7448 Microprocessor PLL Configuration Example

PLL_CFG[0:5]	Example Core and VCO Frequency in MHz											
	Bus-to-Core Multiplier ⁵	Core-to-VCO Multiplier ⁵	Bus (SYSCLK) Frequency									
			33.3 MHz	50 MHz	66.6 MHz	75 MHz	83 MHz	100 MHz	133 MHz	167 MHz	200 MHz	
010000	2x ⁶	1x										
100000	3x ⁶	1x										600
101000	4x ⁶	1x									667	800
101100	5x	1x								667	835	1000
100100	5.5x	1x								733	919	1100
110100	6x	1x						600	800	1002	1200	
010100	6.5x	1x						650	866	1086	1300	
001000	7x	1x						700	931	1169	1400	
000100	7.5x	1x					623	750	1000	1253	1500	
110000	8x	1x				600	664	800	1064	1336	1600	
011000	8.5x	1x				638	706	850	1131	1417	1700	
011110	9x	1x			600	675	747	900	1197	1500		
011100	9.5x	1x			633	712	789	950	1264	1583		
101010	10x	1x			667	750	830	1000	1333	1667		
100010	10.5x	1x			700	938	872	1050	1397			

These requirements are shown graphically in [Figure 16](#).

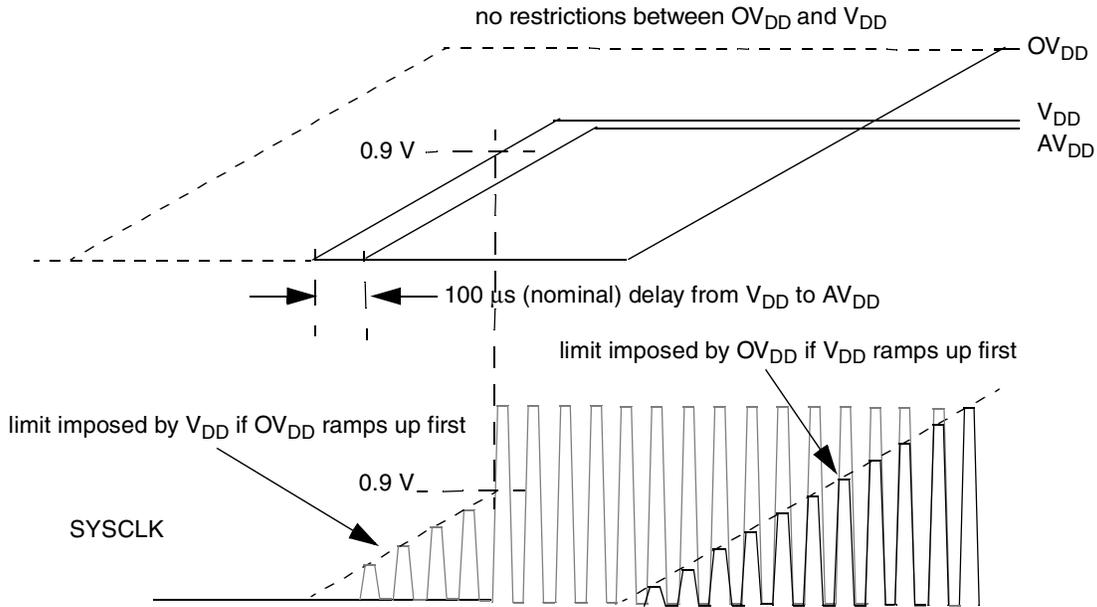


Figure 16. MPC7448 Power Up Sequencing Requirements

Certain stipulations also apply to the manner in which the power rails of the MPC7448 power down, as follows:

- OV_{DD} may ramp down any time before or after V_{DD} .
- The voltage at the SYSCLK input must not exceed V_{DD} once V_{DD} has ramped down below 0.9 V.
- The voltage at the SYSCLK input must not exceed OV_{DD} by more 20% during transients (see overshoot/undershoot specifications in [Figure 2](#)) or 0.3 V DC (see [Table 2](#)) at any time.

9.2.3 Transient Specifications

To ensure the long-term reliability of the device, the MPC7448 requires that transients on the core power rail (V_{DD}) be constrained. The recommended operating voltage specifications provided in [Table 4](#) are DC specifications. That is, the device may be operated continuously with V_{DD} within the specified range without adversely affecting the device's reliability. Excursions above the stated recommended operation range, including overshoot during power-up, can impact the long-term reliability of the device. Excursions are described by their amplitude and duration. Duration is defined as the time period during which the V_{DD} power plane, as measured at the VDD_SENSE pins, will be within a specific voltage range, expressed as percentage of the total time the device will be powered up over the device lifetime. In practice, the period over which transients are measured can be any arbitrary period of time that accurately represents the expected range of processor and system activity. The voltage ranges and durations for normal operation and transients are described in [Table 14](#).

Table 14. VDD Power Supply Transient Specifications

At recommended operating temperatures. See [Table 4](#).

Voltage Region	Voltage Range (V)		Permitted Duration ¹	Notes
	Min	Max		
Normal	V_{DD} minimum	V_{DD} maximum	100%	2
Low Transient	V_{DD} maximum	1.35 V	10%	2, 3
High Transient	1.35 V	1.40 V	0.2%	4

Notes:

1. Permitted duration is defined as the percentage of the total time the device is powered on that the V_{DD} power supply voltage may exist within the specified voltage range.
2. See [Table 4](#) for nominal V_{DD} specifications.
3. To simplify measurement, excursions into the High Transient region are included in this duration.
4. Excursions above the absolute maximum rating of 1.4 V are not permitted; see [Table 2](#).

Note that, to simplify transient measurements, the duration of the excursion into the High Transient region is also included in the Low Transient duration, so that only the time the voltage is above each threshold must be considered. [Figure 19](#) shows an example of measuring voltage transients.

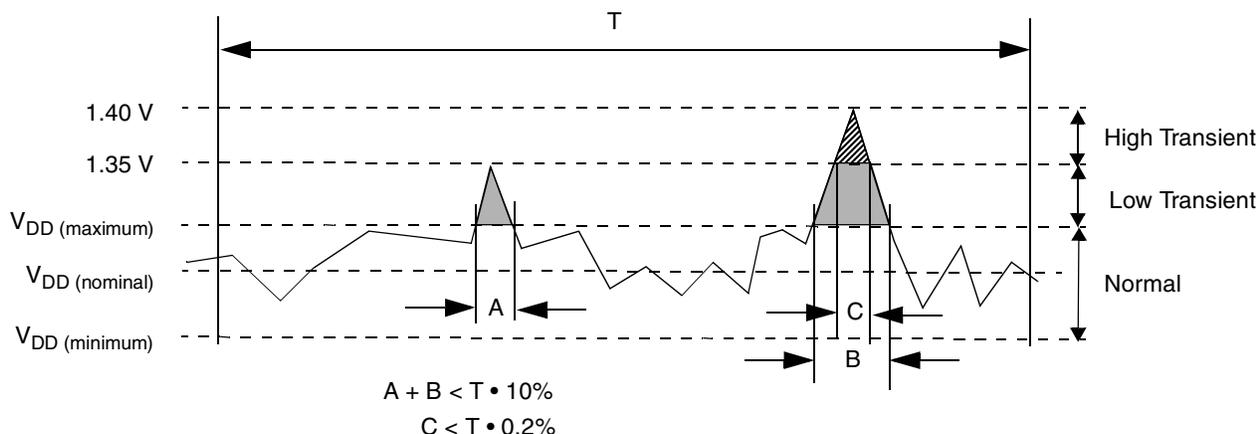


Figure 19. Voltage Transient Example

9.2.4 Decoupling Recommendations

Due to the MPC7448 dynamic power management feature, large address and data buses, and high operating frequencies, the MPC7448 can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the MPC7448 system, and the MPC7448 itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer use sufficient decoupling capacitors, typically one capacitor for every V_{DD} pin, and a similar amount for the OV_{DD} pins, placed as close as possible to the power pins of the MPC7448. It is also recommended that these decoupling capacitors receive their power from separate V_{DD} , OV_{DD} , and GND power planes in the PCB, using short traces to minimize inductance.

These capacitors should have a value of 0.01 or 0.1 μF . Only ceramic surface mount technology (SMT) capacitors should be used to minimize lead inductance. Orientations where connections are made along the length of the part, such as 0204, are preferable but not mandatory. Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993) and contrary to previous recommendations for decoupling Freescale microprocessors, multiple small capacitors of equal value are recommended over using multiple values of capacitance.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V_{DD} and OV_{DD} planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low equivalent series resistance (ESR) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors are 100–330 μF (AVX TPS tantalum or Sanyo OSCON).

9.3 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. Unless otherwise noted, unused active low inputs should be tied to OV_{DD} and unused active high inputs should be connected to GND. All NC (no connect) signals must remain unconnected.

Power and ground connections must be made to all external V_{DD} , OV_{DD} , and GND pins in the MPC7448. For backward compatibility with the MPC7447, MPC7445, and MP7441, or for migrating a system originally designed for one of these devices to the MPC7448, the new power and ground signals (formerly NC, see [Table 11](#)) may be left unconnected if the core frequency is 1 GHz or less. Operation above 1 GHz requires that these additional power and ground signals be connected, and it is strongly recommended that all new designs include the additional connections. See also [Section 7, “Pinout Listings,”](#) for additional information.

The MPC7448 provides VDD_SENSE , $OVDD_SENSE$, and GND_SENSE pins. These pins connect directly to the power/ground planes in the device package and are intended to allow an external device to measure the voltage present on the V_{DD} , OV_{DD} and GND planes in the device package. The most common use for these signals is as a feedback signal to a power supply regulator to allow it to compensate for board losses and supply the correct voltage at the device. (Note that all voltage parameters are specified at the pins of the device.) If not used for this purpose, it is recommended that these signals be connected to test points that can be used in the event that an accurate measurement of the voltage at the device is needed during system debug. Otherwise, these signals should be connected to the appropriate power/ground planes on the circuit board or left unconnected.

9.4 Output Buffer DC Impedance

The MPC7448 processor bus drivers are characterized over process, voltage, and temperature. To measure Z_0 , an external resistor is connected from the chip pad to OV_{DD} or GND. The value of each resistor is varied until the pad voltage is $OV_{DD}/2$. Figure 20 shows the driver impedance measurement.

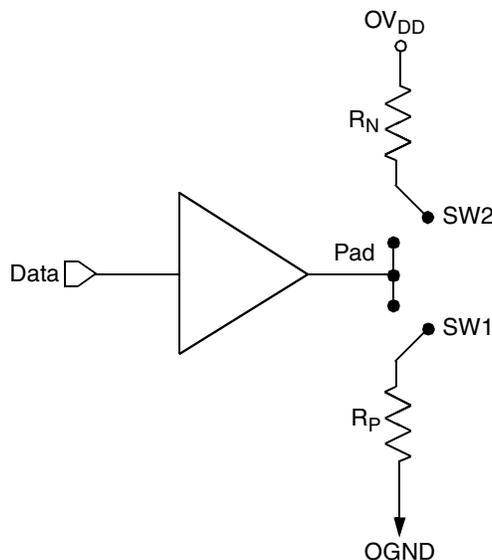


Figure 20. Driver Impedance Measurement

The output impedance is the average of two components—the resistances of the pull-up and pull-down devices. When data is held low, SW2 is closed (SW1 is open), and R_N is trimmed until the voltage at the pad equals $OV_{DD}/2$. R_N then becomes the resistance of the pull-down devices. When data is held high, SW1 is closed (SW2 is open), and R_P is trimmed until the voltage at the pad equals $OV_{DD}/2$. R_P then becomes the resistance of the pull-up devices. R_P and R_N are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N)/2$.

Table 15 summarizes the signal impedance results. The impedance increases with junction temperature and is relatively unaffected by bus voltage.

Table 15. Impedance Characteristics

At recommended operating conditions. See Table 4

Impedance		Processor Bus	Unit
Z_0	Typical	33–42	Ω
	Maximum	31–51	Ω

9.5 Pull-Up/Pull-Down Resistor Requirements

The MPC7448 requires high-resistive (weak: 4.7-K Ω) pull-up resistors on several control pins of the bus interface to maintain the control signals in the negated state after they have been actively negated and released by the MPC7448 or other bus masters. These pins are: \overline{TS} , \overline{ARTRY} , \overline{SHDO} , and \overline{SHDI} .

Some pins designated as being factory test pins must be pulled up to OV_{DD} or down to GND to ensure proper device operation. The pins that must be pulled up to OV_{DD} are $\overline{LSSD_MODE}$ and TEST[0:3]; the pins that must be pulled down to GND are L1_TSTCLK and TEST[4]. The CKSTP_IN signal should

to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must be merged into these signals with logic.

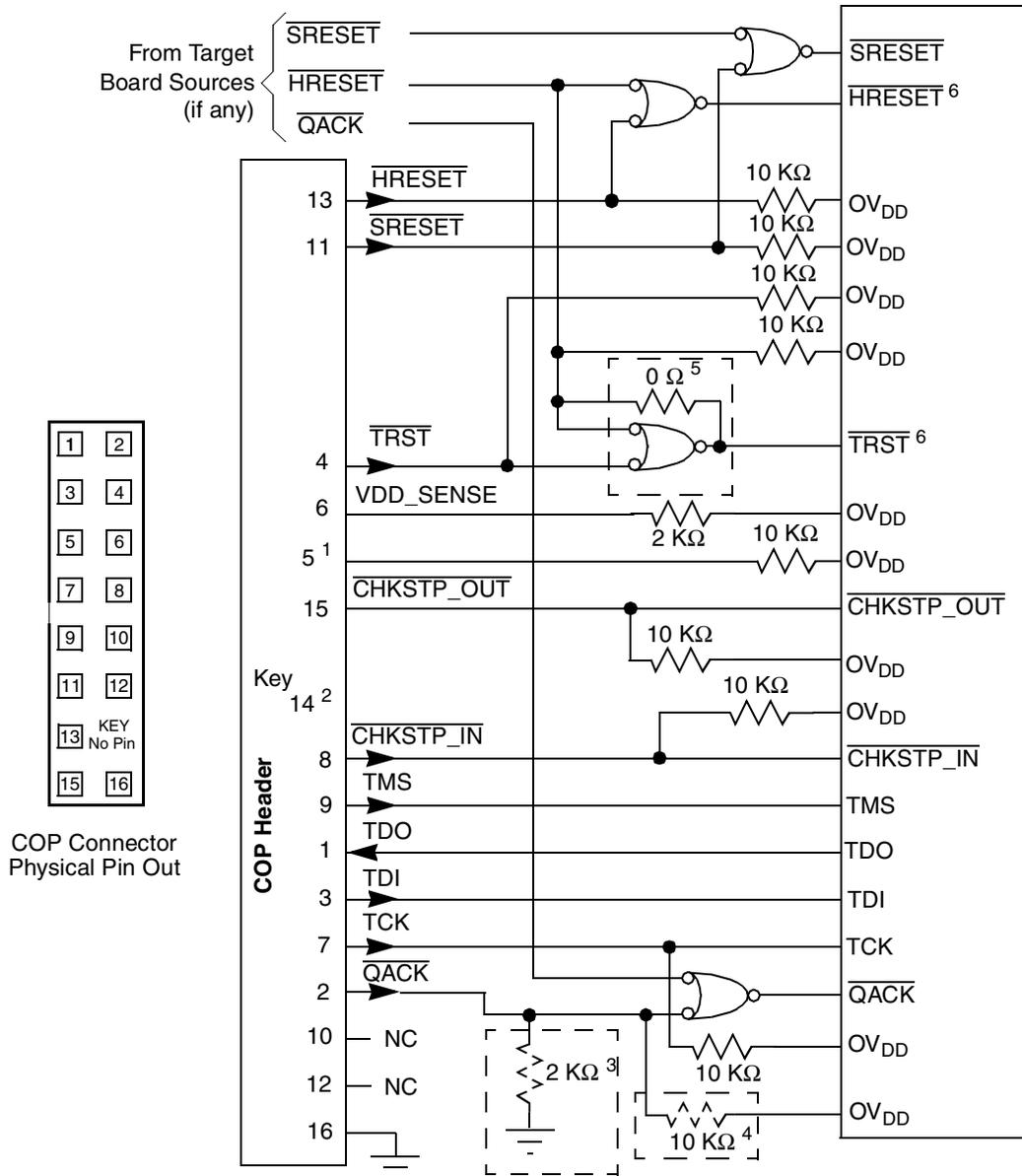
The arrangement shown in [Figure 21](#) allows the COP port to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$, while ensuring that the target can drive $\overline{\text{HRESET}}$ as well. If the JTAG interface and COP header will not be used, $\overline{\text{TRST}}$ should be tied to $\overline{\text{HRESET}}$ through a 0- Ω isolation resistor so that it is asserted when the system reset signal ($\overline{\text{HRESET}}$) is asserted, ensuring that the JTAG scan chain is initialized during power-on. Although Freescale recommends that the COP header be designed into the system as shown in [Figure 21](#), if this is not possible, the isolation resistor will allow future access to $\overline{\text{TRST}}$ in the case where a JTAG interface may need to be wired onto the system in debug situations.

The COP header shown in [Figure 21](#) adds many benefits—breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features are possible through this interface—and can be as inexpensive as an unpopulated footprint for a header to be added when needed.

The COP interface has a standard header for connection to the target system, based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header). The connector typically has pin 14 removed as a connector key.

There is no standardized way to number the COP header shown in [Figure 21](#); consequently, many different pin numbers have been observed from emulator vendors. Some are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom, while still others number the pins counter clockwise from pin 1 (as with an IC). Regardless of the numbering, the signal placement recommended in [Figure 21](#) is common to all known emulators.

The $\overline{\text{QACK}}$ signal shown in [Figure 21](#) is usually connected to the bridge chip or other system control logic in a system and is an input to the MPC7448 informing it that it can go into the quiescent state. Under normal operation this occurs during a low-power mode selection. In order for COP to work, the MPC7448 must see this signal asserted (pulled down). While shown on the COP header, not all emulator products drive this signal. If the product does not, a pull-down resistor can be populated to assert this signal. Additionally, some emulator products implement open-drain type outputs and can only drive $\overline{\text{QACK}}$ asserted; for these tools, a pull-up resistor can be implemented to ensure this signal is negated when it is not being driven by the tool. Note that the pull-up and pull-down resistors on the $\overline{\text{QACK}}$ signal are mutually exclusive and it is never necessary to populate both in a system. To preserve correct power-down operation, $\overline{\text{QACK}}$ should be merged through logic so that it also can be driven by the bridge or system logic.


Notes:

1. RUN/STOP, normally found on pin 5 of the COP header, is not implemented on the MPC7448. Connect pin 5 of the COP header to OV_{DD} with a 10-K Ω pull-up resistor.
2. Key location; pin 14 is not physically present on the COP header.
3. Component not populated. Populate only if debug tool does not drive \overline{QACK} .
4. Populate only if debug tool uses an open-drain type output and does not actively negate \overline{QACK} .
5. If the JTAG interface is implemented, connect \overline{HRESET} from the target source to \overline{TRST} from the COP header through an AND gate to \overline{TRST} of the part. If the JTAG interface is not implemented, connect \overline{HRESET} from the target source to \overline{TRST} of the part through a 0- Ω isolation resistor.
6. The COP port and target board should be able to independently assert \overline{HRESET} and \overline{TRST} to the processor in order to fully control the processor as shown above.

Figure 21. JTAG Interface Connection

9.7 Power and Thermal Management Information

This section provides thermal management information for the high coefficient of thermal expansion (HCTE) package for air-cooled applications. Proper thermal control design is primarily dependent on the system-level design—the heat sink, airflow, and thermal interface material. The MPC7448 implements several features designed to assist with thermal management, including DFS and the temperature diode. DFS reduces the power consumption of the device by reducing the core frequency; see [Section 9.7.5.1, “Power Consumption with DFS Enabled,”](#) for specific information regarding power reduction and DFS. The temperature diode allows an external device to monitor the die temperature in order to detect excessive temperature conditions and alert the system; see [Section 9.7.4, “Temperature Diode,”](#) for more information.

To reduce the die-junction temperature, heat sinks may be attached to the package by several methods—spring clip to holes in the printed-circuit board or package, and mounting clip and screw assembly (see [Figure 22](#)); however, due to the potential large mass of the heat sink, attachment through the printed-circuit board is suggested. In any implementation of a heat sink solution, the force on the die should not exceed ten pounds (45 Newtons).

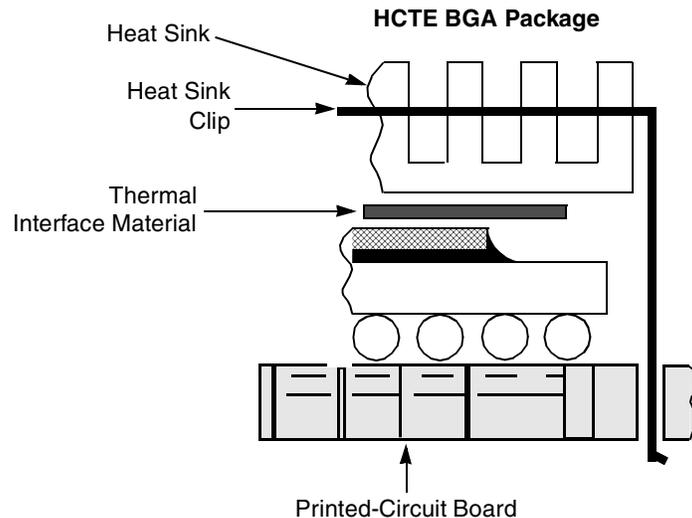


Figure 22. BGA Package Exploded Cross-Sectional View with Several Heat Sink Options

NOTE

A clip on heat sink is not recommended for LGA because there may not be adequate clearance between the device and the circuit board. A through-hole solution is recommended, as shown in [Figure 23](#).

9.7.1 Internal Package Conduction Resistance

For the exposed-die packaging technology described in Table 5, the intrinsic conduction thermal resistance paths are as follows:

- The die junction-to-case thermal resistance (the case is actually the top of the exposed silicon die)
- The die junction-to-board thermal resistance

Figure 24 depicts the primary heat transfer path for a package with an attached heat sink mounted to a printed-circuit board.

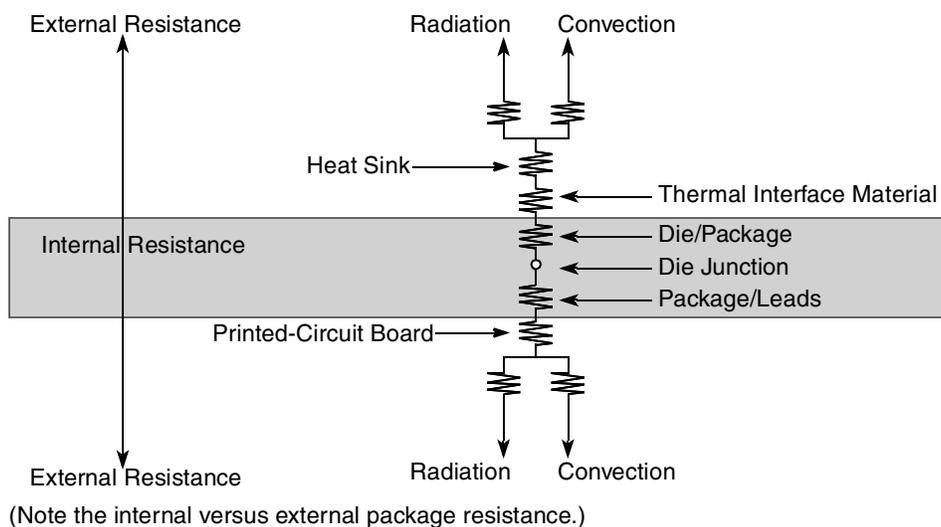


Figure 24. C4 Package with Heat Sink Mounted to a Printed-Circuit Board

Heat generated on the active side of the chip is conducted through the silicon, through the heat sink attach material (or thermal interface material), and, finally, to the heat sink, where it is removed by forced-air convection.

Because the silicon thermal resistance is quite small, the temperature drop in the silicon may be neglected for a first-order analysis. Thus, the thermal interface material and the heat sink conduction/convective thermal resistances are the dominant terms.

9.7.2 Thermal Interface Materials

A thermal interface material is recommended at the package lid-to-heat sink interface to minimize the thermal contact resistance. For those applications where the heat sink is attached by spring clip mechanism, Figure 25 shows the thermal performance of three thin-sheet thermal-interface materials (silicone, graphite/oil, fluoroether oil), a bare joint, and a joint with thermal grease as a function of contact pressure. As shown, the performance of these thermal interface materials improves with increasing contact pressure. The use of thermal grease significantly reduces the interface thermal resistance. That is, the bare joint results in a thermal resistance approximately seven times greater than the thermal grease joint.

Often, heat sinks are attached to the package by means of a spring clip to holes in the printed-circuit board (see Figure 22). Therefore, synthetic grease offers the best thermal performance due to the low interface pressure and is recommended due to the high power dissipation of the MPC7448. Of course, the selection

Due to the complexity and variety of system-level boundary conditions for today's microelectronic equipment, the combined effects of the heat transfer mechanisms (radiation, convection, and conduction) may vary widely. For these reasons, we recommend using conjugate heat transfer models for the board as well as system-level designs.

For system thermal modeling, the MPC7448 thermal model is shown in Figure 26. Four volumes represent this device. Two of the volumes, solder ball-air and substrate, are modeled using the package outline size of the package. The other two, die and bump-underfill, have the same size as the die. The silicon die should be modeled $8.0 \times 7.3 \times 0.86 \text{ mm}^3$ with the heat source applied as a uniform source at the bottom of the volume. The bump and underfill layer is modeled as $8.0 \times 7.3 \times 0.07 \text{ mm}^3$ collapsed in the z-direction with a thermal conductivity of $5.0 \text{ W}/(\text{m} \cdot \text{K})$ in the z-direction. The substrate volume is $25 \times 25 \times 1.14 \text{ mm}^3$ and has $9.9 \text{ W}/(\text{m} \cdot \text{K})$ isotropic conductivity in the xy-plane and $2.95 \text{ W}/(\text{m} \cdot \text{K})$ in the direction of the z-axis. The solder ball and air layer are modeled with the same horizontal dimensions as the substrate and is 0.8 mm thick. For the LGA package the solder and air layer is 0.1 mm thick, but the material properties are the same. It can also be modeled as a collapsed volume using orthotropic material properties: $0.034 \text{ W}/(\text{m} \cdot \text{K})$ in the xy-plane direction and $11.2 \text{ W}/(\text{m} \cdot \text{K})$ in the direction of the z-axis.

Conductivity	Value	Unit
Die ($8.0 \times 7.3 \times 0.86 \text{ mm}^3$)		
Silicon	Temperature-dependent	$\text{W}/(\text{m} \cdot \text{K})$
Bump and Underfill ($8.0 \times 7.3 \times 0.07 \text{ mm}^3$)		
k_z	5.0	$\text{W}/(\text{m} \cdot \text{K})$
Substrate ($25 \times 25 \times 1.14 \text{ mm}^3$)		
k_x	9.9	$\text{W}/(\text{m} \cdot \text{K})$
k_y	9.9	
k_z	2.95	
Solder Ball and Air ($25 \times 25 \times 0.8 \text{ mm}^3$)		
k_x	0.034	$\text{W}/(\text{m} \cdot \text{K})$
k_y	0.034	
k_z	11.2	

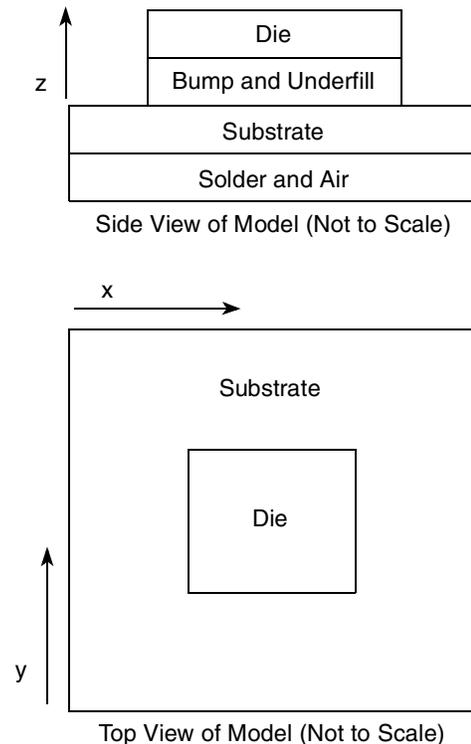


Figure 26. Recommended Thermal Model of MPC7448

Table 16. Valid Divide Ratio Configurations

DFS mode disabled		DFS divide-by-2 mode enabled (HID1[DFS2] = 1 or DFS2 = 0)		DFS divide-by-4 mode enabled (HID1[DFS4] = 1 or DFS4 = 0)	
Bus-to-Core Multiplier Configured by PLL_CFG[0:5] (see Table 12)	HID1[PC0-5] ³	Bus-to-Core Multiplier	HID1[PC0-5] ³	Bus-to-Core Multiplier	HID1[PC0-5] ³
2x ⁴	010000	N/A (unchanged) ¹	unchanged ¹	N/A (unchanged) ¹	unchanged ¹
3x ⁴	100000	N/A (unchanged) ¹	unchanged ¹	N/A (unchanged) ¹	unchanged ¹
4x ⁴	101000	2x ⁴	010000	N/A (unchanged) ¹	unchanged ¹
5x	101100	2.5x ⁴	010101	N/A (unchanged) ¹	unchanged ¹
5.5x	100100	2.75x ⁴	110101 ²	N/A (unchanged) ¹	unchanged ¹
6x	110100	3x ⁴	100000	N/A (unchanged) ¹	unchanged ¹
6.5x	010100	3.25x ⁴	100000 ²	N/A (unchanged) ¹	unchanged ¹
7x	001000	3.5x ⁴	110101	N/A (unchanged) ¹	unchanged ¹
7.5x	000100	3.75x ⁴	110101 ²	N/A (unchanged) ¹	unchanged ¹
8x	110000	4x ⁴	101000 ⁴	2x ⁴	010000
8.5x	011000	4.25x ⁴	101000 ²	N/A (unchanged) ¹	unchanged ¹
9x	011110	4.5x ⁴	011101	2.25x ⁴	010000 ²
9.5x	011100	4.75x ⁴	011101 ²	N/A (unchanged) ¹	unchanged ¹
10x	101010	5x	101100	2.5x ⁴	010101
10.5x	100010	5.25x	101100 ²	N/A (unchanged) ¹	unchanged ¹
11x	100110	5.5x	100100	2.75x ⁴	010101 ²
11.5x	000000	5.75x	100100 ²	N/A (unchanged) ¹	unchanged ¹
12x	101110	6x	110100	3x ⁴	100000
12.5x	111110	6.25x	110100 ²	N/A (unchanged) ¹	unchanged ¹
13x	010110	6.5x	010100	3.25x ⁴	100000 ²
13.5x	111000	6.75	010100 ²	N/A (unchanged) ¹	unchanged ¹
14x	110010	7x	001000	3.5x ⁴	110101
15x	000110	7.5x	000100	3.75x ⁴	110101 ²
16x	110110	8x	110000	4x ⁴	101000
17x	000010	8.5x	011000	4.25x ⁴	101000 ²
18x	001010	9x	011110	4.5x ⁴	011101
20x	001110	10x	101010	5x	101100
21x	010010	10.5x	100010	5.25x	101100 ²

Table 16. Valid Divide Ratio Configurations (continued)

DFS mode disabled		DFS divide-by-2 mode enabled (HID1[DFS2] = 1 or $\overline{\text{DFS2}} = 0$)		DFS divide-by-4 mode enabled (HID1[DFS4] = 1 or $\overline{\text{DFS4}} = 0$)	
Bus-to-Core Multiplier Configured by PLL_CFG[0:5] (see Table 12)	HID1[PC0-5] ³	Bus-to-Core Multiplier	HID1[PC0-5] ³	Bus-to-Core Multiplier	HID1[PC0-5] ³
24x	011010	12x	101110	6x	110100
28x	111010	14x	110010	7x	001000

Notes:

- DFS mode is not supported for this combination of DFS mode and PLL_CFG[0:5] setting. As a result, the processor will ignore these settings and remain at the previous multiplier, as reflected by the HID1[PC0-PC5] bits.
- Though supported by the MPC7448 clock circuitry, multipliers of $n.25x$ and $n.75x$ cannot be expressed as valid PLL configuration codes. As a result, the values displayed in HID1[PC0-PC5] are rounded down to the nearest valid PLL configuration code. However, the actual bus-to-core multiplier is as stated in this table.
- Note that in the HID1 register of the MPC7448, the PC0, PC1, PC2, PC3, PC4, and PC5 bits are bits 15, 16, 17, 18, 19, and 14 (respectively). See the *MPC7450 RISC Microprocessor Reference Manual* for more information.
- Special considerations regarding snooped transactions must be observed for bus-to-core multipliers less than 5x. See the *MPC7450 RISC Microprocessor Reference Manual* for more information.

9.7.5.3 Minimum Core Frequency Requirements with DFS

In many systems, enabling DFS can result in very low processor core frequencies. However, care must be taken to ensure that the resulting processor core frequency is within the limits specified in Table 8. Proper operation of the device is not guaranteed at core frequencies below the specified minimum f_{core} .

10 Document Revision History

Table 17 provides a revision history for this hardware specification.

Table 17. Document Revision History

Revision	Date	Substantive Change(s)
4	3/2007	Table 19: Added 800 MHz processor frequency.
3	10/2006	Section 9.7, "Power and Thermal Management Information": Updated contact information. Table 18, Table 20, and Table 19: Added Revision D PVR. Table 19: Added 600 processor frequency, additional product codes, date codes for 1400 processor frequency, and footnotes 1 and 2. Table 20: Added PPC product code and footnote 1. Table 19 and Table 20: Added Revision D information for 1267 processor frequency.