

Welcome to E-XFL.COM

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC G4
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.7GHz
Co-Processors/DSP	Multimedia; SIMD
RAM Controllers	-
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	1.5V, 1.8V, 2.5V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	360-CLGA, FCCLGA
Supplier Device Package	360-FCCLGA (25x25)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmc7448vs1700ld

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong





- Reliability and serviceability
 - Parity checking on system bus
 - Parity checking on the L1 caches and L2 data tags
 - ECC or parity checking on L2 data

3 Comparison with the MPC7447A, MPC7447, MPC7445, and MPC7441

Table 1 compares the key features of the MPC7448 with the key features of the earlier MPC7447A, MPC7447, MPC7445, and MPC7441. All are based on the MPC7450 RISC microprocessor and are architecturally very similar. The MPC7448 is identical to the MPC7447A, but the MPC7448 supports 1 Mbyte of L2 cache with ECC and the use of dynamic frequency switching (DFS) with more bus-to-core ratios.

Microarchitectural Specs	MPC7448	MPC7447A	MPC7447	MPC7445	MPC7441		
Basic Pipeline	Functions						
Logic inversions per cycle			18				
Pipeline stages up to execute			5				
Total pipeline stages (minimum)			7				
Pipeline maximum instruction throughput		:	3 + branch				
Pipeline Re	esources						
Instruction buffer size			12				
Completion buffer size			16				
Renames (integer, float, vector)	16, 16, 16						
Maximum Execution Throughput							
SFX	3						
Vector	2 (any 2 of 4 units)						
Scalar floating-point			1				
Out-of-Order Window Siz	e in Execut	ion Queues					
SFX integer units		1 en	try $ imes$ 3 queu	ies			
Vector units		In o	rder, 4 queu	es			
Scalar floating-point unit			In order				
Branch Processi	ng Resourc	es					
Prediction structures		BTIC,	BHT, link s	tack			
BTIC size, associativity	128-entry, 4-way						
BHT size	2K-entry						
Link stack depth			8				
Unresolved branches supported	3						
Branch taken penalty (BTIC hit)			1				
Minimum misprediction penalty			6				

Table 1. Microarchitecture Comparison



4 General Parameters

The following list summarizes the general parameters of the MPC7448:

Technology	90 nm CMOS S	90 nm CMOS SOI, nine-layer metal		
Die size	8.0 mm × 7.3 m	m		
Transistor count	90 million			
Logic design	Mixed static and	d dynamic		
Packages	Surface mount 3	Surface mount 360 ceramic ball grid array (HCTE)		
	Surface mount 360 ceramic land grid array (HCTE)			
	Surface mount 3	360 ceramic ball grid array with lead-free spheres (HCTE)		
Core power supply	1.30 V	(1700 MHz device)		
	1.25 V	(1600 MHz device)		
	1.20 V	(1420 MHz device)		
	1.15 V	(1000 MHz device)		
I/O power supply	1.5 V, 1.8 V, or	2.5 V		

5 Electrical and Thermal Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC7448.

5.1 DC Electrical Characteristics

The tables in this section describe the MPC7448 DC electrical characteristics. Table 2 provides the absolute maximum ratings. See Section 9.2, "Power Supply Design and Sequencing," for power sequencing requirements.

Charao	Characteristic		Maximum Value	Unit	Notes
Core supply voltage		V _{DD}	-0.3 to 1.4	V	2
PLL supply voltage		AV _{DD}	-0.3 to 1.4	V	2
Processor bus supply voltage	I/O Voltage Mode = 1.5 V	OV _{DD}	-0.3 to 1.8	V	3
	I/O Voltage Mode = 1.8 V		-0.3 to 2.2		3
	I/O Voltage Mode = 2.5 V		-0.3 to 3.0		3
Input voltage	Processor bus	V _{in}	-0.3 to OV _{DD} + 0.3	V	4
	JTAG signals	V _{in}	–0.3 to OV _{DD} + 0.3	V	
Storage temperature range		T _{stg}	– 55 to 150	•C	

Table 2. Absolute Maximum Ratings ¹

Notes:

1. Functional and tested operating conditions are given in Table 4. Absolute maximum ratings are stress ratings only and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.

- 2. See Section 9.2, "Power Supply Design and Sequencing" for power sequencing requirements.
- 3. Bus must be configured in the corresponding I/O voltage mode; see Table 3.
- 4. Caution: V_{in} must not exceed OV_{DD} by more than 0.3 V at any time including during power-on reset except as allowed by the overshoot specifications. V_{in} may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 2.



Electrical and Thermal Characteristics

Figure 2 shows the undershoot and overshoot voltage on the MPC7448.



Figure 2. Overshoot/Undershoot Voltage

The MPC7448 provides several I/O voltages to support both compatibility with existing systems and migration to future systems. The MPC7448 core voltage must always be provided at the nominal voltage (see Table 4). The input voltage threshold for each bus is selected by sampling the state of the voltage select pins at the negation of the signal HRESET. The output voltage will swing from GND to the maximum voltage applied to the OV_{DD} power pins. Table 3 provides the input threshold voltage settings. Because these settings may change in future products, it is recommended that BVSEL[0:1] be configured using resistor options, jumpers, or some other flexible means, with the capability to reconfigure the termination of this signal in the future, if necessary.

BVSEL0	BVSEL1	I/O Voltage Mode ¹	Notes
0	0	1.8 V	2, 3
0	1	2.5 V	2, 4
1	0	1.5 V	2
1	1	2.5 V	4

Table 3. Input Threshold Voltage Setting

Notes:

- 1. **Caution:** The I/O voltage mode selected must agree with the OV_{DD} voltages supplied. See Table 4.
- 2. If used, pull-down resistors should be less than 250 $\Omega.$
- 3. The pin configuration used to select 1.8V mode on the MPC7448 is not compatible with the pin configuration used to select 1.8V mode on the MPC7447A and earlier devices.
- 4. The pin configuration used to select 2.5V mode on the MPC7448 is fully compatible with the pin configuration used to select 2.5V mode on the MPC7447A and earlier devices.



Electrical and Thermal Characteristics

Table 5 provides the package thermal characteristics for the MPC7448. For more information regarding thermal management, see Section 9.7, "Power and Thermal Management Information."

Characteristic		Value	Unit	Notes
Junction-to-ambient thermal resistance, natural convection, single-layer (1s) board	$R_{ extsf{ heta}JA}$	26	•C/W	2, 3
Junction-to-ambient thermal resistance, natural convection, four-layer (2s2p) board	R_{\thetaJMA}	19	•C/W	2, 4
Junction-to-ambient thermal resistance, 200 ft/min airflow, single-layer (1s) board	R_{\thetaJMA}	22	•C/W	2, 4
Junction-to-ambient thermal resistance, 200 ft/min airflow, four-layer (2s2p) board	R_{\thetaJMA}	16	•C/W	2, 4
Junction-to-board thermal resistance	$R_{ extsf{ heta}JB}$	11	•C/W	5
Junction-to-case thermal resistance	$R_{ extsf{ heta}JC}$	< 0.1	•C/W	6

Table 5. Package Thermal Characteristics¹

Notes:

- 1. Refer to Section 9.7, "Power and Thermal Management Information," for details about thermal management.
- Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, airflow, power dissipation of other components on the board, and board thermal resistance.
- 3. Per JEDEC JESD51-2 with the single-layer board horizontal
- 4. Per JEDEC JESD51-6 with the board horizontal
- 5. Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
- 6. This is the thermal resistance between die and case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the calculated case temperature. The actual value of R_{θJC} for the part is less than 0.1°C/W.

Table 6 provides the DC electrical characteristics for the MPC7448.

Table 6. DC Electrical Specifications

At recommended operating conditions. See Table 4.

Characteristic	Nominal Bus Voltage ¹	Symbol	Min	Max	Unit	Notes
Input high voltage	1.5	V _{IH}	$OV_{DD} imes 0.65$	OV _{DD} + 0.3	V	2
(all inputs)	1.8		$OV_{DD} imes 0.65$	OV _{DD} + 0.3		
	2.5		1.7	OV _{DD} + 0.3		
Input low voltage	1.5	V _{IL}	-0.3	$\mathrm{OV}_\mathrm{DD} imes 0.35$	V	2
(all inputs)	1.8		-0.3	$\mathrm{OV}_\mathrm{DD} imes 0.35$		
	2.5		-0.3	0.7		
Input leakage current, all signals except BVSEL0, LSSD_MODE, TCK, TDI, TMS, TRST:	_	l _{in}	_	50	μA	2, 3
V _{in} = OV _{DD} V _{in} = GND				50 - 50		
Input leakage current, BVSEL0, LSSD_MODE, TCK, TDI, TMS, TRST:	—	l _{in}	—		μA	2, 6
$V_{in} = OV_{DD}$ $V_{in} = GND$				50 - 2000		



Figure 3 provides the SYSCLK input timing diagram.



 V_{M} = Midpoint Voltage (OV_{DD}/2)

Figure 3. SYSCLK Input Timing Diagram

5.2.2 **Processor Bus AC Specifications**

Table 9 provides the processor bus AC timing specifications for the MPC7448 as defined in Figure 4 and Figure 5.

Table 9. Processor Bus AC Timing Specifications¹

At recommended operating conditions. See Table 4.

Parameter	Symbol ²	All Speed Grades		Unit	Notos
Falameter	Symbol	Min	Мах	Unit	Notes
Input setup times: A[0:35], AP[0:4] D[0:63], DP[0:7] AACK, ARTRY, BG, CKSTP_IN, DBG, DTI[0:3], GBL, TT[0:4], QACK, TA, TBEN, TEA, TS, EXT_QUAL, PMON_IN, SHD[0:1]	^t avkh t _D vkh ^t ivkh	1.5 1.5 1.5	—	ns	
BMODE[0:1], BVSEL[0:1]	t _{MVKH}	1.5	—		8
Input hold times: A[0:35], AP[0:4] D[0:63], DP[0:7] AACK, ARTRY, BG, CKSTP_IN, DBG, DTI[0:3], GBL, TT[0:4], QACK, TA, TBEN, TEA, TS, EXT_QUAL, PMON_IN,	t _{АХКН} t _{DXKH} tixkh	0 0 0	 	ns	
BMODE[0:1], BVSEL[0:1]	t _{MXKH}	0	—		8
Output valid times: A[0:35], AP[0:4] D[0:63], DP[0:7] BR, CI, DRDY, GBL, HIT, PMON_OUT, QREQ, TBST, SIZ[0:2], TT[0:4], WT	^t khav ^t khdv ^t khov		1.8 1.8 1.8	ns	
TS ARTRY, SHD[0:1]	t _{KHTSV} t _{KHARV}	_	1.8 1.8		
Output hold times: A[0:35], AP[0:4] D[0:63], DP[0:7] BR, CI, DRDY, GBL, HIT, PMON_OUT, QREQ, TBST, TSIZ[0:2], TT[0:4], WT TS	^t кнах ^t кндх ^t кнох ^t кнтsx	0.5 0.5 0.5	 	ns	
	^t KHARX	0.5	—		F
STOCK to output enable	^I KHOE	0.5	—	ns	5



Electrical and Thermal Characteristics

Table 9. Processor Bus AC Timing Specifications¹ (continued)

At recommended operating conditions. See Table 4.

Parameter	Symbol ²	All Speed Grades		Unit	Notes
Falanetei	Symbol	Min	Мах	onic	Notes
SYSCLK to output high impedance (all except \overline{TS} , \overline{ARTRY} , SHD0, $\overline{SHD1}$)	^t кноz	_	1.8	ns	5
SYSCLK to \overline{TS} high impedance after precharge	t _{KHTSPZ}	_	1	t _{SYSCLK}	3, 4, 5
Maximum delay to ARTRY/SHD0/SHD1 precharge	t _{KHARP}		1	t _{SYSCLK}	3, 5, 6, 7
SYSCLK to ARTRY/SHD0/SHD1 high impedance after precharge	t _{KHARPZ}	_	2	t _{SYSCLK}	3, 5, 6, 7

Notes:

- All input specifications are measured from the midpoint of the signal in question to the midpoint of the rising edge of the input SYSCLK. All output specifications are measured from the midpoint of the rising edge of SYSCLK to the midpoint of the signal in question. All output timings assume a purely resistive 50-Ω load (see Figure 4). Input and output timings are measured at the pin; time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
- 2. The symbology used for timing specifications herein follows the pattern of t_{(signal)(state)(reference)(state)} for inputs and t_{(reference)(state)(signal)(state)} for outputs. For example, t_{IVKH} symbolizes the time input signals (I) reach the valid state (V) relative to the SYSCLK reference (K) going to the high (H) state or input setup time. And t_{KHOV} symbolizes the time from SYSCLK(K) going high (H) until outputs (O) are valid (V) or output valid time. Input hold time can be read as the time that the input signal (I) went invalid (X) with respect to the rising clock edge (KH) (note the position of the reference and its state for inputs) and output hold time can be read as the time from the rising edge (KH) until the output went invalid (OX).
- 3. t_{sysclk} is the period of the external clock (SYSCLK) in ns. The numbers given in the table must be multiplied by the period of SYSCLK to compute the actual time duration (in ns) of the parameter in question.
- 4. According to the bus protocol, TS is driven only by the currently active bus master. It is asserted low and precharged high before returning to high impedance, as shown in Figure 6. The nominal precharge width for TS is t_{SYSCLK}, that is, one clock period. Since no master can assert TS on the following clock edge, there is no concern regarding contention with the precharge. Output valid and output hold timing is tested for the signal asserted. Output valid time is tested for precharge. The high-impedance behavior is guaranteed by design.
- 5. Guaranteed by design and not tested
- 6. According to the bus protocol, ARTRY can be driven by multiple bus masters through the clock period immediately following AACK. Bus contention is not an issue because any master asserting ARTRY will be driving it low. Any master asserting it low in the first clock following AACK will then go to high impedance for a fraction of a cycle, then negated for up to an entire cycle (crossing a bus cycle boundary) before being three-stated again. The nominal precharge width for ARTRY is 1.0 t_{SYSCLK}; that is, it should be high impedance as shown in Figure 6 before the first opportunity for another master to assert ARTRY. Output valid and output hold timing is tested for the signal asserted. The high-impedance behavior is guaranteed by design.
- 7. According to the MPX bus protocol, SHD0 and SHD1 can be driven by multiple bus masters beginning two cycles after TS. Timing is the same as ARTRY, that is, the signal is high impedance for a fraction of a cycle, then negated for up to an entire cycle (crossing a bus cycle boundary) before being three-stated again. The nominal precharge width for SHD0 and SHD1 is 1.0 t_{SYSCLK}. The edges of the precharge vary depending on the programmed ratio of core to bus (PLL configurations).
- BMODE[0:1] and BVSEL[0:1] are mode select inputs. BMODE[0:1] are sampled before and after HRESET negation. BVSEL[0:1] are sampled before HRESET negation. These parameters represent the input setup and hold times for each sample. These values are guaranteed by design and not tested. BMODE[0:1] must remain stable after the second sample; BVSEL[0:1] must remain stable after the first (and only) sample. See Figure 5 for sample timing.



5.2.3 IEEE Std. 1149.1 AC Timing Specifications

Table 10 provides the IEEE Std. 1149.1 (JTAG) AC timing specifications as defined in Figure 8 through Figure 11.

Table 10. JTAG AC Timing Specifications (Independent of SYSCLK)¹

At recommended operating conditions. See Table 4.

Parameter	Symbol	Min	Мах	Unit	Notes
TCK frequency of operation	f _{TCLK}	0	33.3	MHz	
TCK cycle time	t _{TCLK}	30	—	ns	
TCK clock pulse width measured at 1.4 V	t _{JHJL}	15	—	ns	
TCK rise and fall times	$t_{\rm JR}$ and $t_{\rm JF}$	—	2	ns	
TRST assert time	t _{TRST}	25	—	ns	2
Input setup times: Boundary-scan data TMS, TDI	t _{DVJH} t _{IVJH}	4 0	_	ns	3
Input hold times: Boundary-scan data TMS, TDI	^t DXJH t _{IXJH}	20 25		ns	3
Valid times: Boundary-scan data TDO	t _{JLDV} t _{JLOV}	4 4	20 25	ns	4
Output hold times: Boundary-scan data TDO	t _{JLDX} t _{JLOX}	30 30	—	ns	4
TCK to output high impedance: Boundary-scan data TDO	t _{JLDZ} t _{JLOZ}	3 3	19 9	ns	4, 5

Notes:

 All outputs are measured from the midpoint voltage of the falling/rising edge of TCLK to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load (see Figure 7). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.

2. TRST is an asynchronous level sensitive signal. The time is for test purposes only.

3. Non-JTAG signal input timing with respect to TCK.

4. Non-JTAG signal output timing with respect to TCK.

5. Guaranteed by design and characterization.



Electrical and Thermal Characteristics

Figure 7 provides the AC test load for TDO and the boundary-scan outputs of the MPC7448.



Figure 7. Alternate AC Test Load for the JTAG Interface

Figure 8 provides the JTAG clock input timing diagram.



Figure 8. JTAG Clock Input Timing Diagram

Figure 9 provides the $\overline{\text{TRST}}$ timing diagram.



Figure 9. TRST Timing Diagram

Figure 10 provides the boundary-scan timing diagram.



Figure 10. Boundary-Scan Timing Diagram



7 Pinout Listings

Table 11 provides the pinout listing for the MPC7448, 360 HCTE package. The pinouts of the MPC7448 and MPC7447A are compatible, but the requirements regarding the use of the additional power and ground pins have changed. The MPC7448 requires these pins be connected to the appropriate power or ground plane to achieve high core frequencies; see Section 9.3, "Connection Recommendations," for additional information. As a result, these pins should be connected in all new designs.

Additionally, the MPC7448 may be populated on a board designed for a MPC7447 (or MPC7445 or MPC7441), provided the core voltage can be made to match the requirements in Table 4 and all pins defined as 'no connect' for the MPC7447 are unterminated, as required by the *MPC7457 RISC Microprocessor Hardware Specifications*. The MPC7448 uses pins previously marked 'no connect' for the temperature diode pins and for additional power and ground connections. The additional power and ground pins are required to achieve high core frequencies and core frequency will be limited if they are not connected; see Section 9.3, "Connection Recommendations," for additional information. Because these 'no connect' pins in the MPC7447 360 pin package are not driven in functional mode, an MPC7447 can be populated in an MPC7448 board.

NOTE

Caution must be exercised when performing boundary scan test operations on a board designed for an MPC7448, but populated with an MPC7447 or earlier device. This is because in the MPC7447 it is possible to drive the latches associated with the former 'no connect' pins in the MPC7447, potentially causing contention on those pins. To prevent this, ensure that these pins are not connected on the board or, if they are connected, ensure that the states of internal MPC7447 latches do not cause these pins to be driven during board testing.

For the MPC7448, pins that were defined as the TEST[0:4] factory test signal group on the MPC7447A and earlier devices have been assigned new functions. For most of these, the termination recommendations for the TEST[0:4] pins of the MPC7447A are compatible with the MPC7448 and will allow correct operation with no performance loss. The exception is BVSEL1 (TEST3 on the MPC7447A and earlier devices), which may require a different termination depending which I/O voltage mode is desired; see Table 3 for more information.

NOTE

This pinout is not compatible with the MPC750, MPC7400, or MPC7410 360 BGA package.



Pinout Listings

Signal Name	Pin Number	Active	I/O	Notes
A[0:35]	E11, H1, C11, G3, F10, L2, D11, D1, C10, G2, D12, L3, G4, T2, F4, V1, J4, R2, K5, W2, J2, K4, N4, J3, M5, P5, N3, T1, V2, U1, N5, W1, B12, C4, G10, B11	High	I/O	2
AACK	R1	Low	Input	
AP[0:4]	C1, E3, H6, F5, G7	High	I/O	2
ARTRY	N2	Low	I/O	3
AV _{DD}	A8	_	Input	
BG	M1	Low	Input	
BMODE0	G9	Low	Input	4
BMODE1	F8	Low	Input	5
BR	D2	Low	Output	
BVSEL0	B7	High	Input	1, 6
BVSEL1	E10	High	Input	1, 20
CI	J1	Low	Output	
CKSTP_IN	A3	Low	Input	
CKSTP_OUT	B1	Low	Output	
CLK_OUT	H2	High	Output	
D[0:63]	R15, W15, T14, V16, W16, T15, U15, P14, V13, W13, T13, P13, U14, W14, R12, T12, W12, V12, N11, N10, R11, U11, W11, T11, R10, N9, P10, U10, R9, W10, U9, V9, W5, U6, T5, U5, W7, R6, P7, V6, P17, R19, V18, R18, V19, T19, U19, W19, U18, W17, W18, T16, T18, T17, W3, V17, U4, U8, U7, R7, P6, R8, W8, T8	High	I/O	
DBG	M2	Low	Input	
DFS2	A12	Low	Input	20, 21
DFS4	B6	Low	Input	12, 20, 21
DP[0:7]	T3, W4, T4, W9, M6, V3, N8, W6	High	I/O	
DRDY	R3	Low	Output	7
DTI[0:3]	G1, K1, P1, N1	High	Input	8
EXT_QUAL	A11	High	Input	9
GBL	E2	Low	I/O	
GND	B5, C3, D6, D13, E17, F3, G17, H4, H7, H9, H11, H13, J6, J8, J10, J12, K7, K3, K9, K11, K13, L6, L8, L10, L12, M4, M7, M9, M11, M13, N7, P3, P9, P12, R5, R14, R17, T7, T10, U3, U13, U17, V5, V8, V11, V15		_	
GND	A17, A19, B13, B16, B18, E12, E19, F13, F16, F18, G19, H18, J14, L14, M15, M17, M19, N14, N16, P15, P19	_	—	15
GND_SENSE	G12, N13	—	—	19
ПТ	B2	Low	Output	7
HRESET	D8	Low	Input	
INT	D4	Low	Input	
L1_TSTCLK	G8	High	Input	9
L2_TSTCLK	B3	High	Input	10

Table 11. Pinout	Listing for the	e MPC7448, 36	0 HCTE Package



Signal Name	Pin Number	Active	I/O	Notes
LVRAM	B10	_	_	12, 20, 22
NC (no connect)	A6, A14, A15, B14, B15, C14, C15, C16, C17, C18, C19, D14, D15, D16, D17, D18, D19, E14, E15, F14, F15, G14, G15, H15, H16, J15, J16, J17, J18, J19, K15, K16, K17, K18, K19, L15, L16, L17, L18, L19	_	_	11
LSSD_MODE	E8	Low	Input	6, 12
MCP	C9	Low	Input	
OV _{DD}	B4, C2, C12, D5, F2, H3, J5, K2, L5, M3, N6, P2, P8, P11, R4, R13, R16, T6, T9, U2, U12, U16, V4, V7, V10, V14	—	—	
OVDD_SENSE	E18, G18		—	16
PLL_CFG[0:4]	B8, C8, C7, D7, A7	High	Input	
PLL_CFG[5]	D10	High	Input	9, 20
PMON_IN	D9	Low	Input	13
PMON_OUT	A9	Low	Output	
QACK	G5	Low	Input	
QREQ	P4	Low	Output	
SHD[0:1]	E4, H5	Low	I/O	3
SMI	F9	Low	Input	
SRESET	A2	Low	Input	
SYSCLK	A10		Input	
TA	К6	Low	Input	
TBEN	E1	High	Input	
TBST	F11	Low	Output	
ТСК	C6	High	Input	
TDI	B9	High	Input	6
TDO	A4	High	Output	
TEA	L1	Low	Input	
TEMP_ANODE	N18	—	—	17
TEMP_CATHODE	N19		—	17
TMS	F1	High	Input	6
TRST	A5	Low	Input	6, 14
TS	L4	Low	I/O	3
TSIZ[0:2]	G6, F7, E7	High	Output	
TT[0:4]	E5, E6, F6, E9, C5	High	I/O	
WT	D3	Low	Output	
V _{DD}	H8, H10, H12, J7, J9, J11, J13, K8, K10, K12, K14, L7, L9, L11, L13, M8, M10, M12		_	
V _{DD}	A13, A16, A18, B17, B19, C13, E13, E16, F12, F17, F19, G11, G16, H14, H17, H19, M14, M16, M18, N15, N17, P16, P18	_	_	15

Table 11. Pinout Listing for the MPC7448	8, 360 HCTE Package (continued)
--	---------------------------------



Table 11. Pinout Listing for the MPC7448, 360 HCTE Package (continued)

Signal Name	Pin Number	Active	I/O	Notes
VDD_SENSE	G13, N12			18

Notes:

1. OV_{DD} supplies power to the processor bus, JTAG, and all control signals, and is configurable. (V_{DD} supplies power to the processor core, and AV_{DD} supplies power to the PLL after filtering from V_{DD}). To program the I/O voltage, see Table 3. If used, the pull-down resistor should be less than 250 Ω . Because these settings may change in future products, it is recommended BVSEL[0:1] be configured using resistor options, jumpers, or some other flexible means, with the capability to reconfigure the termination of this signal in the future if necessary. For actual recommended value of V_{in} or supply voltages see Table 4.

- 2. Unused address pins must be pulled down to GND and corresponding address parity pins pulled up to OV_{DD}.
- 3. These pins require weak pull-up resistors (for example, 4.7 KΩ) to maintain the control signals in the negated state after they have been actively negated and released by the MPC7448 and other bus masters.

4. This signal selects between MPX bus mode (asserted) and 60x bus mode (negated) and will be sampled at HRESET going high.

5. This signal must be negated during reset, by pull-up resistor to OV_{DD} or negation by ¬HRESET (inverse of HRESET), to ensure proper operation.

- 6. Internal pull up on die.
- 7. Not used in 60x bus mode.

8. These signals must be pulled down to GND if unused, or if the MPC7448 is in 60x bus mode.

9. These input signals are for factory use only and must be pulled down to GND for normal machine operation.

- 10. This test signal is recommended to be tied to HRESET; however, other configurations will not adversely affect performance.
- 11. These signals are for factory use only and must be left unconnected for normal machine operation. Some pins that were NCs on the MPC7447, MPC7445, and MPC7441 have now been defined for other purposes.
- 12. These input signals are for factory use only and must be pulled up to OV_{DD} for normal machine operation.
- 13. This pin can externally cause a performance monitor event. Counting of the event is enabled through software.
- 14. This signal must be asserted during reset, by pull down to GND or assertion by HRESET, to ensure proper operation.
- 15. These pins were NCs on the MPC7447, MPC7445, and MPC7441. See Section 9.3, "Connection Recommendations," for more information.
- 16. These pins were OV_{DD} pins on the MPC7447, MPC7445, and MPC7441. These pins are internally connected to OV_{DD} and are intended to allow an external device (such as a power supply) to detect the I/O voltage level present inside the device package. If unused, it is recommended they be connected to test points to facilitate system debug; otherwise, they may be connected directly to OV_{DD} or left unconnected.
- 17. These pins provide connectivity to the on-chip temperature diode that can be used to determine the die junction temperature of the processor. These pins may be left unterminated if unused.
- 18. These pins are internally connected to V_{DD} and are intended to allow an external device (such as a power supply) to detect the processor core voltage level present inside the device package. If unused, it is recommended they be connected to test points to facilitate system debug; otherwise, they may be connected directly to V_{DD} or left unconnected.
- 19. These pins are internally connected to GND and are intended to allow an external device to detect the processor ground voltage level present inside the device package. If unused, it is recommended they be connected to test points to facilitate system debug; otherwise, they may be connected directly to GND or left unconnected.
- 20. These pins were in the TEST[0:4] factory test pin group on the MPC7447A, MPC7447, MPC7445, and MPC7441. They have been assigned new functions on the MPC7448.
- 21. These pins can be used to enable the supported dynamic frequency switching (DFS) modes via hardware. If both are pulled down, DFS mode is disabled completely and cannot be enabled via software. If unused, they should be pulled up to OV_{DD} to allow software control of DFS. See the *MPC7450 RISC Microprocessor Family Reference Manual* for more information.
- 22. This pin is provided to allow operation of the L2 cache at low core voltages and is for factory use only. See the MPC7450 RISC Microprocessor Family Reference Manual for more information.



Package Description

8.2 Mechanical Dimensions for the MPC7448, 360 HCTE BGA

Figure 13 provides the mechanical dimensions and bottom surface nomenclature for the MPC7448, 360 HCTE BGA package.



Figure 13. Mechanical Dimensions and Bottom Surface Nomenclature for the MPC7448, 360 HCTE BGA Package



8.5 Package Parameters for the MPC7448, 360 HCTE RoHS-Compliant BGA

The package parameters are as provided in the following list. The package type is 25×25 mm, 360-lead high coefficient of thermal expansion ceramic ball grid array (HCTE) with RoHS-compliant lead-free spheres.

Package outline	$25 \times 25 \text{ mm}$			
Interconnects	360 (19 × 19 ball array – 1)			
Pitch	1.27 mm (50 mil)			
Minimum module height	1.92 mm			
Maximum module height	2.40 mm			
Ball diameter	0.75 mm (30 mil)			
Coefficient of thermal expansion12.3 ppm/°C				



System Design Information



Notes:

- 1. RUN/STOP, normally found on pin 5 of the COP header, is not implemented on the MPC7448. Connect pin 5 of the COP header to OV_{DD} with a 10-K Ω pull-up resistor.
- 2. Key location; pin 14 is not physically present on the COP header.
- 3. Component not populated. Populate only if debug tool does not drive QACK.
- 4. Populate only if debug tool uses an open-drain type output and does not actively negate QACK.
- 5. If the JTAG interface is implemented, connect $\overline{\text{HRESET}}$ from the target source to $\overline{\text{TRST}}$ from the COP header though an AND gate to $\overline{\text{TRST}}$ of the part. If the JTAG interface is not implemented, connect $\overline{\text{HRESET}}$ from the target source to $\overline{\text{TRST}}$ of the part through a 0- Ω isolation resistor.
- 6. The COP port and target board should be able to independently assert HRESET and TRST to the processor in order to fully control the processor as shown above.

Figure 21. JTAG Interface Connection



System Design Information

9.7 Power and Thermal Management Information

This section provides thermal management information for the high coefficient of thermal expansion (HCTE) package for air-cooled applications. Proper thermal control design is primarily dependent on the system-level design—the heat sink, airflow, and thermal interface material. The MPC7448 implements several features designed to assist with thermal management, including DFS and the temperature diode. DFS reduces the power consumption of the device by reducing the core frequency; see Section 9.7.5.1, "Power Consumption with DFS Enabled," for specific information regarding power reduction and DFS. The temperature diode allows an external device to monitor the die temperature in order to detect excessive temperature conditions and alert the system; see Section 9.7.4, "Temperature Diode," for more information.

To reduce the die-junction temperature, heat sinks may be attached to the package by several methods—spring clip to holes in the printed-circuit board or package, and mounting clip and screw assembly (see Figure 22); however, due to the potential large mass of the heat sink, attachment through the printed-circuit board is suggested. In any implementation of a heat sink solution, the force on the die should not exceed ten pounds (45 Newtons).



Figure 22. BGA Package Exploded Cross-Sectional View with Several Heat Sink Options

NOTE

A clip on heat sink is not recommended for LGA because there may not be adequate clearance between the device and the circuit board. A through-hole solution is recommended, as shown in Figure 23.



Due to the complexity and variety of system-level boundary conditions for today's microelectronic equipment, the combined effects of the heat transfer mechanisms (radiation, convection, and conduction) may vary widely. For these reasons, we recommend using conjugate heat transfer models for the board as well as system-level designs.

For system thermal modeling, the MPC7448 thermal model is shown in Figure 26. Four volumes represent this device. Two of the volumes, solder ball-air and substrate, are modeled using the package outline size of the package. The other two, die and bump-underfill, have the same size as the die. The silicon die should be modeled $8.0 \times 7.3 \times 0.86$ mm³ with the heat source applied as a uniform source at the bottom of the volume. The bump and underfill layer is modeled as $8.0 \times 7.3 \times 0.07$ mm³ collapsed in the z-direction with a thermal conductivity of 5.0 W/(m • K) in the z-direction. The substrate volume is $25 \times 25 \times 1.14$ mm³ and has 9.9 W/(m • K) isotropic conductivity in the xy-plane and 2.95 W/(m • K) in the direction of the z-axis. The solder ball and air layer are modeled with the same horizontal dimensions as the substrate and is 0.8 mm thick. For the LGA package the solder and air layer is 0.1 mm thick, but the material properties are the same. It can also be modeled as a collapsed volume using orthotropic material properties: 0.034 W/(m • K) in the xy-plane direction and 11.2 W/(m • K) in the direction of the z-axis.

Conductivity	Value	Unit				
Die $(8.0 \times 7.3 \times 0.86 \text{ mm}^3)$			•	Die		
- (-	,	[z		Bump and Underfill	
Silicon	Temperature- dependent	W/(m ∙ K)		Substrate		
$\frac{1}{10000000000000000000000000000000000$		-	Solder and Air			
			-	Side	View of Model (Not to Scale)	
kz	5.0	W/(m ∙ K)				
Substrate (25 \times 25 \times 1.14 mm ³)			<u>×</u>			
k _x	9.9	W/(m • K)			Orthostwate	
k _y	9.9				Substrate	
k _z	2.95					
Solder Ball and Air (25 $ imes$ 25 $ imes$ 0.8 mm ³)					Die	
k _x	0.034	W/(m ∙ K)	1			
k _y	0.034					
k _z	11.2		у			
	1	1				

Top View of Model (Not to Scale)

Figure 26. Recommended Thermal Model of MPC7448



Document Revision History

Revision	Date	Substantive Change(s)				
2		Table 6: Added separate input leakage specification for BVSEL0, <u>LSSD_MODE</u> , <u>TCK</u> , TDI, TMS, <u>TRST</u> signals to correctly indicate leakage current for signals with internal pull-up resistors.				
		Section 5.1: Added paragraph preceding Table 7 and edited notes in Table 7 to clarify core frequencies at which power consumption is measured.				
		Section 5.3: Removed voltage derating specifications; this feature has been made redundant by new device offerings and is no longer supported.				
		Changed names of "Typical–Nominal" and "Typical–Thermal" power consumption parameters to "Typical" and "Thermal", respectively. (Name change only–no specifications were changed.)				
		Table 11: Revised Notes 16, 18, and 19 to reflect current recommendations for connection of SENSE pins.				
		Section 9.3: Added paragraph explaining connection recommendations for SENSE pins. (See also Table 11 entry above.)				
		Table 19: Updated table to reflect changes in specifications for MC7448xxnnnnNC devices. Table 9: Changed all instances of TT[0:3] to TT[0:4]				
		Removed mention of these input signals from output valid times and output hold times:				
		• AACK, CKSTP_IN, DT[0:3]				
		Figure 1/: Modified diagram slightly to correctly show constraint on SYSCLK ramping is related to V_{DE} voltage, not AV _{DE} voltage. (Diagram clarification only: no change in power sequencing requirements.)				
		Added Table 20 to reflect introduction of extended temperature devices and associated hardware				
		specification addendum.				
1		Added 1600 MHz, 1420 MHz, and 1000 MHz devices				
		Section 4: corrected die size				
		Table 2: Revised Note 4 to consider overshoot/undershoot and combined with Note 5.				
		Table 4. Revised operating voltage for 1700 MHz device from \pm 50 mV to \pm 20 mV $/$ =50 mV.				
		Table 11: Added voltage derating information for 1700 MHz devices: this feature is not supported at this				
		time for other speed grades.				
		Added transient specifications for VDD power supply in Section 9.2.3, added Table 15 and Figure 19 and renumbered subsequent tables and figures.				
		Moved Decoupling Recommendations from Section 9.4 to Section 9.2.4 and renumbered subsequent sections.				
		Section 9.2.1: Revised power sequencing requirements.				
		Section 9.7.4: Added thermal diode ideality factor information (previously TBD).				
		Table 17: Expanded table to show HID1 register values when DFS modes are enabled.				
		Section 11.2: updated to include additional N-spec device speed grades				
		Tables 18 and 19: corrected PVR values and added "MC" product code prefix				
0		Initial public release.				

Table 17. Document Revision History (continued)



11 Part Numbering and Marking

Ordering information for the part numbers fully covered by this specification document is provided in Section 11.1, "Part Numbers Fully Addressed by This Document." Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact a local Freescale sales office. In addition to the processor frequency, the part numbering scheme also includes an application modifier that may specify special application conditions. An optional specification modifier may also apply for parts to indicate a specific change in specifications, such as support for an extended temperature range. Finally, each part number contains a revision level code that refers to the die mask revision number. Section 11.2, "Part Numbers Not Fully Addressed by This Document," lists the part numbers that do not fully conform to the specifications of this document. These special part numbers require an additional document called a hardware specification addendum.

11.1 Part Numbers Fully Addressed by This Document

Table 18 provides the Freescale part numbering nomenclature for the MPC7448 part numbers fully addressed by this document. For information regarding other MPC7448 part numbers, see Section 11.2, "Part Numbers Not Fully Addressed by This Document."

XX	7448	XX	nnnn L		X
Product Code	Part Identifier	Package	Processor Frequency	Application Modifier	Revision Level
MC PPC ¹	7448	HX = HCTE BGA VS = RoHS LGA	1700	L: 1.3 V +20/–50 mV 0 to 105 °C	C: 2.1; PVR = 0x8004_0201 D: 2.2; PVR = 0x8004_0202
		VU = ROHS BGA	1600	L: 1.25 V ± 50 mV 0 to 105 °C	
			1420	L: 1.2 V ± 50 mV 0 to 105 °C	
			1000	L: 1.15 V ± 50 mV 0 to 105 °C	

Table 18. Part Numbering Nomenclature

Notes:

1. The P prefix in a Freescale part number designates a "Pilot Production Prototype" as defined by Freescale SOP 3-13. These parts have only preliminary reliability and characterization data. Before pilot production prototypes may be shipped, written authorization from the customer must be on file in the applicable sales office acknowledging the qualification status and the fact that product changes may still occur as pilot production prototypes are shipped.

How to Reach Us:

Home Page: www.freescale.com

email: support@freescale.com

USA/Europe or Locations Not Listed:

Freescale Semiconductor Technical Information Center, CH370 1300 N. Alma School Road Chandler, Arizona 85224 1-800-521-6274 480-768-2130 support@freescale.com

Europe, Middle East, and Africa:

Freescale Halbleiter Deutschland GmbH Technical Information Center Schatzbogen 7 81829 Muenchen, Germany +44 1296 380 456 (English) +46 8 52200080 (English) +49 89 92103 559 (German) +33 1 69 35 48 48 (French) support@freescale.com

Japan:

Freescale Semiconductor Japan Ltd. Headquarters ARCO Tower 15F 1-8-1, Shimo-Meguro, Meguro-ku Tokyo 153-0064, Japan 0120 191014 +81 3 5437 9125 support.japan@freescale.com

Asia/Pacific:

Freescale Semiconductor Hong Kong Ltd. Technical Information Center 2 Dai King Street Tai Po Industrial Estate, Tai Po, N.T., Hong Kong +800 2666 8080 support.asia@freescale.com

For Literature Requests Only:

Freescale Semiconductor Literature Distribution Center P.O. Box 5405 Denver, Colorado 80217 1-800-441-2447 303-675-2140 Fax: 303-675-2150 LDCForFreescaleSemiconductor @hibbertgroup.com

Document Number: MPC7448EC Rev. 4 3/2007 Information in this document is provided solely to enable system and software implementers to use Freescale Semiconductor products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits or integrated circuits based on the information in this document.

Freescale Semiconductor reserves the right to make changes without further notice to any products herein. Freescale Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters which may be provided in Freescale Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. Freescale Semiconductor does not convey any license under its patent rights nor the rights of others. Freescale Semiconductor products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Freescale Semiconductor product could create a situation where personal injury or death may occur. Should Buyer purchase or use Freescale Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold Freescale Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Freescale Semiconductor was negligent regarding the design or manufacture of the part.

Freescale[™] and the Freescale logo are trademarks of Freescale Semiconductor, Inc. The Power Architecture and Power.org word marks and the Power and Power.org logos and related marks are trademarks and service marks licensed by Power.org. The described product is a PowerPC microprocessor. The PowerPC name is a trademark of IBM Corp. and is used under license. IEEE Stds. 1149.1[™] and 754[™] are trademarks of the Institute of Electrical and Electronics Engineers, Inc., (IEEE). This product is not endosed or approved by the IEEE. All other product or service names are the property of their respective owners.

© Freescale Semiconductor, Inc., 2005, 2007.



