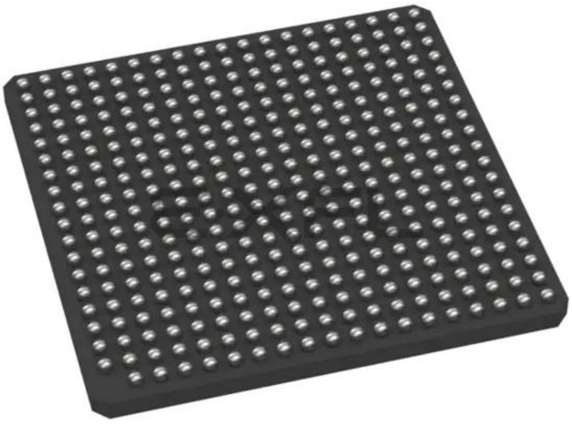

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC G4
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.4GHz
Co-Processors/DSP	Multimedia; SIMD
RAM Controllers	-
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	1.5V, 1.8V, 2.5V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	360-CBGA, FCCBGA
Supplier Device Package	360-FCCBGA (25x25)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmc7448vu1400nc

Email: info@E-XFL.COM Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

2 Features

This section summarizes features of the MPC7448 implementation.

Major features of the MPC7448 are as follows:

- High-performance, superscalar microprocessor
  - Up to four instructions can be fetched from the instruction cache at a time.
  - Up to three instructions plus a branch instruction can be dispatched to the issue queues at a time.
  - Up to 12 instructions can be in the instruction queue (IQ).
  - Up to 16 instructions can be at some stage of execution simultaneously.
  - Single-cycle execution for most instructions
  - One instruction per clock cycle throughput for most instructions
  - Seven-stage pipeline control
- Eleven independent execution units and three register files
  - Branch processing unit (BPU) features static and dynamic branch prediction
    - 128-entry (32-set, four-way set-associative) branch target instruction cache (BTIC), a cache of branch instructions that have been encountered in branch/loop code sequences. If a target instruction is in the BTIC, it is fetched into the instruction queue a cycle sooner than it can be made available from the instruction cache. Typically, a fetch that hits the BTIC provides the first four instructions in the target stream.
    - 2048-entry branch history table (BHT) with 2 bits per entry for four levels of prediction—not taken, strongly not taken, taken, and strongly taken
    - Up to three outstanding speculative branches
    - Branch instructions that do not update the count register (CTR) or link register (LR) are often removed from the instruction stream.
    - Eight-entry link register stack to predict the target address of Branch Conditional to Link Register (**bclr**) instructions
  - Four integer units (IUs) that share 32 GPRs for integer operands
    - Three identical IUs (IU1a, IU1b, and IU1c) can execute all integer instructions except multiply, divide, and move to/from special-purpose register instructions.
    - IU2 executes miscellaneous instructions, including the CR logical operations, integer multiplication and division instructions, and move to/from special-purpose register instructions.
  - Five-stage FPU and 32-entry FPR file
    - Fully IEEE Std. 754™-1985–compliant FPU for both single- and double-precision operations
    - Supports non-IEEE mode for time-critical operations
    - Hardware support for denormalized numbers
    - Thirty-two 64-bit FPRs for single- or double-precision operands

- Monitors all dispatched instructions and retires them in order
- Tracks unresolved branches and flushes instructions after a mispredicted branch
- Retires as many as three instructions per clock cycle

- Separate on-chip L1 instruction and data caches (Harvard architecture)
  - 32-Kbyte, eight-way set-associative instruction and data caches
  - Pseudo least-recently-used (PLRU) replacement algorithm
  - 32-byte (eight-word) L1 cache block
  - Physically indexed/physical tags
  - Cache write-back or write-through operation programmable on a per-page or per-block basis
  - Instruction cache can provide four instructions per clock cycle; data cache can provide four words per clock cycle
  - Caches can be disabled in software.
  - Caches can be locked in software.
  - MESI data cache coherency maintained in hardware
  - Separate copy of data cache tags for efficient snooping
  - Parity support on cache
  - No snooping of instruction cache except for **icbi** instruction
  - Data cache supports AltiVec LRU and transient instructions
  - Critical double- and/or quad-word forwarding is performed as needed. Critical quad-word forwarding is used for AltiVec loads and instruction fetches. Other accesses use critical double-word forwarding.
- Level 2 (L2) cache interface
  - On-chip, 1-Mbyte, eight-way set-associative unified instruction and data cache
  - Cache write-back or write-through operation programmable on a per-page or per-block basis
  - Parity support on cache tags
  - ECC or parity support on data
  - Error injection allows testing of error recovery software
- Separate memory management units (MMUs) for instructions and data
  - 52-bit virtual address, 32- or 36-bit physical address
  - Address translation for 4-Kbyte pages, variable-sized blocks, and 256-Mbyte segments
  - Memory programmable as write-back/write-through, caching-inhibited/caching-allowed, and memory coherency enforced/memory coherency not enforced on a page or block basis
  - Separate IBATs and DBATs (eight each) also defined as SPRs
  - Separate instruction and data translation lookaside buffers (TLBs)
    - Both TLBs are 128-entry, two-way set-associative and use an LRU replacement algorithm.
    - TLBs are hardware- or software-reloadable (that is, a page table search is performed in hardware or by system software on a TLB miss).

- Efficient data flow
  - — Although the VR/LSU interface is 128 bits, the L1/L2 bus interface allows up to 256 bits.
  - — The L1 data cache is fully pipelined to provide 128 bits/cycle to or from the VRs.
  - — The L2 cache is fully pipelined to provide 32 bytes per clock every other cycle to the L1 caches.
  - — As many as 16 out-of-order transactions can be present on the MPX bus.
  - — Store merging for multiple store misses to the same line. Only coherency action taken (address-only) for store misses merged to all 32 bytes of a cache block (no data tenure needed).
  - — Three-entry finished store queue and five-entry completed store queue between the LSU and the L1 data cache
  - — Separate additional queues for efficient buffering of outbound data (such as castouts and write-through stores) from the L1 data cache and L2 cache
- Multiprocessing support features include the following:
  - — Hardware-enforced, MESI cache coherency protocols for data cache
  - — Load/store with reservation instruction pair for atomic memory references, semaphores, and other multiprocessor operations
- Power and thermal management
  - — Dynamic frequency switching (DFS) feature allows processor core frequency to be halved or quartered through software to reduce power consumption.
  - — The following three power-saving modes are available to the system:
    - – Nap—Instruction fetching is halted. Only the clocks for the time base, decrementer, and JTAG logic remain running. The part goes into the doze state to snoop memory operations on the bus and then back to nap using a $\overline{\text{QREQ}}$/$\overline{\text{QACK}}$ processor-system handshake protocol.
    - – Sleep—Power consumption is further reduced by disabling bus snooping, leaving only the PLL in a locked and running state. All internal functional units are disabled.
    - – Deep sleep—When the part is in the sleep state, the system can disable the PLL. The system can then disable the SYSCLK source for greater system power savings. Power-on reset procedures for restarting and relocking the PLL must be followed upon exiting the deep sleep state.
  - — Instruction cache throttling provides control of instruction fetching to limit device temperature.
  - — A new temperature diode that can determine the temperature of the microprocessor
- Performance monitor can be used to help debug system designs and improve software efficiency.
- In-system testability and debugging features through JTAG boundary-scan capability
- Testability
  - — LSSD scan design
  - — IEEE Std. 1149.1™ JTAG interface

Table 1. Microarchitecture Comparison (continued)

Microarchitectural Specs	MPC7448	MPC7447A	MPC7447	MPC7445	MPC7441
Execution Unit Timings (Latency-Throughput)					
Aligned load (integer, float, vector)	3-1, 4-1, 3-1				
Misaligned load (integer, float, vector)	4-2, 5-2, 4-2				
L1 miss, L2 hit latency with ECC (data/instruction)	12/16	—			
L1 miss, L2 hit latency without ECC (data/instruction)	11/15	9/13			
SFX (add, sub, shift, rot, cmp, logicals)	1-1				
Integer multiply (32×8, 32×16, 32×32)	4-1, 4-1, 5-2				
Scalar float	5-1				
VSFX (vector simple)	1-1				
VCFX (vector complex)	4-1				
VFPU (vector float)	4-1				
VPER (vector permute)	2-1				
MMUs					
TLBs (instruction and data)	128-entry, 2-way				
Tablewalk mechanism	Hardware + software				
Instruction BATs/data BATs	8/8	8/8	8/8	8/8	4/4
L1 I Cache/D Cache Features					
Size	32K/32K				
Associativity	8-way				
Locking granularity	Way				
Parity on I cache	Word				
Parity on D cache	Byte				
Number of D cache misses (load/store)	5/2	5/1			
Data stream touch engines	4 streams				
On-Chip Cache Features					
Cache level	L2				
Size/associativity	1-Mbyte/ 8-way	512-Kbyte/8-way		256-Kbyte/8-way	
Access width	256 bits				
Number of 32-byte sectors/line	2	2			
Parity tag	Byte	Byte			
Parity data	Byte	Byte			
Data ECC	64-bit	—			
Thermal Control					
Dynamic frequency switching divide-by-two mode	Yes	Yes	No	No	No
Dynamic frequency switching divide-by-four mode	Yes	No	No	No	No
Thermal diode	Yes	Yes	No	No	No

Figure 2 shows the undershoot and overshoot voltage on the MPC7448.

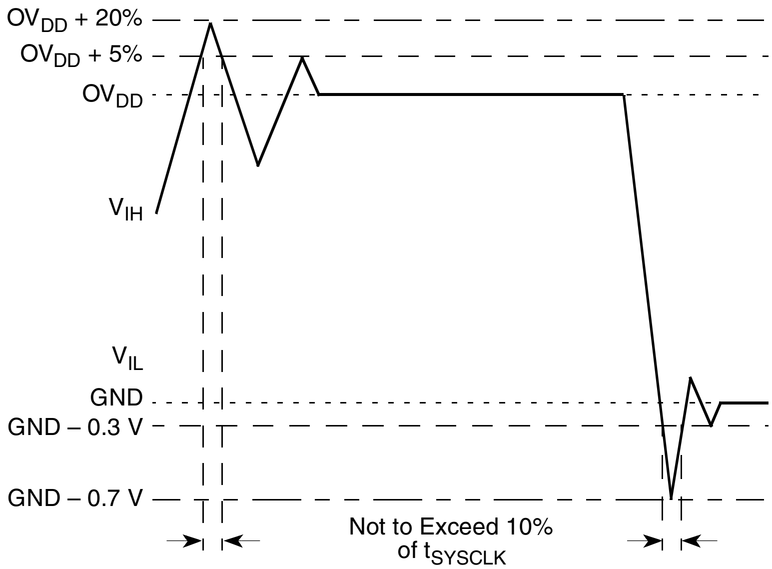


Figure 2. Overshoot/Undershoot Voltage

The MPC7448 provides several I/O voltages to support both compatibility with existing systems and migration to future systems. The MPC7448 core voltage must always be provided at the nominal voltage (see Table 4). The input voltage threshold for each bus is selected by sampling the state of the voltage select pins at the negation of the signal $\overline{\text{HRESET}}$. The output voltage will swing from GND to the maximum voltage applied to the OV_{DD} power pins. Table 3 provides the input threshold voltage settings. Because these settings may change in future products, it is recommended that BVSEL[0:1] be configured using resistor options, jumpers, or some other flexible means, with the capability to reconfigure the termination of this signal in the future, if necessary.

Table 3. Input Threshold Voltage Setting

BVSEL0	BVSEL1	I/O Voltage Mode [1]	Notes
0	0	1.8 V	2, 3
0	1	2.5 V	2, 4
1	0	1.5 V	2
1	1	2.5 V	4

Notes:

1. **Caution:** The I/O voltage mode selected must agree with the OV_{DD} voltages supplied. See Table 4.
2. If used, pull-down resistors should be less than 250 Ω.
3. The pin configuration used to select 1.8V mode on the MPC7448 is not compatible with the pin configuration used to select 1.8V mode on the MPC7447A and earlier devices.
4. The pin configuration used to select 2.5V mode on the MPC7448 is fully compatible with the pin configuration used to select 2.5V mode on the MPC7447A and earlier devices.

when running a typical benchmark at temperatures in a typical system. The Full-Power Mode–Thermal value is intended to represent the sustained power consumption of the device when running a typical code sequence at high temperature and is recommended to be used as the basis for designing a thermal solution; see Section 9.7, "Power and Thermal Management Information" for more information on thermal solutions. The Full-Power Mode–Maximum value is recommended to be used for power supply design because this represents the maximum peak power draw of the device that a power supply must be capable of sourcing without voltage droop. For information on power consumption when dynamic frequency switching is enabled, see Section 9.7.5, "Dynamic Frequency Switching (DFS)."

Table 7. Power Consumption for MPC7448 at Maximum Rated Frequency

	Die Junction Temperature (T_j)	Maximum Processor Core Frequency (Speed Grade, MHz)				Unit	Notes
		1000 MHz	1420 MHz	1600 MHz	1700 MHz		
Full-Power Mode							
Typical	65 •C	15.0	19.0	20.0	21.0	W	1, 2
Thermal	105 •C	18.6	23.3	24.4	25.6	W	1, 5
Maximum	105 •C	21.6	27.1	28.4	29.8	W	1, 3
Nap Mode							
Typical	105 •C	11.1	11.8	13.0	13.0	W	1, 6
Sleep Mode							
Typical	105 •C	10.8	11.4	12.5	12.5	W	1, 6
Deep Sleep Mode (PLL Disabled)							
Typical	105 •C	10.4	11.0	12.0	12.0	W	1, 6

Notes:

1. These values specify the power consumption for the core power supply (V_{DD}) at nominal voltage and apply to all valid processor bus frequencies and configurations. The values do not include I/O supply power (OV_{DD}) or PLL supply power (AV_{DD}). OV_{DD} power is system dependent but is typically < 5% of V_{DD} power. Worst case power consumption for AV_{DD} < 13 mW. Freescale also offers MPC7448 part numbers that meet lower power consumption specifications; for more information on these devices, see Section 11.2, "Part Numbers Not Fully Addressed by This Document."
2. Typical power consumption is an average value measured with the processor operating at its rated maximum processor core frequency (except for Deep Sleep Mode), at nominal recommended V_{DD} (see Table 4) and 65°C while running the Dhrystone 2.1 benchmark and achieving 2.3 Dhrystone MIPs/MHz. This parameter is not 100% tested but periodically sampled.b
3. Maximum power consumption is the average measured with the processor operating at its rated maximum processor core frequency, at nominal V_{DD} and maximum operating junction temperature (see Table 4) while running an entirely cache-resident, contrived sequence of instructions to keep all the execution units maximally busy.
4. Doze mode is not a user-definable state; it is an intermediate state between full-power and either nap or sleep mode. As a result, power consumption for this mode is not tested.
5. Thermal power consumption is an average value measured at the nominal recommended V_{DD} (see Table 4) and 105 °C while running the Dhrystone 2.1 benchmark and achieving 2.3 Dhrystone MIPs/MHz. This parameter is not 100% tested but periodically sampled.
6. Typical power consumption for these modes is measured at the nominal recommended V_{DD} (see Table 4) and 105 °C in the mode described. This parameter is not 100% tested but is periodically sampled.

Figure 6 provides the input/output timing diagram for the MPC7448.

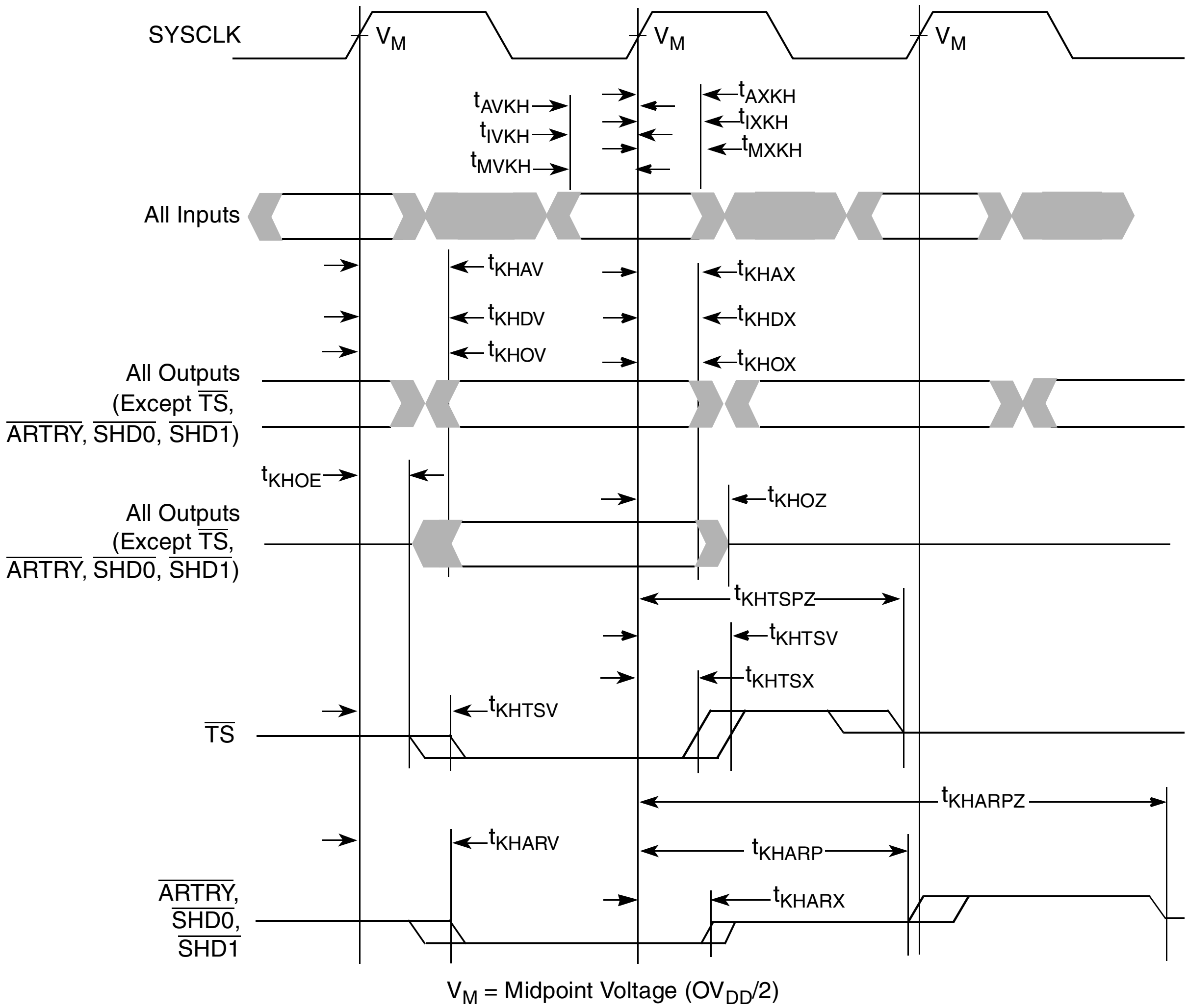


Figure 6. Input/Output Timing Diagram

Figure 7 provides the AC test load for TDO and the boundary-scan outputs of the MPC7448.

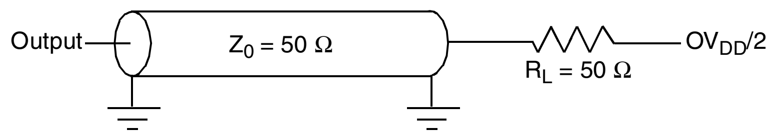


Figure 7. Alternate AC Test Load for the JTAG Interface

Figure 8 provides the JTAG clock input timing diagram.

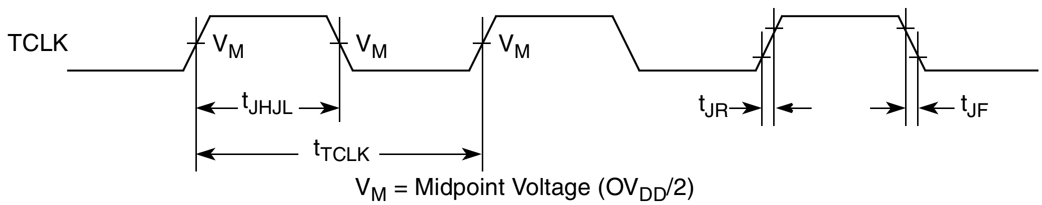


Figure 8. JTAG Clock Input Timing Diagram

Figure 9 provides the $\overline{\text{TRST}}$ timing diagram.

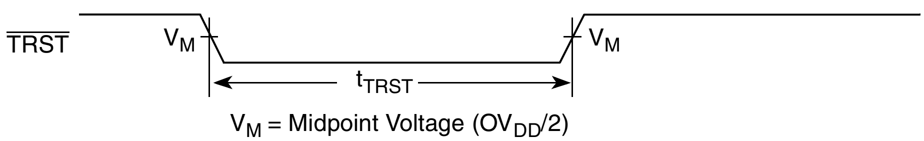


Figure 9. $\overline{\text{TRST}}$ Timing Diagram

Figure 10 provides the boundary-scan timing diagram.

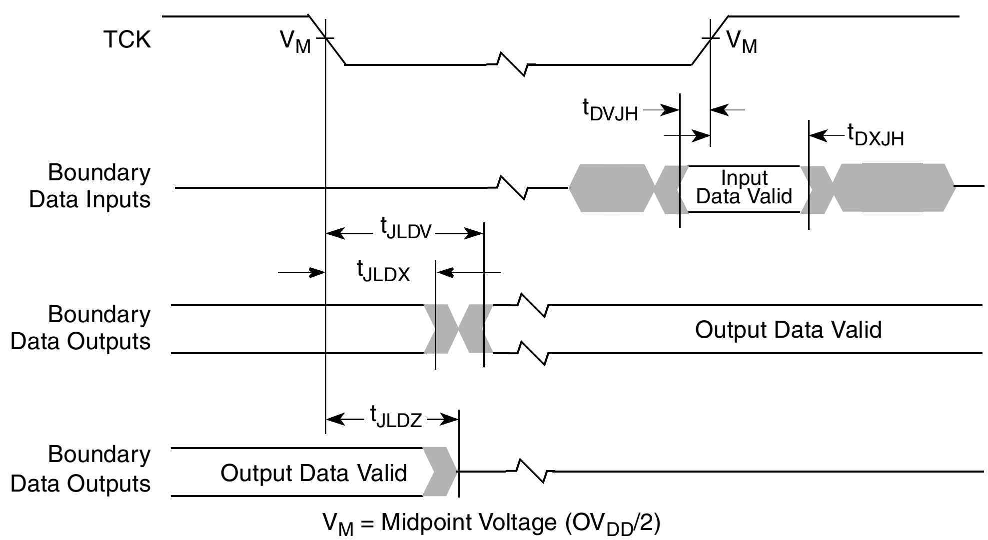


Figure 10. Boundary-Scan Timing Diagram

8 Package Description

The following sections provide the package parameters and mechanical dimensions for the HCTE package.

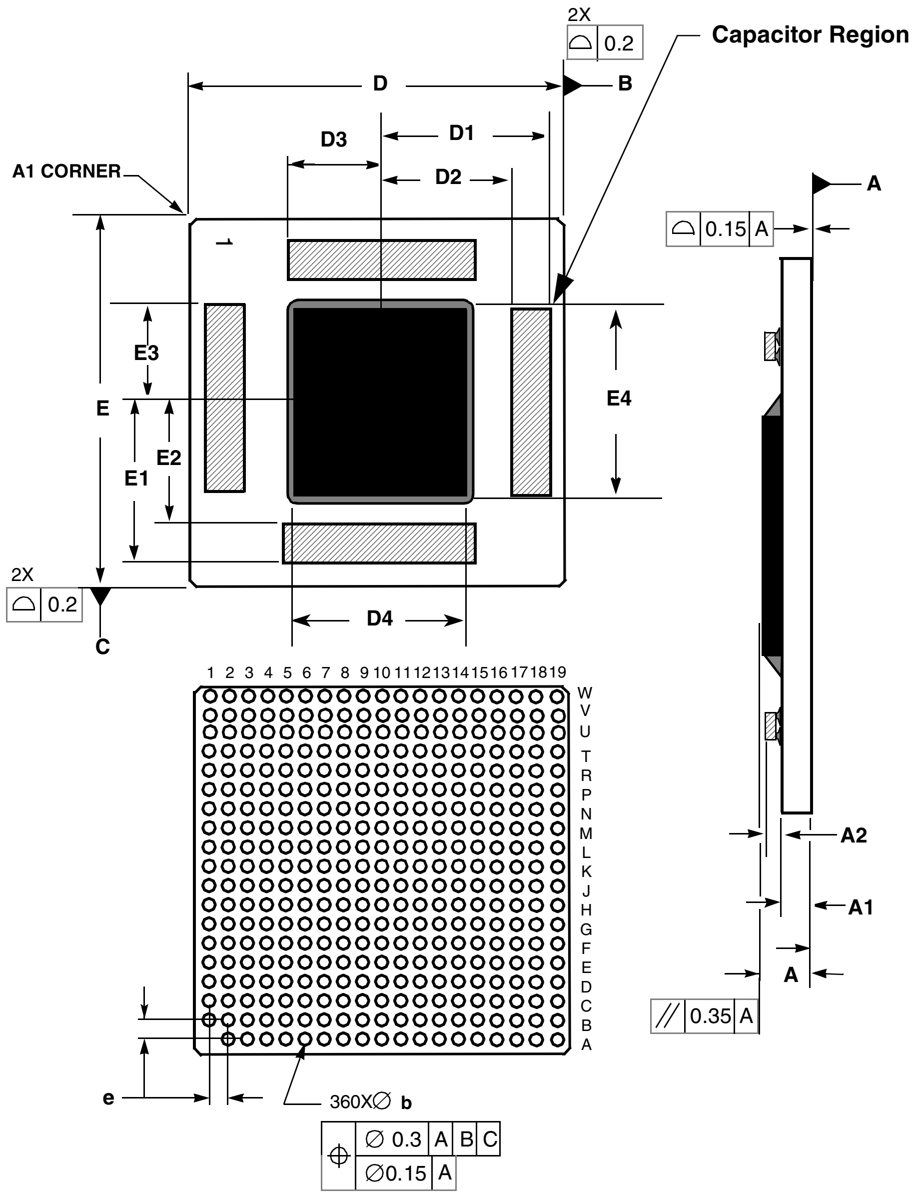
8.1 Package Parameters for the MPC7448, 360 HCTE BGA

The package parameters are as provided in the following list. The package type is 25 × 25 mm, 360-lead high coefficient of thermal expansion ceramic ball grid array (HCTE).

Package outline	25 × 25 mm
Interconnects	360 (19 × 19 ball array – 1)
Pitch	1.27 mm (50 mil)
Minimum module height	2.32 mm
Maximum module height	2.80 mm
Ball diameter	0.89 mm (35 mil)
Coefficient of thermal expansion	12.3 ppm/°C

8.4 Mechanical Dimensions for the MPC7448, 360 HCTE LGA

Figure 13 provides the mechanical dimensions and bottom surface nomenclature for the MPC7448, 360 HCTE LGA package.



NOTES:
1. Dimensioning and tolerancing per ASME Y14.5M, 1994
2. Dimensions in millimeters
3. Top side A1 corner index is a metalized feature with various shapes. Bottom side A1 corner is designated with a pad missing from the array.

	Millimeters	
Dim	**Min**	**Max**
A	1.52	1.80
A1	0.70	0.90
A2	—	0.6
b	0.82	0.93
D	25.00 BSC	
D1	—	11.3
D2	8.0	—
D3	—	6.5
D4	7.2	7.4
e	1.27 BSC	
E	25.00 BSC	
E1	—	11.3
E2	8.0	—
E3	—	6.5
E4	7.9	8.1

Figure 14. Mechanical Dimensions and Bottom Surface Nomenclature for the MPC7448, 360 HCTE LGA Package

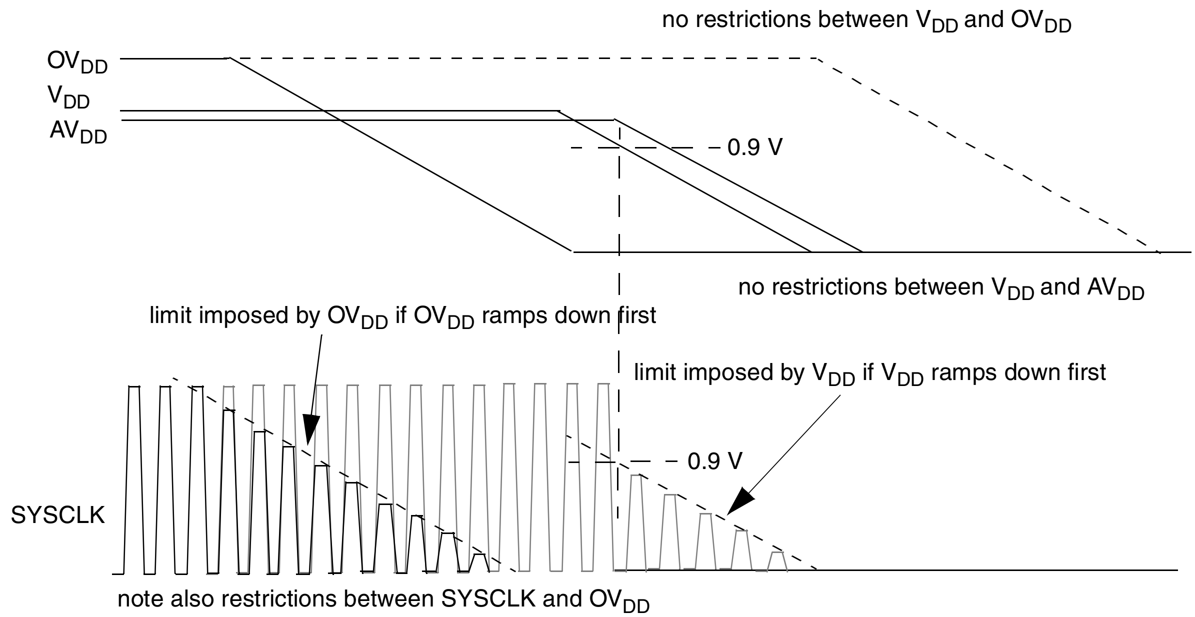


Figure 17. MPC7448 Power Down Sequencing Requirements

There is no requirement regarding AV_{DD} during power down, but it is recommended that AV_{DD} track V_{DD} within the RC time constant of the PLL filter circuit described in Section 9.2.2, "PLL Power Supply Filtering" (nominally 100 µs).

9.2.2 PLL Power Supply Filtering

The AV_{DD} power signal is provided on the MPC7448 to provide power to the clock generation PLL. To ensure stability of the internal clock, the power supplied to the AV_{DD} input signal should be filtered of any noise in the 500-KHz to 10-MHz resonant frequency range of the PLL. The circuit shown in Figure 18 using surface mount capacitors with minimum effective series inductance (ESL) is strongly recommended. In addition to filtering noise from the AV_{DD} input, it also provides the required delay between V_{DD} and AV_{DD} as described in Section 9.2.1, "Power Supply Sequencing."

The circuit should be placed as close as possible to the AV_{DD} pin to minimize noise coupled from nearby circuits. It is often possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of the device footprint.

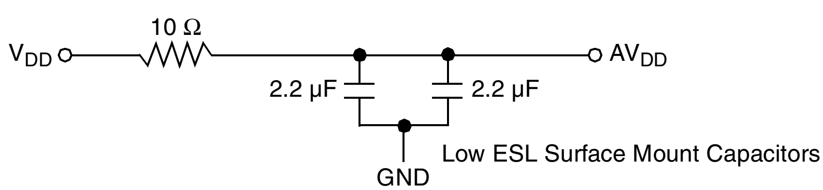


Figure 18. PLL Power Supply Filter Circuit

9.2.4 Decoupling Recommendations

Due to the MPC7448 dynamic power management feature, large address and data buses, and high operating frequencies, the MPC7448 can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the MPC7448 system, and the MPC7448 itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer use sufficient decoupling capacitors, typically one capacitor for every V_{DD} pin, and a similar amount for the OV_{DD} pins, placed as close as possible to the power pins of the MPC7448. It is also recommended that these decoupling capacitors receive their power from separate V_{DD}, OV_{DD}, and GND power planes in the PCB, using short traces to minimize inductance.

These capacitors should have a value of 0.01 or 0.1 µF. Only ceramic surface mount technology (SMT) capacitors should be used to minimize lead inductance. Orientations where connections are made along the length of the part, such as 0204, are preferable but not mandatory. Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993) and contrary to previous recommendations for decoupling Freescale microprocessors, multiple small capacitors of equal value are recommended over using multiple values of capacitance.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V_{DD} and OV_{DD} planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low equivalent series resistance (ESR) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors are 100–330 µF (AVX TPS tantalum or Sanyo OSCON).

9.3 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. Unless otherwise noted, unused active low inputs should be tied to OV_{DD} and unused active high inputs should be connected to GND. All NC (no connect) signals must remain unconnected.

Power and ground connections must be made to all external V_{DD}, OV_{DD}, and GND pins in the MPC7448. For backward compatibility with the MPC7447, MPC7445, and MP7441, or for migrating a system originally designed for one of these devices to the MPC7448, the new power and ground signals (formerly NC, see Table 11) may be left unconnected if the core frequency is 1 GHz or less. Operation above 1 GHz requires that these additional power and ground signals be connected, and it is strongly recommended that all new designs include the additional connections. See also Section 7, “Pinout Listings,” for additional information.

The MPC7448 provides VDD_SENSE, OVDD_SENSE, and GND_SENSE pins. These pins connect directly to the power/ground planes in the device package and are intended to allow an external device to measure the voltage present on the V_{DD}, OV_{DD} and GND planes in the device package. The most common use for these signals is as a feedback signal to a power supply regulator to allow it to compensate for board losses and supply the correct voltage at the device. (Note that all voltage parameters are specified at the pins of the device.) If not used for this purpose, it is recommended that these signals be connected to test points that can be used in the event that an accurate measurement of the voltage at the device is needed during system debug. Otherwise, these signals should be connected to the appropriate power/ground planes on the circuit board or left unconnected.

likewise be pulled up through a pull-up resistor (weak or stronger: 4.7–1 KΩ) to prevent erroneous assertions of this signal.

In addition, the MPC7448 has one open-drain style output that requires a pull-up resistor (weak or stronger: 4.7–1 KΩ) if it is used by the system. This pin is $\overline{\text{CKSTP\_OUT}}$.

BVSEL0 and BVSEL1 should not be allowed to float, and should be configured either via pull-up or pull-down resistors or actively driven by external logic. If pull-down resistors are used to configure BVSEL0 or BVSEL1, the resistors should be less than 250 Ω (see Table 11). Because PLL_CFG[0:5] must remain stable during normal operation, strong pull-up and pull-down resistors (1 KΩ or less) are recommended to configure these signals in order to protect against erroneous switching due to ground bounce, power supply noise, or noise coupling.

During inactive periods on the bus, the address and transfer attributes may not be driven by any master and may, therefore, float in the high-impedance state for relatively long periods of time. Because the MPC7448 must continually monitor these signals for snooping, this float condition may cause excessive power draw by the input receivers on the MPC7448 or by other receivers in the system. These signals can be pulled up through weak (10-KΩ) pull-up resistors by the system, address bus driven mode enabled (see the *MPC7450 RISC Microprocessor Family Users' Manual* for more information on this mode), or they may be otherwise driven by the system during inactive periods of the bus to avoid this additional power draw. Preliminary studies have shown the additional power draw by the MPC7448 input receivers to be negligible and, in any event, none of these measures are necessary for proper device operation. The snooped address and transfer attribute inputs are: A[0:35], AP[0:4], TT[0:4], $\overline{\text{CI}}$, $\overline{\text{WT}}$, and $\overline{\text{GBL}}$.

If address or data parity is not used by the system, and respective parity checking is disabled through HID1, the input receivers for those pins are disabled and do not require pull-up resistors, therefore they may be left unconnected by the system. If extended addressing is not used (HID0[XAEN] = 0), A[0:3] are unused and must be pulled low to GND through weak pull-down resistors; additionally, if address parity checking is enabled (HID1[EBA] = 1) and extended addressing is not used, AP[0] must be pulled up to OV_{DD} through a weak pull-up resistor. If the MPC7448 is in 60x bus mode, DTI[0:3] must be pulled low to GND through weak pull-down resistors.

The data bus input receivers are normally turned off when no read operation is in progress and, therefore, do not require pull-up resistors on the bus. Other data bus receivers in the system, however, may require pull-ups or require that those signals be otherwise driven by the system during inactive periods. The data bus signals are D[0:63] and DP[0:7].

9.6 JTAG Configuration Signals

Boundary-scan testing is enabled through the JTAG interface signals. The $\overline{\text{TRST}}$ signal is optional in the IEEE 1149.1 standard specification, but is typically provided on all processors that implement the PowerPC architecture. While it is possible to force the TAP controller to the reset state using only the TCK and TMS signals, more reliable power-on reset performance will be obtained if the $\overline{\text{TRST}}$ signal is asserted during power-on reset. Because the JTAG interface is also used for accessing the common on-chip processor (COP) function, simply tying $\overline{\text{TRST}}$ to $\overline{\text{HRESET}}$ is not practical.

The COP function of these processors allows a remote computer system (typically a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$ in order

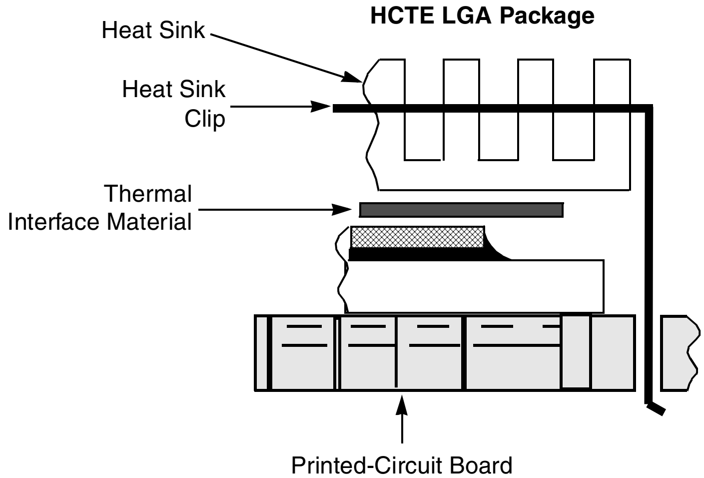


Figure 23. LGA Package Exploded Cross-Sectional View with Several Heat Sink Options

There are several commercially-available heat sinks for the MPC7448 provided by the following vendors:

Aavid Thermalloy 80 Commercial St. Concord, NH 03301 Internet: www.aavidthermalloy.com	603-224-9988
Alpha Novatech 473 Sapena Ct. #12 Santa Clara, CA 95054 Internet: www.alphanovatech.com	408-567-8082
Calgreg Thermal Solutions 60 Alhambra Road, Suite 1 Warwick, RI 02886 Internet: www.calgregthermalsolutions.com	888-732-6100
International Electronic Research Corporation (IERC) 413 North Moss St. Burbank, CA 91502 Internet: www.ctscorp.com	818-842-7277
Tyco Electronics Chip Coolers™ P.O. Box 3668 Harrisburg, PA 17105-3668 Internet: www.tycoelectronics.com	800-522-6752
Wakefield Engineering 33 Bridge St. Pelham, NH 03076 Internet: www.wakefield.com	603-635-2800

Ultimately, the final selection of an appropriate heat sink depends on many factors, such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost.

9.7.1 Internal Package Conduction Resistance

For the exposed-die packaging technology described in Table 5, the intrinsic conduction thermal resistance paths are as follows:

- The die junction-to-case thermal resistance (the case is actually the top of the exposed silicon die)
- The die junction-to-board thermal resistance

Figure 24 depicts the primary heat transfer path for a package with an attached heat sink mounted to a printed-circuit board.

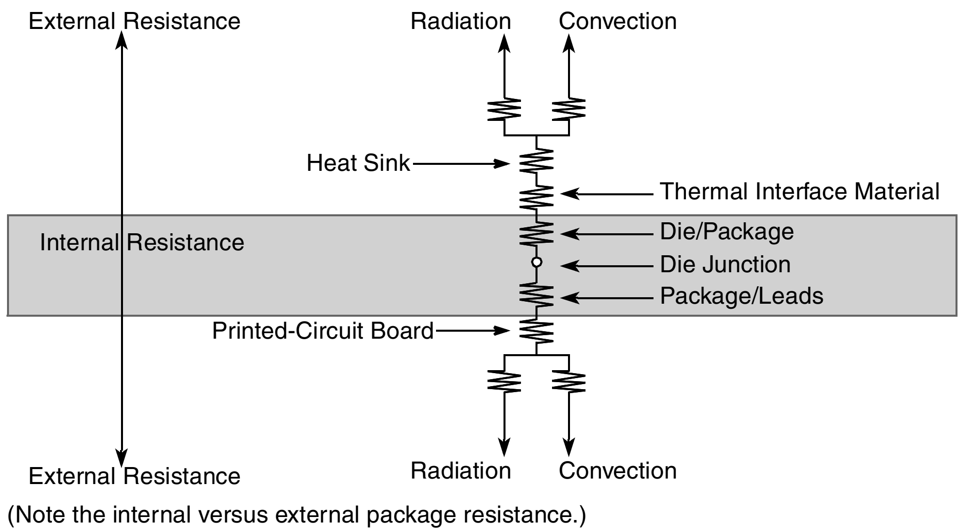


Figure 24. C4 Package with Heat Sink Mounted to a Printed-Circuit Board

Heat generated on the active side of the chip is conducted through the silicon, through the heat sink attach material (or thermal interface material), and, finally, to the heat sink, where it is removed by forced-air convection.

Because the silicon thermal resistance is quite small, the temperature drop in the silicon may be neglected for a first-order analysis. Thus, the thermal interface material and the heat sink conduction/convective thermal resistances are the dominant terms.

9.7.2 Thermal Interface Materials

A thermal interface material is recommended at the package lid-to-heat sink interface to minimize the thermal contact resistance. For those applications where the heat sink is attached by spring clip mechanism, Figure 25 shows the thermal performance of three thin-sheet thermal-interface materials (silicone, graphite/oil, fluoroether oil), a bare joint, and a joint with thermal grease as a function of contact pressure. As shown, the performance of these thermal interface materials improves with increasing contact pressure. The use of thermal grease significantly reduces the interface thermal resistance. That is, the bare joint results in a thermal resistance approximately seven times greater than the thermal grease joint.

Often, heat sinks are attached to the package by means of a spring clip to holes in the printed-circuit board (see Figure 22). Therefore, synthetic grease offers the best thermal performance due to the low interface pressure and is recommended due to the high power dissipation of the MPC7448. Of course, the selection

9.7.4 Temperature Diode

The MPC7448 has a temperature diode on the microprocessor that can be used in conjunction with other system temperature monitoring devices (such as Analog Devices, ADT7461™). These devices use the negative temperature coefficient of a diode operated at a constant current to determine the temperature of the microprocessor and its environment. For proper operation, the monitoring device used should auto-calibrate the device by canceling out the V_{BE} variation of each MPC7448's internal diode.

The following are the specifications of the MPC7448 on-board temperature diode:

$V_f > 0.40$ V

$V_f < 0.90$ V

Operating range 2–300 µA

Diode leakage < 10 nA @ 125°C

Ideality factor over 5–150 µA at 60°C: n = 1.0275 ± 0.9%

Ideality factor is defined as the deviation from the ideal diode equation:

$$I_{fw} = I_s \left[e^{\frac{qV_f}{nKT}} - 1 \right]$$

Another useful equation is:

$$V_H - V_L = n\frac{KT}{q}\left[ln\frac{I_H}{I_L} \right] - 1$$

Where:

- I_{fw} = Forward current
- I_s = Saturation current
- V_d = Voltage at diode
- V_f = Voltage forward biased
- V_H = Diode voltage while I_H is flowing
- V_L = Diode voltage while I_L is flowing
- I_H = Larger diode bias current
- I_L = Smaller diode bias current
- q = Charge of electron (1.6×10^{-19} C)
- n = Ideality factor (normally 1.0)
- K = Boltzman's constant (1.38×10^{-23} Joules/K)
- T = Temperature (Kelvins)

The ratio of I_H to I_L is usually selected to be 10:1. The previous equation simplifies to the following:

$$V_H - V_L = 1.986 \times 10^{-4} \times nT$$

Solving for T, the equation becomes:

$$\mathbf{nT} = \frac{V_H - V_L}{1.986 \times 10^{-4}}$$

9.7.5 Dynamic Frequency Switching (DFS)

The DFS feature in the MPC7448 adds the ability to divide the processor-to-system bus ratio by two or four during normal functional operation. Divide-by-two mode is enabled by setting the HID1[DFS2] bit in software or by asserting the $\overline{\text{DFS2}}$ pin via hardware. The MPC7448 can be returned for full speed by clearing HID1[DFS2] or negating $\overline{\text{DFS2}}$. Similarly, divide-by-four mode is enabled by setting HID1[DFS4] in software or by asserting the $\overline{\text{DFS4}}$ pin. In all cases, the frequency change occurs in 1 clock cycle and no idle waiting period is required to switch between modes. Note that asserting either $\overline{\text{DFS2}}$ or $\overline{\text{DFS4}}$ overrides software control of DFS, and that asserting both $\overline{\text{DFS2}}$ and $\overline{\text{DFS4}}$ disables DFS completely, including software control. Additional information regarding DFS can be found in the *MPC7450 RISC Microprocessor Family Reference Manual*. Note that minimum core frequency requirements must be observed when enabling DFS, and the resulting core frequency must meet the requirements for f_{core_DFS} given in Table 8.

9.7.5.1 Power Consumption with DFS Enabled

Power consumption with DFS enabled can be approximated using the following formula:

$$\mathbf{P_{DFS}} = \left[\frac{f_{DFS}}{f}\,(P - P_{DS})\right] + P_{DS}$$

Where:

P_{DFS} = Power consumption with DFS enabled

f_{DFS} = Core frequency with DFS enabled

f = Core frequency prior to enabling DFS

P = Power consumption prior to enabling DFS (see Table 7)

P_{DS} = Deep sleep mode power consumption (see Table 7)

The above is an approximation only. Power consumption with DFS enabled is not tested or guaranteed.

9.7.5.2 Bus-to-Core Multiplier Constraints with DFS

DFS is not available for all bus-to-core multipliers as configured by PLL_CFG[0:5] during hard reset. The complete listing is shown in Table 16. Shaded cells represent DFS modes that are not available for a particular PLL_CFG[0:5] setting. Should software or hardware attempt to transition to a multiplier that is not supported, the device will remain at its current multiplier. For example, if a transition from DFS-disabled to an unsupported divide-by-2 or divide-by-4 setting is attempted, the bus-to-core multiplier will remain at the setting configured by the PLL_CFG[0:5] pins. In the case of an attempted transition from a supported divide-by-2 mode to an unsupported divide-by-4 mode, the device will remain in divide-by-2 mode. In all cases, the HID1[PC0-5] bits will correctly reflect the current bus-to-core frequency multiplier.

Table 16. Valid Divide Ratio Configurations

DFS mode disabled		DFS divide-by-2 mode enabled (HID1[DFS2] = 1 or $\overline{DFS2}$ = 0)		DFS divide-by-4 mode enabled (HID1[DFS4] = 1 or $\overline{DFS4}$ = 0)	
Bus-to-Core Multiplier Configured by PLL_CFG[0:5] (see Table 12)	HID1[PC0-5] [3]	Bus-to-Core Multiplier	HID1[PC0-5] [3]	Bus-to-Core Multiplier	HID1[PC0-5] [3]
2x [4]	010000	N/A (unchanged) [1]	unchanged [1]	N/A (unchanged) [1]	unchanged [1]
3x [4]	100000	N/A (unchanged) [1]	unchanged [1]	N/A (unchanged) [1]	unchanged [1]
4x [4]	101000	2x [4]	010000	N/A (unchanged) [1]	unchanged [1]
5x	101100	2.5x [4]	010101	N/A (unchanged) [1]	unchanged [1]
5.5x	100100	2.75x [4]	110101 [2]	N/A (unchanged) [1]	unchanged [1]
6x	110100	3x [4]	100000	N/A (unchanged) [1]	unchanged [1]
6.5x	010100	3.25x [4]	100000 [2]	N/A (unchanged) [1]	unchanged [1]
7x	001000	3.5x [4]	110101	N/A (unchanged) [1]	unchanged [1]
7.5x	000100	3.75x [4]	110101 [2]	N/A (unchanged) [1]	unchanged [1]
8x	110000	4x [4]	101000 [4]	2x [4]	010000
8.5x	011000	4.25x [4]	101000 [2]	N/A (unchanged) [1]	unchanged [1]
9x	011110	4.5x [4]	011101	2.25x [4]	010000 [2]
9.5x	011100	4.75x [4]	011101 [2]	N/A (unchanged) [1]	unchanged [1]
10x	101010	5x	101100	2.5x [4]	010101
10.5x	100010	5.25x	101100 [2]	N/A (unchanged) [1]	unchanged [1]
11x	100110	5.5x	100100	2.75x [4]	010101 [2]
11.5x	000000	5.75x	100100 [2]	N/A (unchanged) [1]	unchanged [1]
12x	101110	6x	110100	3x [4]	100000
12.5x	111110	6.25x	110100 [2]	N/A (unchanged) [1]	unchanged [1]
13x	010110	6.5x	010100	3.25x [4]	100000 [2]
13.5x	111000	6.75	010100 [2]	N/A (unchanged) [1]	unchanged [1]
14x	110010	7x	001000	3.5x [4]	110101
15x	000110	7.5x	000100	3.75x [4]	110101 [2]
16x	110110	8x	110000	4x [4]	101000
17x	000010	8.5x	011000	4.25x [4]	101000 [2]
18x	001010	9x	011110	4.5x [4]	011101
20x	001110	10x	101010	5x	101100
21x	010010	10.5x	100010	5.25x	101100 [2]

Table 16. Valid Divide Ratio Configurations (continued)

DFS mode disabled		DFS divide-by-2 mode enabled (HID1[DFS2] = 1 or $\overline{DFS2}$ = 0)		DFS divide-by-4 mode enabled (HID1[DFS4] = 1 or $\overline{DFS4}$ = 0)	
Bus-to-Core Multiplier Configured by PLL_CFG[0:5] (see Table 12)	**HID1[PC0-5] [3]**	**Bus-to-Core Multiplier**	**HID1[PC0-5] [3]**	**Bus-to-Core Multiplier**	**HID1[PC0-5] [3]**
24x	011010	12x	101110	6x	110100
28x	111010	14x	110010	7x	001000

Notes:
1. DFS mode is not supported for this combination of DFS mode and PLL_CFG[0:5] setting. As a result, the processor will ignore these settings and remain at the previous multiplier, as reflected by the HID1[PC0-PC5] bits.
2. Though supported by the MPC7448 clock circuitry, multipliers of *n*.25x and *n*.75x cannot be expressed as valid PLL configuration codes. As a result, the values displayed in HID1[PC0-PC5] are rounded down to the nearest valid PLL configuration code. However, the actual bus-to-core multiplier is as stated in this table.
3. Note that in the HID1 register of the MPC7448, the PC0, PC1, PC2, PC3, PC4, and PC5 bits are bits 15, 16, 17, 18, 19, and 14 (respectively). See the *MPC7450 RISC Microprocessor Reference Manual* for more information.
4. Special considerations regarding snooped transactions must be observed for bus-to-core multipliers less than 5x. See the *MPC7450 RISC Microprocessor Reference Manual* for more information.

9.7.5.3 Minimum Core Frequency Requirements with DFS

In many systems, enabling DFS can result in very low processor core frequencies. However, care must be taken to ensure that the resulting processor core frequency is within the limits specified in Table 8. Proper operation of the device is not guaranteed at core frequencies below the specified minimum f_{core}.

10 Document Revision History

Table 17 provides a revision history for this hardware specification.

Table 17. Document Revision History

Revision	Date	Substantive Change(s)
4	3/2007	Table 19: Added 800 MHz processor frequency.
3	10/2006	Section 9.7, “Power and Thermal Management Information”: Updated contact information. Table 18, Table 20, and Table 19: Added Revision D PVR. Table 19: Added 600 processor frequency, additional product codes, date codes for 1400 processor frequency, and footnotes 1 and 2. Table 20: Added PPC product code and footnote 1. Table 19 and Table 20: Added Revision D information for 1267 processor frequency.

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