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Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC G4
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.267GHz
Co-Processors/DSP	Multimedia; SIMD
RAM Controllers	-
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	1.5V, 1.8V, 2.5V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	360-BCBGA, FCCBGA
Supplier Device Package	360-FCCBGA (25x25)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc7448hx1267nc

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



2 Features

This section summarizes features of the MPC7448 implementation.

Major features of the MPC7448 are as follows:

- High-performance, superscalar microprocessor
 - Up to four instructions can be fetched from the instruction cache at a time.
 - Up to three instructions plus a branch instruction can be dispatched to the issue queues at a time.
 - Up to 12 instructions can be in the instruction queue (IQ).
 - Up to 16 instructions can be at some stage of execution simultaneously.
 - Single-cycle execution for most instructions
 - One instruction per clock cycle throughput for most instructions
 - Seven-stage pipeline control
- Eleven independent execution units and three register files
 - Branch processing unit (BPU) features static and dynamic branch prediction
 - 128-entry (32-set, four-way set-associative) branch target instruction cache (BTIC), a cache of branch instructions that have been encountered in branch/loop code sequences. If a target instruction is in the BTIC, it is fetched into the instruction queue a cycle sooner than it can be made available from the instruction cache. Typically, a fetch that hits the BTIC provides the first four instructions in the target stream.
 - 2048-entry branch history table (BHT) with 2 bits per entry for four levels of prediction—not taken, strongly not taken, taken, and strongly taken
 - Up to three outstanding speculative branches
 - Branch instructions that do not update the count register (CTR) or link register (LR) are often removed from the instruction stream.
 - Eight-entry link register stack to predict the target address of Branch Conditional to Link Register (bclr) instructions
 - Four integer units (IUs) that share 32 GPRs for integer operands
 - Three identical IUs (IU1a, IU1b, and IU1c) can execute all integer instructions except multiply, divide, and move to/from special-purpose register instructions.
 - IU2 executes miscellaneous instructions, including the CR logical operations, integer multiplication and division instructions, and move to/from special-purpose register instructions.
 - Five-stage FPU and 32-entry FPR file
 - Fully IEEE Std. 754TM-1985–compliant FPU for both single- and double-precision operations
 - Supports non-IEEE mode for time-critical operations
 - Hardware support for denormalized numbers
 - Thirty-two 64-bit FPRs for single- or double-precision operands





- Monitors all dispatched instructions and retires them in order
- Tracks unresolved branches and flushes instructions after a mispredicted branch
- Retires as many as three instructions per clock cycle
- Separate on-chip L1 instruction and data caches (Harvard architecture)
 - 32-Kbyte, eight-way set-associative instruction and data caches
 - Pseudo least-recently-used (PLRU) replacement algorithm
 - 32-byte (eight-word) L1 cache block
 - Physically indexed/physical tags
 - Cache write-back or write-through operation programmable on a per-page or per-block basis
 - Instruction cache can provide four instructions per clock cycle; data cache can provide four words per clock cycle
 - Caches can be disabled in software.
 - Caches can be locked in software.
 - MESI data cache coherency maintained in hardware
 - Separate copy of data cache tags for efficient snooping
 - Parity support on cache
 - No snooping of instruction cache except for **icbi** instruction
 - Data cache supports AltiVec LRU and transient instructions
 - Critical double- and/or quad-word forwarding is performed as needed. Critical quad-word forwarding is used for AltiVec loads and instruction fetches. Other accesses use critical double-word forwarding.
- Level 2 (L2) cache interface
 - On-chip, 1-Mbyte, eight-way set-associative unified instruction and data cache
 - Cache write-back or write-through operation programmable on a per-page or per-block basis
 - Parity support on cache tags
 - ECC or parity support on data
 - Error injection allows testing of error recovery software
- Separate memory management units (MMUs) for instructions and data
 - 52-bit virtual address, 32- or 36-bit physical address
 - Address translation for 4-Kbyte pages, variable-sized blocks, and 256-Mbyte segments
 - Memory programmable as write-back/write-through, caching-inhibited/caching-allowed, and memory coherency enforced/memory coherency not enforced on a page or block basis
 - Separate IBATs and DBATs (eight each) also defined as SPRs
 - Separate instruction and data translation lookaside buffers (TLBs)
 - Both TLBs are 128-entry, two-way set-associative and use an LRU replacement algorithm.
 - TLBs are hardware- or software-reloadable (that is, a page table search is performed in hardware or by system software on a TLB miss).



Electrical and Thermal Characteristics

when running a typical benchmark at temperatures in a typical system. The Full-Power Mode–Thermal value is intended to represent the sustained power consumption of the device when running a typical code sequence at high temperature and is recommended to be used as the basis for designing a thermal solution; see Section 9.7, "Power and Thermal Management Information" for more information on thermal solutions. The Full-Power Mode–Maximum value is recommended to be used for power supply design because this represents the maximum peak power draw of the device that a power supply must be capable of sourcing without voltage droop. For information on power consumption when dynamic frequency switching is enabled, see Section 9.7.5, "Dynamic Frequency Switching (DFS)."

Die Junction Maximum Processor Core Frequency (Speed Grade, MHz)						Nata			
	Temperature (T _j)	1000 MHz	1420 MHz	1600 MHz	1700 MHz	Unit	Notes		
	Full-Power Mode								
Typical	65 •C	15.0	19.0	20.0	21.0	W	1, 2		
Thermal	105 •C	18.6	23.3	24.4	25.6	W	1, 5		
Maximum	105 •C	21.6	27.1	28.4	29.8	W	1, 3		
			Nap Mod	e	·				
Typical	105 •C	11.1	11.8	13.0	13.0	W	1, 6		
			Sleep Mod	le					
Typical	105 • C	10.8	11.4	12.5	12.5	W	1, 6		
Deep Sleep Mode (PLL Disabled)									
Typical	105 •C	10.4	11.0	12.0	12.0	W	1, 6		

Table 7. Power Consumption for MPC7448 at Maximum Rated Frequency

Notes:

- These values specify the power consumption for the core power supply (V_{DD}) at nominal voltage and apply to all valid processor bus frequencies and configurations. The values do not include I/O supply power (OV_{DD}) or PLL supply power (AV_{DD}). OV_{DD} power is system dependent but is typically < 5% of V_{DD} power. Worst case power consumption for AV_{DD} < 13 mW. Freescale also offers MPC7448 part numbers that meet lower power consumption specifications; for more information on these devices, see Section 11.2, "Part Numbers Not Fully Addressed by This Document."
- 2. Typical power consumption is an average value measured with the processor operating at its rated maximum processor core frequency (except for Deep Sleep Mode), at nominal recommended V_{DD} (see Table 4) and 65°C while running the Dhrystone 2.1 benchmark and achieving 2.3 Dhrystone MIPs/MHz. This parameter is not 100% tested but periodically sampled.b
- 3. Maximum power consumption is the average measured with the processor operating at its rated maximum processor core frequency, at nominal V_{DD} and maximum operating junction temperature (see Table 4) while running an entirely cache-resident, contrived sequence of instructions to keep all the execution units maximally busy.
- 4. Doze mode is not a user-definable state; it is an intermediate state between full-power and either nap or sleep mode. As a result, power consumption for this mode is not tested.
- Thermal power consumption is an average value measured at the nominal recommended V_{DD} (see Table 4) and 105 °C while running the Dhrystone 2.1 benchmark and achieving 2.3 Dhrystone MIPs/MHz. This parameter is not 100% tested but periodically sampled.
- 6. Typical power consumption for these modes is measured at the nominal recommended V_{DD} (see Table 4) and 105 °C in the mode described. This parameter is not 100% tested but is periodically sampled.



Electrical and Thermal Characteristics





Figure 6. Input/Output Timing Diagram



5.2.3 IEEE Std. 1149.1 AC Timing Specifications

Table 10 provides the IEEE Std. 1149.1 (JTAG) AC timing specifications as defined in Figure 8 through Figure 11.

Table 10. JTAG AC Timing Specifications (Independent of SYSCLK)¹

At recommended operating conditions. See Table 4.

Parameter	Symbol	Min	Мах	Unit	Notes
TCK frequency of operation	f _{TCLK}	0	33.3	MHz	
TCK cycle time	t _{TCLK}	30	—	ns	
TCK clock pulse width measured at 1.4 V	t _{JHJL}	15	—	ns	
TCK rise and fall times	$t_{\rm JR}$ and $t_{\rm JF}$	—	2	ns	
TRST assert time	t _{TRST}	25	—	ns	2
Input setup times: Boundary-scan data TMS, TDI	t _{DVJH} t _{IVJH}	4 0	_	ns	3
Input hold times: Boundary-scan data TMS, TDI	^t DXJH t _{IXJH}	20 25		ns	3
Valid times: Boundary-scan data TDO	t _{JLDV} t _{JLOV}	4 4	20 25	ns	4
Output hold times: Boundary-scan data TDO	t _{JLDX} t _{JLOX}	30 30	—	ns	4
TCK to output high impedance: Boundary-scan data TDO	t _{JLDZ} t _{JLOZ}	3 3	19 9	ns	4, 5

Notes:

 All outputs are measured from the midpoint voltage of the falling/rising edge of TCLK to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load (see Figure 7). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.

2. TRST is an asynchronous level sensitive signal. The time is for test purposes only.

3. Non-JTAG signal input timing with respect to TCK.

4. Non-JTAG signal output timing with respect to TCK.

5. Guaranteed by design and characterization.



Signal Name	Pin Number	Active	I/O	Notes
LVRAM	B10	_	_	12, 20, 22
NC (no connect)	A6, A14, A15, B14, B15, C14, C15, C16, C17, C18, C19, D14, D15, D16, D17, D18, D19, E14, E15, F14, F15, G14, G15, H15, H16, J15, J16, J17, J18, J19, K15, K16, K17, K18, K19, L15, L16, L17, L18, L19	_	_	11
LSSD_MODE	E8	Low	Input	6, 12
MCP	C9	Low	Input	
OV _{DD}	B4, C2, C12, D5, F2, H3, J5, K2, L5, M3, N6, P2, P8, P11, R4, R13, R16, T6, T9, U2, U12, U16, V4, V7, V10, V14	—	—	
OVDD_SENSE	E18, G18		—	16
PLL_CFG[0:4]	B8, C8, C7, D7, A7	High	Input	
PLL_CFG[5]	D10	High	Input	9, 20
PMON_IN	D9	Low	Input	13
PMON_OUT	A9	Low	Output	
QACK	G5	Low	Input	
QREQ	P4	Low	Output	
SHD[0:1]	E4, H5	Low	I/O	3
SMI	F9	Low	Input	
SRESET	A2	Low	Input	
SYSCLK	A10		Input	
TA	К6	Low	Input	
TBEN	E1	High	Input	
TBST	F11	Low	Output	
ТСК	C6	High	Input	
TDI	B9	High	Input	6
TDO	A4	High	Output	
TEA	L1	Low	Input	
TEMP_ANODE	N18	—	—	17
TEMP_CATHODE	N19		—	17
TMS	F1	High	Input	6
TRST	A5	Low	Input	6, 14
TS	L4	Low	I/O	3
TSIZ[0:2]	G6, F7, E7	High	Output	
TT[0:4]	E5, E6, F6, E9, C5	High	I/O	
WT	D3	Low	Output	
V _{DD}	H8, H10, H12, J7, J9, J11, J13, K8, K10, K12, K14, L7, L9, L11, L13, M8, M10, M12	—	—	
V _{DD}	A13, A16, A18, B17, B19, C13, E13, E16, F12, F17, F19, G11, G16, H14, H17, H19, M14, M16, M18, N15, N17, P16, P18	_	_	15

Table 11. Pinout Listing for the MPC744	8, 360 HCTE Package (continued)
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8.3 Package Parameters for the MPC7448, 360 HCTE LGA

The package parameters are as provided in the following list. The package type is 25×25 mm, 360 pin high coefficient of thermal expansion ceramic land grid array (HCTE).

Package outline	$25 \times 25 \text{ mm}$			
Interconnects	$360 (19 \times 19 \text{ ball array} - 1)$			
Pitch	1.27 mm (50 mil)			
Minimum module height	1.52 mm			
Maximum module height	1.80 mm			
Pad diameter	0.89 mm (35 mil)			
Coefficient of thermal expansion12.3 ppm/°C				



Package Description

8.6 Mechanical Dimensions for the MPC7448, 360 HCTE RoHS-Compliant BGA

Figure 13 provides the mechanical dimensions and bottom surface nomenclature for the MPC7448, 360 HCTE BGA package with RoHS-compliant lead-free spheres.



Figure 15. Mechanical Dimensions and Bottom Surface Nomenclature for the MPC7448, 360 HCTE RoHS-Compliant BGA Package



	Example Core and VCO Frequency in MHz										
PLL_CFG[0:5]	Rue te Cere	Corro to VCO	Bus (SYSCLK) Frequency								
	Multiplier ⁵	Multiplier ⁵	33.3 MHz	50 MHz	66.6 MHz	75 MHz	83 MHz	100 MHz	133 MHz	167 MHz	200 MHz
100110	11x	1x			733	825	913	1100	1467		
000000	11.5x	1x			766	863	955	1150	1533		
101110	12x	1x		600	800	900	996	1200	1600		
111110	12.5x	1x		625	833	938	1038	1250	1667		
010110	13x	1x		650	865	975	1079	1300			
111000	13.5x	1x		675	900	1013	1121	1350			
110010	14x	1x		700	933	1050	1162	1400			
000110	15x	1x		750	1000	1125	1245	1500			
110110	16x	1x		800	1066	1200	1328	1600			
000010	17x	1x		850	1132	1275	1417	1700			
001010	18x	1x	600	900	1200	1350	1500				
001110	20x	1x	667	1000	1332	1500	1666				
010010	21x	1x	700	1050	1399	1575					
011010	24x	1x	800	1200	1600						
111010	28x	1x	933	1400							
001100	PLL b	oypass		PLL off, S	SYSCLK	clocks co	re circuit	ry directly	/		
111100	PLI	_ off		PL	L off, no	core cloc	king occu	urs			

Table 12. MPC7448 Microprocessor PLL Configuration Example (continued)

Notes:

1. PLL_CFG[0:5] settings not listed are reserved.

2. The sample bus-to-core frequencies shown are for reference only. Some PLL configurations may select bus, core, or VCO frequencies which are not useful, not supported, or not tested for by the MPC7448; see Section 5.2.1, "Clock AC Specifications," for valid SYSCLK, core, and VCO frequencies.

3. In PLL-bypass mode, the SYSCLK input signal clocks the internal processor directly and the PLL is disabled. However, the bus interface unit requires a 2x clock to function. Therefore, an additional signal, EXT_QUAL, must be driven at half the frequency of SYSCLK and offset in phase to meet the required input setup t_{IVKH} and hold time t_{IXKH} (see Table 9). The result will be that the processor bus frequency will be one-half SYSCLK, while the internal processor is clocked at SYSCLK frequency. This mode is intended for factory use and emulator tool use only.

Note: The AC timing specifications given in this document do not apply in PLL-bypass mode.

- 4. In PLL-off mode, no clocking occurs inside the MPC7448 regardless of the SYSCLK input.
- 5. Applicable when DFS modes are disabled. These multipliers change when operating in a DFS mode. See Section 9.7.5, "Dynamic Frequency Switching (DFS)" for more information.
- 6. Bus-to-core multipliers less than 5x require that assertion of AACK be delayed by one or two bus cycles to allow the processor to generate a response to a snooped transaction. See the *MPC7450 RISC Microprocessor Reference Manual* for more information.



9.1.2 System Bus Clock (SYSCLK) and Spread Spectrum Sources

Spread spectrum clock sources are an increasingly popular way to control electromagnetic interference emissions (EMI) by spreading the emitted noise to a wider spectrum and reducing the peak noise magnitude in order to meet industry and government requirements. These clock sources intentionally add long-term jitter in order to diffuse the EMI spectral content. The jitter specification given in Table 8 considers short-term (cycle-to-cycle) jitter only and the clock generator's cycle-to-cycle output jitter should meet the MPC7448 input cycle-to-cycle jitter requirement. Frequency modulation and spread are separate concerns, and the MPC7448 is compatible with spread spectrum sources if the recommendations listed in Table 13 are observed.

At recommended operating conditions. See Table 4.

Parameter	Min	Мах	Unit	Notes
Frequency modulation	—	50	kHz	1
Frequency spread	—	1.0	%	1, 2

Notes:

2. SYSCLK frequencies resulting from frequency spreading, and the resulting core and VCO frequencies, must meet the minimum and maximum specifications given in Table 8.

It is imperative to note that the processor's minimum and maximum SYSCLK, core, and VCO frequencies must not be exceeded regardless of the type of clock source. Therefore, systems in which the processor is operated at its maximum rated core or bus frequency should avoid violating the stated limits by using down-spreading only.

9.2 Power Supply Design and Sequencing

The following sections provide detailed information regarding power supply design for the MPC7448.

9.2.1 Power Supply Sequencing

The MPC7448 requires its power rails and clock to be applied in a specific sequence to ensure proper device operation and to prevent device damage. The power sequencing requirements are as follows:

- AV_{DD} must be delayed with respect to V_{DD} by the RC time constant of the PLL filter circuit described in Section 9.2.2, "PLL Power Supply Filtering". This time constant is nominally 100 μs.
- OV_{DD} may ramp anytime before or after V_{DD} and AV_{DD} .

Additionally, the following requirements exist regarding the application of SYSCLK:

- The voltage at the SYSCLK input must not exceed V_{DD} until V_{DD} has ramped to 0.9 V.
- The voltage at the SYSCLK input must not exceed OV_{DD} by more 20% during transients (see overshoot/undershoot specifications in Figure 2) or 0.3 V DC (see Table 2) at any time.

^{1.} Guaranteed by design



These requirements are shown graphically in Figure 16.



Figure 16. MPC7448 Power Up Sequencing Requirements

Certain stipulations also apply to the manner in which the power rails of the MPC7448 power down, as follows:

- OV_{DD} may ramp down any time before or after V_{DD}.
- The voltage at the SYSCLK input must not exceed V_{DD} once V_{DD} has ramped down below 0.9 V.
- The voltage at the SYSCLK input must not exceed OV_{DD} by more 20% during transients (see overshoot/undershoot specifications in Figure 2) or 0.3 V DC (see Table 2) at any time.





Figure 17. MPC7448 Power Down Sequencing Requirements

There is no requirement regarding AV_{DD} during power down, but it is recommended that AV_{DD} track V_{DD} within the RC time constant of the PLL filter circuit described in Section 9.2.2, "PLL Power Supply Filtering" (nominally 100 μ s).

9.2.2 PLL Power Supply Filtering

The AV_{DD} power signal is provided on the MPC7448 to provide power to the clock generation PLL. To ensure stability of the internal clock, the power supplied to the AV_{DD} input signal should be filtered of any noise in the 500-KHz to 10-MHz resonant frequency range of the PLL. The circuit shown in Figure 18 using surface mount capacitors with minimum effective series inductance (ESL) is strongly recommended. In addition to filtering noise from the AV_{DD} input, it also provides the required delay between V_{DD} and AV_{DD} as described in Section 9.2.1, "Power Supply Sequencing."

The circuit should be placed as close as possible to the AV_{DD} pin to minimize noise coupled from nearby circuits. It is often possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of the device footprint.



Figure 18. PLL Power Supply Filter Circuit



9.2.4 Decoupling Recommendations

Due to the MPC7448 dynamic power management feature, large address and data buses, and high operating frequencies, the MPC7448 can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the MPC7448 system, and the MPC7448 itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer use sufficient decoupling capacitors, typically one capacitor for every V_{DD} pin, and a similar amount for the OV_{DD} pins, placed as close as possible to the power pins of the MPC7448. It is also recommended that these decoupling capacitors receive their power from separate V_{DD} , OV_{DD}, and GND power planes in the PCB, using short traces to minimize inductance.

These capacitors should have a value of 0.01 or 0.1 μ F. Only ceramic surface mount technology (SMT) capacitors should be used to minimize lead inductance. Orientations where connections are made along the length of the part, such as 0204, are preferable but not mandatory. Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993) and contrary to previous recommendations for decoupling Freescale microprocessors, multiple small capacitors of equal value are recommended over using multiple values of capacitance.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V_{DD} and OV_{DD} planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low equivalent series resistance (ESR) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors are 100–330 μ F (AVX TPS tantalum or Sanyo OSCON).

9.3 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. Unless otherwise noted, unused active low inputs should be tied to OV_{DD} and unused active high inputs should be connected to GND. All NC (no connect) signals must remain unconnected.

Power and ground connections must be made to all external V_{DD} , OV_{DD} , and GND pins in the MPC7448. For backward compatibility with the MPC7447, MPC7445, and MP7441, or for migrating a system originally designed for one of these devices to the MPC7448, the new power and ground signals (formerly NC, see Table 11) may be left unconnected if the core frequency is 1 GHz or less. Operation above 1 GHz requires that these additional power and ground signals be connected, and it is strongly recommended that all new designs include the additional connections. See also Section 7, "Pinout Listings," for additional information.

The MPC7448 provides VDD_SENSE, OVDD_SENSE, and GND_SENSE pins. These pins connect directly to the power/ground planes in the device package and are intended to allow an external device to measure the voltage present on the V_{DD} , OV_{DD} and GND planes in the device package. The most common use for these signals is as a feedback signal to a power supply regulator to allow it to compensate for board losses and supply the correct voltage at the device. (Note that all voltage parameters are specified at the pins of the device.) If not used for this purpose, it is recommended that these signals be connected to test points that can be used in the event that an accurate measurement of the voltage at the device is needed during system debug. Otherwise, these signals should be connected to the appropriate power/ground planes on the circuit board or left unconnected.



9.7 Power and Thermal Management Information

This section provides thermal management information for the high coefficient of thermal expansion (HCTE) package for air-cooled applications. Proper thermal control design is primarily dependent on the system-level design—the heat sink, airflow, and thermal interface material. The MPC7448 implements several features designed to assist with thermal management, including DFS and the temperature diode. DFS reduces the power consumption of the device by reducing the core frequency; see Section 9.7.5.1, "Power Consumption with DFS Enabled," for specific information regarding power reduction and DFS. The temperature diode allows an external device to monitor the die temperature in order to detect excessive temperature conditions and alert the system; see Section 9.7.4, "Temperature Diode," for more information.

To reduce the die-junction temperature, heat sinks may be attached to the package by several methods—spring clip to holes in the printed-circuit board or package, and mounting clip and screw assembly (see Figure 22); however, due to the potential large mass of the heat sink, attachment through the printed-circuit board is suggested. In any implementation of a heat sink solution, the force on the die should not exceed ten pounds (45 Newtons).



Figure 22. BGA Package Exploded Cross-Sectional View with Several Heat Sink Options

NOTE

A clip on heat sink is not recommended for LGA because there may not be adequate clearance between the device and the circuit board. A through-hole solution is recommended, as shown in Figure 23.



9.7.1 Internal Package Conduction Resistance

For the exposed-die packaging technology described in Table 5, the intrinsic conduction thermal resistance paths are as follows:

- The die junction-to-case thermal resistance (the case is actually the top of the exposed silicon die)
- The die junction-to-board thermal resistance

Figure 24 depicts the primary heat transfer path for a package with an attached heat sink mounted to a printed-circuit board.



Figure 24. C4 Package with Heat Sink Mounted to a Printed-Circuit Board

Heat generated on the active side of the chip is conducted through the silicon, through the heat sink attach material (or thermal interface material), and, finally, to the heat sink, where it is removed by forced-air convection.

Because the silicon thermal resistance is quite small, the temperature drop in the silicon may be neglected for a first-order analysis. Thus, the thermal interface material and the heat sink conduction/convective thermal resistances are the dominant terms.

9.7.2 Thermal Interface Materials

A thermal interface material is recommended at the package lid-to-heat sink interface to minimize the thermal contact resistance. For those applications where the heat sink is attached by spring clip mechanism, Figure 25 shows the thermal performance of three thin-sheet thermal-interface materials (silicone, graphite/oil, fluoroether oil), a bare joint, and a joint with thermal grease as a function of contact pressure. As shown, the performance of these thermal interface materials improves with increasing contact pressure. The use of thermal grease significantly reduces the interface thermal resistance. That is, the bare joint results in a thermal resistance approximately seven times greater than the thermal grease joint.

Often, heat sinks are attached to the package by means of a spring clip to holes in the printed-circuit board (see Figure 22). Therefore, synthetic grease offers the best thermal performance due to the low interface pressure and is recommended due to the high power dissipation of the MPC7448. Of course, the selection



of any thermal interface material depends on many factors—thermal performance requirements, manufacturability, service temperature, dielectric properties, cost, and so on.



Figure 25. Thermal Performance of Select Thermal Interface Material

The board designer can choose between several types of thermal interfaces. Heat sink adhesive materials should be selected based on high conductivity and mechanical strength to meet equipment shock/vibration requirements. There are several commercially available thermal interfaces and adhesive materials provided by the following vendors:

The Bergquist Company	800-347-4572
18930 West 78 th St.	
Chanhassen, MN 55317	
Internet: www.bergquistcompany.com	
Chomerics, Inc.	781-935-4850
77 Dragon Ct.	
Woburn, MA 01801	
Internet: www.chomerics.com	
Dow-Corning Corporation	800-248-2481
Corporate Center	
P.O. Box 994.	
Midland, MI 48686-0994	
Internet: www.dowcorning.com	

DFS mode disabled		DFS divide-by-2 ((HID1[DFS2] = 1	mode enabled or DFS2 = 0)	DFS divide-by-4 mode enabled (HID1[DFS4] = 1 or DFS4 = 0)		
Bus-to-Core Multiplier Configured by PLL_CFG[0:5] (see Table 12)	HID1[PC0-5] ³	Bus-to-Core Multiplier	HID1[PC0-5] ³	Bus-to-Core Multiplier	HID1[PC0-5] ³	
2x ⁴	010000	N/A (unchanged) ¹	unchanged ¹	N/A (unchanged) ¹	unchanged ¹	
3x ⁴	100000	N/A (unchanged) ¹	unchanged ¹	N/A (unchanged) ¹	unchanged ¹	
4x ⁴	101000	2x ⁴	010000	N/A (unchanged) ¹	unchanged ¹	
5x	101100	2.5x ⁴	010101	N/A (unchanged) ¹	unchanged ¹	
5.5x	100100	2.75x ⁴	110101 ²	N/A (unchanged) ¹	unchanged ¹	
6x	110100	3x ⁴	100000	N/A (unchanged) ¹	unchanged ¹	
6.5x	010100	3.25x ⁴	100000 ²	N/A (unchanged) ¹	unchanged ¹	
7x	001000	3.5x ⁴	110101	N/A (unchanged) ¹	unchanged ¹	
7.5x	000100	3.75x ⁴	110101 ²	N/A (unchanged) ¹	unchanged ¹	
8x	110000	4x ⁴	101000 ⁴	2x ⁴	010000	
8.5x	011000	4.25x ⁴	101000 ²	N/A (unchanged) ¹	unchanged ¹	
9x	011110	4.5x ⁴	011101	2.25x ⁴	010000 ²	
9.5x	011100	4.75x ⁴	011101 ²	N/A (unchanged) ¹	unchanged ¹	
10x	101010	5x	101100	2.5x ⁴	010101	
10.5x	100010	5.25x	101100 ²	N/A (unchanged) ¹	unchanged ¹	
11x	100110	5.5x	100100	2.75x ⁴	010101 ²	
11.5x	000000	5.75x	100100 ²	N/A (unchanged) ¹	unchanged ¹	
12x	101110	6x	110100	3x ⁴	100000	
12.5x	111110	6.25x	110100 ²	N/A (unchanged) ¹	unchanged ¹	
13x	010110	6.5x	010100	3.25x ⁴	100000 ²	
13.5x	111000	6.75	010100 ²	N/A (unchanged) ¹	unchanged ¹	
14x	110010	7x	001000	3.5x ⁴	110101	
15x	000110	7.5x	000100	3.75x ⁴	110101 ²	
16x	110110	8x	110000	4x ⁴	101000	
17x	000010	8.5x	011000	4.25x ⁴	101000 ²	
18x	001010	9x	011110	4.5x ⁴	011101	
20x	001110	10x	101010	5x	101100	
21x	010010	10.5x	100010	5.25x	101100 ²	

Table 16. Valid Divide Ratio Configurations



Document Revision History

Revision	Date	Substantive Change(s)
2		Table 6: Added separate input leakage specification for BVSEL0, <u>LSSD_MODE</u> , <u>TCK</u> , TDI, TMS, <u>TRST</u> signals to correctly indicate leakage current for signals with internal pull-up resistors.
		Section 5.1: Added paragraph preceding Table 7 and edited notes in Table 7 to clarify core frequencies at which power consumption is measured.
		Section 5.3: Removed voltage derating specifications; this feature has been made redundant by new device offerings and is no longer supported.
		Changed names of "Typical–Nominal" and "Typical–Thermal" power consumption parameters to "Typical" and "Thermal", respectively. (Name change only–no specifications were changed.)
		Table 11: Revised Notes 16, 18, and 19 to reflect current recommendations for connection of SENSE pins.
		Section 9.3: Added paragraph explaining connection recommendations for SENSE pins. (See also Table 11 entry above.)
		Table 19: Updated table to reflect changes in specifications for MC7448xxnnnnNC devices. Table 9: Changed all instances of TT[0:3] to TT[0:4]
		Removed mention of these input signals from output valid times and output hold times:
		• AACK, CKSTP_IN, DT[0:3]
		Figure 17: Modified diagram slightly to correctly snow constraint on SYSCLK ramping is related to V _{DD}
		Added Table 20 to reflect introduction of extended temperature devices and associated hardware
		specification addendum.
1		Added 1600 MHz, 1420 MHz, and 1000 MHz devices
		Section 4: corrected die size
		Table 2: Revised Note 4 to consider overshoot/undershoot and combined with Note 5.
		Table 4. Revised operating voltage for 1700 MHz device from \pm 50 mV to \pm 20 mV $/$ =50 mV.
		Table 11: Added voltage derating information for 1700 MHz devices: this feature is not supported at this
		time for other speed grades.
		Added transient specifications for VDD power supply in Section 9.2.3, added Table 15 and Figure 19 and renumbered subsequent tables and figures.
		Moved Decoupling Recommendations from Section 9.4 to Section 9.2.4 and renumbered subsequent sections.
		Section 9.2.1: Revised power sequencing requirements.
		Section 9.7.4: Added thermal diode ideality factor information (previously TBD).
		Table 17: Expanded table to show HID1 register values when DFS modes are enabled.
		Section 11.2: updated to include additional N-spec device speed grades
		Tables 18 and 19: corrected PVR values and added "MC" product code prefix
0		Initial public release.

Table 17. Document Revision History (continued)



11 Part Numbering and Marking

Ordering information for the part numbers fully covered by this specification document is provided in Section 11.1, "Part Numbers Fully Addressed by This Document." Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact a local Freescale sales office. In addition to the processor frequency, the part numbering scheme also includes an application modifier that may specify special application conditions. An optional specification modifier may also apply for parts to indicate a specific change in specifications, such as support for an extended temperature range. Finally, each part number contains a revision level code that refers to the die mask revision number. Section 11.2, "Part Numbers Not Fully Addressed by This Document," lists the part numbers that do not fully conform to the specifications of this document. These special part numbers require an additional document called a hardware specification addendum.

11.1 Part Numbers Fully Addressed by This Document

Table 18 provides the Freescale part numbering nomenclature for the MPC7448 part numbers fully addressed by this document. For information regarding other MPC7448 part numbers, see Section 11.2, "Part Numbers Not Fully Addressed by This Document."

XX	7448	XX	nnnn	L	X
Product Code	Part Identifier	Package	Processor Frequency	Application Modifier	Revision Level
MC PPC ¹	7448	HX = HCTE BGA VS = RoHS LGA VU = RoHS BGA	1700	L: 1.3 V +20/–50 mV 0 to 105 °C	C: 2.1; PVR = 0x8004_0201 D: 2.2; PVR = 0x8004_0202
			1600	L: 1.25 V ± 50 mV 0 to 105 °C	
			1420	L: 1.2 V ± 50 mV 0 to 105 °C	
			1000	L: 1.15 V ± 50 mV 0 to 105 °C	

Table 18. Part Numbering Nomenclature

Notes:

1. The P prefix in a Freescale part number designates a "Pilot Production Prototype" as defined by Freescale SOP 3-13. These parts have only preliminary reliability and characterization data. Before pilot production prototypes may be shipped, written authorization from the customer must be on file in the applicable sales office acknowledging the qualification status and the fact that product changes may still occur as pilot production prototypes are shipped.



Part Numbering and Marking

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11.2 Part Numbers Not Fully Addressed by This Document

Parts with application modifiers or revision levels not fully addressed in this specification document are described in separate hardware specification addenda which supplement and supersede this document. As such parts are released, these specifications will be listed in this section.

Table 19. Part Numbers Addressed by MC7448xxnnnnNx Series Hardware Specification Addendu	m
(Document Order No. MPC7448ECS01AD)	

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XX	7448	XX	nnnn	N	X
Product Code	Part Identifier	Package	Processor Frequency	Application Modifier	Revision Level
MC	7448	HX = HCTE BGA VS = RoHS LGA VU = RoHS BGA	1400	N: 1.15 V \pm 50 mV 0 to 105 °C (date code 0613 and later) ²	C: 2.1; PVR = 0x8004_0201 D: 2.2; PVR = 0x8004_0202
MC PPC ¹			1400	N: 1.1 V \pm 50 mV 0 to 105 °C (date code 0612 and prior) ²	
MC PPC ¹			1267 Revision C only	N: 1.1 V ± 50 mV 0 to 105 °C	
MC PPC ¹			1267 Revision D only	N: 1.05 V ± 50 mV 0 to 105 °C	
MC PPC ¹			1250	N: 1.1 V ± 50 mV 0 to 105 °C	
MC PPC ¹			1000 867 800 667 600	N: 1.0 V ± 50 mV 0 to 105 °C	

Notes:

- 1. The P prefix in a Freescale part number designates a "Pilot Production Prototype" as defined by Freescale SOP 3-13. These parts have only preliminary reliability and characterization data. Before pilot production prototypes can be shipped, written authorization from the customer must be on file in the applicable sales office acknowledging the qualification status and the fact that product changes may still occur as pilot production prototypes are shipped.
- Core voltage for 1400 MHz devices currently in production (date code of 0613 and later) is 1.15 V ± 50 mV; all such devices have the MC product code. The 1400 MHz devices with date code of 0612 and prior specified core voltage of 1.1 V ± 50 mV; this includes all 1400 MHz devices with the PPC product code. See Section 11.3, "Part Marking," for information on part marking.