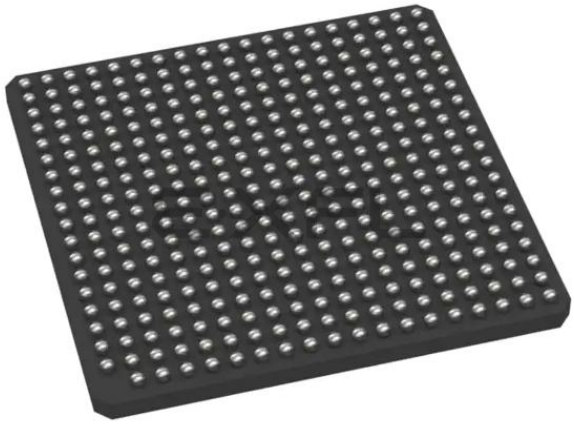

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC G4
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.4GHz
Co-Processors/DSP	Multimedia; SIMD
RAM Controllers	-
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	1.5V, 1.8V, 2.5V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	360-BCBGA, FCCBGA
Supplier Device Package	360-FCCBGA (25x25)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc7448hx1400nc

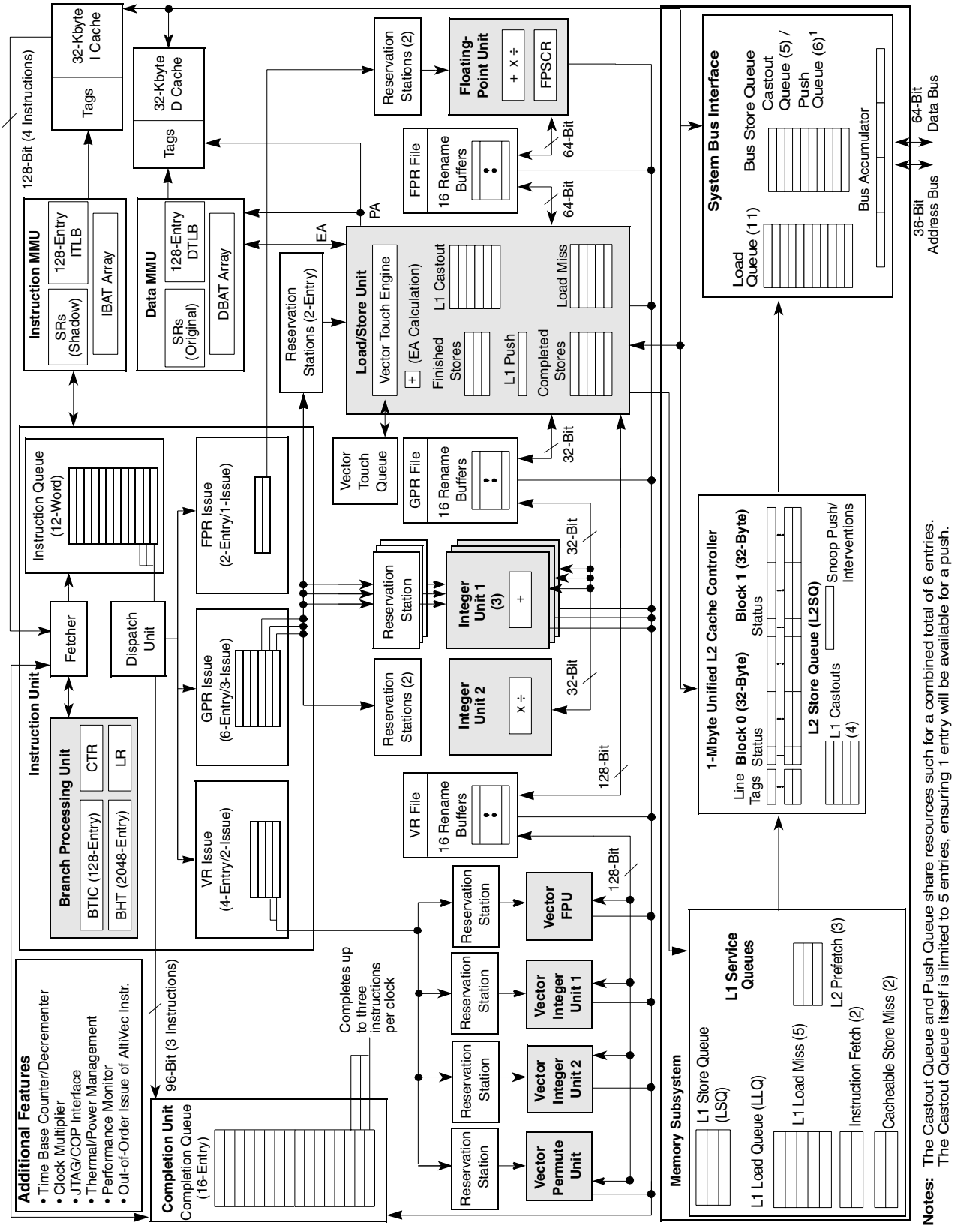


Figure 1. MPC7448 Block Diagram

  - Monitors all dispatched instructions and retires them in order
  - Tracks unresolved branches and flushes instructions after a mispredicted branch
  - Retires as many as three instructions per clock cycle
- Separate on-chip L1 instruction and data caches (Harvard architecture)
  - 32-Kbyte, eight-way set-associative instruction and data caches
  - Pseudo least-recently-used (PLRU) replacement algorithm
  - 32-byte (eight-word) L1 cache block
  - Physically indexed/physical tags
  - Cache write-back or write-through operation programmable on a per-page or per-block basis
  - Instruction cache can provide four instructions per clock cycle; data cache can provide four words per clock cycle
  - Caches can be disabled in software.
  - Caches can be locked in software.
  - MESI data cache coherency maintained in hardware
  - Separate copy of data cache tags for efficient snooping
  - Parity support on cache
  - No snooping of instruction cache except for **icbi** instruction
  - Data cache supports AltiVec LRU and transient instructions
  - Critical double- and/or quad-word forwarding is performed as needed. Critical quad-word forwarding is used for AltiVec loads and instruction fetches. Other accesses use critical double-word forwarding.
- Level 2 (L2) cache interface
  - On-chip, 1-Mbyte, eight-way set-associative unified instruction and data cache
  - Cache write-back or write-through operation programmable on a per-page or per-block basis
  - Parity support on cache tags
  - ECC or parity support on data
  - Error injection allows testing of error recovery software
- Separate memory management units (MMUs) for instructions and data
  - 52-bit virtual address, 32- or 36-bit physical address
  - Address translation for 4-Kbyte pages, variable-sized blocks, and 256-Mbyte segments
  - Memory programmable as write-back/write-through, caching-inhibited/caching-allowed, and memory coherency enforced/memory coherency not enforced on a page or block basis
  - Separate IBATs and DBATs (eight each) also defined as SPRs
  - Separate instruction and data translation lookaside buffers (TLBs)
    - Both TLBs are 128-entry, two-way set-associative and use an LRU replacement algorithm.
    - TLBs are hardware- or software-reloadable (that is, a page table search is performed in hardware or by system software on a TLB miss).

Table 1. Microarchitecture Comparison (continued)

Microarchitectural Specs	MPC7448	MPC7447A	MPC7447	MPC7445	MPC7441
Execution Unit Timings (Latency-Throughput)					
Aligned load (integer, float, vector)	3-1, 4-1, 3-1				
Misaligned load (integer, float, vector)	4-2, 5-2, 4-2				
L1 miss, L2 hit latency with ECC (data/instruction)	12/16	—			
L1 miss, L2 hit latency without ECC (data/instruction)	11/15	9/13			
SFX (add, sub, shift, rot, cmp, logicals)	1-1				
Integer multiply (32 × 8, 32 × 16, 32 × 32)	4-1, 4-1, 5-2				
Scalar float	5-1				
VSFX (vector simple)	1-1				
VCFX (vector complex)	4-1				
VFPU (vector float)	4-1				
VPER (vector permute)	2-1				
MMUs					
TLBs (instruction and data)	128-entry, 2-way				
Tablewalk mechanism	Hardware + software				
Instruction BATs/data BATs	8/8	8/8	8/8	8/8	4/4
L1 I Cache/D Cache Features					
Size	32K/32K				
Associativity	8-way				
Locking granularity	Way				
Parity on I cache	Word				
Parity on D cache	Byte				
Number of D cache misses (load/store)	5/2	5/1			
Data stream touch engines	4 streams				
On-Chip Cache Features					
Cache level	L2				
Size/associativity	1-Mbyte/ 8-way	512-Kbyte/8-way		256-Kbyte/8-way	
Access width	256 bits				
Number of 32-byte sectors/line	2	2			
Parity tag	Byte	Byte			
Parity data	Byte	Byte			
Data ECC	64-bit	—			
Thermal Control					
Dynamic frequency switching divide-by-two mode	Yes	Yes	No	No	No
Dynamic frequency switching divide-by-four mode	Yes	No	No	No	No
Thermal diode	Yes	Yes	No	No	No

Figure 2 shows the undershoot and overshoot voltage on the MPC7448.

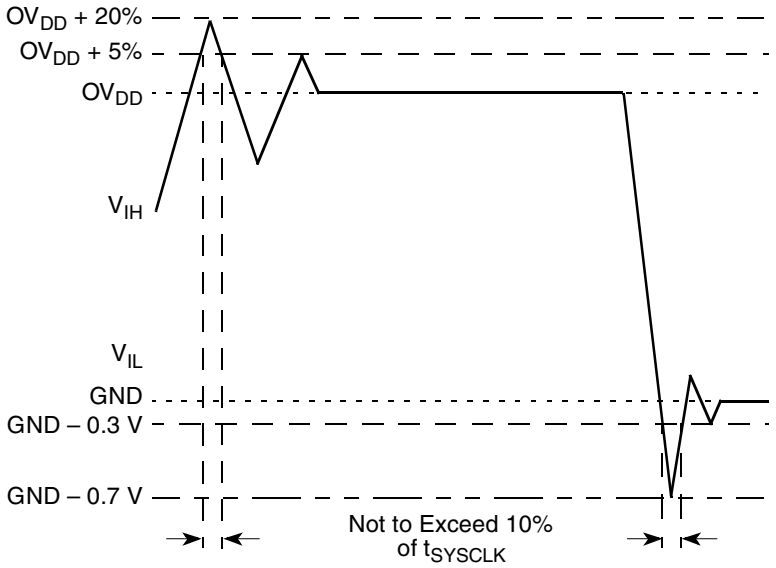


Figure 2. Overshoot/Undershoot Voltage

The MPC7448 provides several I/O voltages to support both compatibility with existing systems and migration to future systems. The MPC7448 core voltage must always be provided at the nominal voltage (see Table 4). The input voltage threshold for each bus is selected by sampling the state of the voltage select pins at the negation of the signal $\overline{\text{HRESET}}$. The output voltage will swing from GND to the maximum voltage applied to the OV_{DD} power pins. Table 3 provides the input threshold voltage settings. Because these settings may change in future products, it is recommended that BVSEL[0:1] be configured using resistor options, jumpers, or some other flexible means, with the capability to reconfigure the termination of this signal in the future, if necessary.

Table 3. Input Threshold Voltage Setting

BVSEL0	BVSEL1	I/O Voltage Mode[1]	Notes
0	0	1.8 V	2, 3
0	1	2.5 V	2, 4
1	0	1.5 V	2
1	1	2.5 V	4

Notes:

1. **Caution:** The I/O voltage mode selected must agree with the OV_{DD} voltages supplied. See Table 4.
2. If used, pull-down resistors should be less than 250 Ω.
3. The pin configuration used to select 1.8V mode on the MPC7448 is not compatible with the pin configuration used to select 1.8V mode on the MPC7447A and earlier devices.
4. The pin configuration used to select 2.5V mode on the MPC7448 is fully compatible with the pin configuration used to select 2.5V mode on the MPC7447A and earlier devices.

Table 5 provides the package thermal characteristics for the MPC7448. For more information regarding thermal management, see Section 9.7, "Power and Thermal Management Information."

Table 5. Package Thermal Characteristics[1]

Characteristic	Symbol	Value	Unit	Notes
Junction-to-ambient thermal resistance, natural convection, single-layer (1s) board	$R_{\theta JA}$	26	•C/W	2, 3
Junction-to-ambient thermal resistance, natural convection, four-layer (2s2p) board	$R_{\theta JMA}$	19	•C/W	2, 4
Junction-to-ambient thermal resistance, 200 ft/min airflow, single-layer (1s) board	$R_{\theta JMA}$	22	•C/W	2, 4
Junction-to-ambient thermal resistance, 200 ft/min airflow, four-layer (2s2p) board	$R_{\theta JMA}$	16	•C/W	2, 4
Junction-to-board thermal resistance	$R_{\theta JB}$	11	•C/W	5
Junction-to-case thermal resistance	$R_{\theta JC}$	< 0.1	•C/W	6

Notes:

1. Refer to Section 9.7, "Power and Thermal Management Information," for details about thermal management.
2. Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, airflow, power dissipation of other components on the board, and board thermal resistance.
3. Per JEDEC JESD51-2 with the single-layer board horizontal
4. Per JEDEC JESD51-6 with the board horizontal
5. Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
6. This is the thermal resistance between die and case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the calculated case temperature. The actual value of $R_{\theta JC}$ for the part is less than 0.1°C/W.

Table 6 provides the DC electrical characteristics for the MPC7448.

Table 6. DC Electrical Specifications

At recommended operating conditions. See Table 4.

Characteristic	Nominal Bus Voltage [1]	Symbol	Min	Max	Unit	Notes
Input high voltage (all inputs)	1.5	V_{IH}	$OV_{DD} \times 0.65$	$OV_{DD} + 0.3$	V	2
	1.8		$OV_{DD} \times 0.65$	$OV_{DD} + 0.3$		
	2.5		1.7	$OV_{DD} + 0.3$		
Input low voltage (all inputs)	1.5	V_{IL}	–0.3	$OV_{DD} \times 0.35$	V	2
	1.8		–0.3	$OV_{DD} \times 0.35$		
	2.5		–0.3	0.7		
Input leakage current, all signals except BVSEL0, LSSD_MODE, TCK, TDI, TMS, TRST: $V_{in} = OV_{DD}$ V_{in} = GND	—	I_{in}	—	 50 – 50	µA	2, 3
Input leakage current, BVSEL0, LSSD_MODE, TCK, TDI, TMS, TRST: $V_{in} = OV_{DD}$ V_{in} = GND	—	I_{in}	—	 50 – 2000	µA	2, 6

Table 8. Clock AC Timing Specifications

At recommended operating conditions. See Table 4.

Characteristic		Symbol	Maximum Processor Core Frequency (Speed Grade)								Unit	Notes
			1000 MHz		1420 MHz		1600 MHz		1700 MHz			
			Min	Max	Min	Max	Min	Max	Min	Max		
Processor core frequency	DFS mode disabled	f_{core}	600	1000	600	1420	600	1600	600	1700	MHz	1, 8
	DFS mode enabled	f_{core_DF}	300	500	300	710	300	800	300	850		9
VCO frequency		f_{VCO}	600	1000	600	1420	600	800	600	1700	MHz	1, 10
SYSCLK frequency		f_{SYSCLK}	33	200	33	200	33	200	33	200	MHz	1, 2, 8
SYSCLK cycle time		t_{SYSCLK}	5.0	30	5.0	30	5.0	30	5.0	30	ns	2
SYSCLK rise and fall time		t_{KR}, t_{KF}	—	0.5	—	0.5	—	0.5	—	0.5	ns	3
SYSCLK duty cycle measured at $OV_{DD}/2$		t_{KHKL}/t_{SYSCLK}	40	60	40	60	40	60	40	60	%	4
SYSCLK cycle-to-cycle jitter			—	150	—	150	—	150	—	150	ps	5, 6
Internal PLL relock time			—	100	—	100	—	100	—	100	µs	7

Notes:

1. **Caution**: The SYSCLK frequency and PLL_CFG[0:5] settings must be chosen such that the resulting SYSCLK (bus) frequency, processor core frequency, and PLL (VCO) frequency do not exceed their respective maximum or minimum operating frequencies. Refer to the PLL_CFG[0:5] signal description in Section 9.1.1, “PLL Configuration,” for valid PLL_CFG[0:5] settings.
2. Actual maximum system bus frequency is system-dependent. See Section 5.2.1, “Clock AC Specifications.”
3. Rise and fall times for the SYSCLK input measured from 0.4 to 1.4 V
4. Timing is guaranteed by design and characterization.
5. Guaranteed by design
6. The SYSCLK driver’s closed loop jitter bandwidth should be less than 1.5 MHz at –3 dB.
7. Relock timing is guaranteed by design and characterization. PLL-relock time is the maximum amount of time required for PLL lock after a stable V_{DD} and SYSCLK are reached during the power-on reset sequence. This specification also applies when the PLL has been disabled and subsequently re-enabled during sleep mode. Also note that $\overline{\text{HRESET}}$ must be held asserted for a minimum of 255 bus clocks after the PLL-relock time during the power-on reset sequence.
8. This reflects the maximum and minimum core frequencies when the dynamic frequency switching feature (DFS) is disabled. f_{core_DFS} provides the maximum and minimum core frequencies when operating in a DFS mode.
9. This specification supports the Dynamic Frequency Switching (DFS) feature and is applicable only when one of the DFS modes (divide-by-2 or divide-by-4) is enabled. When DFS is disabled, the core frequency must conform to the maximum and minimum frequencies stated for f_{core}.
10. Use of the DFS feature does not affect VCO frequency.

Figure 4 provides the AC test load for the MPC7448.

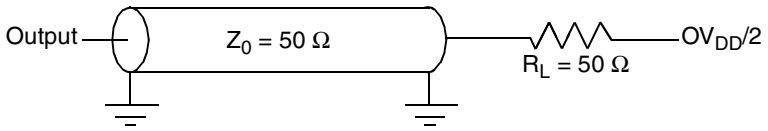


Figure 4. AC Test Load

Figure 5 provides the $\overline{\text{BMODE}}$[0:1] input timing diagram for the MPC7448. These mode select inputs are sampled once before and once after $\overline{\text{HRESET}}$ negation.

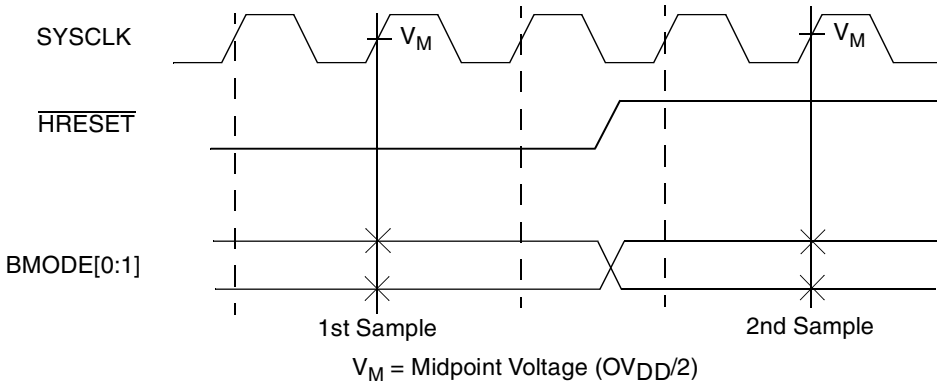


Figure 5. $\overline{\text{BMODE}}$[0:1] Input Sample Timing Diagram

Figure 7 provides the AC test load for TDO and the boundary-scan outputs of the MPC7448.

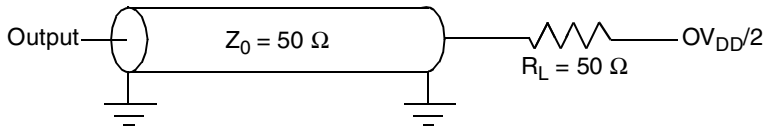


Figure 7. Alternate AC Test Load for the JTAG Interface

Figure 8 provides the JTAG clock input timing diagram.

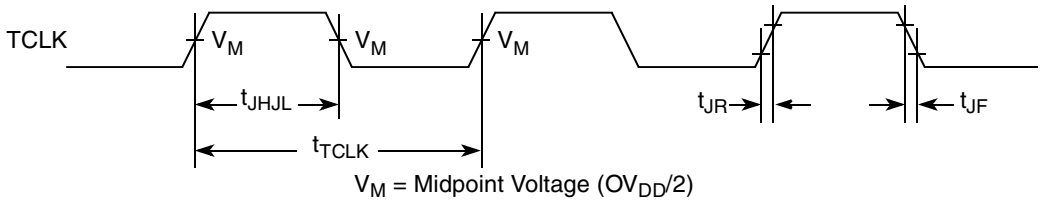


Figure 8. JTAG Clock Input Timing Diagram

Figure 9 provides the $\overline{\text{TRST}}$ timing diagram.

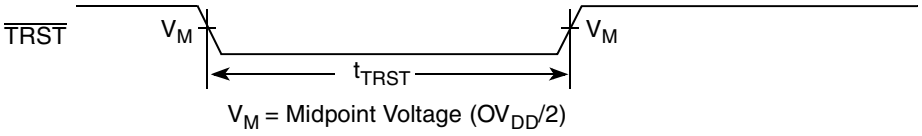


Figure 9. $\overline{\text{TRST}}$ Timing Diagram

Figure 10 provides the boundary-scan timing diagram.

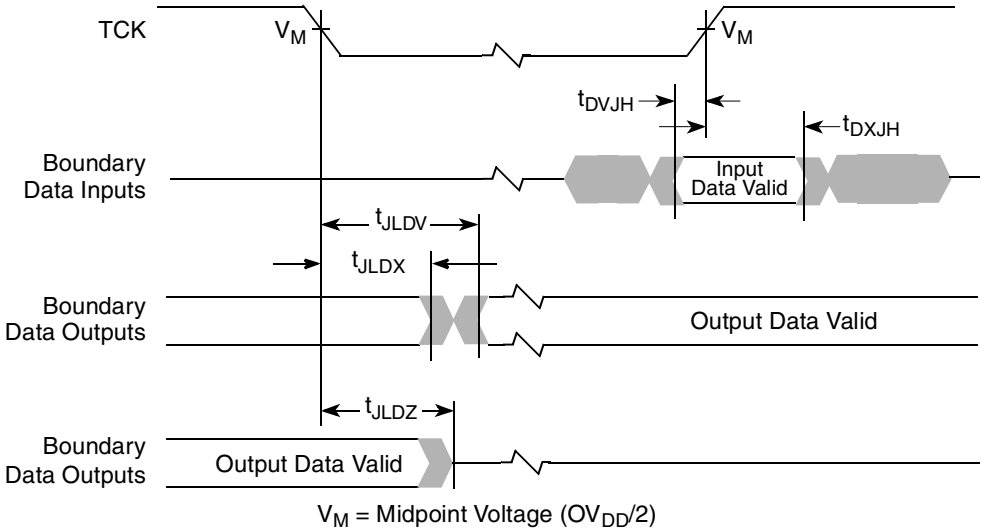


Figure 10. Boundary-Scan Timing Diagram

Figure 11 provides the test access port timing diagram.

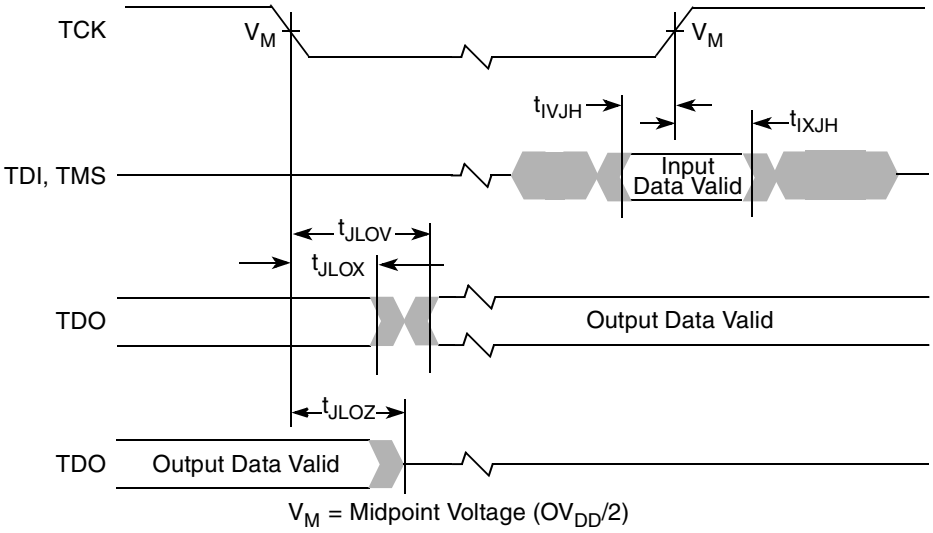


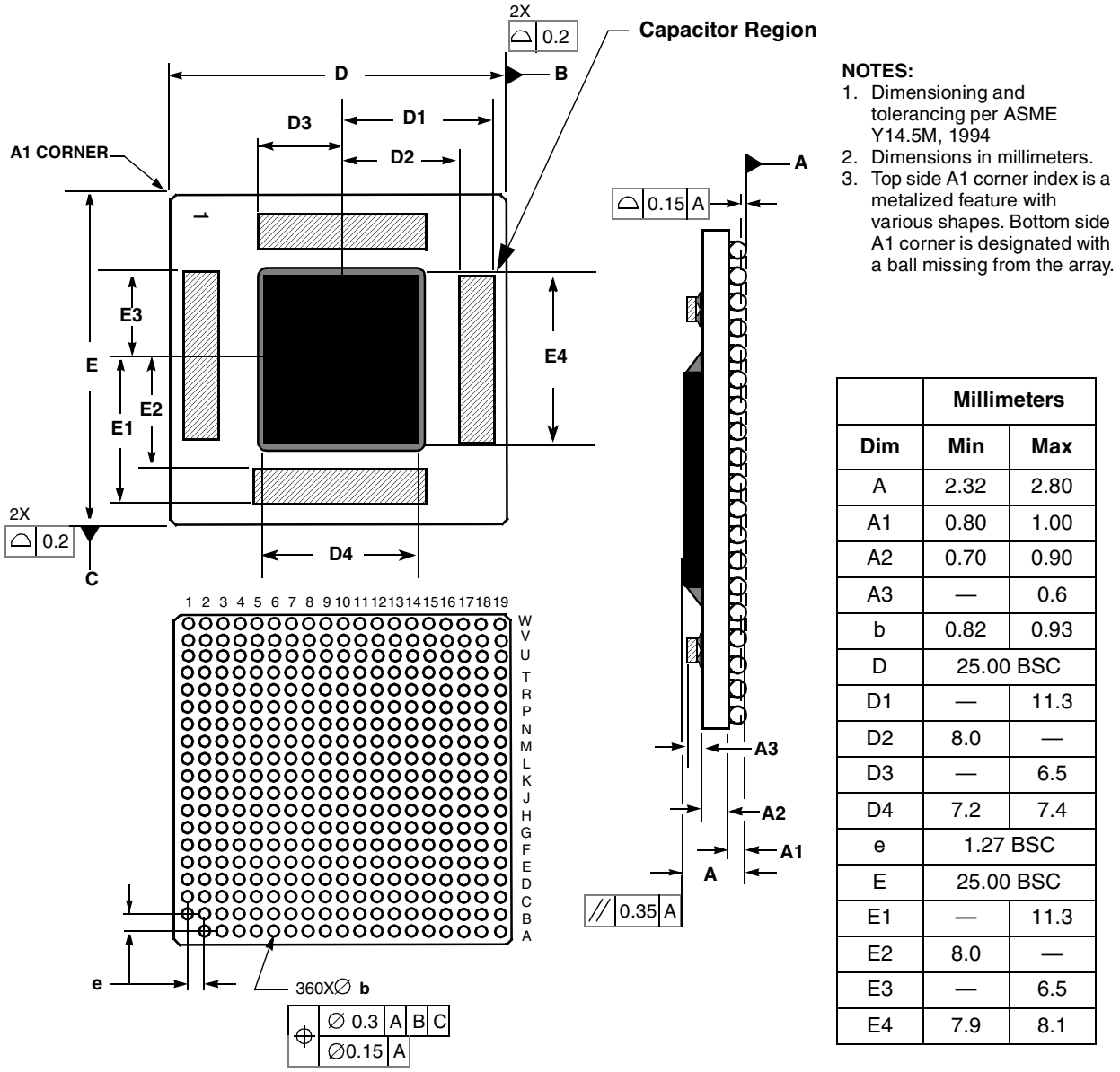
Figure 11. Test Access Port Timing Diagram

5.3 Voltage and Frequency Derating

Voltage and frequency derating is no longer supported for part numbers described by this document beginning with datecode 0613. (See Section 11, “Part Numbering and Marking,” for information on date code markings.) It is supported by some MPC7448 part numbers which target low-power applications; see Section 11.2, “Part Numbers Not Fully Addressed by This Document” and the referenced MPC7448 Hardware Specification Addenda for more information on these low-power devices. For those devices which previously supported this feature, information has been archived in the *Chip Errata for the MPC7448* (document order no. MPC7448CE).

8.2 Mechanical Dimensions for the MPC7448, 360 HCTE BGA

Figure 13 provides the mechanical dimensions and bottom surface nomenclature for the MPC7448, 360 HCTE BGA package.



NOTES:
1. Dimensioning and tolerancing per ASME Y14.5M, 1994
2. Dimensions in millimeters.
3. Top side A1 corner index is a metalized feature with various shapes. Bottom side A1 corner is designated with a ball missing from the array.

	Millimeters	
Dim	Min	Max
A	2.32	2.80
A1	0.80	1.00
A2	0.70	0.90
A3	—	0.6
b	0.82	0.93
D	25.00 BSC	
D1	—	11.3
D2	8.0	—
D3	—	6.5
D4	7.2	7.4
e	1.27 BSC	
E	25.00 BSC	
E1	—	11.3
E2	8.0	—
E3	—	6.5
E4	7.9	8.1

Figure 13. Mechanical Dimensions and Bottom Surface Nomenclature for the MPC7448, 360 HCTE BGA Package

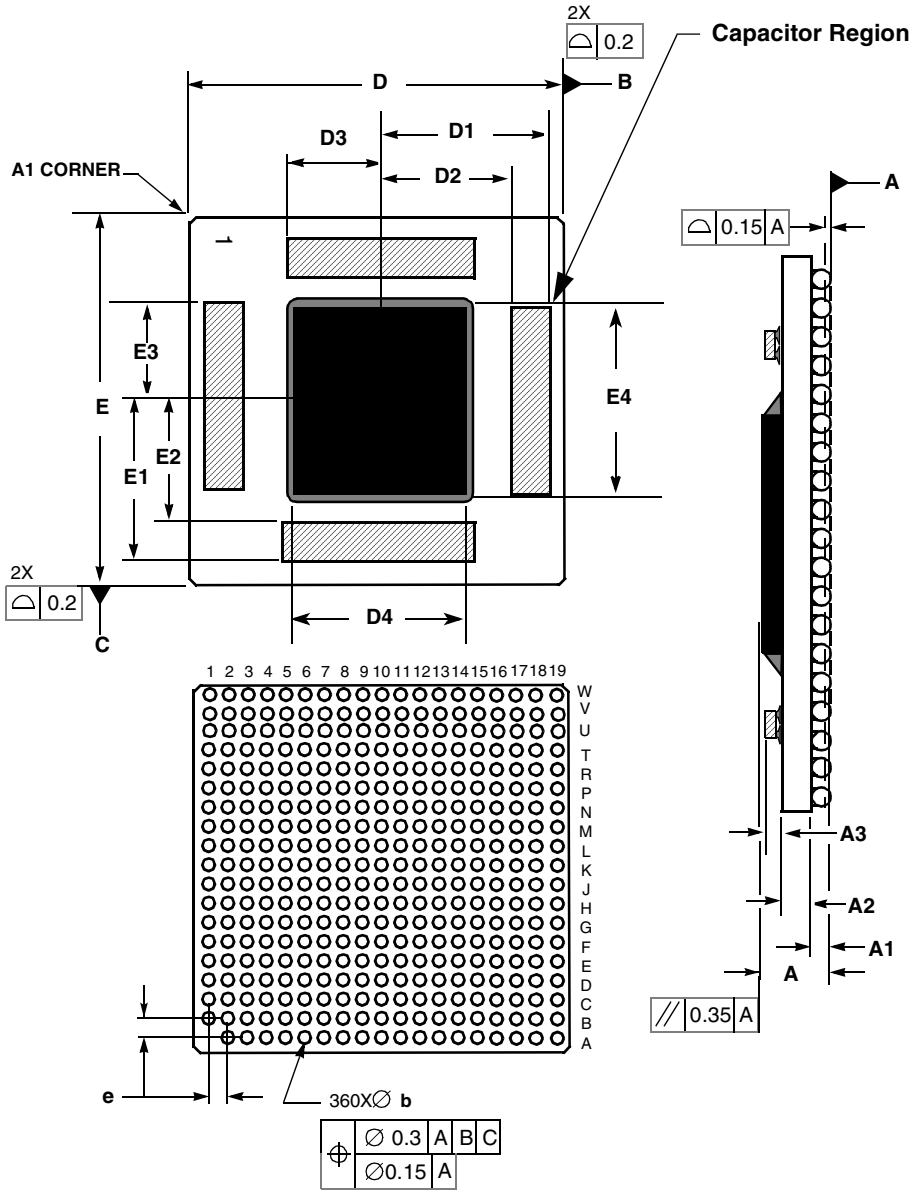
8.5 Package Parameters for the MPC7448, 360 HCTE RoHS-Compliant BGA

The package parameters are as provided in the following list. The package type is 25 × 25 mm, 360-lead high coefficient of thermal expansion ceramic ball grid array (HCTE) with RoHS-compliant lead-free spheres.

Package outline	25 × 25 mm
Interconnects	360 (19 × 19 ball array – 1)
Pitch	1.27 mm (50 mil)
Minimum module height	1.92 mm
Maximum module height	2.40 mm
Ball diameter	0.75 mm (30 mil)
Coefficient of thermal expansion	12.3 ppm/°C

8.6 Mechanical Dimensions for the MPC7448, 360 HCTE RoHS-Compliant BGA

Figure 13 provides the mechanical dimensions and bottom surface nomenclature for the MPC7448, 360 HCTE BGA package with RoHS-compliant lead-free spheres.



NOTES:
1. Dimensioning and tolerancing per ASME Y14.5M, 1994
2. Dimensions in millimeters.
3. Top side A1 corner index is a metalized feature with various shapes. Bottom side A1 corner is designated with a ball missing from the array.
4. Dimension A1 represents the collapsed sphere diameter.

	Millimeters	
Dim	**Min**	**Max**
A	1.92	2.40
A1 [4]	0.40	0.60
A2	0.70	0.90
A3	—	0.6
b	0.60	0.90
D	25.00 BSC	
D1	—	11.3
D2	8.0	—
D3	—	6.5
D4	7.2	7.4
e	1.27 BSC	
E	25.00 BSC	
E1	—	11.3
E2	8.0	—
E3	—	6.5
E4	7.9	8.1

Figure 15. Mechanical Dimensions and Bottom Surface Nomenclature for the MPC7448, 360 HCTE RoHS-Compliant BGA Package

9 System Design Information

This section provides system and thermal design requirements and recommendations for successful application of the MPC7448.

9.1 Clocks

The following sections provide more detailed information regarding the clocking of the MPC7448.

9.1.1 PLL Configuration

The MPC7448 PLL is configured by the PLL_CFG[0:5] signals. For a given SYSCLK (bus) frequency, the PLL configuration signals set the internal CPU and VCO frequency of operation. The PLL configuration for the MPC7448 is shown in Table 12. In this example, shaded cells represent settings that, for a given SYSCLK frequency, result in core and/or VCO frequencies that do not comply with Table 8. When enabled, dynamic frequency switching (DFS) also affects the core frequency by halving or quartering the bus-to-core multiplier; see Section 9.7.5, "Dynamic Frequency Switching (DFS)," for more information. Note that when DFS is enabled the resulting core frequency must meet the adjusted minimum core frequency requirements (f_{core_DFS}) described in Table 8. Note that the PLL_CFG[5] is currently used for factory test only and should be tied low, and that the MPC7448 PLL configuration settings are compatible with the MPC7447A PLL configuration settings when PLL_CFG[5] = 0.

Table 12. MPC7448 Microprocessor PLL Configuration Example

PLL_CFG[0:5]	Example Core and VCO Frequency in MHz									
	Bus-to-Core Multiplier [5]	Core-to-VCO Multiplier [5]	Bus (SYSCLK) Frequency							
			33.3 MHz	50 MHz	66.6 MHz	75 MHz	83 MHz	100 MHz	133 MHz	167 MHz	200 MHz
010000	2x [6]	1x									
100000	3x [6]	1x									600
101000	4x [6]	1x								667	800
101100	5x	1x							667	835	1000
100100	5.5x	1x							733	919	1100
110100	6x	1x						600	800	1002	1200
010100	6.5x	1x						650	866	1086	1300
001000	7x	1x						700	931	1169	1400
000100	7.5x	1x					623	750	1000	1253	1500
110000	8x	1x				600	664	800	1064	1336	1600
011000	8.5x	1x				638	706	850	1131	1417	1700
011110	9x	1x			600	675	747	900	1197	1500	
011100	9.5x	1x			633	712	789	950	1264	1583	
101010	10x	1x			667	750	830	1000	1333	1667	
100010	10.5x	1x			700	938	872	1050	1397		

These requirements are shown graphically in Figure 16.

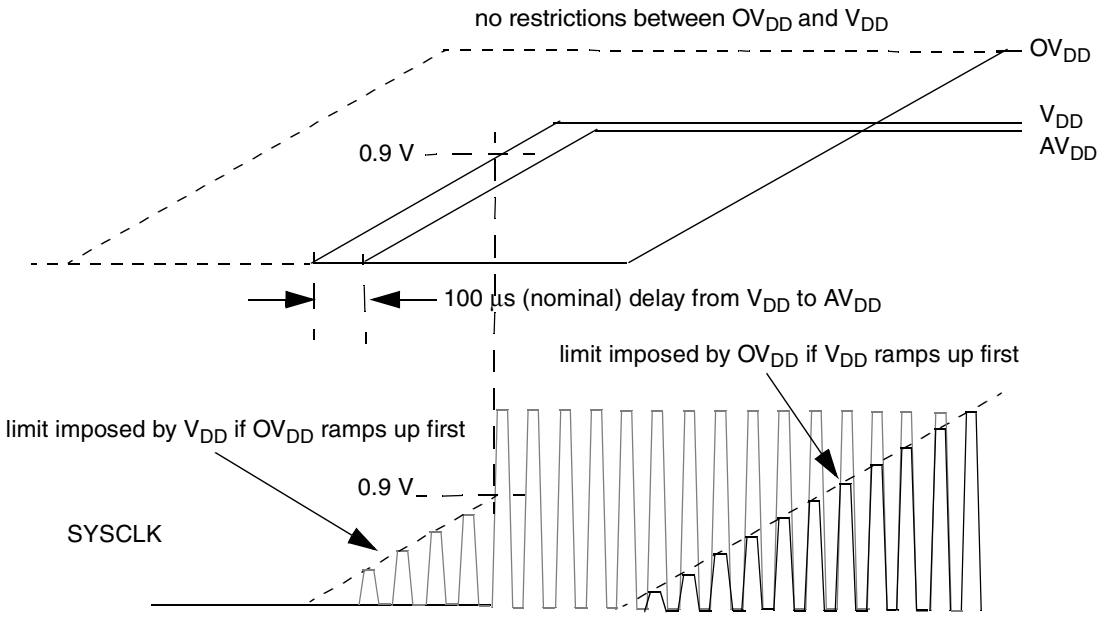


Figure 16. MPC7448 Power Up Sequencing Requirements

Certain stipulations also apply to the manner in which the power rails of the MPC7448 power down, as follows:

- OV_{DD} may ramp down any time before or after V_{DD}.
- The voltage at the SYSCLK input must not exceed V_{DD} once V_{DD} has ramped down below 0.9 V.
- The voltage at the SYSCLK input must not exceed OV_{DD} by more 20% during transients (see overshoot/undershoot specifications in Figure 2) or 0.3 V DC (see Table 2) at any time.

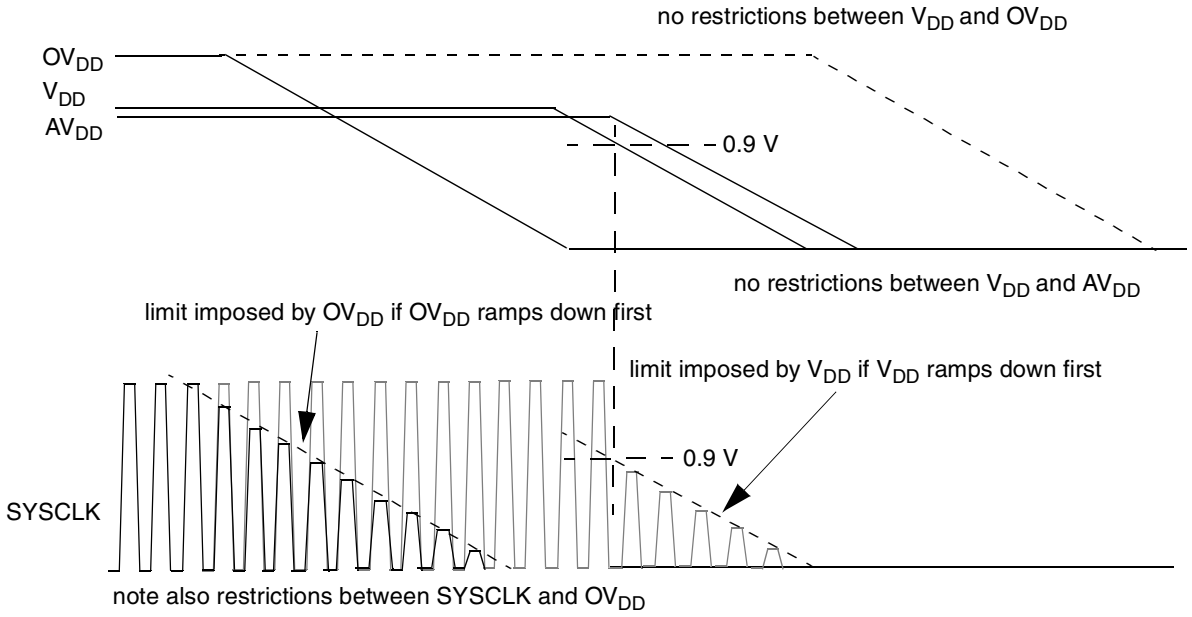


Figure 17. MPC7448 Power Down Sequencing Requirements

There is no requirement regarding AV_{DD} during power down, but it is recommended that AV_{DD} track V_{DD} within the RC time constant of the PLL filter circuit described in Section 9.2.2, "PLL Power Supply Filtering" (nominally 100 µs).

9.2.2 PLL Power Supply Filtering

The AV_{DD} power signal is provided on the MPC7448 to provide power to the clock generation PLL. To ensure stability of the internal clock, the power supplied to the AV_{DD} input signal should be filtered of any noise in the 500-KHz to 10-MHz resonant frequency range of the PLL. The circuit shown in Figure 18 using surface mount capacitors with minimum effective series inductance (ESL) is strongly recommended. In addition to filtering noise from the AV_{DD} input, it also provides the required delay between V_{DD} and AV_{DD} as described in Section 9.2.1, "Power Supply Sequencing."

The circuit should be placed as close as possible to the AV_{DD} pin to minimize noise coupled from nearby circuits. It is often possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of the device footprint.

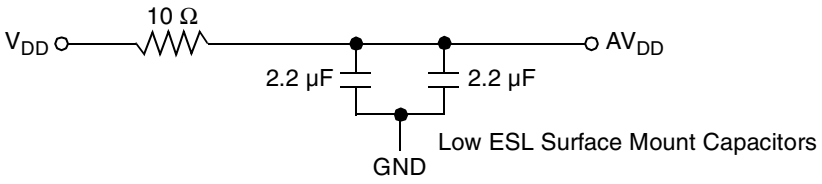


Figure 18. PLL Power Supply Filter Circuit

9.2.3 Transient Specifications

The ensure the long-term reliability of the device, the MPC7448 requires that transients on the core power rail (V_{DD}) be constrained. The recommended operating voltage specifications provided in Table 4 are DC specifications. That is, the device may be operated continuously with V_{DD} within the specified range without adversely affecting the device's reliability. Excursions above the stated recommended operation range, including overshoot during power-up, can impact the long-term reliability of the device. Excursions are described by their amplitude and duration. Duration is defined as the time period during which the V_{DD} power plane, as measured at the VDD_SENSE pins, will be within a specific voltage range, expressed as percentage of the total time the device will be powered up over the device lifetime. In practice, the period over which transients are measured can be any arbitrary period of time that accurately represents the expected range of processor and system activity. The voltage ranges and durations for normal operation and transients are described in Table 14.

Table 14. VDD Power Supply Transient Specifications

At recommended operating temperatures. See Table 4.

Voltage Region	Voltage Range (V)		Permitted Duration [1]	Notes
	Min	Max		
Normal	V_{DD} minimum	V_{DD} maximum	100%	2
Low Transient	V_{DD} maximum	1.35 V	10%	2, 3
High Transient	1.35 V	1.40 V	0.2%	4

Notes:
1. Permitted duration is defined as the percentage of the total time the device is powered on that the V_{DD} power supply voltage may exist within the specified voltage range.
2. See Table 4 for nominal V_{DD} specifications.
3. To simplify measurement, excursions into the High Transient region are included in this duration.
4. Excursions above the absolute maximum rating of 1.4 V are not permitted; see Table 2.

Note that, to simplify transient measurements, the duration of the excursion into the High Transient region is also included in the Low Transient duration, so that only the time the voltage is above each threshold must be considered. Figure 19 shows an example of measuring voltage transients.

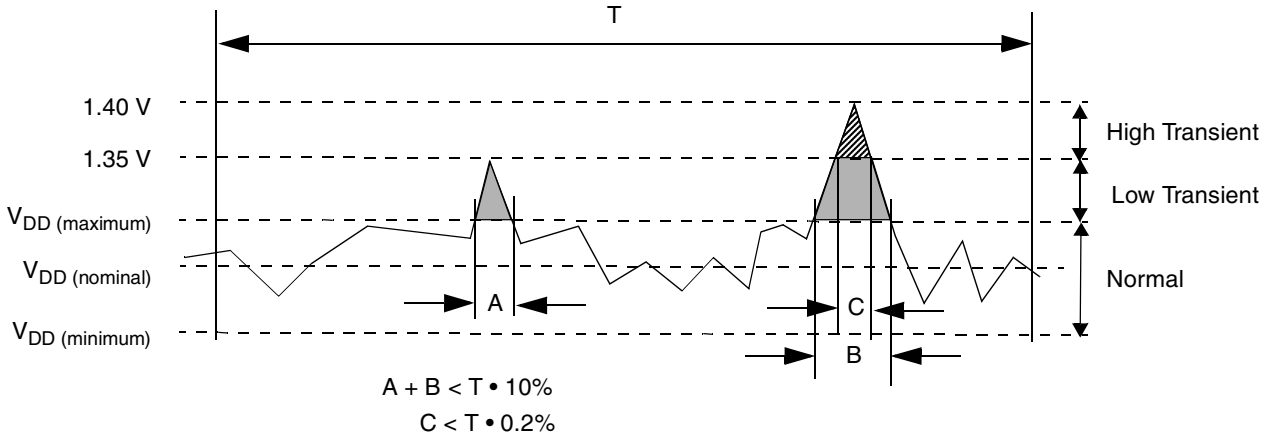


Figure 19. Voltage Transient Example

9.7 Power and Thermal Management Information

This section provides thermal management information for the high coefficient of thermal expansion (HCTE) package for air-cooled applications. Proper thermal control design is primarily dependent on the system-level design—the heat sink, airflow, and thermal interface material. The MPC7448 implements several features designed to assist with thermal management, including DFS and the temperature diode. DFS reduces the power consumption of the device by reducing the core frequency; see Section 9.7.5.1, "Power Consumption with DFS Enabled," for specific information regarding power reduction and DFS. The temperature diode allows an external device to monitor the die temperature in order to detect excessive temperature conditions and alert the system; see Section 9.7.4, "Temperature Diode," for more information.

To reduce the die-junction temperature, heat sinks may be attached to the package by several methods—spring clip to holes in the printed-circuit board or package, and mounting clip and screw assembly (see Figure 22); however, due to the potential large mass of the heat sink, attachment through the printed-circuit board is suggested. In any implementation of a heat sink solution, the force on the die should not exceed ten pounds (45 Newtons).

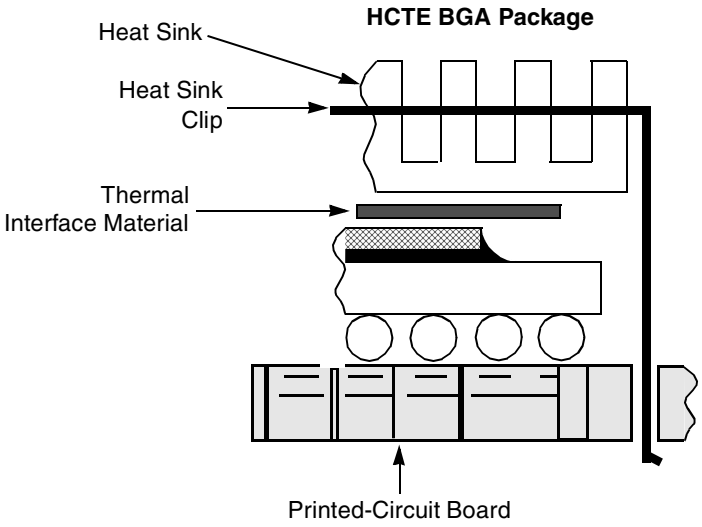


Figure 22. BGA Package Exploded Cross-Sectional View with Several Heat Sink Options

NOTE

A clip on heat sink is not recommended for LGA because there may not be adequate clearance between the device and the circuit board. A through-hole solution is recommended, as shown in Figure 23.

Due to the complexity and variety of system-level boundary conditions for today's microelectronic equipment, the combined effects of the heat transfer mechanisms (radiation, convection, and conduction) may vary widely. For these reasons, we recommend using conjugate heat transfer models for the board as well as system-level designs.

For system thermal modeling, the MPC7448 thermal model is shown in Figure 26. Four volumes represent this device. Two of the volumes, solder ball-air and substrate, are modeled using the package outline size of the package. The other two, die and bump-underfill, have the same size as the die. The silicon die should be modeled $8.0 \times 7.3 \times 0.86$ mm^3 with the heat source applied as a uniform source at the bottom of the volume. The bump and underfill layer is modeled as $8.0 \times 7.3 \times 0.07$ mm^{3}collapsed in the z-direction with a thermal conductivity of 5.0 W/(m • K) in the z-direction. The substrate volume is $25 \times 25 \times 1.14$ mm^3 and has 9.9 W/(m • K) isotropic conductivity in the xy-plane and 2.95 W/(m • K) in the direction of the z-axis. The solder ball and air layer are modeled with the same horizontal dimensions as the substrate and is 0.8 mm thick. For the LGA package the solder and air layer is 0.1 mm thick, but the material properties are the same. It can also be modeled as a collapsed volume using orthotropic material properties: 0.034 W/(m • K) in the xy-plane direction and 11.2 W/(m • K) in the direction of the z-axis.

Conductivity	Value	Unit
Die ($8.0 \times 7.3 \times 0.86$ mm^3)		
Silicon	Temperature-dependent	W/(m • K)
Bump and Underfill ($8.0 \times 7.3 \times 0.07$ mm^3)		
k_z	5.0	W/(m • K)
Substrate ($25 \times 25 \times 1.14$ mm^3)		
k_x	9.9	W/(m • K)
k_y	9.9	
k_z	2.95	
Solder Ball and Air ($25 \times 25 \times 0.8$ mm^3)		
k_x	0.034	W/(m • K)
k_y	0.034	
k_z	11.2	

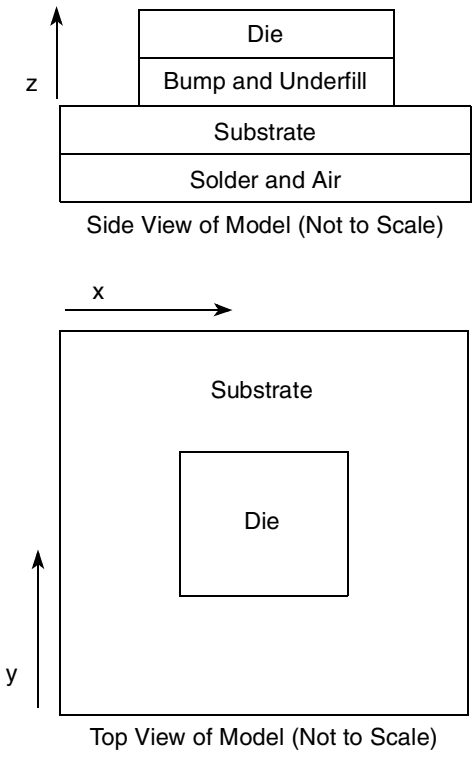


Figure 26. Recommended Thermal Model of MPC7448

Table 16. Valid Divide Ratio Configurations (continued)

DFS mode disabled		DFS divide-by-2 mode enabled (HID1[DFS2] = 1 or $\overline{\text{DFS2}}$ = 0)		DFS divide-by-4 mode enabled (HID1[DFS4] = 1 or $\overline{\text{DFS4}}$ = 0)	
Bus-to-Core Multiplier Configured by PLL_CFG[0:5] (see Table 12)	HID1[PC0-5] [3]	Bus-to-Core Multiplier	HID1[PC0-5] [3]	Bus-to-Core Multiplier	HID1[PC0-5] [3]
24x	011010	12x	101110	6x	110100
28x	111010	14x	110010	7x	001000

Notes:
1. DFS mode is not supported for this combination of DFS mode and PLL_CFG[0:5] setting. As a result, the processor will ignore these settings and remain at the previous multiplier, as reflected by the HID1[PC0-PC5] bits.
2. Though supported by the MPC7448 clock circuitry, multipliers of *n*.25x and *n*.75x cannot be expressed as valid PLL configuration codes. As a result, the values displayed in HID1[PC0-PC5] are rounded down to the nearest valid PLL configuration code. However, the actual bus-to-core multiplier is as stated in this table.
3. Note that in the HID1 register of the MPC7448, the PC0, PC1, PC2, PC3, PC4, and PC5 bits are bits 15, 16, 17, 18, 19, and 14 (respectively). See the *MPC7450 RISC Microprocessor Reference Manual* for more information.
4. Special considerations regarding snooped transactions must be observed for bus-to-core multipliers less than 5x. See the *MPC7450 RISC Microprocessor Reference Manual* for more information.

9.7.5.3 Minimum Core Frequency Requirements with DFS

In many systems, enabling DFS can result in very low processor core frequencies. However, care must be taken to ensure that the resulting processor core frequency is within the limits specified in Table 8. Proper operation of the device is not guaranteed at core frequencies below the specified minimum f_{core}.

10 Document Revision History

Table 17 provides a revision history for this hardware specification.

Table 17. Document Revision History

Revision	Date	Substantive Change(s)
4	3/2007	Table 19: Added 800 MHz processor frequency.
3	10/2006	Section 9.7, “Power and Thermal Management Information”: Updated contact information. Table 18, Table 20, and Table 19: Added Revision D PVR. Table 19: Added 600 processor frequency, additional product codes, date codes for 1400 processor frequency, and footnotes 1 and 2. Table 20: Added PPC product code and footnote 1. Table 19 and Table 20: Added Revision D information for 1267 processor frequency.

11.2 Part Numbers Not Fully Addressed by This Document

Parts with application modifiers or revision levels not fully addressed in this specification document are described in separate hardware specification addenda which supplement and supersede this document. As such parts are released, these specifications will be listed in this section.

Table 19. Part Numbers Addressed by MC7448*xxnnnn*N*x* Series Hardware Specification Addendum (Document Order No. MPC7448ECS01AD)

xx	**7448**	***xx***	***nnnn***	**N**	***x***
Product Code	**Part Identifier**	**Package**	**Processor Frequency**	**Application Modifier**	**Revision Level**
MC	7448	HX = HCTE BGA VS = RoHS LGA VU = RoHS BGA	1400	N: 1.15 V ± 50 mV 0 to 105 °C (date code 0613 and later) [2]	C: 2.1; PVR = 0x8004_0201 D: 2.2; PVR = 0x8004_0202
MC PPC[1]			1400	N: 1.1 V ± 50 mV 0 to 105 °C (date code 0612 and prior) [2]	
MC PPC[1]			1267 Revision C only	N: 1.1 V ± 50 mV 0 to 105 °C	
MC PPC[1]			1267 Revision D only	N: 1.05 V ± 50 mV 0 to 105 °C	
MC PPC[1]			1250	N: 1.1 V ± 50 mV 0 to 105 °C	
MC PPC[1]			1000 867 800 667 600	N: 1.0 V ± 50 mV 0 to 105 °C	

Notes:

1. The P prefix in a Freescale part number designates a “Pilot Production Prototype” as defined by Freescale SOP 3-13. These parts have only preliminary reliability and characterization data. Before pilot production prototypes can be shipped, written authorization from the customer must be on file in the applicable sales office acknowledging the qualification status and the fact that product changes may still occur as pilot production prototypes are shipped.
2. Core voltage for 1400 MHz devices currently in production (date code of 0613 and later) is 1.15 V ± 50 mV; all such devices have the MC product code. The 1400 MHz devices with date code of 0612 and prior specified core voltage of 1.1 V ± 50 mV; this includes all 1400 MHz devices with the PPC product code. See Section 11.3, “Part Marking,” for information on part marking.