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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC G4
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.42GHz
Co-Processors/DSP	Multimedia; SIMD
RAM Controllers	-
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	1.5V, 1.8V, 2.5V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	360-BCBGA, FCCBGA
Supplier Device Package	360-FCCBGA (25x25)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc7448hx1420lc

- Efficient data flow
  - Although the VR/LSU interface is 128 bits, the L1/L2 bus interface allows up to 256 bits.
  - The L1 data cache is fully pipelined to provide 128 bits/cycle to or from the VRs.
  - The L2 cache is fully pipelined to provide 32 bytes per clock every other cycle to the L1 caches.
  - As many as 16 out-of-order transactions can be present on the MPX bus.
  - Store merging for multiple store misses to the same line. Only coherency action taken (address-only) for store misses merged to all 32 bytes of a cache block (no data tenure needed).
  - Three-entry finished store queue and five-entry completed store queue between the LSU and the L1 data cache
  - Separate additional queues for efficient buffering of outbound data (such as castouts and write-through stores) from the L1 data cache and L2 cache
- Multiprocessing support features include the following:
  - Hardware-enforced, MESI cache coherency protocols for data cache
  - Load/store with reservation instruction pair for atomic memory references, semaphores, and other multiprocessor operations
- Power and thermal management
  - Dynamic frequency switching (DFS) feature allows processor core frequency to be halved or quartered through software to reduce power consumption.
  - The following three power-saving modes are available to the system:
    - Nap—Instruction fetching is halted. Only the clocks for the time base, decrementer, and JTAG logic remain running. The part goes into the doze state to snoop memory operations on the bus and then back to nap using a $\overline{\text{QREQ}}$/$\overline{\text{QACK}}$ processor-system handshake protocol.
    - Sleep—Power consumption is further reduced by disabling bus snooping, leaving only the PLL in a locked and running state. All internal functional units are disabled.
    - Deep sleep—When the part is in the sleep state, the system can disable the PLL. The system can then disable the SYSCLK source for greater system power savings. Power-on reset procedures for restarting and relocking the PLL must be followed upon exiting the deep sleep state.
  - Instruction cache throttling provides control of instruction fetching to limit device temperature.
  - A new temperature diode that can determine the temperature of the microprocessor
- Performance monitor can be used to help debug system designs and improve software efficiency.
- In-system testability and debugging features through JTAG boundary-scan capability
- Testability
  - LSSD scan design
  - IEEE Std. 1149.1™ JTAG interface

4 General Parameters

The following list summarizes the general parameters of the MPC7448:

Technology	90 nm CMOS SOI, nine-layer metal	
Die size	8.0 mm × 7.3 mm	
Transistor count	90 million	
Logic design	Mixed static and dynamic	
Packages	Surface mount 360 ceramic ball grid array (HCTE)	
	Surface mount 360 ceramic land grid array (HCTE)	
	Surface mount 360 ceramic ball grid array with lead-free spheres (HCTE)	
Core power supply	1.30 V	(1700 MHz device)
	1.25 V	(1600 MHz device)
	1.20 V	(1420 MHz device)
	1.15 V	(1000 MHz device)
I/O power supply	1.5 V, 1.8 V, or 2.5 V	

5 Electrical and Thermal Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC7448.

5.1 DC Electrical Characteristics

The tables in this section describe the MPC7448 DC electrical characteristics. Table 2 provides the absolute maximum ratings. See Section 9.2, “Power Supply Design and Sequencing,” for power sequencing requirements.

Table 2. Absolute Maximum Ratings [1]

Characteristic		Symbol	Maximum Value	Unit	Notes
Core supply voltage		V_{DD}	–0.3 to 1.4	V	2
PLL supply voltage		AV_{DD}	–0.3 to 1.4	V	2
Processor bus supply voltage	I/O Voltage Mode = 1.5 V	OV_{DD}	–0.3 to 1.8	V	3
	I/O Voltage Mode = 1.8 V		–0.3 to 2.2		3
	I/O Voltage Mode = 2.5 V		–0.3 to 3.0		3
Input voltage	Processor bus	V_{in}	–0.3 to OV_{DD} + 0.3	V	4
	JTAG signals	V_{in}	–0.3 to OV_{DD} + 0.3	V	
Storage temperature range		T_{stg}	– 55 to 150	•C	

Notes:

1. Functional and tested operating conditions are given in Table 4. Absolute maximum ratings are stress ratings only and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. See Section 9.2, “Power Supply Design and Sequencing” for power sequencing requirements.
3. Bus must be configured in the corresponding I/O voltage mode; see Table 3.
4. **Caution**: V_{in} must not exceed OV_{DD} by more than 0.3 V at any time including during power-on reset except as allowed by the overshoot specifications. V_{in} may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 2.

Table 9. Processor Bus AC Timing Specifications[1] (continued)

At recommended operating conditions. See Table 4.

Parameter	Symbol [2]	All Speed Grades		Unit	Notes
		Min	Max		
SYSCLK to output high impedance (all except $\overline{TS}$, $\overline{ARTRY}$, $\overline{SHD0}$, $\overline{SHD1}$)	t_{KHOZ}	—	1.8	ns	5
SYSCLK to $\overline{TS}$ high impedance after precharge	t_{KHTSPZ}	—	1	t_{SYSCLK}	3, 4, 5
Maximum delay to $\overline{ARTRY}$/$\overline{SHD0}$/$\overline{SHD1}$ precharge	t_{KHARP}	—	1	t_{SYSCLK}	3, 5, 6, 7
SYSCLK to $\overline{ARTRY}$/$\overline{SHD0}$/$\overline{SHD1}$ high impedance after precharge	t_{KHARPZ}	—	2	t_{SYSCLK}	3, 5, 6, 7

Notes:

1. All input specifications are measured from the midpoint of the signal in question to the midpoint of the rising edge of the input SYSCLK. All output specifications are measured from the midpoint of the rising edge of SYSCLK to the midpoint of the signal in question. All output timings assume a purely resistive 50-Ω load (see Figure 4). Input and output timings are measured at the pin; time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. The symbology used for timing specifications herein follows the pattern of $t_{(signal)(state)(reference)(state)}$ for inputs and $t_{(reference)(state)(signal)(state)}$ for outputs. For example, t_{IVKH} symbolizes the time input signals (I) reach the valid state (V) relative to the SYSCLK reference (K) going to the high (H) state or input setup time. And t_{KHOV} symbolizes the time from SYSCLK(K) going high (H) until outputs (O) are valid (V) or output valid time. Input hold time can be read as the time that the input signal (I) went invalid (X) with respect to the rising clock edge (KH) (note the position of the reference and its state for inputs) and output hold time can be read as the time from the rising edge (KH) until the output went invalid (OX).
3. t_{sysclk} is the period of the external clock (SYSCLK) in ns. The numbers given in the table must be multiplied by the period of SYSCLK to compute the actual time duration (in ns) of the parameter in question.
4. According to the bus protocol, $\overline{TS}$ is driven only by the currently active bus master. It is asserted low and precharged high before returning to high impedance, as shown in Figure 6. The nominal precharge width for $\overline{TS}$ is t_{SYSCLK}, that is, one clock period. Since no master can assert $\overline{TS}$ on the following clock edge, there is no concern regarding contention with the precharge. Output valid and output hold timing is tested for the signal asserted. Output valid time is tested for precharge.The high-impedance behavior is guaranteed by design.
5. Guaranteed by design and not tested
6. According to the bus protocol, $\overline{ARTRY}$ can be driven by multiple bus masters through the clock period immediately following $\overline{AACK}$. Bus contention is not an issue because any master asserting $\overline{ARTRY}$ will be driving it low. Any master asserting it low in the first clock following $\overline{AACK}$ will then go to high impedance for a fraction of a cycle, then negated for up to an entire cycle (crossing a bus cycle boundary) before being three-stated again. The nominal precharge width for $\overline{ARTRY}$ is 1.0 t_{SYSCLK}; that is, it should be high impedance as shown in Figure 6 before the first opportunity for another master to assert $\overline{ARTRY}$. Output valid and output hold timing is tested for the signal asserted.The high-impedance behavior is guaranteed by design.
7. According to the MPX bus protocol, $\overline{SHD0}$ and $\overline{SHD1}$ can be driven by multiple bus masters beginning two cycles after $\overline{TS}$. Timing is the same as $\overline{ARTRY}$, that is, the signal is high impedance for a fraction of a cycle, then negated for up to an entire cycle (crossing a bus cycle boundary) before being three-stated again. The nominal precharge width for $\overline{SHD0}$ and $\overline{SHD1}$ is 1.0 t_{SYSCLK}. The edges of the precharge vary depending on the programmed ratio of core to bus (PLL configurations).
8. $\overline{BMODE}$[0:1] and BVSEL[0:1] are mode select inputs. $\overline{BMODE}$[0:1] are sampled before and after $\overline{HRESET}$ negation. BVSEL[0:1] are sampled before $\overline{HRESET}$ negation. These parameters represent the input setup and hold times for each sample. These values are guaranteed by design and not tested. $\overline{BMODE}$[0:1] must remain stable after the second sample; BVSEL[0:1] must remain stable after the first (and only) sample. See Figure 5 for sample timing.

5.2.3 IEEE Std. 1149.1 AC Timing Specifications

Table 10 provides the IEEE Std. 1149.1 (JTAG) AC timing specifications as defined in Figure 8 through Figure 11.

Table 10. JTAG AC Timing Specifications (Independent of SYSCLK)[1]

At recommended operating conditions. See Table 4.

Parameter	Symbol	Min	Max	Unit	Notes
TCK frequency of operation	f_{TCLK}	0	33.3	MHz	
TCK cycle time	t_{TCLK}	30	—	ns	
TCK clock pulse width measured at 1.4 V	t_{JHJL}	15	—	ns	
TCK rise and fall times	t_{JR} and t_{JF}	—	2	ns	
$\overline{\text{TRST}}$ assert time	t_{TRST}	25	—	ns	2
Input setup times: Boundary-scan data TMS, TDI	 t_{DVJH} t_{IVJH}	 4 0	 — —	ns	3
Input hold times: Boundary-scan data TMS, TDI	 t_{DXJH} t_{IXJH}	 20 25	 — —	ns	3
Valid times: Boundary-scan data TDO	 t_{JLDV} t_{JLOV}	 4 4	 20 25	ns	4
Output hold times: Boundary-scan data TDO	 t_{JLDX} t_{JLOX}	 30 30	 — —	ns	4
TCK to output high impedance: Boundary-scan data TDO	 t_{JLDZ} t_{JLOZ}	 3 3	 19 9	ns	4, 5

Notes:

1. All outputs are measured from the midpoint voltage of the falling/rising edge of TCLK to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load (see Figure 7). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. $\overline{\text{TRST}}$ is an asynchronous level sensitive signal. The time is for test purposes only.
3. Non-JTAG signal input timing with respect to TCK.
4. Non-JTAG signal output timing with respect to TCK.
5. Guaranteed by design and characterization.

Figure 11 provides the test access port timing diagram.

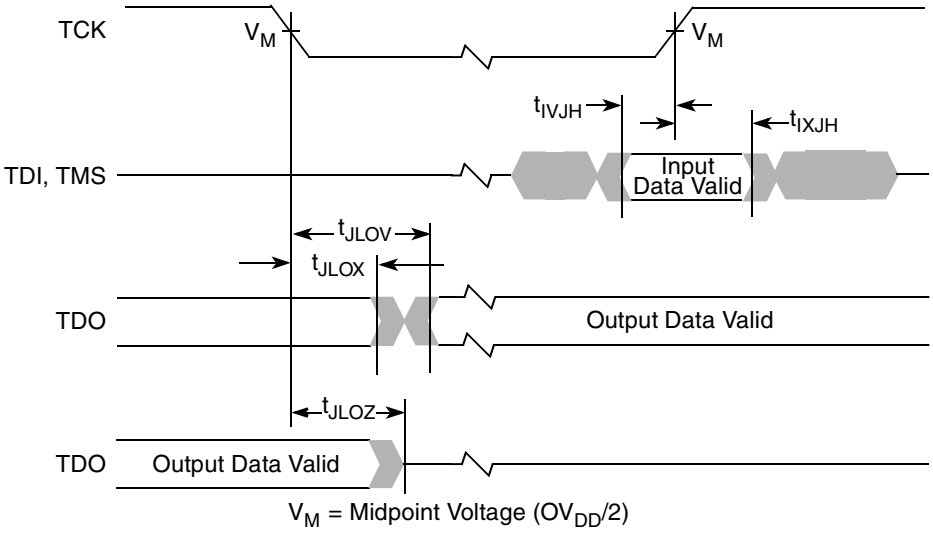


Figure 11. Test Access Port Timing Diagram

5.3 Voltage and Frequency Derating

Voltage and frequency derating is no longer supported for part numbers described by this document beginning with datecode 0613. (See Section 11, “Part Numbering and Marking,” for information on date code markings.) It is supported by some MPC7448 part numbers which target low-power applications; see Section 11.2, “Part Numbers Not Fully Addressed by This Document” and the referenced MPC7448 Hardware Specification Addenda for more information on these low-power devices. For those devices which previously supported this feature, information has been archived in the *Chip Errata for the MPC7448* (document order no. MPC7448CE).

Table 11. Pinout Listing for the MPC7448, 360 HCTE Package (continued)

Signal Name	Pin Number	Active	I/O	Notes
$\overline{\text{LVRAM}}$	B10	—	—	12, 20, 22
NC (no connect)	A6, A14, A15, B14, B15, C14, C15, C16, C17, C18, C19, D14, D15, D16, D17, D18, D19, E14, E15, F14, F15, G14, G15, H15, H16, J15, J16, J17, J18, J19, K15, K16, K17, K18, K19, L15, L16, L17, L18, L19	—	—	11
$\overline{\text{LSSD\_MODE}}$	E8	Low	Input	6, 12
$\overline{\text{MCP}}$	C9	Low	Input	
OV_{DD}	B4, C2, C12, D5, F2, H3, J5, K2, L5, M3, N6, P2, P8, P11, R4, R13, R16, T6, T9, U2, U12, U16, V4, V7, V10, V14	—	—	
OVDD_SENSE	E18, G18	—	—	16
PLL_CFG[0:4]	B8, C8, C7, D7, A7	High	Input	
PLL_CFG[5]	D10	High	Input	9, 20
$\overline{\text{PMON\_IN}}$	D9	Low	Input	13
$\overline{\text{PMON\_OUT}}$	A9	Low	Output	
$\overline{\text{QACK}}$	G5	Low	Input	
$\overline{\text{QREQ}}$	P4	Low	Output	
$\overline{\text{SHD}}$[0:1]	E4, H5	Low	I/O	3
$\overline{\text{SMI}}$	F9	Low	Input	
$\overline{\text{SRESET}}$	A2	Low	Input	
SYSCLK	A10	—	Input	
$\overline{\text{TA}}$	K6	Low	Input	
TBEN	E1	High	Input	
$\overline{\text{TBST}}$	F11	Low	Output	
TCK	C6	High	Input	
TDI	B9	High	Input	6
TDO	A4	High	Output	
$\overline{\text{TEA}}$	L1	Low	Input	
TEMP_ANODE	N18	—	—	17
TEMP_CATHODE	N19	—	—	17
TMS	F1	High	Input	6
$\overline{\text{TRST}}$	A5	Low	Input	6, 14
$\overline{\text{TS}}$	L4	Low	I/O	3
TSIZ[0:2]	G6, F7, E7	High	Output	
TT[0:4]	E5, E6, F6, E9, C5	High	I/O	
$\overline{\text{WT}}$	D3	Low	Output	
V_{DD}	H8, H10, H12, J7, J9, J11, J13, K8, K10, K12, K14, L7, L9, L11, L13, M8, M10, M12	—	—	
V_{DD}	A13, A16, A18, B17, B19, C13, E13, E16, F12, F17, F19, G11, G16, H14, H17, H19, M14, M16, M18, N15, N17, P16, P18	—	—	15

Table 11. Pinout Listing for the MPC7448, 360 HCTE Package (continued)

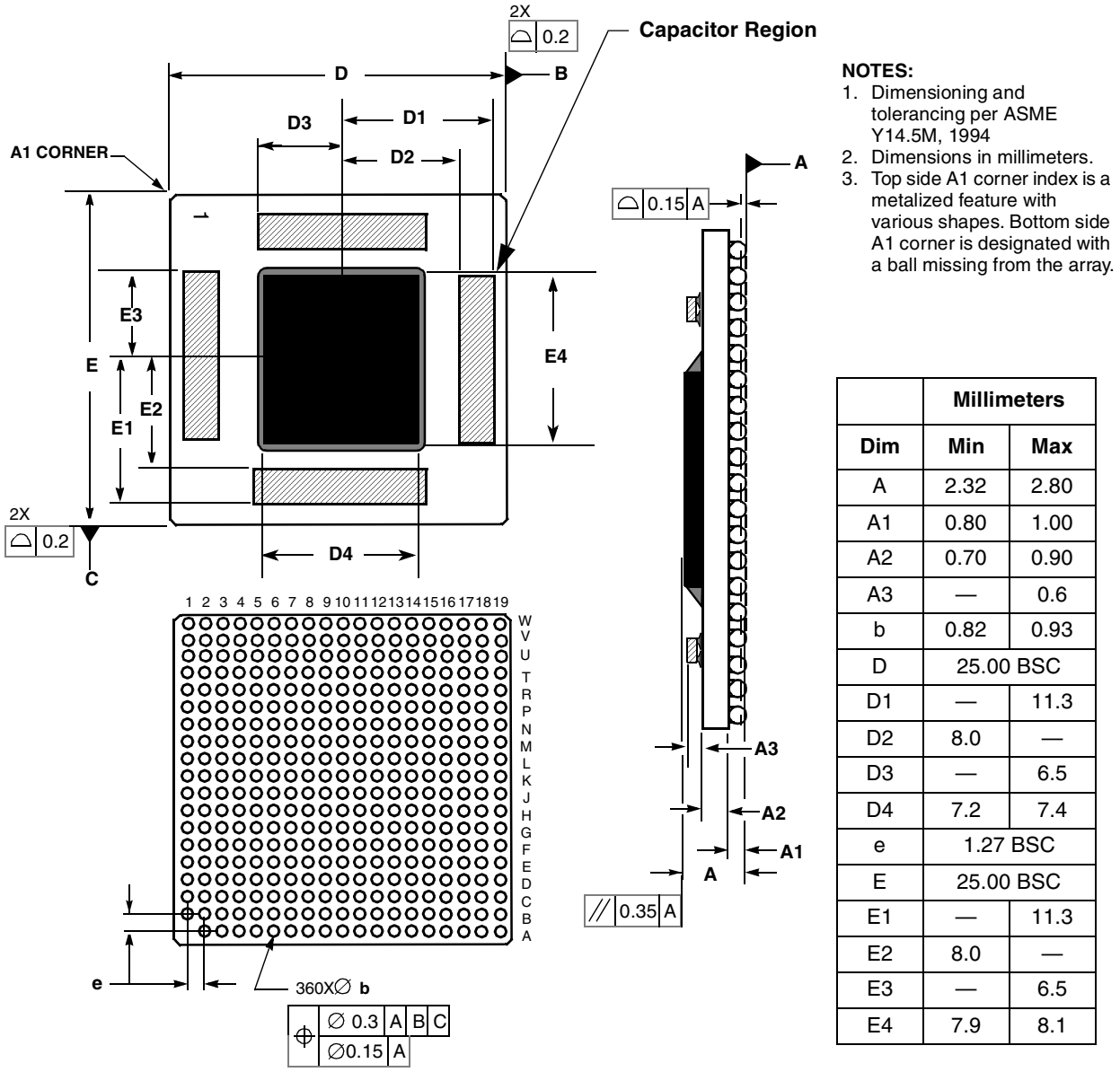
Signal Name	Pin Number	Active	I/O	Notes
VDD_SENSE	G13, N12	—	—	18

Notes:

1. OV_{DD} supplies power to the processor bus, JTAG, and all control signals, and is configurable. (V_{DD} supplies power to the processor core, and AV_{DD} supplies power to the PLL after filtering from V_{DD}). To program the I/O voltage, see Table 3. If used, the pull-down resistor should be less than 250 Ω. Because these settings may change in future products, it is recommended BVSEL[0:1] be configured using resistor options, jumpers, or some other flexible means, with the capability to reconfigure the termination of this signal in the future if necessary. For actual recommended value of V_{in} or supply voltages see Table 4.
2. Unused address pins must be pulled down to GND and corresponding address parity pins pulled up to OV_{DD}.
3. These pins require weak pull-up resistors (for example, 4.7 KΩ) to maintain the control signals in the negated state after they have been actively negated and released by the MPC7448 and other bus masters.
4. This signal selects between MPX bus mode (asserted) and 60x bus mode (negated) and will be sampled at $\overline{\text{HRESET}}$ going high.
5. This signal must be negated during reset, by pull-up resistor to OV_{DD} or negation by ¬$\overline{\text{HRESET}}$ (inverse of $\overline{\text{HRESET}}$), to ensure proper operation.
6. Internal pull up on die.
7. Not used in 60x bus mode.
8. These signals must be pulled down to GND if unused, or if the MPC7448 is in 60x bus mode.
9. These input signals are for factory use only and must be pulled down to GND for normal machine operation.
10. This test signal is recommended to be tied to $\overline{\text{HRESET}}$; however, other configurations will not adversely affect performance.
11. These signals are for factory use only and must be left unconnected for normal machine operation. Some pins that were NCs on the MPC7447, MPC7445, and MPC7441 have now been defined for other purposes.
12. These input signals are for factory use only and must be pulled up to OV_{DD} for normal machine operation.
13. This pin can externally cause a performance monitor event. Counting of the event is enabled through software.
14. This signal must be asserted during reset, by pull down to GND or assertion by $\overline{\text{HRESET}}$, to ensure proper operation.
15. These pins were NCs on the MPC7447, MPC7445, and MPC7441. See Section 9.3, “Connection Recommendations,” for more information.
16. These pins were OV_{DD} pins on the MPC7447, MPC7445, and MPC7441. These pins are internally connected to OV_{DD} and are intended to allow an external device (such as a power supply) to detect the I/O voltage level present inside the device package. If unused, it is recommended they be connected to test points to facilitate system debug; otherwise, they may be connected directly to OV_{DD} or left unconnected.
17. These pins provide connectivity to the on-chip temperature diode that can be used to determine the die junction temperature of the processor. These pins may be left unterminated if unused.
18. These pins are internally connected to V_{DD} and are intended to allow an external device (such as a power supply) to detect the processor core voltage level present inside the device package. If unused, it is recommended they be connected to test points to facilitate system debug; otherwise, they may be connected directly to V_{DD} or left unconnected.
19. These pins are internally connected to GND and are intended to allow an external device to detect the processor ground voltage level present inside the device package. If unused, it is recommended they be connected to test points to facilitate system debug; otherwise, they may be connected directly to GND or left unconnected.
20. These pins were in the TEST[0:4] factory test pin group on the MPC7447A, MPC7447, MPC7445, and MPC7441. They have been assigned new functions on the MPC7448.
21. These pins can be used to enable the supported dynamic frequency switching (DFS) modes via hardware. If both are pulled down, DFS mode is disabled completely and cannot be enabled via software. If unused, they should be pulled up to OV_{DD} to allow software control of DFS. See the *MPC7450 RISC Microprocessor Family Reference Manual* for more information.
22. This pin is provided to allow operation of the L2 cache at low core voltages and is for factory use only. See the *MPC7450 RISC Microprocessor Family Reference Manual* for more information.

8.2 Mechanical Dimensions for the MPC7448, 360 HCTE BGA

Figure 13 provides the mechanical dimensions and bottom surface nomenclature for the MPC7448, 360 HCTE BGA package.



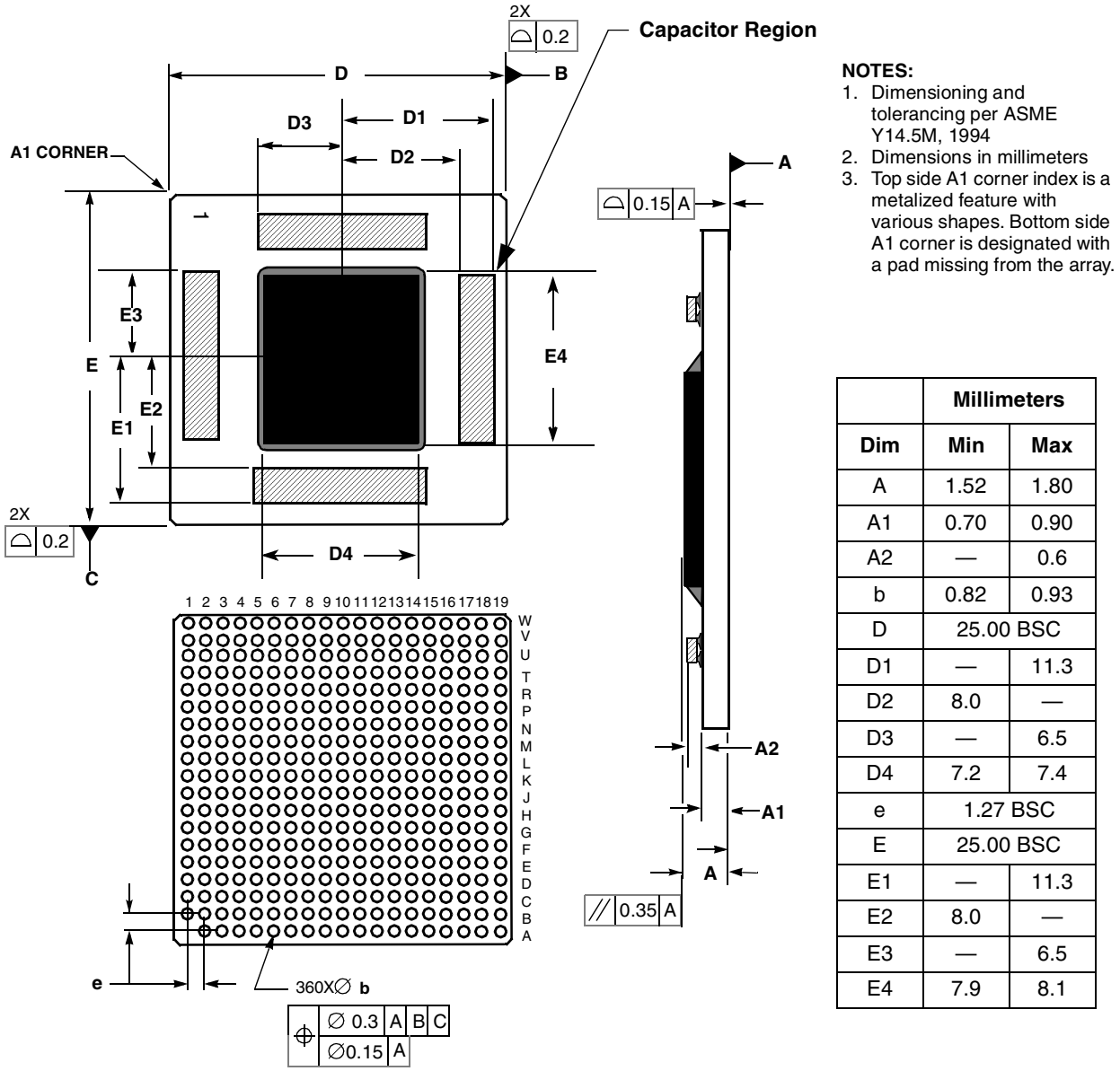
NOTES:
1. Dimensioning and tolerancing per ASME Y14.5M, 1994
2. Dimensions in millimeters.
3. Top side A1 corner index is a metalized feature with various shapes. Bottom side A1 corner is designated with a ball missing from the array.

	Millimeters	
Dim	Min	Max
A	2.32	2.80
A1	0.80	1.00
A2	0.70	0.90
A3	—	0.6
b	0.82	0.93
D	25.00 BSC	
D1	—	11.3
D2	8.0	—
D3	—	6.5
D4	7.2	7.4
e	1.27 BSC	
E	25.00 BSC	
E1	—	11.3
E2	8.0	—
E3	—	6.5
E4	7.9	8.1

Figure 13. Mechanical Dimensions and Bottom Surface Nomenclature for the MPC7448, 360 HCTE BGA Package

8.4 Mechanical Dimensions for the MPC7448, 360 HCTE LGA

Figure 13 provides the mechanical dimensions and bottom surface nomenclature for the MPC7448, 360 HCTE LGA package.



NOTES:
1. Dimensioning and tolerancing per ASME Y14.5M, 1994
2. Dimensions in millimeters
3. Top side A1 corner index is a metalized feature with various shapes. Bottom side A1 corner is designated with a pad missing from the array.

	Millimeters	
Dim	Min	Max
A	1.52	1.80
A1	0.70	0.90
A2	—	0.6
b	0.82	0.93
D	25.00 BSC	
D1	—	11.3
D2	8.0	—
D3	—	6.5
D4	7.2	7.4
e	1.27 BSC	
E	25.00 BSC	
E1	—	11.3
E2	8.0	—
E3	—	6.5
E4	7.9	8.1

Figure 14. Mechanical Dimensions and Bottom Surface Nomenclature for the MPC7448, 360 HCTE LGA Package

8.5 Package Parameters for the MPC7448, 360 HCTE RoHS-Compliant BGA

The package parameters are as provided in the following list. The package type is 25 × 25 mm, 360-lead high coefficient of thermal expansion ceramic ball grid array (HCTE) with RoHS-compliant lead-free spheres.

Package outline	25 × 25 mm
Interconnects	360 (19 × 19 ball array – 1)
Pitch	1.27 mm (50 mil)
Minimum module height	1.92 mm
Maximum module height	2.40 mm
Ball diameter	0.75 mm (30 mil)
Coefficient of thermal expansion	12.3 ppm/°C

Table 12. MPC7448 Microprocessor PLL Configuration Example (continued)

PLL_CFG[0:5]	Example Core and VCO Frequency in MHz										
	Bus-to-Core Multiplier [5]	Core-to-VCO Multiplier [5]	Bus (SYSCLK) Frequency								
			33.3 MHz	50 MHz	66.6 MHz	75 MHz	83 MHz	100 MHz	133 MHz	167 MHz	200 MHz
100110	11x	1x			733	825	913	1100	1467		
000000	11.5x	1x			766	863	955	1150	1533		
101110	12x	1x		600	800	900	996	1200	1600		
111110	12.5x	1x		625	833	938	1038	1250	1667		
010110	13x	1x		650	865	975	1079	1300			
111000	13.5x	1x		675	900	1013	1121	1350			
110010	14x	1x		700	933	1050	1162	1400			
000110	15x	1x		750	1000	1125	1245	1500			
110110	16x	1x		800	1066	1200	1328	1600			
000010	17x	1x		850	1132	1275	1417	1700			
001010	18x	1x	600	900	1200	1350	1500				
001110	20x	1x	667	1000	1332	1500	1666				
010010	21x	1x	700	1050	1399	1575					
011010	24x	1x	800	1200	1600						
111010	28x	1x	933	1400							
001100	PLL bypass		PLL off, SYSCLK clocks core circuitry directly								
111100	PLL off		PLL off, no core clocking occurs								

Notes:

1. PLL_CFG[0:5] settings not listed are reserved.
2. The sample bus-to-core frequencies shown are for reference only. Some PLL configurations may select bus, core, or VCO frequencies which are not useful, not supported, or not tested for by the MPC7448; see Section 5.2.1, "Clock AC Specifications," for valid SYSCLK, core, and VCO frequencies.
3. In PLL-bypass mode, the SYSCLK input signal clocks the internal processor directly and the PLL is disabled. However, the bus interface unit requires a 2x clock to function. Therefore, an additional signal, EXT_QUAL, must be driven at half the frequency of SYSCLK and offset in phase to meet the required input setup t_{IVKH} and hold time t_{IXKH} (see Table 9). The result will be that the processor bus frequency will be one-half SYSCLK, while the internal processor is clocked at SYSCLK frequency. This mode is intended for factory use and emulator tool use only.
   Note: The AC timing specifications given in this document do not apply in PLL-bypass mode.
4. In PLL-off mode, no clocking occurs inside the MPC7448 regardless of the SYSCLK input.
5. Applicable when DFS modes are disabled. These multipliers change when operating in a DFS mode. See Section 9.7.5, "Dynamic Frequency Switching (DFS)" for more information.
6. Bus-to-core multipliers less than 5x require that assertion of AACK be delayed by one or two bus cycles to allow the processor to generate a response to a snooped transaction. See the *MPC7450 RISC Microprocessor Reference Manual* for more information.

These requirements are shown graphically in Figure 16.

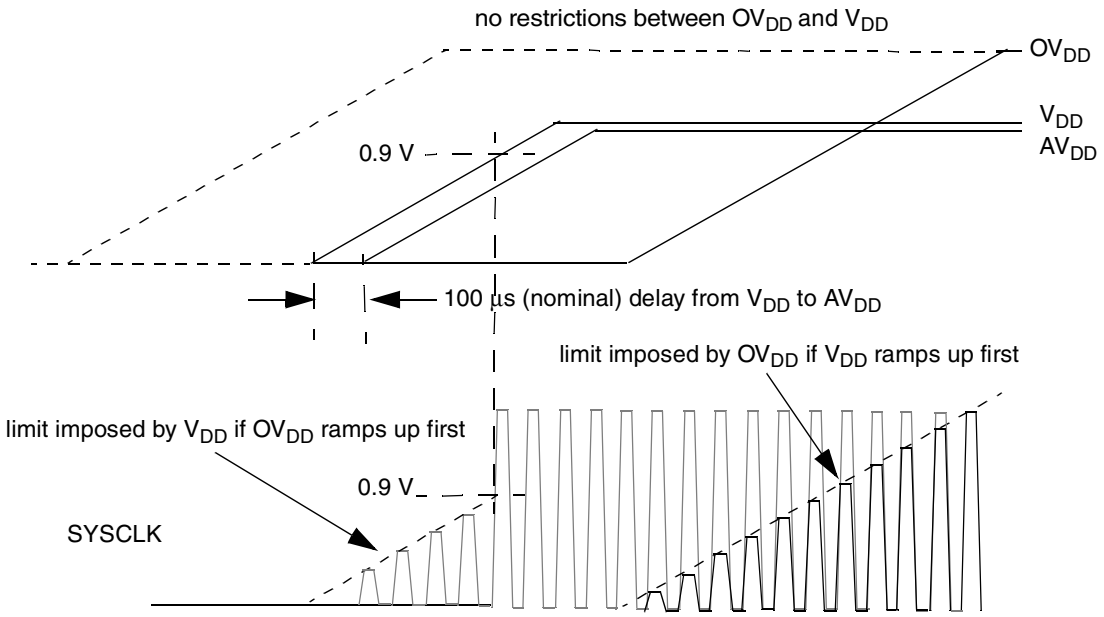


Figure 16. MPC7448 Power Up Sequencing Requirements

Certain stipulations also apply to the manner in which the power rails of the MPC7448 power down, as follows:

- OV_{DD} may ramp down any time before or after V_{DD}.
- The voltage at the SYSCLK input must not exceed V_{DD} once V_{DD} has ramped down below 0.9 V.
- The voltage at the SYSCLK input must not exceed OV_{DD} by more 20% during transients (see overshoot/undershoot specifications in Figure 2) or 0.3 V DC (see Table 2) at any time.

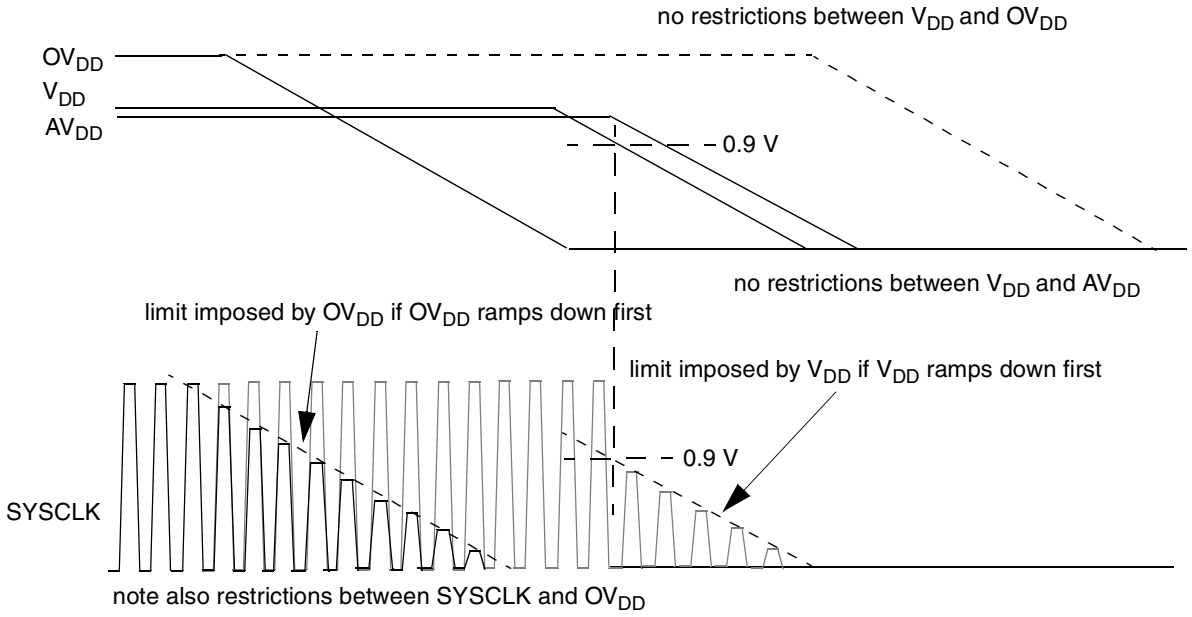


Figure 17. MPC7448 Power Down Sequencing Requirements

There is no requirement regarding AV_{DD} during power down, but it is recommended that AV_{DD} track V_{DD} within the RC time constant of the PLL filter circuit described in Section 9.2.2, "PLL Power Supply Filtering" (nominally 100 µs).

9.2.2 PLL Power Supply Filtering

The AV_{DD} power signal is provided on the MPC7448 to provide power to the clock generation PLL. To ensure stability of the internal clock, the power supplied to the AV_{DD} input signal should be filtered of any noise in the 500-KHz to 10-MHz resonant frequency range of the PLL. The circuit shown in Figure 18 using surface mount capacitors with minimum effective series inductance (ESL) is strongly recommended. In addition to filtering noise from the AV_{DD} input, it also provides the required delay between V_{DD} and AV_{DD} as described in Section 9.2.1, "Power Supply Sequencing."

The circuit should be placed as close as possible to the AV_{DD} pin to minimize noise coupled from nearby circuits. It is often possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of the device footprint.

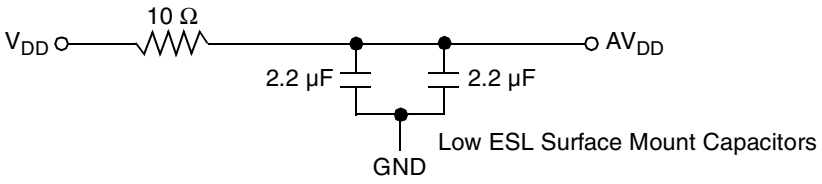


Figure 18. PLL Power Supply Filter Circuit

9.2.4 Decoupling Recommendations

Due to the MPC7448 dynamic power management feature, large address and data buses, and high operating frequencies, the MPC7448 can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the MPC7448 system, and the MPC7448 itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer use sufficient decoupling capacitors, typically one capacitor for every V_{DD} pin, and a similar amount for the OV_{DD} pins, placed as close as possible to the power pins of the MPC7448. It is also recommended that these decoupling capacitors receive their power from separate V_{DD}, OV_{DD}, and GND power planes in the PCB, using short traces to minimize inductance.

These capacitors should have a value of 0.01 or 0.1 µF. Only ceramic surface mount technology (SMT) capacitors should be used to minimize lead inductance. Orientations where connections are made along the length of the part, such as 0204, are preferable but not mandatory. Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993) and contrary to previous recommendations for decoupling Freescale microprocessors, multiple small capacitors of equal value are recommended over using multiple values of capacitance.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V_{DD} and OV_{DD} planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low equivalent series resistance (ESR) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors are 100–330 µF (AVX TPS tantalum or Sanyo OSCON).

9.3 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. Unless otherwise noted, unused active low inputs should be tied to OV_{DD} and unused active high inputs should be connected to GND. All NC (no connect) signals must remain unconnected.

Power and ground connections must be made to all external V_{DD}, OV_{DD}, and GND pins in the MPC7448. For backward compatibility with the MPC7447, MPC7445, and MP7441, or for migrating a system originally designed for one of these devices to the MPC7448, the new power and ground signals (formerly NC, see Table 11) may be left unconnected if the core frequency is 1 GHz or less. Operation above 1 GHz requires that these additional power and ground signals be connected, and it is strongly recommended that all new designs include the additional connections. See also Section 7, “Pinout Listings,” for additional information.

The MPC7448 provides VDD_SENSE, OVDD_SENSE, and GND_SENSE pins. These pins connect directly to the power/ground planes in the device package and are intended to allow an external device to measure the voltage present on the V_{DD}, OV_{DD} and GND planes in the device package. The most common use for these signals is as a feedback signal to a power supply regulator to allow it to compensate for board losses and supply the correct voltage at the device. (Note that all voltage parameters are specified at the pins of the device.) If not used for this purpose, it is recommended that these signals be connected to test points that can be used in the event that an accurate measurement of the voltage at the device is needed during system debug. Otherwise, these signals should be connected to the appropriate power/ground planes on the circuit board or left unconnected.

9.4 Output Buffer DC Impedance

The MPC7448 processor bus drivers are characterized over process, voltage, and temperature. To measure Z_0, an external resistor is connected from the chip pad to OV_{DD} or GND. The value of each resistor is varied until the pad voltage is $OV_{DD}/2$. Figure 20 shows the driver impedance measurement.

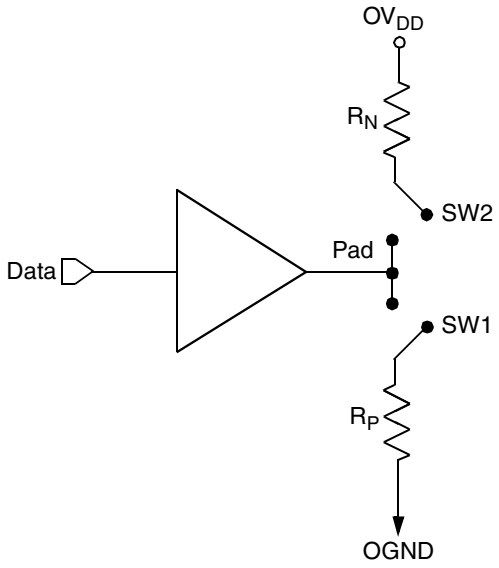


Figure 20. Driver Impedance Measurement

The output impedance is the average of two components—the resistances of the pull-up and pull-down devices. When data is held low, SW2 is closed (SW1 is open), and R_N is trimmed until the voltage at the pad equals $OV_{DD}/2$. R_N then becomes the resistance of the pull-down devices. When data is held high, SW1 is closed (SW2 is open), and R_P is trimmed until the voltage at the pad equals $OV_{DD}/2$. R_P then becomes the resistance of the pull-up devices. R_P and R_N are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N)/2$.

Table 15 summarizes the signal impedance results. The impedance increases with junction temperature and is relatively unaffected by bus voltage.

Table 15. Impedance Characteristics

At recommended operating conditions. See Table 4

Impedance		Processor Bus	Unit
Z_0	Typical	33–42	Ω
	Maximum	31–51	Ω

9.5 Pull-Up/Pull-Down Resistor Requirements

The MPC7448 requires high-resistive (weak: 4.7-KΩ) pull-up resistors on several control pins of the bus interface to maintain the control signals in the negated state after they have been actively negated and released by the MPC7448 or other bus masters. These pins are: $\overline{TS}$, $\overline{ARTRY}$, $\overline{SHDO}$, and $\overline{SHD1}$.

Some pins designated as being factory test pins must be pulled up to OV_{DD} or down to GND to ensure proper device operation. The pins that must be pulled up to OV_{DD} are $\overline{LSSD\_MODE}$ and TEST[0:3]; the pins that must be pulled down to GND are L1_TSTCLK and TEST[4]. The $\overline{CKSTP\_IN}$ signal should

likewise be pulled up through a pull-up resistor (weak or stronger: 4.7–1 KΩ) to prevent erroneous assertions of this signal.

In addition, the MPC7448 has one open-drain style output that requires a pull-up resistor (weak or stronger: 4.7–1 KΩ) if it is used by the system. This pin is $\overline{\text{CKSTP\_OUT}}$.

BVSEL0 and BVSEL1 should not be allowed to float, and should be configured either via pull-up or pull-down resistors or actively driven by external logic. If pull-down resistors are used to configure BVSEL0 or BVSEL1, the resistors should be less than 250 Ω (see Table 11). Because PLL_CFG[0:5] must remain stable during normal operation, strong pull-up and pull-down resistors (1 KΩ or less) are recommended to configure these signals in order to protect against erroneous switching due to ground bounce, power supply noise, or noise coupling.

During inactive periods on the bus, the address and transfer attributes may not be driven by any master and may, therefore, float in the high-impedance state for relatively long periods of time. Because the MPC7448 must continually monitor these signals for snooping, this float condition may cause excessive power draw by the input receivers on the MPC7448 or by other receivers in the system. These signals can be pulled up through weak (10-KΩ) pull-up resistors by the system, address bus driven mode enabled (see the *MPC7450 RISC Microprocessor Family Users' Manual* for more information on this mode), or they may be otherwise driven by the system during inactive periods of the bus to avoid this additional power draw. Preliminary studies have shown the additional power draw by the MPC7448 input receivers to be negligible and, in any event, none of these measures are necessary for proper device operation. The snooped address and transfer attribute inputs are: A[0:35], AP[0:4], TT[0:4], $\overline{\text{CI}}$, $\overline{\text{WT}}$, and $\overline{\text{GBL}}$.

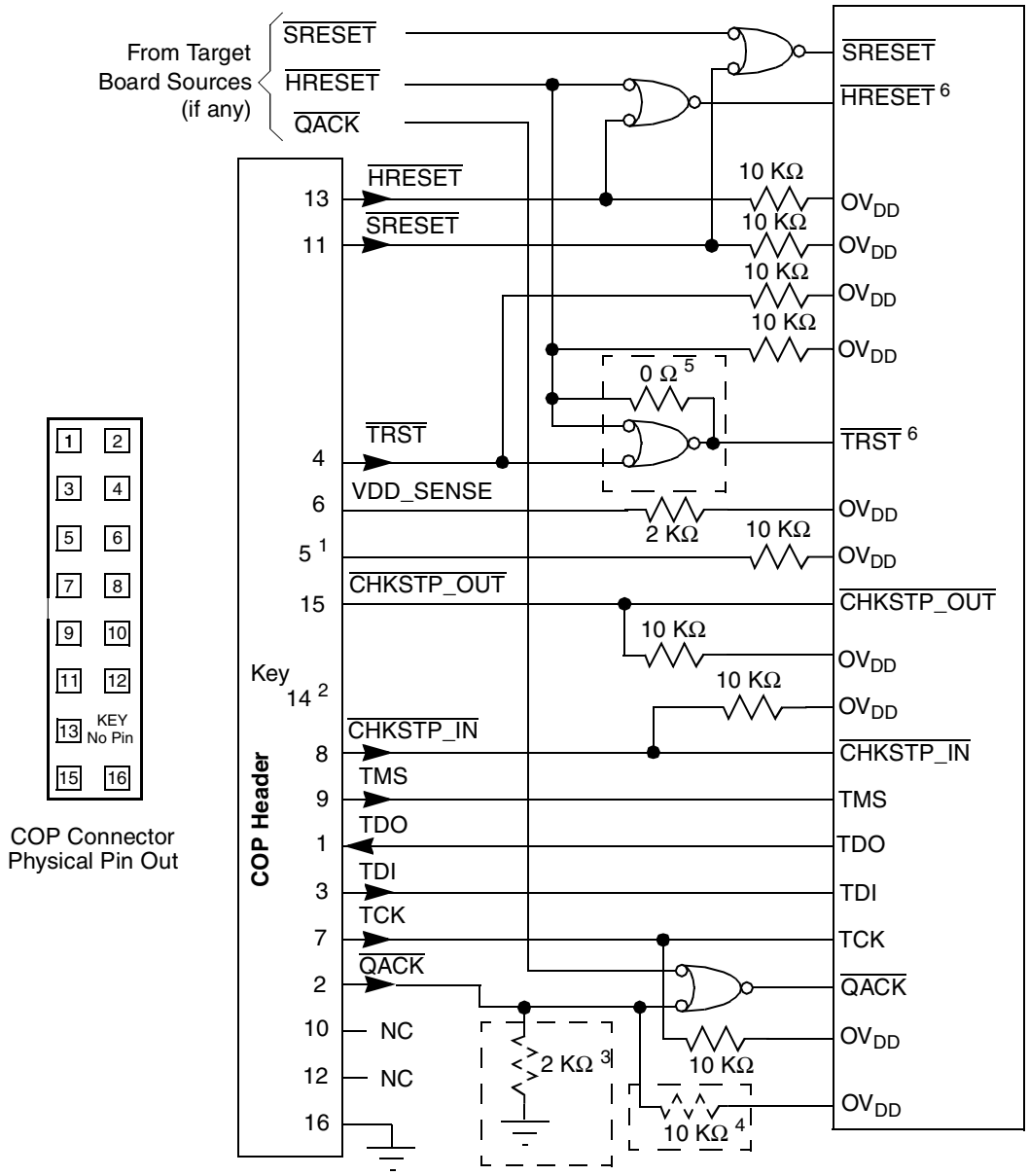
If address or data parity is not used by the system, and respective parity checking is disabled through HID1, the input receivers for those pins are disabled and do not require pull-up resistors, therefore they may be left unconnected by the system. If extended addressing is not used (HID0[XAEN] = 0), A[0:3] are unused and must be pulled low to GND through weak pull-down resistors; additionally, if address parity checking is enabled (HID1[EBA] = 1) and extended addressing is not used, AP[0] must be pulled up to OV_{DD} through a weak pull-up resistor. If the MPC7448 is in 60x bus mode, DTI[0:3] must be pulled low to GND through weak pull-down resistors.

The data bus input receivers are normally turned off when no read operation is in progress and, therefore, do not require pull-up resistors on the bus. Other data bus receivers in the system, however, may require pull-ups or require that those signals be otherwise driven by the system during inactive periods. The data bus signals are D[0:63] and DP[0:7].

9.6 JTAG Configuration Signals

Boundary-scan testing is enabled through the JTAG interface signals. The $\overline{\text{TRST}}$ signal is optional in the IEEE 1149.1 standard specification, but is typically provided on all processors that implement the PowerPC architecture. While it is possible to force the TAP controller to the reset state using only the TCK and TMS signals, more reliable power-on reset performance will be obtained if the $\overline{\text{TRST}}$ signal is asserted during power-on reset. Because the JTAG interface is also used for accessing the common on-chip processor (COP) function, simply tying $\overline{\text{TRST}}$ to $\overline{\text{HRESET}}$ is not practical.

The COP function of these processors allows a remote computer system (typically a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$ in order



Notes:

1. RUN/$\overline{\text{STOP}}$, normally found on pin 5 of the COP header, is not implemented on the MPC7448. Connect pin 5 of the COP header to OV_{DD} with a 10-KΩ pull-up resistor.
2. Key location; pin 14 is not physically present on the COP header.
3. Component not populated. Populate only if debug tool does not drive $\overline{\text{QACK}}$.
4. Populate only if debug tool uses an open-drain type output and does not actively negate $\overline{\text{QACK}}$.
5. If the JTAG interface is implemented, connect $\overline{\text{HRESET}}$ from the target source to $\overline{\text{TRST}}$ from the COP header though an AND gate to $\overline{\text{TRST}}$ of the part. If the JTAG interface is not implemented, connect $\overline{\text{HRESET}}$ from the target source to $\overline{\text{TRST}}$ of the part through a 0-Ω isolation resistor.
6. The COP port and target board should be able to independently assert $\overline{\text{HRESET}}$ and $\overline{\text{TRST}}$ to the processor in order to fully control the processor as shown above.

Figure 21. JTAG Interface Connection

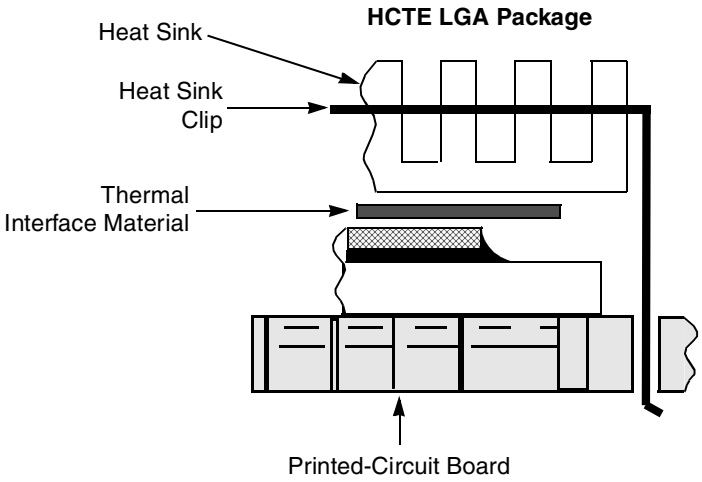


Figure 23. LGA Package Exploded Cross-Sectional View with Several Heat Sink Options

There are several commercially-available heat sinks for the MPC7448 provided by the following vendors:

Aavid Thermalloy 80 Commercial St. Concord, NH 03301 Internet: www.aavidthermalloy.com	603-224-9988
Alpha Novatech 473 Sapena Ct. #12 Santa Clara, CA 95054 Internet: www.alphanovatech.com	408-567-8082
Calgreg Thermal Solutions 60 Alhambra Road, Suite 1 Warwick, RI 02886 Internet: www.calgregthermalsolutions.com	888-732-6100
International Electronic Research Corporation (IERC) 413 North Moss St. Burbank, CA 91502 Internet: www.ctscorp.com	818-842-7277
Tyco Electronics Chip Coolers™ P.O. Box 3668 Harrisburg, PA 17105-3668 Internet: www.tycoelectronics.com	800-522-6752
Wakefield Engineering 33 Bridge St. Pelham, NH 03076 Internet: www.wakefield.com	603-635-2800

Ultimately, the final selection of an appropriate heat sink depends on many factors, such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost.

of any thermal interface material depends on many factors—thermal performance requirements, manufacturability, service temperature, dielectric properties, cost, and so on.

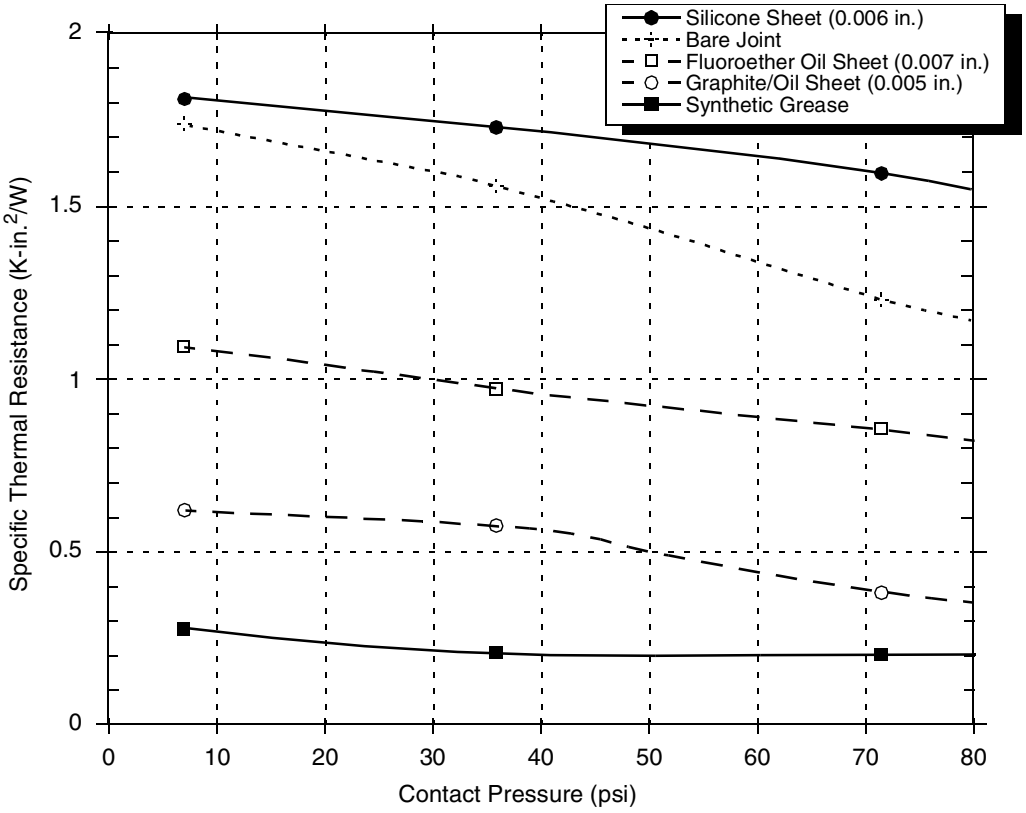


Figure 25. Thermal Performance of Select Thermal Interface Material

The board designer can choose between several types of thermal interfaces. Heat sink adhesive materials should be selected based on high conductivity and mechanical strength to meet equipment shock/vibration requirements. There are several commercially available thermal interfaces and adhesive materials provided by the following vendors:

The Bergquist Company 18930 West 78th St. Chanhassen, MN 55317 Internet: www.bergquistcompany.com	800-347-4572
Chomerics, Inc. 77 Dragon Ct. Woburn, MA 01801 Internet: www.chomerics.com	781-935-4850
Dow-Corning Corporation Corporate Center P.O. Box 994. Midland, MI 48686-0994 Internet: www.dowcorning.com	800-248-2481

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Technical Information Center
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+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
support@freescale.com

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku
Tokyo 153-0064, Japan
0120 191014
+81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
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Document Number: MPC7448EC
Rev. 4
3/2007