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Understanding [Embedded - Microprocessors](#)

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC G4
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.6GHz
Co-Processors/DSP	Multimedia; SIMD
RAM Controllers	-
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	1.5V, 1.8V, 2.5V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	360-BCBGA, FCCBGA
Supplier Device Package	360-FCCBGA (25x25)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc7448hx1600lc

- Monitors all dispatched instructions and retires them in order
- Tracks unresolved branches and flushes instructions after a mispredicted branch
- Retires as many as three instructions per clock cycle
- Separate on-chip L1 instruction and data caches (Harvard architecture)
 - 32-Kbyte, eight-way set-associative instruction and data caches
 - Pseudo least-recently-used (PLRU) replacement algorithm
 - 32-byte (eight-word) L1 cache block
 - Physically indexed/physical tags
 - Cache write-back or write-through operation programmable on a per-page or per-block basis
 - Instruction cache can provide four instructions per clock cycle; data cache can provide four words per clock cycle
 - Caches can be disabled in software.
 - Caches can be locked in software.
 - MESI data cache coherency maintained in hardware
 - Separate copy of data cache tags for efficient snooping
 - Parity support on cache
 - No snooping of instruction cache except for **icbi** instruction
 - Data cache supports AltiVec LRU and transient instructions
 - Critical double- and/or quad-word forwarding is performed as needed. Critical quad-word forwarding is used for AltiVec loads and instruction fetches. Other accesses use critical double-word forwarding.
- Level 2 (L2) cache interface
 - On-chip, 1-Mbyte, eight-way set-associative unified instruction and data cache
 - Cache write-back or write-through operation programmable on a per-page or per-block basis
 - Parity support on cache tags
 - ECC or parity support on data
 - Error injection allows testing of error recovery software
- Separate memory management units (MMUs) for instructions and data
 - 52-bit virtual address, 32- or 36-bit physical address
 - Address translation for 4-Kbyte pages, variable-sized blocks, and 256-Mbyte segments
 - Memory programmable as write-back/write-through, caching-inhibited/caching-allowed, and memory coherency enforced/memory coherency not enforced on a page or block basis
 - Separate IBATs and DBATs (eight each) also defined as SPRs
 - Separate instruction and data translation lookaside buffers (TLBs)
 - Both TLBs are 128-entry, two-way set-associative and use an LRU replacement algorithm.
 - TLBs are hardware- or software-reloadable (that is, a page table search is performed in hardware or by system software on a TLB miss).

- Efficient data flow
 - Although the VR/LSU interface is 128 bits, the L1/L2 bus interface allows up to 256 bits.
 - The L1 data cache is fully pipelined to provide 128 bits/cycle to or from the VRs.
 - The L2 cache is fully pipelined to provide 32 bytes per clock every other cycle to the L1 caches.
 - As many as 16 out-of-order transactions can be present on the MPX bus.
 - Store merging for multiple store misses to the same line. Only coherency action taken (address-only) for store misses merged to all 32 bytes of a cache block (no data tenure needed).
 - Three-entry finished store queue and five-entry completed store queue between the LSU and the L1 data cache
 - Separate additional queues for efficient buffering of outbound data (such as castouts and write-through stores) from the L1 data cache and L2 cache
- Multiprocessing support features include the following:
 - Hardware-enforced, MESI cache coherency protocols for data cache
 - Load/store with reservation instruction pair for atomic memory references, semaphores, and other multiprocessor operations
- Power and thermal management
 - Dynamic frequency switching (DFS) feature allows processor core frequency to be halved or quartered through software to reduce power consumption.
 - The following three power-saving modes are available to the system:
 - Nap—Instruction fetching is halted. Only the clocks for the time base, decremter, and JTAG logic remain running. The part goes into the doze state to snoop memory operations on the bus and then back to nap using a $\overline{QREQ}/\overline{QACK}$ processor-system handshake protocol.
 - Sleep—Power consumption is further reduced by disabling bus snooping, leaving only the PLL in a locked and running state. All internal functional units are disabled.
 - Deep sleep—When the part is in the sleep state, the system can disable the PLL. The system can then disable the SYSCLK source for greater system power savings. Power-on reset procedures for restarting and relocking the PLL must be followed upon exiting the deep sleep state.
 - Instruction cache throttling provides control of instruction fetching to limit device temperature.
 - A new temperature diode that can determine the temperature of the microprocessor
- Performance monitor can be used to help debug system designs and improve software efficiency.
- In-system testability and debugging features through JTAG boundary-scan capability
- Testability
 - LSSD scan design
 - IEEE Std. 1149.1™ JTAG interface

- Reliability and serviceability
 - Parity checking on system bus
 - Parity checking on the L1 caches and L2 data tags
 - ECC or parity checking on L2 data

3 Comparison with the MPC7447A, MPC7447, MPC7445, and MPC7441

Table 1 compares the key features of the MPC7448 with the key features of the earlier MPC7447A, MPC7447, MPC7445, and MPC7441. All are based on the MPC7450 RISC microprocessor and are architecturally very similar. The MPC7448 is identical to the MPC7447A, but the MPC7448 supports 1 Mbyte of L2 cache with ECC and the use of dynamic frequency switching (DFS) with more bus-to-core ratios.

Table 1. Microarchitecture Comparison

Microarchitectural Specs	MPC7448	MPC7447A	MPC7447	MPC7445	MPC7441
Basic Pipeline Functions					
Logic inversions per cycle	18				
Pipeline stages up to execute	5				
Total pipeline stages (minimum)	7				
Pipeline maximum instruction throughput	3 + branch				
Pipeline Resources					
Instruction buffer size	12				
Completion buffer size	16				
Renames (integer, float, vector)	16, 16, 16				
Maximum Execution Throughput					
SFX	3				
Vector	2 (any 2 of 4 units)				
Scalar floating-point	1				
Out-of-Order Window Size in Execution Queues					
SFX integer units	1 entry × 3 queues				
Vector units	In order, 4 queues				
Scalar floating-point unit	In order				
Branch Processing Resources					
Prediction structures	BTIC, BHT, link stack				
BTIC size, associativity	128-entry, 4-way				
BHT size	2K-entry				
Link stack depth	8				
Unresolved branches supported	3				
Branch taken penalty (BTIC hit)	1				
Minimum misprediction penalty	6				

Table 5 provides the package thermal characteristics for the MPC7448. For more information regarding thermal management, see Section 9.7, “Power and Thermal Management Information.”

Table 5. Package Thermal Characteristics¹

Characteristic	Symbol	Value	Unit	Notes
Junction-to-ambient thermal resistance, natural convection, single-layer (1s) board	$R_{\theta JA}$	26	°C/W	2, 3
Junction-to-ambient thermal resistance, natural convection, four-layer (2s2p) board	$R_{\theta JMA}$	19	°C/W	2, 4
Junction-to-ambient thermal resistance, 200 ft/min airflow, single-layer (1s) board	$R_{\theta JMA}$	22	°C/W	2, 4
Junction-to-ambient thermal resistance, 200 ft/min airflow, four-layer (2s2p) board	$R_{\theta JMA}$	16	°C/W	2, 4
Junction-to-board thermal resistance	$R_{\theta JB}$	11	°C/W	5
Junction-to-case thermal resistance	$R_{\theta JC}$	< 0.1	°C/W	6

Notes:

1. Refer to Section 9.7, “Power and Thermal Management Information,” for details about thermal management.
2. Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, airflow, power dissipation of other components on the board, and board thermal resistance.
3. Per JEDEC JESD51-2 with the single-layer board horizontal
4. Per JEDEC JESD51-6 with the board horizontal
5. Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
6. This is the thermal resistance between die and case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the calculated case temperature. The actual value of $R_{\theta JC}$ for the part is less than 0.1°C/W.

Table 6 provides the DC electrical characteristics for the MPC7448.

Table 6. DC Electrical Specifications

At recommended operating conditions. See Table 4.

Characteristic	Nominal Bus Voltage ¹	Symbol	Min	Max	Unit	Notes
Input high voltage (all inputs)	1.5	V_{IH}	$OV_{DD} \times 0.65$	$OV_{DD} + 0.3$	V	2
	1.8		$OV_{DD} \times 0.65$	$OV_{DD} + 0.3$		
	2.5		1.7	$OV_{DD} + 0.3$		
Input low voltage (all inputs)	1.5	V_{IL}	−0.3	$OV_{DD} \times 0.35$	V	2
	1.8		−0.3	$OV_{DD} \times 0.35$		
	2.5		−0.3	0.7		
Input leakage current, all signals except BVSELO, LSSD_MODE, TCK, TDI, TMS, TRST: $V_{in} = OV_{DD}$ $V_{in} = GND$	—	I_{in}	—	50 − 50	μA	2, 3
Input leakage current, BVSELO, LSSD_MODE, TCK, TDI, TMS, TRST: $V_{in} = OV_{DD}$ $V_{in} = GND$	—	I_{in}	—	50 − 2000	μA	2, 6

Table 8. Clock AC Timing Specifications

At recommended operating conditions. See [Table 4](#).

Characteristic		Symbol	Maximum Processor Core Frequency (Speed Grade)								Unit	Notes
			1000 MHz		1420 MHz		1600 MHz		1700 MHz			
			Min	Max	Min	Max	Min	Max	Min	Max		
Processor core frequency	DFS mode disabled	f _{core}	600	1000	600	1420	600	1600	600	1700	MHz	1, 8
	DFS mode enabled	f _{core—DF}	300	500	300	710	300	800	300	850		9
VCO frequency		f _{VCO}	600	1000	600	1420	600	800	600	1700	MHz	1, 10
SYSCLK frequency		f _{SYSCLK}	33	200	33	200	33	200	33	200	MHz	1, 2, 8
SYSCLK cycle time		t _{SYSCLK}	5.0	30	5.0	30	5.0	30	5.0	30	ns	2
SYSCLK rise and fall time		t _{KR} , t _{KF}	—	0.5	—	0.5	—	0.5	—	0.5	ns	3
SYSCLK duty cycle measured at OV _{DD} /2		t _{KHKL} / t _{SYSCLK}	40	60	40	60	40	60	40	60	%	4
SYSCLK cycle-to-cycle jitter			—	150	—	150	—	150	—	150	ps	5, 6
Internal PLL relock time			—	100	—	100	—	100	—	100	μs	7

Notes:

- Caution:** The SYSCLK frequency and PLL_CFG[0:5] settings must be chosen such that the resulting SYSCLK (bus) frequency, processor core frequency, and PLL (VCO) frequency do not exceed their respective maximum or minimum operating frequencies. Refer to the PLL_CFG[0:5] signal description in [Section 9.1.1, "PLL Configuration,"](#) for valid PLL_CFG[0:5] settings.
- Actual maximum system bus frequency is system-dependent. See [Section 5.2.1, "Clock AC Specifications."](#)
- Rise and fall times for the SYSCLK input measured from 0.4 to 1.4 V
- Timing is guaranteed by design and characterization.
- Guaranteed by design
- The SYSCLK driver's closed loop jitter bandwidth should be less than 1.5 MHz at –3 dB.
- Relock timing is guaranteed by design and characterization. PLL-relock time is the maximum amount of time required for PLL lock after a stable V_{DD} and SYSCLK are reached during the power-on reset sequence. This specification also applies when the PLL has been disabled and subsequently re-enabled during sleep mode. Also note that \overline{HRESET} must be held asserted for a minimum of 255 bus clocks after the PLL-relock time during the power-on reset sequence.
- This reflects the maximum and minimum core frequencies when the dynamic frequency switching feature (DFS) is disabled. f_{core_DFS} provides the maximum and minimum core frequencies when operating in a DFS mode.
- This specification supports the Dynamic Frequency Switching (DFS) feature and is applicable only when one of the DFS modes (divide-by-2 or divide-by-4) is enabled. When DFS is disabled, the core frequency must conform to the maximum and minimum frequencies stated for f_{core} .
- Use of the DFS feature does not affect VCO frequency.

Table 9. Processor Bus AC Timing Specifications¹ (continued)

At recommended operating conditions. See Table 4.

Parameter	Symbol ²	All Speed Grades		Unit	Notes
		Min	Max		
SYSCLK to output high impedance (all except \overline{TS} , \overline{ARTRY} , $\overline{SHD0}$, $\overline{SHD1}$)	t_{KHOZ}	—	1.8	ns	5
SYSCLK to \overline{TS} high impedance after precharge	t_{KHTSPZ}	—	1	t_{SYSCLK}	3, 4, 5
Maximum delay to $\overline{ARTRY}/\overline{SHD0}/\overline{SHD1}$ precharge	t_{KHARP}	—	1	t_{SYSCLK}	3, 5, 6, 7
SYSCLK to $\overline{ARTRY}/\overline{SHD0}/\overline{SHD1}$ high impedance after precharge	t_{KHARPZ}	—	2	t_{SYSCLK}	3, 5, 6, 7

Notes:

1. All input specifications are measured from the midpoint of the signal in question to the midpoint of the rising edge of the input SYSCLK. All output specifications are measured from the midpoint of the rising edge of SYSCLK to the midpoint of the signal in question. All output timings assume a purely resistive 50-Ω load (see Figure 4). Input and output timings are measured at the pin; time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. The symbology used for timing specifications herein follows the pattern of $t_{(signal)(state)(reference)(state)}$ for inputs and $t_{(reference)(state)(signal)(state)}$ for outputs. For example, t_{VKH} symbolizes the time input signals (I) reach the valid state (V) relative to the SYSCLK reference (K) going to the high (H) state or input setup time. And t_{KHOV} symbolizes the time from SYSCLK(K) going high (H) until outputs (O) are valid (V) or output valid time. Input hold time can be read as the time that the input signal (I) went invalid (X) with respect to the rising clock edge (KH) (note the position of the reference and its state for inputs) and output hold time can be read as the time from the rising edge (KH) until the output went invalid (OX).
3. t_{sysclk} is the period of the external clock (SYSCLK) in ns. The numbers given in the table must be multiplied by the period of SYSCLK to compute the actual time duration (in ns) of the parameter in question.
4. According to the bus protocol, \overline{TS} is driven only by the currently active bus master. It is asserted low and precharged high before returning to high impedance, as shown in Figure 6. The nominal precharge width for \overline{TS} is t_{SYSCLK} , that is, one clock period. Since no master can assert \overline{TS} on the following clock edge, there is no concern regarding contention with the precharge. Output valid and output hold timing is tested for the signal asserted. Output valid time is tested for precharge. The high-impedance behavior is guaranteed by design.
5. Guaranteed by design and not tested
6. According to the bus protocol, \overline{ARTRY} can be driven by multiple bus masters through the clock period immediately following \overline{AACK} . Bus contention is not an issue because any master asserting \overline{ARTRY} will be driving it low. Any master asserting it low in the first clock following \overline{AACK} will then go to high impedance for a fraction of a cycle, then negated for up to an entire cycle (crossing a bus cycle boundary) before being three-stated again. The nominal precharge width for \overline{ARTRY} is $1.0 t_{SYSCLK}$; that is, it should be high impedance as shown in Figure 6 before the first opportunity for another master to assert \overline{ARTRY} . Output valid and output hold timing is tested for the signal asserted. The high-impedance behavior is guaranteed by design.
7. According to the MPX bus protocol, $\overline{SHD0}$ and $\overline{SHD1}$ can be driven by multiple bus masters beginning two cycles after \overline{TS} . Timing is the same as \overline{ARTRY} , that is, the signal is high impedance for a fraction of a cycle, then negated for up to an entire cycle (crossing a bus cycle boundary) before being three-stated again. The nominal precharge width for $\overline{SHD0}$ and $\overline{SHD1}$ is $1.0 t_{SYSCLK}$. The edges of the precharge vary depending on the programmed ratio of core to bus (PLL configurations).
8. $\overline{BMODE}[0:1]$ and $BVSEL[0:1]$ are mode select inputs. $\overline{BMODE}[0:1]$ are sampled before and after \overline{HRESET} negation. $BVSEL[0:1]$ are sampled before \overline{HRESET} negation. These parameters represent the input setup and hold times for each sample. These values are guaranteed by design and not tested. $\overline{BMODE}[0:1]$ must remain stable after the second sample; $BVSEL[0:1]$ must remain stable after the first (and only) sample. See Figure 5 for sample timing.

5.2.3 IEEE Std. 1149.1 AC Timing Specifications

Table 10 provides the IEEE Std. 1149.1 (JTAG) AC timing specifications as defined in Figure 8 through Figure 11.

Table 10. JTAG AC Timing Specifications (Independent of SYSCLK)¹

At recommended operating conditions. See Table 4.

Parameter	Symbol	Min	Max	Unit	Notes
TCK frequency of operation	f_{TCLK}	0	33.3	MHz	
TCK cycle time	t_{TCLK}	30	—	ns	
TCK clock pulse width measured at 1.4 V	t_{HJL}	15	—	ns	
TCK rise and fall times	t_{JR} and t_{JF}	—	2	ns	
\overline{TRST} assert time	t_{TRST}	25	—	ns	2
Input setup times: Boundary-scan data TMS, TDI	t_{DVJH} t_{IVJH}	4 0	— —	ns	3
Input hold times: Boundary-scan data TMS, TDI	t_{DXJH} t_{IXJH}	20 25	— —	ns	3
Valid times: Boundary-scan data TDO	t_{JLDV} t_{JLOV}	4 4	20 25	ns	4
Output hold times: Boundary-scan data TDO	t_{JLDX} t_{JLOX}	30 30	— —	ns	4
TCK to output high impedance: Boundary-scan data TDO	t_{JLDZ} t_{JLOZ}	3 3	19 9	ns	4, 5

Notes:

1. All outputs are measured from the midpoint voltage of the falling/rising edge of TCLK to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load (see Figure 7). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. \overline{TRST} is an asynchronous level sensitive signal. The time is for test purposes only.
3. Non-JTAG signal input timing with respect to TCK.
4. Non-JTAG signal output timing with respect to TCK.
5. Guaranteed by design and characterization.

8.4 Mechanical Dimensions for the MPC7448, 360 HCTE LGA

Figure 13 provides the mechanical dimensions and bottom surface nomenclature for the MPC7448, 360 HCTE LGA package.

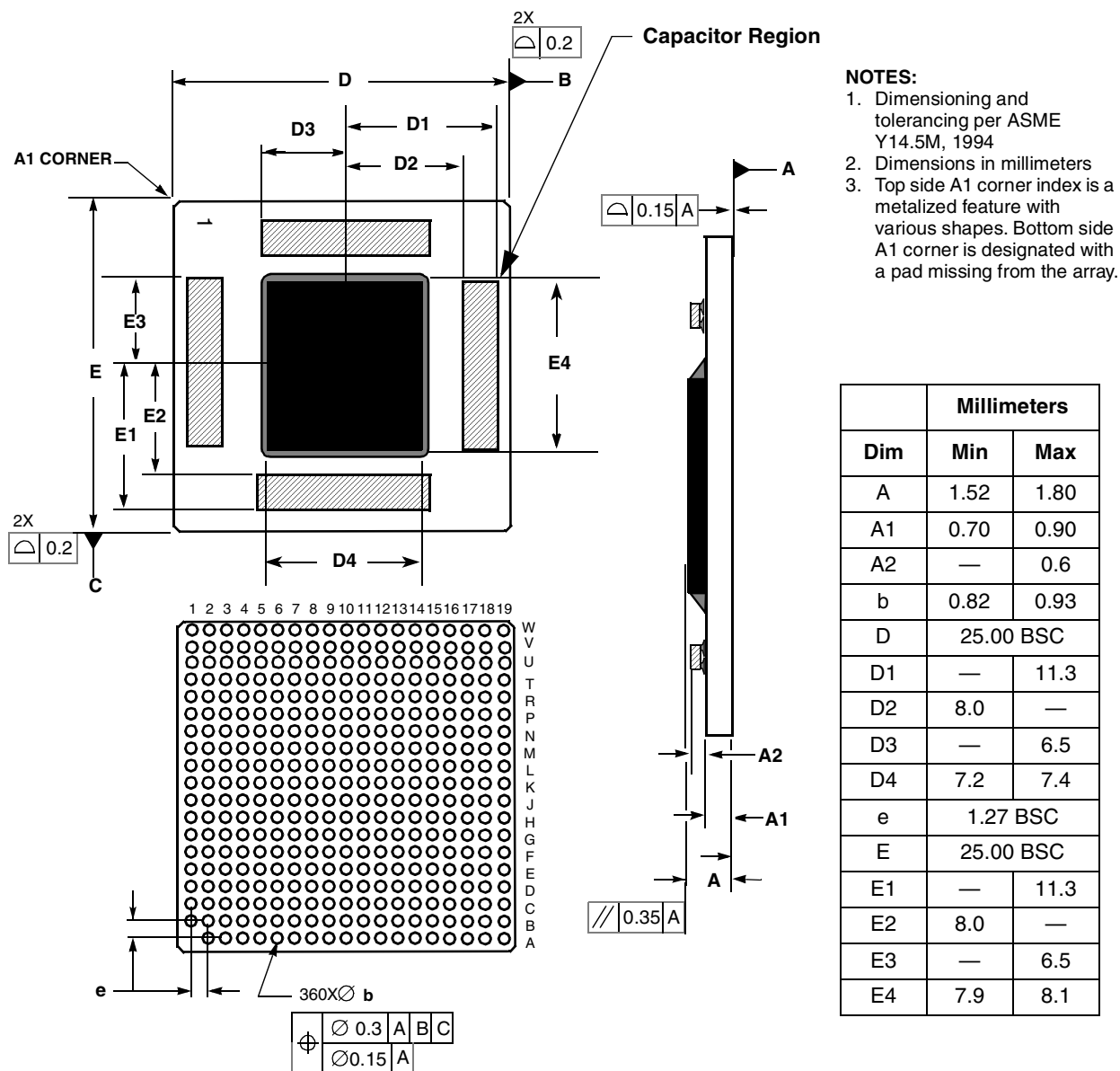


Figure 14. Mechanical Dimensions and Bottom Surface Nomenclature for the MPC7448, 360 HCTE LGA Package

9 System Design Information

This section provides system and thermal design requirements and recommendations for successful application of the MPC7448.

9.1 Clocks

The following sections provide more detailed information regarding the clocking of the MPC7448.

9.1.1 PLL Configuration

The MPC7448 PLL is configured by the PLL_CFG[0:5] signals. For a given SYSCLK (bus) frequency, the PLL configuration signals set the internal CPU and VCO frequency of operation. The PLL configuration for the MPC7448 is shown in Table 12. In this example, shaded cells represent settings that, for a given SYSCLK frequency, result in core and/or VCO frequencies that do not comply with Table 8. When enabled, dynamic frequency switching (DFS) also affects the core frequency by halving or quartering the bus-to-core multiplier; see Section 9.7.5, “Dynamic Frequency Switching (DFS),” for more information. Note that when DFS is enabled the resulting core frequency must meet the adjusted minimum core frequency requirements ($f_{\text{core_DFS}}$) described in Table 8. Note that the PLL_CFG[5] is currently used for factory test only and should be tied low, and that the MPC7448 PLL configuration settings are compatible with the MPC7447A PLL configuration settings when PLL_CFG[5] = 0.

Table 12. MPC7448 Microprocessor PLL Configuration Example

PLL_CFG[0:5]	Example Core and VCO Frequency in MHz										
	Bus-to-Core Multiplier ⁵	Core-to-VCO Multiplier ⁵	Bus (SYSCLK) Frequency								
			33.3 MHz	50 MHz	66.6 MHz	75 MHz	83 MHz	100 MHz	133 MHz	167 MHz	200 MHz
010000	2x ⁶	1x									
100000	3x ⁶	1x									600
101000	4x ⁶	1x								667	800
101100	5x	1x							667	835	1000
100100	5.5x	1x							733	919	1100
110100	6x	1x						600	800	1002	1200
010100	6.5x	1x						650	866	1086	1300
001000	7x	1x						700	931	1169	1400
000100	7.5x	1x					623	750	1000	1253	1500
110000	8x	1x				600	664	800	1064	1336	1600
011000	8.5x	1x				638	706	850	1131	1417	1700
011110	9x	1x			600	675	747	900	1197	1500	
011100	9.5x	1x			633	712	789	950	1264	1583	
101010	10x	1x			667	750	830	1000	1333	1667	
100010	10.5x	1x			700	938	872	1050	1397		

Table 12. MPC7448 Microprocessor PLL Configuration Example (continued)

PLL_CFG[0:5]	Example Core and VCO Frequency in MHz										
	Bus-to-Core Multiplier ⁵	Core-to-VCO Multiplier ⁵	Bus (SYSCLK) Frequency								
			33.3 MHz	50 MHz	66.6 MHz	75 MHz	83 MHz	100 MHz	133 MHz	167 MHz	200 MHz
100110	11x	1x			733	825	913	1100	1467		
000000	11.5x	1x			766	863	955	1150	1533		
101110	12x	1x		600	800	900	996	1200	1600		
111110	12.5x	1x		625	833	938	1038	1250	1667		
010110	13x	1x		650	865	975	1079	1300			
111000	13.5x	1x		675	900	1013	1121	1350			
110010	14x	1x		700	933	1050	1162	1400			
000110	15x	1x		750	1000	1125	1245	1500			
110110	16x	1x		800	1066	1200	1328	1600			
000010	17x	1x		850	1132	1275	1417	1700			
001010	18x	1x	600	900	1200	1350	1500				
001110	20x	1x	667	1000	1332	1500	1666				
010010	21x	1x	700	1050	1399	1575					
011010	24x	1x	800	1200	1600						
111010	28x	1x	933	1400							
001100	PLL bypass		PLL off, SYSCLK clocks core circuitry directly								
111100	PLL off		PLL off, no core clocking occurs								

Notes:

1. PLL_CFG[0:5] settings not listed are reserved.
2. The sample bus-to-core frequencies shown are for reference only. Some PLL configurations may select bus, core, or VCO frequencies which are not useful, not supported, or not tested for by the MPC7448; see [Section 5.2.1, "Clock AC Specifications,"](#) for valid SYSCLK, core, and VCO frequencies.
3. In PLL-bypass mode, the SYSCLK input signal clocks the internal processor directly and the PLL is disabled. However, the bus interface unit requires a 2x clock to function. Therefore, an additional signal, EXT_QUAL, must be driven at half the frequency of SYSCLK and offset in phase to meet the required input setup $t_{V_{KH}}$ and hold time $t_{X_{KH}}$ (see [Table 9](#)). The result will be that the processor bus frequency will be one-half SYSCLK, while the internal processor is clocked at SYSCLK frequency. This mode is intended for factory use and emulator tool use only.
Note: The AC timing specifications given in this document do not apply in PLL-bypass mode.
4. In PLL-off mode, no clocking occurs inside the MPC7448 regardless of the SYSCLK input.
5. Applicable when DFS modes are disabled. These multipliers change when operating in a DFS mode. See [Section 9.7.5, "Dynamic Frequency Switching \(DFS\)"](#) for more information.
6. Bus-to-core multipliers less than 5x require that assertion of AACK be delayed by one or two bus cycles to allow the processor to generate a response to a snooped transaction. See the *MPC7450 RISC Microprocessor Reference Manual* for more information.

9.2.4 Decoupling Recommendations

Due to the MPC7448 dynamic power management feature, large address and data buses, and high operating frequencies, the MPC7448 can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the MPC7448 system, and the MPC7448 itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer use sufficient decoupling capacitors, typically one capacitor for every V_{DD} pin, and a similar amount for the OV_{DD} pins, placed as close as possible to the power pins of the MPC7448. It is also recommended that these decoupling capacitors receive their power from separate V_{DD} , OV_{DD} , and GND power planes in the PCB, using short traces to minimize inductance.

These capacitors should have a value of 0.01 or 0.1 μF . Only ceramic surface mount technology (SMT) capacitors should be used to minimize lead inductance. Orientations where connections are made along the length of the part, such as 0204, are preferable but not mandatory. Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993) and contrary to previous recommendations for decoupling Freescale microprocessors, multiple small capacitors of equal value are recommended over using multiple values of capacitance.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V_{DD} and OV_{DD} planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low equivalent series resistance (ESR) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors are 100–330 μF (AVX TPS tantalum or Sanyo OSCON).

9.3 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. Unless otherwise noted, unused active low inputs should be tied to OV_{DD} and unused active high inputs should be connected to GND. All NC (no connect) signals must remain unconnected.

Power and ground connections must be made to all external V_{DD} , OV_{DD} , and GND pins in the MPC7448. For backward compatibility with the MPC7447, MPC7445, and MP7441, or for migrating a system originally designed for one of these devices to the MPC7448, the new power and ground signals (formerly NC, see [Table 11](#)) may be left unconnected if the core frequency is 1 GHz or less. Operation above 1 GHz requires that these additional power and ground signals be connected, and it is strongly recommended that all new designs include the additional connections. See also [Section 7, “Pinout Listings,”](#) for additional information.

The MPC7448 provides VDD_SENSE , $OVDD_SENSE$, and GND_SENSE pins. These pins connect directly to the power/ground planes in the device package and are intended to allow an external device to measure the voltage present on the V_{DD} , OV_{DD} and GND planes in the device package. The most common use for these signals is as a feedback signal to a power supply regulator to allow it to compensate for board losses and supply the correct voltage at the device. (Note that all voltage parameters are specified at the pins of the device.) If not used for this purpose, it is recommended that these signals be connected to test points that can be used in the event that an accurate measurement of the voltage at the device is needed during system debug. Otherwise, these signals should be connected to the appropriate power/ground planes on the circuit board or left unconnected.

9.4 Output Buffer DC Impedance

The MPC7448 processor bus drivers are characterized over process, voltage, and temperature. To measure Z_0 , an external resistor is connected from the chip pad to OV_{DD} or GND. The value of each resistor is varied until the pad voltage is $OV_{DD}/2$. Figure 20 shows the driver impedance measurement.

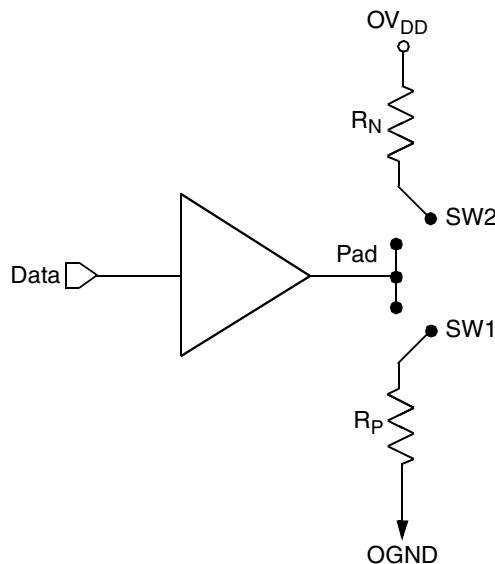


Figure 20. Driver Impedance Measurement

The output impedance is the average of two components—the resistances of the pull-up and pull-down devices. When data is held low, SW2 is closed (SW1 is open), and R_N is trimmed until the voltage at the pad equals $OV_{DD}/2$. R_N then becomes the resistance of the pull-down devices. When data is held high, SW1 is closed (SW2 is open), and R_P is trimmed until the voltage at the pad equals $OV_{DD}/2$. R_P then becomes the resistance of the pull-up devices. R_P and R_N are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N)/2$.

Table 15 summarizes the signal impedance results. The impedance increases with junction temperature and is relatively unaffected by bus voltage.

Table 15. Impedance Characteristics

At recommended operating conditions. See Table 4

Impedance		Processor Bus	Unit
Z_0	Typical	33–42	Ω
	Maximum	31–51	Ω

9.5 Pull-Up/Pull-Down Resistor Requirements

The MPC7448 requires high-resistive (weak: 4.7-K Ω) pull-up resistors on several control pins of the bus interface to maintain the control signals in the negated state after they have been actively negated and released by the MPC7448 or other bus masters. These pins are: \overline{TS} , \overline{ARTRY} , \overline{SHDO} , and \overline{SHDI} .

Some pins designated as being factory test pins must be pulled up to OV_{DD} or down to GND to ensure proper device operation. The pins that must be pulled up to OV_{DD} are $\overline{LSSD_MODE}$ and TEST[0:3]; the pins that must be pulled down to GND are L1_TSTCLK and TEST[4]. The CKSTP_IN signal should

likewise be pulled up through a pull-up resistor (weak or stronger: 4.7–1 K Ω) to prevent erroneous assertions of this signal.

In addition, the MPC7448 has one open-drain style output that requires a pull-up resistor (weak or stronger: 4.7–1 K Ω) if it is used by the system. This pin is $\overline{\text{CKSTP_OUT}}$.

BVSEL0 and BVSEL1 should not be allowed to float, and should be configured either via pull-up or pull-down resistors or actively driven by external logic. If pull-down resistors are used to configure BVSEL0 or BVSEL1, the resistors should be less than 250 Ω (see Table 11). Because PLL_CFG[0:5] must remain stable during normal operation, strong pull-up and pull-down resistors (1 K Ω or less) are recommended to configure these signals in order to protect against erroneous switching due to ground bounce, power supply noise, or noise coupling.

During inactive periods on the bus, the address and transfer attributes may not be driven by any master and may, therefore, float in the high-impedance state for relatively long periods of time. Because the MPC7448 must continually monitor these signals for snooping, this float condition may cause excessive power draw by the input receivers on the MPC7448 or by other receivers in the system. These signals can be pulled up through weak (10-K Ω) pull-up resistors by the system, address bus driven mode enabled (see the *MPC7450 RISC Microprocessor Family Users' Manual* for more information on this mode), or they may be otherwise driven by the system during inactive periods of the bus to avoid this additional power draw. Preliminary studies have shown the additional power draw by the MPC7448 input receivers to be negligible and, in any event, none of these measures are necessary for proper device operation. The snooped address and transfer attribute inputs are: A[0:35], AP[0:4], TT[0:4], $\overline{\text{CI}}$, $\overline{\text{WT}}$, and $\overline{\text{GBL}}$.

If address or data parity is not used by the system, and respective parity checking is disabled through HID1, the input receivers for those pins are disabled and do not require pull-up resistors, therefore they may be left unconnected by the system. If extended addressing is not used (HID0[XAEN] = 0), A[0:3] are unused and must be pulled low to GND through weak pull-down resistors; additionally, if address parity checking is enabled (HID1[EBA] = 1) and extended addressing is not used, AP[0] must be pulled up to OV_{DD} through a weak pull-up resistor. If the MPC7448 is in 60x bus mode, DTI[0:3] must be pulled low to GND through weak pull-down resistors.

The data bus input receivers are normally turned off when no read operation is in progress and, therefore, do not require pull-up resistors on the bus. Other data bus receivers in the system, however, may require pull-ups or require that those signals be otherwise driven by the system during inactive periods. The data bus signals are D[0:63] and DP[0:7].

9.6 JTAG Configuration Signals

Boundary-scan testing is enabled through the JTAG interface signals. The $\overline{\text{TRST}}$ signal is optional in the IEEE 1149.1 standard specification, but is typically provided on all processors that implement the PowerPC architecture. While it is possible to force the TAP controller to the reset state using only the TCK and TMS signals, more reliable power-on reset performance will be obtained if the $\overline{\text{TRST}}$ signal is asserted during power-on reset. Because the JTAG interface is also used for accessing the common on-chip processor (COP) function, simply tying $\overline{\text{TRST}}$ to HRESET is not practical.

The COP function of these processors allows a remote computer system (typically a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert HRESET or $\overline{\text{TRST}}$ in order

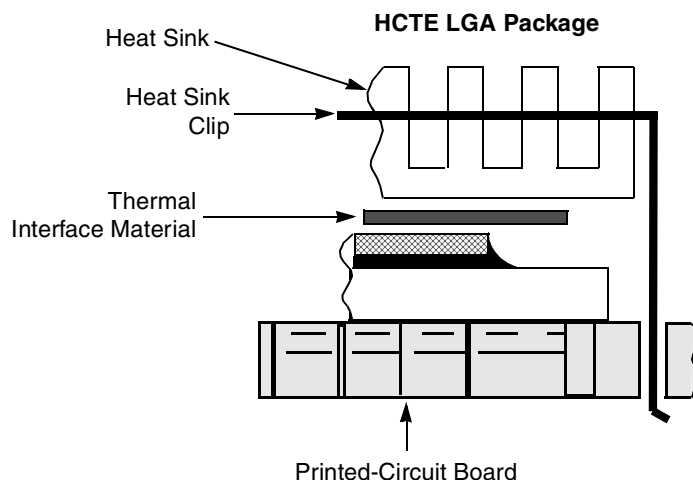


Figure 23. LGA Package Exploded Cross-Sectional View with Several Heat Sink Options

There are several commercially-available heat sinks for the MPC7448 provided by the following vendors:

Aavid Thermalloy	603-224-9988
80 Commercial St.	
Concord, NH 03301	
Internet: www.aavidthermalloy.com	
Alpha Novatech	408-567-8082
473 Sapena Ct. #12	
Santa Clara, CA 95054	
Internet: www.alphanovatech.com	
Calgreg Thermal Solutions	888-732-6100
60 Alhambra Road, Suite 1	
Warwick, RI 02886	
Internet: www.calgregthermalsolutions.com	
International Electronic Research Corporation (IERC)	818-842-7277
413 North Moss St.	
Burbank, CA 91502	
Internet: www.ctscorp.com	
Tyco Electronics	800-522-6752
Chip Coolers™	
P.O. Box 3668	
Harrisburg, PA 17105-3668	
Internet: www.tycoelectronics.com	
Wakefield Engineering	603-635-2800
33 Bridge St.	
Pelham, NH 03076	
Internet: www.wakefield.com	

Ultimately, the final selection of an appropriate heat sink depends on many factors, such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost.

9.7.1 Internal Package Conduction Resistance

For the exposed-die packaging technology described in Table 5, the intrinsic conduction thermal resistance paths are as follows:

- The die junction-to-case thermal resistance (the case is actually the top of the exposed silicon die)
- The die junction-to-board thermal resistance

Figure 24 depicts the primary heat transfer path for a package with an attached heat sink mounted to a printed-circuit board.

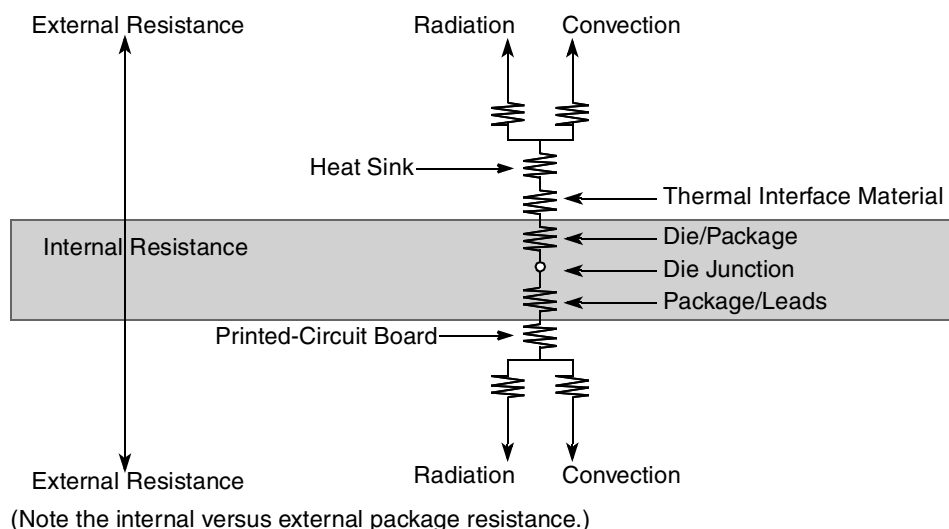


Figure 24. C4 Package with Heat Sink Mounted to a Printed-Circuit Board

Heat generated on the active side of the chip is conducted through the silicon, through the heat sink attach material (or thermal interface material), and, finally, to the heat sink, where it is removed by forced-air convection.

Because the silicon thermal resistance is quite small, the temperature drop in the silicon may be neglected for a first-order analysis. Thus, the thermal interface material and the heat sink conduction/convective thermal resistances are the dominant terms.

9.7.2 Thermal Interface Materials

A thermal interface material is recommended at the package lid-to-heat sink interface to minimize the thermal contact resistance. For those applications where the heat sink is attached by spring clip mechanism, Figure 25 shows the thermal performance of three thin-sheet thermal-interface materials (silicone, graphite/oil, fluoroether oil), a bare joint, and a joint with thermal grease as a function of contact pressure. As shown, the performance of these thermal interface materials improves with increasing contact pressure. The use of thermal grease significantly reduces the interface thermal resistance. That is, the bare joint results in a thermal resistance approximately seven times greater than the thermal grease joint.

Often, heat sinks are attached to the package by means of a spring clip to holes in the printed-circuit board (see Figure 22). Therefore, synthetic grease offers the best thermal performance due to the low interface pressure and is recommended due to the high power dissipation of the MPC7448. Of course, the selection

Shin-Etsu MicroSi, Inc.
10028 S. 51st St.
Phoenix, AZ 85044
Internet: www.microsi.com

888-642-7674

Laird Technologies - Thermal
(formerly Thermagon Inc.)
4707 Detroit Ave.
Cleveland, OH 44102
Internet: www.lairdtech.com

888-246-905

The following section provides a heat sink selection example using one of the commercially available heat sinks.

9.7.3 Heat Sink Selection Example

For preliminary heat sink sizing, the die-junction temperature can be expressed as follows:

$$T_j = T_i + T_r + (R_{\theta JC} + R_{\theta int} + R_{\theta sa}) \times P_d$$

where:

- T_j is the die-junction temperature
- T_i is the inlet cabinet ambient temperature
- T_r is the air temperature rise within the computer cabinet
- $R_{\theta JC}$ is the junction-to-case thermal resistance
- $R_{\theta int}$ is the adhesive or interface material thermal resistance
- $R_{\theta sa}$ is the heat sink base-to-ambient thermal resistance
- P_d is the power dissipated by the device

During operation, the die-junction temperatures (T_j) should be maintained less than the value specified in [Table 4](#). The temperature of air cooling the component greatly depends on the ambient inlet air temperature and the air temperature rise within the electronic cabinet. An electronic cabinet inlet-air temperature (T_i) may range from 30°C to 40°C. The air temperature rise within a cabinet (T_r) may be in the range of 5°C to 10°C. The thermal resistance of the thermal interface material ($R_{\theta int}$) is typically about 1.1 °C/W. For example, assuming a T_i of 30°C, a T_r of 5°C, an HCTE package $R_{\theta JC} = 0.1$, and a power consumption (P_d) of 25.6 W, the following expression for T_j is obtained:

$$\text{Die-junction temperature: } T_j = 30^\circ\text{C} + 5^\circ\text{C} + (0.1^\circ\text{C/W} + 1.1^\circ\text{C/W} + \theta_{sa}) \times 25.6$$

For this example, a $R_{\theta sa}$ value of 1.53 °C/W or less is required to maintain the die junction temperature below the maximum value of [Table 4](#).

Though the die junction-to-ambient and the heat sink-to-ambient thermal resistances are a common figure-of-merit used for comparing the thermal performance of various microelectronic packaging technologies, one should exercise caution when only using this metric in determining thermal management because no single parameter can adequately describe three-dimensional heat flow. The final die-junction operating temperature is not only a function of the component-level thermal resistance, but the system-level design and its operating conditions. In addition to the component's power consumption, a number of factors affect the final operating die-junction temperature—airflow, board population (local heat flux of adjacent components), heat sink efficiency, heat sink attach, heat sink placement, next-level interconnect technology, system air temperature rise, altitude, and so on.

Solving for T, the equation becomes:

$$nT = \frac{V_H - V_L}{1.986 \times 10^{-4}}$$

9.7.5 Dynamic Frequency Switching (DFS)

The DFS feature in the MPC7448 adds the ability to divide the processor-to-system bus ratio by two or four during normal functional operation. Divide-by-two mode is enabled by setting the HID1[DFS2] bit in software or by asserting the $\overline{\text{DFS2}}$ pin via hardware. The MPC7448 can be returned for full speed by clearing HID1[DFS2] or negating $\overline{\text{DFS2}}$. Similarly, divide-by-four mode is enabled by setting HID1[DFS4] in software or by asserting the $\overline{\text{DFS4}}$ pin. In all cases, the frequency change occurs in 1 clock cycle and no idle waiting period is required to switch between modes. Note that asserting either $\overline{\text{DFS2}}$ or $\overline{\text{DFS4}}$ overrides software control of DFS, and that asserting both $\overline{\text{DFS2}}$ and $\overline{\text{DFS4}}$ disables DFS completely, including software control. Additional information regarding DFS can be found in the *MPC7450 RISC Microprocessor Family Reference Manual*. Note that minimum core frequency requirements must be observed when enabling DFS, and the resulting core frequency must meet the requirements for $f_{\text{core_DFS}}$ given in [Table 8](#).

9.7.5.1 Power Consumption with DFS Enabled

Power consumption with DFS enabled can be approximated using the following formula:

$$P_{\text{DFS}} = \left[\frac{f_{\text{DFS}}}{f} (P - P_{\text{DS}}) \right] + P_{\text{DS}}$$

Where:

P_{DFS} = Power consumption with DFS enabled

f_{DFS} = Core frequency with DFS enabled

f = Core frequency prior to enabling DFS

P = Power consumption prior to enabling DFS (see [Table 7](#))

P_{DS} = Deep sleep mode power consumption (see [Table 7](#))

The above is an approximation only. Power consumption with DFS enabled is not tested or guaranteed.

9.7.5.2 Bus-to-Core Multiplier Constraints with DFS

DFS is not available for all bus-to-core multipliers as configured by PLL_CFG[0:5] during hard reset. The complete listing is shown in [Table 16](#). Shaded cells represent DFS modes that are not available for a particular PLL_CFG[0:5] setting. Should software or hardware attempt to transition to a multiplier that is not supported, the device will remain at its current multiplier. For example, if a transition from DFS-disabled to an unsupported divide-by-2 or divide-by-4 setting is attempted, the bus-to-core multiplier will remain at the setting configured by the PLL_CFG[0:5] pins. In the case of an attempted transition from a supported divide-by-2 mode to an unsupported divide-by-4 mode, the device will remain in divide-by-2 mode. In all cases, the HID1[PC0-5] bits will correctly reflect the current bus-to-core frequency multiplier.

Table 16. Valid Divide Ratio Configurations

DFS mode disabled		DFS divide-by-2 mode enabled (HID1[DFS2] = 1 or DFS2 = 0)		DFS divide-by-4 mode enabled (HID1[DFS4] = 1 or DFS4 = 0)	
Bus-to-Core Multiplier Configured by PLL_CFG[0:5] (see Table 12)	HID1[PC0-5] ³	Bus-to-Core Multiplier	HID1[PC0-5] ³	Bus-to-Core Multiplier	HID1[PC0-5] ³
2x ⁴	010000	N/A (unchanged) ¹	unchanged ¹	N/A (unchanged) ¹	unchanged ¹
3x ⁴	100000	N/A (unchanged) ¹	unchanged ¹	N/A (unchanged) ¹	unchanged ¹
4x ⁴	101000	2x ⁴	010000	N/A (unchanged) ¹	unchanged ¹
5x	101100	2.5x ⁴	010101	N/A (unchanged) ¹	unchanged ¹
5.5x	100100	2.75x ⁴	110101 ²	N/A (unchanged) ¹	unchanged ¹
6x	110100	3x ⁴	100000	N/A (unchanged) ¹	unchanged ¹
6.5x	010100	3.25x ⁴	100000 ²	N/A (unchanged) ¹	unchanged ¹
7x	001000	3.5x ⁴	110101	N/A (unchanged) ¹	unchanged ¹
7.5x	000100	3.75x ⁴	110101 ²	N/A (unchanged) ¹	unchanged ¹
8x	110000	4x ⁴	101000 ⁴	2x ⁴	010000
8.5x	011000	4.25x ⁴	101000 ²	N/A (unchanged) ¹	unchanged ¹
9x	011110	4.5x ⁴	011101	2.25x ⁴	010000 ²
9.5x	011100	4.75x ⁴	011101 ²	N/A (unchanged) ¹	unchanged ¹
10x	101010	5x	101100	2.5x ⁴	010101
10.5x	100010	5.25x	101100 ²	N/A (unchanged) ¹	unchanged ¹
11x	100110	5.5x	100100	2.75x ⁴	010101 ²
11.5x	000000	5.75x	100100 ²	N/A (unchanged) ¹	unchanged ¹
12x	101110	6x	110100	3x ⁴	100000
12.5x	111110	6.25x	110100 ²	N/A (unchanged) ¹	unchanged ¹
13x	010110	6.5x	010100	3.25x ⁴	100000 ²
13.5x	111000	6.75	010100 ²	N/A (unchanged) ¹	unchanged ¹
14x	110010	7x	001000	3.5x ⁴	110101
15x	000110	7.5x	000100	3.75x ⁴	110101 ²
16x	110110	8x	110000	4x ⁴	101000
17x	000010	8.5x	011000	4.25x ⁴	101000 ²
18x	001010	9x	011110	4.5x ⁴	011101
20x	001110	10x	101010	5x	101100
21x	010010	10.5x	100010	5.25x	101100 ²

**Table 20. Part Numbers Addressed by MC7448TxxnnnnNx Series Hardware Specification Addendum
(Document Order No. MPC7448ECS02AD)**

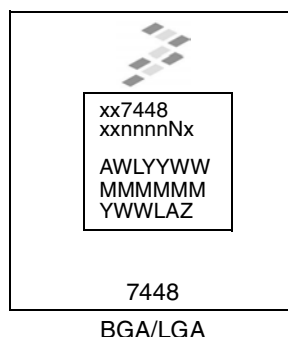
xx	7448	T	xx	nnnn	N	x
Product Code	Part Identifier	Specification Modifier	Package	Processor Frequency	Application Modifier	Revision Level
MC PPC ¹	7448	T = Extended Temperature Device	HX = HCTE BGA	1400	N: 1.15 V ± 50 mV – 40 to 105 °C	C: 2.1; PVR = 0x8004_0201 D: 2.2; PVR = 0x8004_0202
				1267 Revision C only	N: 1.1 V ± 50 mV – 40 to 105 °C	
				1267 Revision D only	N: 1.05 V ± 50 mV – 40 to 105 °C	
				1000	N: 1.0 V ± 50 mV – 40 to 105 °C	

Notes:

- The P prefix in a Freescale part number designates a “Pilot Production Prototype” as defined by Freescale SOP 3-13. These parts have only preliminary reliability and characterization data. Before pilot production prototypes can be shipped, written authorization from the customer must be on file in the applicable sales office acknowledging the qualification status and the fact that product changes may still occur as pilot production prototypes are shipped.

11.3 Part Marking

Parts are marked as the example shown in [Figure 27](#).



Notes:

- AWLYYWW is the test code, where YYWW is the date code (YY = year, WW = work week)
- MMMMMM is the M00 (mask) number.
- YWWLAZ is the assembly traceability code.

Figure 27. Part Marking for BGA and LGA Device

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