

Welcome to E-XFL.COM

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC G4
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.6GHz
Co-Processors/DSP	Multimedia; SIMD
RAM Controllers	-
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	1.5V, 1.8V, 2.5V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	360-BCBGA, FCCBGA
Supplier Device Package	360-FCCBGA (25x25)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc7448hx1600ld

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



MPC7448 RISC Microprocessor Hardware Specifications, Rev. 4

Overview

NM



Features

- Efficient data flow
 - Although the VR/LSU interface is 128 bits, the L1/L2 bus interface allows up to 256 bits.
 - The L1 data cache is fully pipelined to provide 128 bits/cycle to or from the VRs.
 - The L2 cache is fully pipelined to provide 32 bytes per clock every other cycle to the L1 caches.
 - As many as 16 out-of-order transactions can be present on the MPX bus.
 - Store merging for multiple store misses to the same line. Only coherency action taken (address-only) for store misses merged to all 32 bytes of a cache block (no data tenure needed).
 - Three-entry finished store queue and five-entry completed store queue between the LSU and the L1 data cache
 - Separate additional queues for efficient buffering of outbound data (such as castouts and write-through stores) from the L1 data cache and L2 cache
- Multiprocessing support features include the following:
 - Hardware-enforced, MESI cache coherency protocols for data cache
 - Load/store with reservation instruction pair for atomic memory references, semaphores, and other multiprocessor operations
- Power and thermal management
 - Dynamic frequency switching (DFS) feature allows processor core frequency to be halved or quartered through software to reduce power consumption.
 - The following three power-saving modes are available to the system:
 - Nap—Instruction fetching is halted. Only the clocks for the time base, decrementer, and JTAG logic remain running. The part goes into the doze state to snoop memory operations on the bus and then back to nap using a <u>QREQ</u>/<u>QACK</u> processor-system handshake protocol.
 - Sleep—Power consumption is further reduced by disabling bus snooping, leaving only the PLL in a locked and running state. All internal functional units are disabled.
 - Deep sleep—When the part is in the sleep state, the system can disable the PLL. The system
 can then disable the SYSCLK source for greater system power savings. Power-on reset
 procedures for restarting and relocking the PLL must be followed upon exiting the deep
 sleep state.
 - Instruction cache throttling provides control of instruction fetching to limit device temperature.
 - A new temperature diode that can determine the temperature of the microprocessor
- Performance monitor can be used to help debug system designs and improve software efficiency.
- In-system testability and debugging features through JTAG boundary-scan capability
- Testability
 - LSSD scan design
 - IEEE Std. 1149.1TM JTAG interface



Figure 2 shows the undershoot and overshoot voltage on the MPC7448.



Figure 2. Overshoot/Undershoot Voltage

The MPC7448 provides several I/O voltages to support both compatibility with existing systems and migration to future systems. The MPC7448 core voltage must always be provided at the nominal voltage (see Table 4). The input voltage threshold for each bus is selected by sampling the state of the voltage select pins at the negation of the signal HRESET. The output voltage will swing from GND to the maximum voltage applied to the OV_{DD} power pins. Table 3 provides the input threshold voltage settings. Because these settings may change in future products, it is recommended that BVSEL[0:1] be configured using resistor options, jumpers, or some other flexible means, with the capability to reconfigure the termination of this signal in the future, if necessary.

BVSEL0	BVSEL1	I/O Voltage Mode ¹	Notes
0	0	1.8 V	2, 3
0	1	2.5 V	2, 4
1	0	1.5 V	2
1	1	2.5 V	4

Table 3. Input Threshold Voltage Setting

Notes:

- 1. **Caution:** The I/O voltage mode selected must agree with the OV_{DD} voltages supplied. See Table 4.
- 2. If used, pull-down resistors should be less than 250 $\Omega.$
- 3. The pin configuration used to select 1.8V mode on the MPC7448 is not compatible with the pin configuration used to select 1.8V mode on the MPC7447A and earlier devices.
- 4. The pin configuration used to select 2.5V mode on the MPC7448 is fully compatible with the pin configuration used to select 2.5V mode on the MPC7447A and earlier devices.

Table 4 provides the recommended operating conditions for the MPC7448 part numbers described by this document; see Section 11.1, "Part Numbers Fully Addressed by This Document," for more information. See Section 9.2, "Power Supply Design and Sequencing" for power sequencing requirements.

Characteristic			Recommended Value									Notes
		Symbol	ol 1000 MHz		1420 MHz		1600 MHz		1700 MHz		Unit	Notes
			Min	Max	Min	Max	Min	Max	Min	Max		
Core suppl	y voltage	V _{DD}	1.15 V ± 50 mV		1.2 V ± 50 mV		1.25 V ± 50 mV		1.3 V +20/ - 50 mV		V	3, 4, 5
PLL supply	voltage	AV _{DD}	1.15 V	± 50 mV	1.2 V ±	⊧ 50 mV	1.25 V	± 50 mV	1.3 \ - 50	/ +20/) mV	V	2, 3, 4
Processor	I/O Voltage Mode = 1.5 V	OV _{DD}	1.5 V ± 5%		1.5 V ± 5% 1.5 V ±		′ ± 5%	1.5 V	′ ± 5%	V	4	
supply	I/O Voltage Mode = 1.8 V		1.8 V ± 5%		1.8 V ± 5% 1.8 V ± 5%		′ ± 5%	1.8 V ± 5%			4	
voltage	I/O Voltage Mode = 2.5 V	.5 V 2.5 V ± 5% 2.4		2.5 V	2.5 V ± 5% 2.5 V ± 5%		2.5 V ± 5%			4		
Input	Processor bus	V _{in}	GND	OV_{DD}	GND	OV_{DD}	GND	OV_{DD}	GND	OV_DD	V	
voitage	JTAG signals	V _{in}	GND	OV_{DD}	GND	OV_{DD}	GND	OV_{DD}	GND	OV_DD		
Die-junction	n temperature	Тj	0	105	0	105	0	105	0	105	•C	6

Table 4. Recommended Operating Conditions¹

Notes:

1. These are the recommended and tested operating conditions.

2. This voltage is the input to the filter discussed in Section 9.2.2, "PLL Power Supply Filtering," and not necessarily the voltage at the AV_{DD} pin, which may be reduced from V_{DD} by the filter.

3. Some early devices supported voltage and frequency derating whereby VDD (and AVDD) could be reduced to reduce power consumption. This feature has been superseded and is no longer supported. See Section 5.3, "Voltage and Frequency Derating," for more information.

4. Caution: Power sequencing requirements must be met; see Section 9.2, "Power Supply Design and Sequencing".

- 5. Caution: See Section 9.2.3, "Transient Specifications" for information regarding transients on this power supply.
- 6. For information on extended temperature devices, see Section 11.2, "Part Numbers Not Fully Addressed by This Document."



when running a typical benchmark at temperatures in a typical system. The Full-Power Mode–Thermal value is intended to represent the sustained power consumption of the device when running a typical code sequence at high temperature and is recommended to be used as the basis for designing a thermal solution; see Section 9.7, "Power and Thermal Management Information" for more information on thermal solutions. The Full-Power Mode–Maximum value is recommended to be used for power supply design because this represents the maximum peak power draw of the device that a power supply must be capable of sourcing without voltage droop. For information on power consumption when dynamic frequency switching is enabled, see Section 9.7.5, "Dynamic Frequency Switching (DFS)."

	Die Junction	Maximum Pr	Maximum Processor Core Frequency (Speed Grade, MHz)								
	Temperature (T _j)	1000 MHz	1420 MHz	1600 MHz	1700 MHz	Unit	Notes				
Full-Power Mode											
Typical	65 •C	15.0	19.0	20.0	21.0	W	1, 2				
Thermal	105 •C	18.6	23.3	24.4	25.6	W	1, 5				
Maximum	105 •C	21.6	27.1	28.4	29.8	W	1, 3				
Nap Mode											
Typical	105 •C	11.1	11.8	13.0	13.0	W	1, 6				
Sleep Mode											
Typical	105 • C	10.8	11.4	12.5	12.5	W	1, 6				
Deep Sleep Mode (PLL Disabled)											
Typical	105 •C	10.4	11.0	12.0	12.0	W	1, 6				

Table 7. Power Consumption for MPC7448 at Maximum Rated Frequency

Notes:

- These values specify the power consumption for the core power supply (V_{DD}) at nominal voltage and apply to all valid processor bus frequencies and configurations. The values do not include I/O supply power (OV_{DD}) or PLL supply power (AV_{DD}). OV_{DD} power is system dependent but is typically < 5% of V_{DD} power. Worst case power consumption for AV_{DD} < 13 mW. Freescale also offers MPC7448 part numbers that meet lower power consumption specifications; for more information on these devices, see Section 11.2, "Part Numbers Not Fully Addressed by This Document."
- 2. Typical power consumption is an average value measured with the processor operating at its rated maximum processor core frequency (except for Deep Sleep Mode), at nominal recommended V_{DD} (see Table 4) and 65°C while running the Dhrystone 2.1 benchmark and achieving 2.3 Dhrystone MIPs/MHz. This parameter is not 100% tested but periodically sampled.b
- 3. Maximum power consumption is the average measured with the processor operating at its rated maximum processor core frequency, at nominal V_{DD} and maximum operating junction temperature (see Table 4) while running an entirely cache-resident, contrived sequence of instructions to keep all the execution units maximally busy.
- 4. Doze mode is not a user-definable state; it is an intermediate state between full-power and either nap or sleep mode. As a result, power consumption for this mode is not tested.
- Thermal power consumption is an average value measured at the nominal recommended V_{DD} (see Table 4) and 105 °C while running the Dhrystone 2.1 benchmark and achieving 2.3 Dhrystone MIPs/MHz. This parameter is not 100% tested but periodically sampled.
- 6. Typical power consumption for these modes is measured at the nominal recommended V_{DD} (see Table 4) and 105 °C in the mode described. This parameter is not 100% tested but is periodically sampled.



5.2 AC Electrical Characteristics

This section provides the AC electrical characteristics for the MPC7448. After fabrication, functional parts are sorted by maximum processor core frequency as shown in Section 5.2.1, "Clock AC Specifications," and tested for conformance to the AC specifications for that frequency. The processor core frequency, determined by the bus (SYSCLK) frequency and the settings of the PLL_CFG[0:5] signals, can be dynamically modified using dynamic frequency switching (DFS). Parts are sold by maximum processor core frequency; see Section 11, "Part Numbering and Marking," for information on ordering parts. DFS is described in Section 9.7.5, "Dynamic Frequency Switching (DFS)."

5.2.1 Clock AC Specifications

Table 8 provides the clock AC timing specifications as defined in Figure 3 and represents the tested operating frequencies of the devices. The maximum system bus frequency, f_{SYSCLK}, given in Table 8, is considered a practical maximum in a typical single-processor system. This does not exclude multi-processor systems, but these typically require considerably more design effort to achieve the maximum rated bus frequency. The actual maximum SYSCLK frequency for any application of the MPC7448 will be a function of the AC timings of the microprocessor(s), the AC timings for the system controller, bus loading, circuit board topology, trace lengths, and so forth, and may be less than the value given in Table 8.



Table 8. Clock AC Timing Specifications

At recommended operating conditions. See Table 4.

			Maximum Processor Core Frequency (Speed Grade)									
Characteristic		Symbol	1000	MHz	1420	MHz	1600 MHz		1700 MHz		Unit	Notes
			Min	Max	Min	Max	Min	Max	Min	Max		
Processor	DFS mode disabled	f _{core}	600	1000	600	1420	600	1600	600	1700	MHz	1, 8
core frequency	DFS mode enabled	f _{core_DF}	300	500	300	710	300	800	300	850		9
VCO frequency		f _{VCO}	600	1000	600	1420	600	800	600	1700	MHz	1, 10
SYSCLK fre	equency	f _{SYSCLK}	33	200	33	200	33	200	33	200	MHz	1, 2, 8
SYSCLK cy	cle time	t _{SYSCLK}	5.0	30	5.0	30	5.0	30	5.0	30	ns	2
SYSCLK ris	e and fall time	t _{KR} , t _{KF}	—	0.5		0.5	_	0.5		0.5	ns	3
SYSCLK duty cycle measured at OV _{DD} /2		t _{KHKL} ∕ t _{SYSCLK}	40	60	40	60	40	60	40	60	%	4
SYSCLK cycle-to-cycle jitter			—	150	_	150	_	150	_	150	ps	5, 6
Internal PLL	relock time		_	100	_	100	_	100	_	100	μs	7

Notes:

- 1. **Caution**: The SYSCLK frequency and PLL_CFG[0:5] settings must be chosen such that the resulting SYSCLK (bus) frequency, processor core frequency, and PLL (VCO) frequency do not exceed their respective maximum or minimum operating frequencies. Refer to the PLL_CFG[0:5] signal description in Section 9.1.1, "PLL Configuration," for valid PLL_CFG[0:5] settings.
- 2. Actual maximum system bus frequency is system-dependent. See Section 5.2.1, "Clock AC Specifications."
- 3. Rise and fall times for the SYSCLK input measured from 0.4 to 1.4 V
- 4. Timing is guaranteed by design and characterization.
- 5. Guaranteed by design
- 6. The SYSCLK driver's closed loop jitter bandwidth should be less than 1.5 MHz at -3 dB.
- 7. Relock timing is guaranteed by design and characterization. PLL-relock time is the maximum amount of time required for PLL lock after a stable V_{DD} and SYSCLK are reached during the power-on reset sequence. This specification also applies when the PLL has been disabled and subsequently re-enabled during sleep mode. Also note that HRESET must be held asserted for a minimum of 255 bus clocks after the PLL-relock time during the power-on reset sequence.
- 8. This reflects the maximum and minimum core frequencies when the dynamic frequency switching feature (DFS) is disabled. f_{core DFS} provides the maximum and minimum core frequencies when operating in a DFS mode.
- 9. This specification supports the Dynamic Frequency Switching (DFS) feature and is applicable only when one of the DFS modes (divide-by-2 or divide-by-4) is enabled. When DFS is disabled, the core frequency must conform to the maximum and minimum frequencies stated for f_{core}.
- 10.Use of the DFS feature does not affect VCO frequency.



Figure 4 provides the AC test load for the MPC7448.



Figure 5 provides the BMODE[0:1] input timing diagram for the MPC7448. These mode select inputs are sampled once before and once after HRESET negation.



Figure 5. BMODE[0:1] Input Sample Timing Diagram







Figure 6. Input/Output Timing Diagram



Figure 7 provides the AC test load for TDO and the boundary-scan outputs of the MPC7448.



Figure 7. Alternate AC Test Load for the JTAG Interface

Figure 8 provides the JTAG clock input timing diagram.



Figure 8. JTAG Clock Input Timing Diagram

Figure 9 provides the $\overline{\text{TRST}}$ timing diagram.



Figure 9. TRST Timing Diagram

Figure 10 provides the boundary-scan timing diagram.



Figure 10. Boundary-Scan Timing Diagram

MPC7448 RISC Microprocessor Hardware Specifications, Rev. 4



Table 11. Pinout Listing for the MPC7448, 360 HCTE Package (continued)

Signal Name	Pin Number	Active	I/O	Notes
VDD_SENSE	G13, N12			18

Notes:

1. OV_{DD} supplies power to the processor bus, JTAG, and all control signals, and is configurable. (V_{DD} supplies power to the processor core, and AV_{DD} supplies power to the PLL after filtering from V_{DD}). To program the I/O voltage, see Table 3. If used, the pull-down resistor should be less than 250 Ω . Because these settings may change in future products, it is recommended BVSEL[0:1] be configured using resistor options, jumpers, or some other flexible means, with the capability to reconfigure the termination of this signal in the future if necessary. For actual recommended value of V_{in} or supply voltages see Table 4.

2. Unused address pins must be pulled down to GND and corresponding address parity pins pulled up to OV_{DD}.

3. These pins require weak pull-up resistors (for example, 4.7 KΩ) to maintain the control signals in the negated state after they have been actively negated and released by the MPC7448 and other bus masters.

4. This signal selects between MPX bus mode (asserted) and 60x bus mode (negated) and will be sampled at HRESET going high.

5. This signal must be negated during reset, by pull-up resistor to OV_{DD} or negation by ¬HRESET (inverse of HRESET), to ensure proper operation.

6. Internal pull up on die.

7. Not used in 60x bus mode.

8. These signals must be pulled down to GND if unused, or if the MPC7448 is in 60x bus mode.

9. These input signals are for factory use only and must be pulled down to GND for normal machine operation.

10. This test signal is recommended to be tied to HRESET; however, other configurations will not adversely affect performance.

11. These signals are for factory use only and must be left unconnected for normal machine operation. Some pins that were NCs on the MPC7447, MPC7445, and MPC7441 have now been defined for other purposes.

- 12. These input signals are for factory use only and must be pulled up to OV_{DD} for normal machine operation.
- 13. This pin can externally cause a performance monitor event. Counting of the event is enabled through software.
- 14. This signal must be asserted during reset, by pull down to GND or assertion by HRESET, to ensure proper operation.
- 15. These pins were NCs on the MPC7447, MPC7445, and MPC7441. See Section 9.3, "Connection Recommendations," for more information.
- 16. These pins were OV_{DD} pins on the MPC7447, MPC7445, and MPC7441. These pins are internally connected to OV_{DD} and are intended to allow an external device (such as a power supply) to detect the I/O voltage level present inside the device package. If unused, it is recommended they be connected to test points to facilitate system debug; otherwise, they may be connected directly to OV_{DD} or left unconnected.
- 17. These pins provide connectivity to the on-chip temperature diode that can be used to determine the die junction temperature of the processor. These pins may be left unterminated if unused.
- 18. These pins are internally connected to V_{DD} and are intended to allow an external device (such as a power supply) to detect the processor core voltage level present inside the device package. If unused, it is recommended they be connected to test points to facilitate system debug; otherwise, they may be connected directly to V_{DD} or left unconnected.
- 19. These pins are internally connected to GND and are intended to allow an external device to detect the processor ground voltage level present inside the device package. If unused, it is recommended they be connected to test points to facilitate system debug; otherwise, they may be connected directly to GND or left unconnected.
- 20. These pins were in the TEST[0:4] factory test pin group on the MPC7447A, MPC7447, MPC7445, and MPC7441. They have been assigned new functions on the MPC7448.
- 21. These pins can be used to enable the supported dynamic frequency switching (DFS) modes via hardware. If both are pulled down, DFS mode is disabled completely and cannot be enabled via software. If unused, they should be pulled up to OV_{DD} to allow software control of DFS. See the *MPC7450 RISC Microprocessor Family Reference Manual* for more information.
- 22. This pin is provided to allow operation of the L2 cache at low core voltages and is for factory use only. See the MPC7450 RISC Microprocessor Family Reference Manual for more information.



8 Package Description

The following sections provide the package parameters and mechanical dimensions for the HCTE package.

8.1 Package Parameters for the MPC7448, 360 HCTE BGA

The package parameters are as provided in the following list. The package type is 25×25 mm, 360-lead high coefficient of thermal expansion ceramic ball grid array (HCTE).

Package outline	$25 \times 25 \text{ mm}$					
Interconnects	360 (19 \times 19 ball array – 1)					
Pitch	1.27 mm (50 mil)					
Minimum module height	2.32 mm					
Maximum module height	2.80 mm					
Ball diameter 0.89 mm (35 mil)						
Coefficient of thermal expansion12.3 ppm/°C						



Package Description

8.2 Mechanical Dimensions for the MPC7448, 360 HCTE BGA

Figure 13 provides the mechanical dimensions and bottom surface nomenclature for the MPC7448, 360 HCTE BGA package.



Figure 13. Mechanical Dimensions and Bottom Surface Nomenclature for the MPC7448, 360 HCTE BGA Package



System Design Information

These requirements are shown graphically in Figure 16.



Figure 16. MPC7448 Power Up Sequencing Requirements

Certain stipulations also apply to the manner in which the power rails of the MPC7448 power down, as follows:

- OV_{DD} may ramp down any time before or after V_{DD}.
- The voltage at the SYSCLK input must not exceed V_{DD} once V_{DD} has ramped down below 0.9 V.
- The voltage at the SYSCLK input must not exceed OV_{DD} by more 20% during transients (see overshoot/undershoot specifications in Figure 2) or 0.3 V DC (see Table 2) at any time.



9.2.4 Decoupling Recommendations

Due to the MPC7448 dynamic power management feature, large address and data buses, and high operating frequencies, the MPC7448 can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the MPC7448 system, and the MPC7448 itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer use sufficient decoupling capacitors, typically one capacitor for every V_{DD} pin, and a similar amount for the OV_{DD} pins, placed as close as possible to the power pins of the MPC7448. It is also recommended that these decoupling capacitors receive their power from separate V_{DD} , OV_{DD}, and GND power planes in the PCB, using short traces to minimize inductance.

These capacitors should have a value of 0.01 or 0.1 μ F. Only ceramic surface mount technology (SMT) capacitors should be used to minimize lead inductance. Orientations where connections are made along the length of the part, such as 0204, are preferable but not mandatory. Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993) and contrary to previous recommendations for decoupling Freescale microprocessors, multiple small capacitors of equal value are recommended over using multiple values of capacitance.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V_{DD} and OV_{DD} planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low equivalent series resistance (ESR) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors are 100–330 μ F (AVX TPS tantalum or Sanyo OSCON).

9.3 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. Unless otherwise noted, unused active low inputs should be tied to OV_{DD} and unused active high inputs should be connected to GND. All NC (no connect) signals must remain unconnected.

Power and ground connections must be made to all external V_{DD} , OV_{DD} , and GND pins in the MPC7448. For backward compatibility with the MPC7447, MPC7445, and MP7441, or for migrating a system originally designed for one of these devices to the MPC7448, the new power and ground signals (formerly NC, see Table 11) may be left unconnected if the core frequency is 1 GHz or less. Operation above 1 GHz requires that these additional power and ground signals be connected, and it is strongly recommended that all new designs include the additional connections. See also Section 7, "Pinout Listings," for additional information.

The MPC7448 provides VDD_SENSE, OVDD_SENSE, and GND_SENSE pins. These pins connect directly to the power/ground planes in the device package and are intended to allow an external device to measure the voltage present on the V_{DD} , OV_{DD} and GND planes in the device package. The most common use for these signals is as a feedback signal to a power supply regulator to allow it to compensate for board losses and supply the correct voltage at the device. (Note that all voltage parameters are specified at the pins of the device.) If not used for this purpose, it is recommended that these signals be connected to test points that can be used in the event that an accurate measurement of the voltage at the device is needed during system debug. Otherwise, these signals should be connected to the appropriate power/ground planes on the circuit board or left unconnected.

likewise be pulled up through a pull-up resistor (weak or stronger: 4.7–1 K Ω) to prevent erroneous assertions of this signal.

In addition, the MPC7448 has one open-drain style output that requires a pull-up resistor (weak or stronger: $4.7-1 \text{ K}\Omega$) if it is used by the system. This pin is CKSTP_OUT.

BVSEL0 and BVSEL1 should not be allowed to float, and should be configured either via pull-up or pull-down resistors or actively driven by external logic. If pull-down resistors are used to configure BVSEL0 or BVSEL1, the resistors should be less than 250 Ω (see Table 11). Because PLL_CFG[0:5] must remain stable during normal operation, strong pull-up and pull-down resistors (1 K Ω or less) are recommended to configure these signals in order to protect against erroneous switching due to ground bounce, power supply noise, or noise coupling.

During inactive periods on the bus, the address and transfer attributes may not be driven by any master and may, therefore, float in the high-impedance state for relatively long periods of time. Because the MPC7448 must continually monitor these signals for snooping, this float condition may cause excessive power draw by the input receivers on the MPC7448 or by other receivers in the system. These signals can be pulled up through weak (10-K Ω) pull-up resistors by the system, address bus driven mode enabled (see the *MPC7450 RISC Microprocessor Family Users' Manual* for more information on this mode), or they may be otherwise driven by the system during inactive periods of the bus to avoid this additional power draw. Preliminary studies have shown the additional power draw by the MPC7448 input receivers to be negligible and, in any event, none of these measures are necessary for proper device operation. The snooped address and transfer attribute inputs are: A[0:35], AP[0:4], TT[0:4], \overline{CI} , \overline{WT} , and \overline{GBL} .

If address or data parity is not used by the system, and respective parity checking is disabled through HID1, the input receivers for those pins are disabled and do not require pull-up resistors, therefore they may be left unconnected by the system. If extended addressing is not used (HID0[XAEN] = 0), A[0:3] are unused and must be pulled low to GND through weak pull-down resistors; additionally, if address parity checking is enabled (HID1[EBA] = 1) and extended addressing is not used, AP[0] must be pulled up to OV_{DD} through a weak pull-up resistor. If the MPC7448 is in 60x bus mode, DTI[0:3] must be pulled low to GND through weak pull-down resistors.

The data bus input receivers are normally turned off when no read operation is in progress and, therefore, do not require pull-up resistors on the bus. Other data bus receivers in the system, however, may require pull-ups or require that those signals be otherwise driven by the system during inactive periods. The data bus signals are D[0:63] and DP[0:7].

9.6 JTAG Configuration Signals

Boundary-scan testing is enabled through the JTAG interface signals. The TRST signal is optional in the IEEE 1149.1 standard specification, but is typically provided on all processors that implement the PowerPC architecture. While it is possible to force the TAP controller to the reset state using only the TCK and TMS signals, more reliable power-on reset performance will be obtained if the TRST signal is asserted during power-on reset. Because the JTAG interface is also used for accessing the common on-chip processor (COP) function, simply tying TRST to HRESET is not practical.

The COP function of these processors allows a remote computer system (typically a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert HRESET or TRST in order



System Design Information

to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must be merged into these signals with logic.

The arrangement shown in Figure 21 allows the COP port to independently assert HRESET or TRST, while ensuring that the target can drive HRESET as well. If the JTAG interface and COP header will not be used, TRST should be tied to HRESET through a 0- Ω isolation resistor so that it is asserted when the system reset signal (HRESET) is asserted, ensuring that the JTAG scan chain is initialized during power-on. Although Freescale recommends that the COP header be designed into the system as shown in Figure 21, if this is not possible, the isolation resistor will allow future access to TRST in the case where a JTAG interface may need to be wired onto the system in debug situations.

The COP header shown in Figure 21 adds many benefits—breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features are possible through this interface—and can be as inexpensive as an unpopulated footprint for a header to be added when needed.

The COP interface has a standard header for connection to the target system, based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header). The connector typically has pin 14 removed as a connector key.

There is no standardized way to number the COP header shown in Figure 21; consequently, many different pin numbers have been observed from emulator vendors. Some are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom, while still others number the pins counter clockwise from pin 1 (as with an IC). Regardless of the numbering, the signal placement recommended in Figure 21 is common to all known emulators.

The \overline{QACK} signal shown in Figure 21 is usually connected to the bridge chip or other system control logic in a system and is an input to the MPC7448 informing it that it can go into the quiescent state. Under normal operation this occurs during a low-power mode selection. In order for COP to work, the MPC7448 must see this signal asserted (pulled down). While shown on the COP header, not all emulator products drive this signal. If the product does not, a pull-down resistor can be populated to assert this signal. Additionally, some emulator products implement open-drain type outputs and can only drive \overline{QACK} asserted; for these tools, a pull-up resistor can be implemented to ensure this signal is negated when it is not being driven by the tool. Note that the pull-up and pull-down resistors on the \overline{QACK} signal are mutually exclusive and it is never necessary to populate both in a system. To preserve correct power-down operation, \overline{QACK} should be merged through logic so that it also can be driven by the bridge or system logic.



System Design Information

9.7 Power and Thermal Management Information

This section provides thermal management information for the high coefficient of thermal expansion (HCTE) package for air-cooled applications. Proper thermal control design is primarily dependent on the system-level design—the heat sink, airflow, and thermal interface material. The MPC7448 implements several features designed to assist with thermal management, including DFS and the temperature diode. DFS reduces the power consumption of the device by reducing the core frequency; see Section 9.7.5.1, "Power Consumption with DFS Enabled," for specific information regarding power reduction and DFS. The temperature diode allows an external device to monitor the die temperature in order to detect excessive temperature conditions and alert the system; see Section 9.7.4, "Temperature Diode," for more information.

To reduce the die-junction temperature, heat sinks may be attached to the package by several methods—spring clip to holes in the printed-circuit board or package, and mounting clip and screw assembly (see Figure 22); however, due to the potential large mass of the heat sink, attachment through the printed-circuit board is suggested. In any implementation of a heat sink solution, the force on the die should not exceed ten pounds (45 Newtons).



Figure 22. BGA Package Exploded Cross-Sectional View with Several Heat Sink Options

NOTE

A clip on heat sink is not recommended for LGA because there may not be adequate clearance between the device and the circuit board. A through-hole solution is recommended, as shown in Figure 23.



Due to the complexity and variety of system-level boundary conditions for today's microelectronic equipment, the combined effects of the heat transfer mechanisms (radiation, convection, and conduction) may vary widely. For these reasons, we recommend using conjugate heat transfer models for the board as well as system-level designs.

For system thermal modeling, the MPC7448 thermal model is shown in Figure 26. Four volumes represent this device. Two of the volumes, solder ball-air and substrate, are modeled using the package outline size of the package. The other two, die and bump-underfill, have the same size as the die. The silicon die should be modeled $8.0 \times 7.3 \times 0.86$ mm³ with the heat source applied as a uniform source at the bottom of the volume. The bump and underfill layer is modeled as $8.0 \times 7.3 \times 0.07$ mm³ collapsed in the z-direction with a thermal conductivity of 5.0 W/(m • K) in the z-direction. The substrate volume is $25 \times 25 \times 1.14$ mm³ and has 9.9 W/(m • K) isotropic conductivity in the xy-plane and 2.95 W/(m • K) in the direction of the z-axis. The solder ball and air layer are modeled with the same horizontal dimensions as the substrate and is 0.8 mm thick. For the LGA package the solder and air layer is 0.1 mm thick, but the material properties are the same. It can also be modeled as a collapsed volume using orthotropic material properties: 0.034 W/(m • K) in the xy-plane direction and 11.2 W/(m • K) in the direction of the z-axis.

$\begin{tabular}{ c c c c } \hline \hline Die & \hline \hline Die & \hline \hline Die & \hline \hline \hline \hline & \hline $	Conductivity	Value	Unit			
zBump and UnderfillSiliconTemperature- dependentW/(m • K)Bump and Underfill (8.0 × 7.3 × 0.07 mm³)Solder and Air k_z 5.0W/(m • K) k_z 5.0W/(m • K)Substrate (25 × 25 × 1.14 mm³)W/(m • K) k_χ 9.9W/(m • K) k_z 2.95Die k_x 0.034W/(m • K) k_χ 0.034W/(m • K)	Die (8.0 \times 7.3 \times 0.86 mm ³)			,	•	Die
SiliconTemperature- dependent $W/(m \cdot K)$ Bump and Underfill (8.0 × 7.3 × 0.07 mm³) $Solder and Air$ kz5.0 $W/(m \cdot K)$ kx9.9 $W/(m \cdot K)$ kz9.9 $W/(m \cdot K)$ kz2.95Solder Ball and Air (25 × 25 × 0.8 mm³) Die kx0.034 $W/(m \cdot K)$						Bump and Underfill
Solder and AirSolder and AirKz 5.0 W/(m • K)Substrate (25 × 25 × 1.14 mm³)Side View of Model (Not to Scale) k_x 9.9 W/(m • K) k_y 9.9 W/(m • K) k_z 2.95 Solder Ball and Air (25 × 25 × 0.8 mm³)Die k_x 0.034 W/(m • K)	Silicon	Temperature- dependent	W/(m • K)			Substrate
Substrate (3.5 × 1.6 × 0.01 mm) k_z 5.0 $W/(m \cdot K)$ Substrate (25 × 25 × 1.14 mm³) $W/(m \cdot K)$ k_x 9.9 $W/(m \cdot K)$ k_z 2.95Solder Ball and Air (25 × 25 × 0.8 mm³) Die k_x 0.034 $W/(m \cdot K)$	Bump and Un	derfill (8.0 × 7.3 × 0.07)	-		Solder and Air	
$ \begin{array}{ c c c c } \hline k_z & 5.0 & W/(m \cdot K) \\ \hline Substrate (25 \times 25 \times 1.14 mm^3) \\ \hline k_x & 9.9 & W/(m \cdot K) \\ \hline k_y & 9.9 & \\ \hline k_z & 2.95 & \\ \hline \hline Solder Ball and Air (25 \times 25 \times 0.8 mm^3) \\ \hline k_x & 0.034 & W/(m \cdot K) \\ \hline k_y & 0.034 & \\ \hline \end{array} $	Bump and Underini (8.0 × 7.3 × 0.07 mm ⁺)				Side	View of Model (Not to Scale)
Substrate (25 × 25 × 1.14 mm ³) k_x 9.9 W/(m • K) k_y 9.9 W/(m • K) k_z 2.95 Die Die k_x 0.034 W/(m • K) k_y 0.034 W/(m • K)	kz	5.0	W/(m ∙ K)			
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	Substrate (25 \times 25 \times 1.14 mm ³)				<u> </u>	→
k _y 9.9 Substrate k _z 2.95 k_z b_z Solder Ball and Air (25 × 25 × 0.8 mm ³) Die Die k _x 0.034 $W/(m \cdot K)$ $M/(m \cdot K)$	k _x	9.9	W/(m • K)			Orthostwate
$\begin{tabular}{ c c c c c } \hline k_z & 2.95 & \\ \hline Solder Ball $and Air (25 \times 25 \times 0.8 mm^3)$ \\ \hline k_x & 0.034 & \\ \hline k_y & 0.034 & \\ \hline \end{tabular}$	k _y	9.9				Substrate
Solder Ball and Air (25 × 25 × 0.8 mm ³) k _x 0.034 W/(m • K) k _y 0.034 W/(m • K)	k _z	2.95				
k _x 0.034 W/(m ⋅ K) k _y 0.034 Image: W/(m ⋅ K)	Solder Ball and Air (25 $ imes$ 25 $ imes$ 0.8 mm ³)					Die
k _y 0.034	k _x	0.034	W/(m • K)	1		
	k _y	0.034				
k _z 11.2 y	k _z	11.2		У		

Top View of Model (Not to Scale)

Figure 26. Recommended Thermal Model of MPC7448



11 Part Numbering and Marking

Ordering information for the part numbers fully covered by this specification document is provided in Section 11.1, "Part Numbers Fully Addressed by This Document." Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact a local Freescale sales office. In addition to the processor frequency, the part numbering scheme also includes an application modifier that may specify special application conditions. An optional specification modifier may also apply for parts to indicate a specific change in specifications, such as support for an extended temperature range. Finally, each part number contains a revision level code that refers to the die mask revision number. Section 11.2, "Part Numbers Not Fully Addressed by This Document," lists the part numbers that do not fully conform to the specifications of this document. These special part numbers require an additional document called a hardware specification addendum.

11.1 Part Numbers Fully Addressed by This Document

Table 18 provides the Freescale part numbering nomenclature for the MPC7448 part numbers fully addressed by this document. For information regarding other MPC7448 part numbers, see Section 11.2, "Part Numbers Not Fully Addressed by This Document."

XX	7448	XX	nnnn	L	X
Product Code	Part Identifier	Package	Processor Frequency	Application Modifier	Revision Level
MC PPC ¹	7448	HX = HCTE BGA VS = RoHS LGA	1700	L: 1.3 V +20/–50 mV 0 to 105 °C	C: 2.1; PVR = 0x8004_0201 D: 2.2; PVR = 0x8004_0202
		VU = ROHS BGA	1600	L: 1.25 V ± 50 mV 0 to 105 °C	
			1420	L: 1.2 V ± 50 mV 0 to 105 °C	
			1000	L: 1.15 V ± 50 mV 0 to 105 °C	

Table 18. Part Numbering Nomenclature

Notes:

1. The P prefix in a Freescale part number designates a "Pilot Production Prototype" as defined by Freescale SOP 3-13. These parts have only preliminary reliability and characterization data. Before pilot production prototypes may be shipped, written authorization from the customer must be on file in the applicable sales office acknowledging the qualification status and the fact that product changes may still occur as pilot production prototypes are shipped.