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#### Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

### Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

#### Details

Product Status	Obsolete
Core Processor	PowerPC G4
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.0GHz
Co-Processors/DSP	Multimedia; SIMD
RAM Controllers	-
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	1.5V, 1.8V, 2.5V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	360-CLGA, FCCLGA
Supplier Device Package	360-FCCLGA (25x25)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc7448vs1000lc

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



#### Electrical and Thermal Characteristics

Figure 2 shows the undershoot and overshoot voltage on the MPC7448.



Figure 2. Overshoot/Undershoot Voltage

The MPC7448 provides several I/O voltages to support both compatibility with existing systems and migration to future systems. The MPC7448 core voltage must always be provided at the nominal voltage (see Table 4). The input voltage threshold for each bus is selected by sampling the state of the voltage select pins at the negation of the signal HRESET. The output voltage will swing from GND to the maximum voltage applied to the  $OV_{DD}$  power pins. Table 3 provides the input threshold voltage settings. Because these settings may change in future products, it is recommended that BVSEL[0:1] be configured using resistor options, jumpers, or some other flexible means, with the capability to reconfigure the termination of this signal in the future, if necessary.

BVSEL0	BVSEL1	I/O Voltage Mode <sup>1</sup>	Notes
0	0	1.8 V	2, 3
0	1	2.5 V	2, 4
1	0	1.5 V	2
1	1	2.5 V	4

Table 3. Input Threshold Voltage Setting

Notes:

- 1. **Caution:** The I/O voltage mode selected must agree with the OV<sub>DD</sub> voltages supplied. See Table 4.
- 2. If used, pull-down resistors should be less than 250  $\Omega.$
- 3. The pin configuration used to select 1.8V mode on the MPC7448 is not compatible with the pin configuration used to select 1.8V mode on the MPC7447A and earlier devices.
- 4. The pin configuration used to select 2.5V mode on the MPC7448 is fully compatible with the pin configuration used to select 2.5V mode on the MPC7447A and earlier devices.



### **Electrical and Thermal Characteristics**

when running a typical benchmark at temperatures in a typical system. The Full-Power Mode–Thermal value is intended to represent the sustained power consumption of the device when running a typical code sequence at high temperature and is recommended to be used as the basis for designing a thermal solution; see Section 9.7, "Power and Thermal Management Information" for more information on thermal solutions. The Full-Power Mode–Maximum value is recommended to be used for power supply design because this represents the maximum peak power draw of the device that a power supply must be capable of sourcing without voltage droop. For information on power consumption when dynamic frequency switching is enabled, see Section 9.7.5, "Dynamic Frequency Switching (DFS)."

	Die Junction	Maximum Pr		Notos							
	Temperature (T <sub>j</sub> )	1000 MHz	1000 MHz 1420 MHz 1600 MHz		1700 MHz	Unit	Notes				
	Full-Power Mode										
Typical	65 <b>•C</b>	15.0	19.0	20.0	21.0	W	1, 2				
Thermal	105 <b>•C</b>	18.6	23.3	24.4	25.6	W	1, 5				
Maximum	105 <b>•C</b>	21.6	27.1	28.4	29.8	W	1, 3				
			Nap Mod	e	·						
Typical	105 <b>•C</b>	11.1	11.8	13.0	13.0	W	1, 6				
			Sleep Mod	le							
Typical	105 <b>•</b> C	10.8	11.4	12.5	12.5	W	1, 6				
	Deep Sleep Mode (PLL Disabled)										
Typical	105 <b>•C</b>	10.4	11.0	12.0	12.0	W	1, 6				

### Table 7. Power Consumption for MPC7448 at Maximum Rated Frequency

Notes:

- These values specify the power consumption for the core power supply (V<sub>DD</sub>) at nominal voltage and apply to all valid processor bus frequencies and configurations. The values do not include I/O supply power (OV<sub>DD</sub>) or PLL supply power (AV<sub>DD</sub>). OV<sub>DD</sub> power is system dependent but is typically < 5% of V<sub>DD</sub> power. Worst case power consumption for AV<sub>DD</sub> < 13 mW. Freescale also offers MPC7448 part numbers that meet lower power consumption specifications; for more information on these devices, see Section 11.2, "Part Numbers Not Fully Addressed by This Document."
- 2. Typical power consumption is an average value measured with the processor operating at its rated maximum processor core frequency (except for Deep Sleep Mode), at nominal recommended V<sub>DD</sub> (see Table 4) and 65°C while running the Dhrystone 2.1 benchmark and achieving 2.3 Dhrystone MIPs/MHz. This parameter is not 100% tested but periodically sampled.b
- 3. Maximum power consumption is the average measured with the processor operating at its rated maximum processor core frequency, at nominal V<sub>DD</sub> and maximum operating junction temperature (see Table 4) while running an entirely cache-resident, contrived sequence of instructions to keep all the execution units maximally busy.
- 4. Doze mode is not a user-definable state; it is an intermediate state between full-power and either nap or sleep mode. As a result, power consumption for this mode is not tested.
- Thermal power consumption is an average value measured at the nominal recommended V<sub>DD</sub> (see Table 4) and 105 °C while running the Dhrystone 2.1 benchmark and achieving 2.3 Dhrystone MIPs/MHz. This parameter is not 100% tested but periodically sampled.
- 6. Typical power consumption for these modes is measured at the nominal recommended V<sub>DD</sub> (see Table 4) and 105 °C in the mode described. This parameter is not 100% tested but is periodically sampled.



## 5.2 AC Electrical Characteristics

This section provides the AC electrical characteristics for the MPC7448. After fabrication, functional parts are sorted by maximum processor core frequency as shown in Section 5.2.1, "Clock AC Specifications," and tested for conformance to the AC specifications for that frequency. The processor core frequency, determined by the bus (SYSCLK) frequency and the settings of the PLL\_CFG[0:5] signals, can be dynamically modified using dynamic frequency switching (DFS). Parts are sold by maximum processor core frequency; see Section 11, "Part Numbering and Marking," for information on ordering parts. DFS is described in Section 9.7.5, "Dynamic Frequency Switching (DFS)."

### 5.2.1 Clock AC Specifications

Table 8 provides the clock AC timing specifications as defined in Figure 3 and represents the tested operating frequencies of the devices. The maximum system bus frequency, f<sub>SYSCLK</sub>, given in Table 8, is considered a practical maximum in a typical single-processor system. This does not exclude multi-processor systems, but these typically require considerably more design effort to achieve the maximum rated bus frequency. The actual maximum SYSCLK frequency for any application of the MPC7448 will be a function of the AC timings of the microprocessor(s), the AC timings for the system controller, bus loading, circuit board topology, trace lengths, and so forth, and may be less than the value given in Table 8.



Figure 4 provides the AC test load for the MPC7448.



Figure 5 provides the BMODE[0:1] input timing diagram for the MPC7448. These mode select inputs are sampled once before and once after HRESET negation.



Figure 5. BMODE[0:1] Input Sample Timing Diagram



### 5.2.3 IEEE Std. 1149.1 AC Timing Specifications

Table 10 provides the IEEE Std. 1149.1 (JTAG) AC timing specifications as defined in Figure 8 through Figure 11.

Table 10. JTAG AC Timing Specifications (Independent of SYSCLK)<sup>1</sup>

At recommended operating conditions. See Table 4.

Parameter	Symbol	Min	Мах	Unit	Notes
TCK frequency of operation	f <sub>TCLK</sub>	0	33.3	MHz	
TCK cycle time	t <sub>TCLK</sub>	30	—	ns	
TCK clock pulse width measured at 1.4 V	t <sub>JHJL</sub>	15	—	ns	
TCK rise and fall times	$t_{\rm JR}$ and $t_{\rm JF}$	—	2	ns	
TRST assert time	t <sub>TRST</sub>	25	—	ns	2
Input setup times: Boundary-scan data TMS, TDI	t <sub>DVJH</sub> t <sub>IVJH</sub>	4 0	_	ns	3
Input hold times: Boundary-scan data TMS, TDI	<sup>t</sup> DXJH t <sub>IXJH</sub>	20 25		ns	3
Valid times: Boundary-scan data TDO	t <sub>JLDV</sub> t <sub>JLOV</sub>	4 4	20 25	ns	4
Output hold times: Boundary-scan data TDO	t <sub>JLDX</sub> t <sub>JLOX</sub>	30 30	—	ns	4
TCK to output high impedance: Boundary-scan data TDO	t <sub>JLDZ</sub> t <sub>JLOZ</sub>	3 3	19 9	ns	4, 5

Notes:

 All outputs are measured from the midpoint voltage of the falling/rising edge of TCLK to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load (see Figure 7). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.

2. TRST is an asynchronous level sensitive signal. The time is for test purposes only.

3. Non-JTAG signal input timing with respect to TCK.

4. Non-JTAG signal output timing with respect to TCK.

5. Guaranteed by design and characterization.



Figure 11 provides the test access port timing diagram.



Figure 11. Test Access Port Timing Diagram

### 5.3 Voltage and Frequency Derating

Voltage and frequency derating is no longer supported for part numbers described by this document beginning with datecode 0613. (See Section 11, "Part Numbering and Marking," for information on date code markings.) It is supported by some MPC7448 part numbers which target low-power applications; see Section 11.2, "Part Numbers Not Fully Addressed by This Document" and the referenced MPC7448 Hardware Specification Addenda for more information on these low-power devices. For those devices which previously supported this feature, information has been archived in the *Chip Errata for the MPC7448* (document order no. MPC7448CE).



**Pinout Listings** 

Signal Name	Pin Number	Active	I/O	Notes
A[0:35]	E11, H1, C11, G3, F10, L2, D11, D1, C10, G2, D12, L3, G4, T2, F4, V1, J4, R2, K5, W2, J2, K4, N4, J3, M5, P5, N3, T1, V2, U1, N5, W1, B12, C4, G10, B11	High	I/O	2
AACK	R1	Low	Input	
AP[0:4]	C1, E3, H6, F5, G7	High	I/O	2
ARTRY	N2	Low	I/O	3
AV <sub>DD</sub>	A8	_	Input	
BG	M1	Low	Input	
BMODE0	G9	Low	Input	4
BMODE1	F8	Low	Input	5
BR	D2	Low	Output	
BVSEL0	B7	High	Input	1,6
BVSEL1	E10	High	Input	1, 20
CI	J1	Low	Output	
CKSTP_IN	A3	Low	Input	
CKSTP_OUT	B1	Low	Output	
CLK_OUT	H2	High	Output	
D[0:63]	R15, W15, T14, V16, W16, T15, U15, P14, V13, W13, T13, P13, U14, W14, R12, T12, W12, V12, N11, N10, R11, U11, W11, T11, R10, N9, P10, U10, R9, W10, U9, V9, W5, U6, T5, U5, W7, R6, P7, V6, P17, R19, V18, R18, V19, T19, U19, W19, U18, W17, W18, T16, T18, T17, W3, V17, U4, U8, U7, R7, P6, R8, W8, T8	High	I/O	
DBG	M2	Low	Input	
DFS2	A12	Low	Input	20, 21
DFS4	B6	Low	Input	12, 20, 21
DP[0:7]	T3, W4, T4, W9, M6, V3, N8, W6	High	I/O	
DRDY	R3	Low	Output	7
DTI[0:3]	G1, K1, P1, N1	High	Input	8
EXT_QUAL	A11	High	Input	9
GBL	E2	Low	I/O	
GND	B5, C3, D6, D13, E17, F3, G17, H4, H7, H9, H11, H13, J6, J8, J10, J12, K7, K3, K9, K11, K13, L6, L8, L10, L12, M4, M7, M9, M11, M13, N7, P3, P9, P12, R5, R14, R17, T7, T10, U3, U13, U17, V5, V8, V11, V15		_	
GND	A17, A19, B13, B16, B18, E12, E19, F13, F16, F18, G19, H18, J14, L14, M15, M17, M19, N14, N16, P15, P19	_	—	15
GND_SENSE	G12, N13	—	—	19
ПТ	B2	Low	Output	7
HRESET	D8	Low	Input	
INT	D4	Low	Input	
L1_TSTCLK	G8	High	Input	9
L2_TSTCLK	B3	High	Input	10

Table 11. Pinout	Listing for the	e MPC7448, 36	0 HCTE Package

MPC7448 RISC Microprocessor Hardware Specifications, Rev. 4



Signal Name	Pin Number	Active	I/O	Notes
LVRAM	B10	_	_	12, 20, 22
NC (no connect)	A6, A14, A15, B14, B15, C14, C15, C16, C17, C18, C19, D14, D15, D16, D17, D18, D19, E14, E15, F14, F15, G14, G15, H15, H16, J15, J16, J17, J18, J19, K15, K16, K17, K18, K19, L15, L16, L17, L18, L19	_	_	11
LSSD_MODE	E8	Low	Input	6, 12
MCP	C9	Low	Input	
OV <sub>DD</sub>	B4, C2, C12, D5, F2, H3, J5, K2, L5, M3, N6, P2, P8, P11, R4, R13, R16, T6, T9, U2, U12, U16, V4, V7, V10, V14	—	—	
OVDD_SENSE	E18, G18		—	16
PLL_CFG[0:4]	B8, C8, C7, D7, A7	High	Input	
PLL_CFG[5]	D10	High	Input	9, 20
PMON_IN	D9	Low	Input	13
PMON_OUT	A9	Low	Output	
QACK	G5	Low	Input	
QREQ	P4	Low	Output	
SHD[0:1]	E4, H5	Low	I/O	3
SMI	F9	Low	Input	
SRESET	A2	Low	Input	
SYSCLK	A10		Input	
TA	К6	Low	Input	
TBEN	E1	High	Input	
TBST	F11	Low	Output	
ТСК	C6	High	Input	
TDI	B9	High	Input	6
TDO	A4	High	Output	
TEA	L1	Low	Input	
TEMP_ANODE	N18	—	—	17
TEMP_CATHODE	N19		—	17
TMS	F1	High	Input	6
TRST	A5	Low	Input	6, 14
TS	L4	Low	I/O	3
TSIZ[0:2]	G6, F7, E7	High	Output	
TT[0:4]	E5, E6, F6, E9, C5	High	I/O	
WT	D3	Low	Output	
V <sub>DD</sub>	H8, H10, H12, J7, J9, J11, J13, K8, K10, K12, K14, L7, L9, L11, L13, M8, M10, M12	—	—	
V <sub>DD</sub>	A13, A16, A18, B17, B19, C13, E13, E16, F12, F17, F19, G11, G16, H14, H17, H19, M14, M16, M18, N15, N17, P16, P18	_	_	15

Table 11. Pinout Listing for the MPC744	8, 360 HCTE Package (continued)
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### MPC7448 RISC Microprocessor Hardware Specifications, Rev. 4



### Table 11. Pinout Listing for the MPC7448, 360 HCTE Package (continued)

Signal Name	Pin Number	Active	I/O	Notes
VDD_SENSE	G13, N12			18

### Notes:

1.  $OV_{DD}$  supplies power to the processor bus, JTAG, and all control signals, and is configurable. ( $V_{DD}$  supplies power to the processor core, and  $AV_{DD}$  supplies power to the PLL after filtering from  $V_{DD}$ ). To program the I/O voltage, see Table 3. If used, the pull-down resistor should be less than 250  $\Omega$ . Because these settings may change in future products, it is recommended BVSEL[0:1] be configured using resistor options, jumpers, or some other flexible means, with the capability to reconfigure the termination of this signal in the future if necessary. For actual recommended value of  $V_{in}$  or supply voltages see Table 4.

2. Unused address pins must be pulled down to GND and corresponding address parity pins pulled up to OV<sub>DD</sub>.

3. These pins require weak pull-up resistors (for example, 4.7 KΩ) to maintain the control signals in the negated state after they have been actively negated and released by the MPC7448 and other bus masters.

4. This signal selects between MPX bus mode (asserted) and 60x bus mode (negated) and will be sampled at HRESET going high.

5. This signal must be negated during reset, by pull-up resistor to OV<sub>DD</sub> or negation by ¬HRESET (inverse of HRESET), to ensure proper operation.

6. Internal pull up on die.

7. Not used in 60x bus mode.

8. These signals must be pulled down to GND if unused, or if the MPC7448 is in 60x bus mode.

9. These input signals are for factory use only and must be pulled down to GND for normal machine operation.

10. This test signal is recommended to be tied to HRESET; however, other configurations will not adversely affect performance.

11. These signals are for factory use only and must be left unconnected for normal machine operation. Some pins that were NCs on the MPC7447, MPC7445, and MPC7441 have now been defined for other purposes.

- 12. These input signals are for factory use only and must be pulled up to OV<sub>DD</sub> for normal machine operation.
- 13. This pin can externally cause a performance monitor event. Counting of the event is enabled through software.
- 14. This signal must be asserted during reset, by pull down to GND or assertion by HRESET, to ensure proper operation.
- 15. These pins were NCs on the MPC7447, MPC7445, and MPC7441. See Section 9.3, "Connection Recommendations," for more information.
- 16. These pins were OV<sub>DD</sub> pins on the MPC7447, MPC7445, and MPC7441. These pins are internally connected to OV<sub>DD</sub> and are intended to allow an external device (such as a power supply) to detect the I/O voltage level present inside the device package. If unused, it is recommended they be connected to test points to facilitate system debug; otherwise, they may be connected directly to OV<sub>DD</sub> or left unconnected.
- 17. These pins provide connectivity to the on-chip temperature diode that can be used to determine the die junction temperature of the processor. These pins may be left unterminated if unused.
- 18. These pins are internally connected to V<sub>DD</sub> and are intended to allow an external device (such as a power supply) to detect the processor core voltage level present inside the device package. If unused, it is recommended they be connected to test points to facilitate system debug; otherwise, they may be connected directly to V<sub>DD</sub> or left unconnected.
- 19. These pins are internally connected to GND and are intended to allow an external device to detect the processor ground voltage level present inside the device package. If unused, it is recommended they be connected to test points to facilitate system debug; otherwise, they may be connected directly to GND or left unconnected.
- 20. These pins were in the TEST[0:4] factory test pin group on the MPC7447A, MPC7447, MPC7445, and MPC7441. They have been assigned new functions on the MPC7448.
- 21. These pins can be used to enable the supported dynamic frequency switching (DFS) modes via hardware. If both are pulled down, DFS mode is disabled completely and cannot be enabled via software. If unused, they should be pulled up to OV<sub>DD</sub> to allow software control of DFS. See the *MPC7450 RISC Microprocessor Family Reference Manual* for more information.
- 22. This pin is provided to allow operation of the L2 cache at low core voltages and is for factory use only. See the MPC7450 RISC Microprocessor Family Reference Manual for more information.



Package Description

# 8.2 Mechanical Dimensions for the MPC7448, 360 HCTE BGA

Figure 13 provides the mechanical dimensions and bottom surface nomenclature for the MPC7448, 360 HCTE BGA package.



Figure 13. Mechanical Dimensions and Bottom Surface Nomenclature for the MPC7448, 360 HCTE BGA Package





# 9 System Design Information

This section provides system and thermal design requirements and recommendations for successful application of the MPC7448.

# 9.1 Clocks

The following sections provide more detailed information regarding the clocking of the MPC7448.

### 9.1.1 PLL Configuration

The MPC7448 PLL is configured by the PLL\_CFG[0:5] signals. For a given SYSCLK (bus) frequency, the PLL configuration signals set the internal CPU and VCO frequency of operation. The PLL configuration for the MPC7448 is shown in Table 12. In this example, shaded cells represent settings that, for a given SYSCLK frequency, result in core and/or VCO frequencies that do not comply with Table 8. When enabled, dynamic frequency switching (DFS) also affects the core frequency by halving or quartering the bus-to-core multiplier; see Section 9.7.5, "Dynamic Frequency Switching (DFS)," for more information. Note that when DFS is enabled the resulting core frequency must meet the adjusted minimum core frequency requirements ( $f_{core_DFS}$ ) described in Table 8. Note that the PLL\_CFG[5] is currently used for factory test only and should be tied low, and that the MPC7448 PLL configuration settings are compatible with the MPC7447A PLL configuration settings when PLL\_CFG[5] = 0.

	Example Core and VCO Frequency in MHz										
PLL_CFG[0:5]	Bus-to-Core Co Multiplier <sup>5</sup> M	Coro to VCO	Bus (SYSCLK) Frequency								
		Multiplier <sup>5</sup>	33.3 MHz	50 MHz	66.6 MHz	75 MHz	83 MHz	100 MHz	133 MHz	167 MHz	200 MHz
010000	2x <sup>6</sup>	1x									
100000	3x <sup>6</sup>	1x									600
101000	4x <sup>6</sup>	1x								667	800
101100	5x	1x							667	835	1000
100100	5.5x	1x							733	919	1100
110100	6x	1x						600	800	1002	1200
010100	6.5x	1x						650	866	1086	1300
001000	7x	1x						700	931	1169	1400
000100	7.5x	1x					623	750	1000	1253	1500
110000	8x	1x				600	664	800	1064	1336	1600
011000	8.5x	1x				638	706	850	1131	1417	1700
011110	9x	1x			600	675	747	900	1197	1500	
011100	9.5x	1x			633	712	789	950	1264	1583	
101010	10x	1x			667	750	830	1000	1333	1667	
100010	10.5x	1x			700	938	872	1050	1397		

Table 12. MPC7448 Microprocessor PLL Configuration Example



# 9.1.2 System Bus Clock (SYSCLK) and Spread Spectrum Sources

Spread spectrum clock sources are an increasingly popular way to control electromagnetic interference emissions (EMI) by spreading the emitted noise to a wider spectrum and reducing the peak noise magnitude in order to meet industry and government requirements. These clock sources intentionally add long-term jitter in order to diffuse the EMI spectral content. The jitter specification given in Table 8 considers short-term (cycle-to-cycle) jitter only and the clock generator's cycle-to-cycle output jitter should meet the MPC7448 input cycle-to-cycle jitter requirement. Frequency modulation and spread are separate concerns, and the MPC7448 is compatible with spread spectrum sources if the recommendations listed in Table 13 are observed.

At recommended operating conditions. See Table 4.

Parameter	Min	Max	Unit	Notes
Frequency modulation	—	50	kHz	1
Frequency spread	—	1.0	%	1, 2

Notes:

2. SYSCLK frequencies resulting from frequency spreading, and the resulting core and VCO frequencies, must meet the minimum and maximum specifications given in Table 8.

It is imperative to note that the processor's minimum and maximum SYSCLK, core, and VCO frequencies must not be exceeded regardless of the type of clock source. Therefore, systems in which the processor is operated at its maximum rated core or bus frequency should avoid violating the stated limits by using down-spreading only.

# 9.2 Power Supply Design and Sequencing

The following sections provide detailed information regarding power supply design for the MPC7448.

### 9.2.1 Power Supply Sequencing

The MPC7448 requires its power rails and clock to be applied in a specific sequence to ensure proper device operation and to prevent device damage. The power sequencing requirements are as follows:

- AV<sub>DD</sub> must be delayed with respect to V<sub>DD</sub> by the RC time constant of the PLL filter circuit described in Section 9.2.2, "PLL Power Supply Filtering". This time constant is nominally 100 μs.
- $OV_{DD}$  may ramp anytime before or after  $V_{DD}$  and  $AV_{DD}$ .

Additionally, the following requirements exist regarding the application of SYSCLK:

- The voltage at the SYSCLK input must not exceed  $V_{DD}$  until  $V_{DD}$  has ramped to 0.9 V.
- The voltage at the SYSCLK input must not exceed OV<sub>DD</sub> by more 20% during transients (see overshoot/undershoot specifications in Figure 2) or 0.3 V DC (see Table 2) at any time.

<sup>1.</sup> Guaranteed by design



### 9.2.4 Decoupling Recommendations

Due to the MPC7448 dynamic power management feature, large address and data buses, and high operating frequencies, the MPC7448 can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the MPC7448 system, and the MPC7448 itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer use sufficient decoupling capacitors, typically one capacitor for every  $V_{DD}$  pin, and a similar amount for the OV<sub>DD</sub> pins, placed as close as possible to the power pins of the MPC7448. It is also recommended that these decoupling capacitors receive their power from separate  $V_{DD}$ , OV<sub>DD</sub>, and GND power planes in the PCB, using short traces to minimize inductance.

These capacitors should have a value of 0.01 or 0.1  $\mu$ F. Only ceramic surface mount technology (SMT) capacitors should be used to minimize lead inductance. Orientations where connections are made along the length of the part, such as 0204, are preferable but not mandatory. Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993) and contrary to previous recommendations for decoupling Freescale microprocessors, multiple small capacitors of equal value are recommended over using multiple values of capacitance.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the  $V_{DD}$  and  $OV_{DD}$  planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low equivalent series resistance (ESR) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors are 100–330  $\mu$ F (AVX TPS tantalum or Sanyo OSCON).

# 9.3 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. Unless otherwise noted, unused active low inputs should be tied to  $OV_{DD}$  and unused active high inputs should be connected to GND. All NC (no connect) signals must remain unconnected.

Power and ground connections must be made to all external  $V_{DD}$ ,  $OV_{DD}$ , and GND pins in the MPC7448. For backward compatibility with the MPC7447, MPC7445, and MP7441, or for migrating a system originally designed for one of these devices to the MPC7448, the new power and ground signals (formerly NC, see Table 11) may be left unconnected if the core frequency is 1 GHz or less. Operation above 1 GHz requires that these additional power and ground signals be connected, and it is strongly recommended that all new designs include the additional connections. See also Section 7, "Pinout Listings," for additional information.

The MPC7448 provides VDD\_SENSE, OVDD\_SENSE, and GND\_SENSE pins. These pins connect directly to the power/ground planes in the device package and are intended to allow an external device to measure the voltage present on the  $V_{DD}$ ,  $OV_{DD}$  and GND planes in the device package. The most common use for these signals is as a feedback signal to a power supply regulator to allow it to compensate for board losses and supply the correct voltage at the device. (Note that all voltage parameters are specified at the pins of the device.) If not used for this purpose, it is recommended that these signals be connected to test points that can be used in the event that an accurate measurement of the voltage at the device is needed during system debug. Otherwise, these signals should be connected to the appropriate power/ground planes on the circuit board or left unconnected.



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to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must be merged into these signals with logic.

The arrangement shown in Figure 21 allows the COP port to independently assert HRESET or TRST, while ensuring that the target can drive HRESET as well. If the JTAG interface and COP header will not be used, TRST should be tied to HRESET through a 0- $\Omega$  isolation resistor so that it is asserted when the system reset signal (HRESET) is asserted, ensuring that the JTAG scan chain is initialized during power-on. Although Freescale recommends that the COP header be designed into the system as shown in Figure 21, if this is not possible, the isolation resistor will allow future access to TRST in the case where a JTAG interface may need to be wired onto the system in debug situations.

The COP header shown in Figure 21 adds many benefits—breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features are possible through this interface—and can be as inexpensive as an unpopulated footprint for a header to be added when needed.

The COP interface has a standard header for connection to the target system, based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header). The connector typically has pin 14 removed as a connector key.

There is no standardized way to number the COP header shown in Figure 21; consequently, many different pin numbers have been observed from emulator vendors. Some are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom, while still others number the pins counter clockwise from pin 1 (as with an IC). Regardless of the numbering, the signal placement recommended in Figure 21 is common to all known emulators.

The  $\overline{QACK}$  signal shown in Figure 21 is usually connected to the bridge chip or other system control logic in a system and is an input to the MPC7448 informing it that it can go into the quiescent state. Under normal operation this occurs during a low-power mode selection. In order for COP to work, the MPC7448 must see this signal asserted (pulled down). While shown on the COP header, not all emulator products drive this signal. If the product does not, a pull-down resistor can be populated to assert this signal. Additionally, some emulator products implement open-drain type outputs and can only drive  $\overline{QACK}$ asserted; for these tools, a pull-up resistor can be implemented to ensure this signal is negated when it is not being driven by the tool. Note that the pull-up and pull-down resistors on the  $\overline{QACK}$  signal are mutually exclusive and it is never necessary to populate both in a system. To preserve correct power-down operation,  $\overline{QACK}$  should be merged through logic so that it also can be driven by the bridge or system logic.



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## 9.7.4 Temperature Diode

The MPC7448 has a temperature diode on the microprocessor that can be used in conjunction with other system temperature monitoring devices (such as Analog Devices, ADT7461<sup>TM</sup>). These devices use the negative temperature coefficient of a diode operated at a constant current to determine the temperature of the microprocessor and its environment. For proper operation, the monitoring device used should auto-calibrate the device by canceling out the V<sub>BE</sub> variation of each MPC7448's internal diode.

The following are the specifications of the MPC7448 on-board temperature diode:

 $V_{f} > 0.40 V$ 

 $V_{f} < 0.90 V$ 

Operating range 2–300 µA

Diode leakage  $< 10 \text{ nA} @ 125^{\circ}\text{C}$ 

Ideality factor over 5–150  $\mu A$  at 60°C:  $n=1.0275\pm0.9\%$ 

Ideality factor is defined as the deviation from the ideal diode equation:

$$I_{fw} = I_s e^{\frac{qV_f}{nKT}} - 1$$

Another useful equation is:

$$\mathbf{V}_{\mathrm{H}} - \mathbf{V}_{\mathrm{L}} = \mathbf{n} \frac{\mathrm{KT}}{\mathrm{q}} \left[ \mathbf{I} \mathbf{n} \frac{\mathrm{I}_{\mathrm{H}}}{\mathrm{I}_{\mathrm{L}}} \right] - \mathbf{1}$$

Where:

 $I_{fw} = Forward current$ 

 $I_s = Saturation current$ 

 $V_d = Voltage at diode$ 

 $V_f = Voltage forward biased$ 

 $V_H = Diode \text{ voltage while } I_H \text{ is flowing}$ 

 $V_L$  = Diode voltage while  $I_L$  is flowing

 $I_{H} = Larger diode bias current$ 

 $I_L =$ Smaller diode bias current

q = Charge of electron (1.6 x  $10^{-19}$  C)

$$n =$$
Ideality factor (normally 1.0)

K = Boltzman's constant (1.38 x 
$$10^{-23}$$
 Joules/K)

The ratio of  $I_H$  to  $I_L$  is usually selected to be 10:1. The previous equation simplifies to the following:

$$V_{H} - V_{L} = 1.986 \times 10^{-4} \times nT$$



Solving for T, the equation becomes:

$$\mathbf{nT} = \frac{\mathbf{V}_{\mathrm{H}} - \mathbf{V}_{\mathrm{L}}}{1.986 \times 10^{-4}}$$

### 9.7.5 Dynamic Frequency Switching (DFS)

The DFS feature in the MPC7448 adds the ability to divide the processor-to-system bus ratio by two or four during normal functional operation. Divide-by-two mode is enabled by setting the HID1[DFS2] bit in software or by asserting the  $\overline{DFS2}$  pin via hardware. The MPC7448 can be returned for full speed by clearing HID1[DFS2] or negating  $\overline{DFS2}$ . Similarly, divide-by-four mode is enabled by setting HID1[DFS4] in software or by asserting the  $\overline{DFS4}$  pin. In all cases, the frequency change occurs in 1 clock cycle and no idle waiting period is required to switch between modes. Note that asserting either  $\overline{DFS2}$  or  $\overline{DFS4}$  overrides software control of DFS, and that asserting both  $\overline{DFS2}$  and  $\overline{DFS4}$  disables DFS completely, including software control. Additional information regarding DFS can be found in the *MPC7450 RISC Microprocessor Family Reference Manual*. Note that minimum core frequency requirements must be observed when enabling DFS, and the resulting core frequency must meet the requirements for f<sub>core DFS</sub> given in Table 8.

### 9.7.5.1 Power Consumption with DFS Enabled

Power consumption with DFS enabled can be approximated using the following formula:

$$\mathbf{P}_{\mathbf{DFS}} = \begin{bmatrix} \overline{f}_{\mathbf{DFS}} & (\mathbf{P} - \mathbf{P}_{\mathbf{DS}}) \end{bmatrix} + \mathbf{P}_{\mathbf{DS}}$$

Where:

 $P_{DFS}$  = Power consumption with DFS enabled

 $f_{DFS}$  = Core frequency with DFS enabled

f = Core frequency prior to enabling DFS

P = Power consumption prior to enabling DFS (see Table 7)

 $P_{DS}$  = Deep sleep mode power consumption (see Table 7)

The above is an approximation only. Power consumption with DFS enabled is not tested or guaranteed.

### 9.7.5.2 Bus-to-Core Multiplier Constraints with DFS

DFS is not available for all bus-to-core multipliers as configured by PLL\_CFG[0:5] during hard reset. The complete listing is shown in Table 16. Shaded cells represent DFS modes that are not available for a particular PLL\_CFG[0:5] setting. Should software or hardware attempt to transition to a multiplier that is not supported, the device will remain at its current multiplier. For example, if a transition from DFS-disabled to an unsupported divide-by-2 or divide-by-4 setting is attempted, the bus-to-core multiplier will remain at the setting configured by the PLL\_CFG[0:5] pins. In the case of an attempted transition from a supported divide-by-2 mode to an unsupported divide-by-4 mode, the device will remain in divide-by-2 mode. In all cases, the HID1[PC0-5] bits will correctly reflect the current bus-to-core frequency multiplier.

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		7		
			Δ	

DFS mode disabled		DFS divide-by-2 (HID1[DFS2] = 1	mode enabled or DFS2 = 0)	DFS divide-by-4 mode enabled (HID1[DFS4] = 1 or DFS4 = 0)	
Bus-to-Core Multiplier Configured by PLL_CFG[0:5] (see Table 12)	bre Multiplier gured by CFG[0:5] Table 12) HID1[PC0-5] <sup>3</sup> Bus-to-Core Multiplier		HID1[PC0-5] <sup>3</sup>	Bus-to-Core Multiplier	HID1[PC0-5] <sup>3</sup>
24x	011010	12x	101110	6x	110100
28x	111010	14x	110010	7x	001000

Table 16. Valid Divide Ratio Configurations (continued	Table	16.	Valid	Divide	Ratio	Configura	tions	(continued
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Notes:

1. DFS mode is not supported for this combination of DFS mode and PLL\_CFG[0:5] setting. As a result, the processor will ignore these settings and remain at the previous multiplier, as reflected by the HID1[PC0-PC5] bits.

2. Though supported by the MPC7448 clock circuitry, multipliers of *n*.25x and *n*.75x cannot be expressed as valid PLL configuration codes. As a result, the values displayed in HID1[PC0-PC5] are rounded down to the nearest valid PLL configuration code. However, the actual bus-to-core multiplier is as stated in this table.

- 3. Note that in the HID1 register of the MPC7448, the PC0, PC1, PC2, PC3, PC4, and PC5 bits are bits 15, 16, 17, 18, 19, and 14 (respectively). See the *MPC7450 RISC Microprocessor Reference Manual* for more information.
- 4. Special considerations regarding snooped transactions must be observed for bus-to-core multipliers less than 5x. See the *MPC7450 RISC Microprocessor Reference Manual* for more information.

### 9.7.5.3 Minimum Core Frequency Requirements with DFS

In many systems, enabling DFS can result in very low processor core frequencies. However, care must be taken to ensure that the resulting processor core frequency is within the limits specified in Table 8. Proper operation of the device is not guaranteed at core frequencies below the specified minimum  $f_{core}$ .

# **10 Document Revision History**

Table 17 provides a revision history for this hardware specification.

Table 17.	Document	Revision	History
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Revision	Date	Substantive Change(s)
4	3/2007	Table 19: Added 800 MHz processor frequency.
3	10/2006	Section 9.7, "Power and Thermal Management Information": Updated contact information. Table 18, Table 20, and Table 19: Added Revision D PVR. Table 19: Added 600 processor frequency, additional product codes, date codes for 1400 processor frequency, and footnotes 1 and 2. Table 20: Added PPC product code and footnote 1. Table 19 and Table 20: Added Revision D information for 1267 processor frequency.



# **11 Part Numbering and Marking**

Ordering information for the part numbers fully covered by this specification document is provided in Section 11.1, "Part Numbers Fully Addressed by This Document." Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact a local Freescale sales office. In addition to the processor frequency, the part numbering scheme also includes an application modifier that may specify special application conditions. An optional specification modifier may also apply for parts to indicate a specific change in specifications, such as support for an extended temperature range. Finally, each part number contains a revision level code that refers to the die mask revision number. Section 11.2, "Part Numbers Not Fully Addressed by This Document," lists the part numbers that do not fully conform to the specifications of this document. These special part numbers require an additional document called a hardware specification addendum.

# 11.1 Part Numbers Fully Addressed by This Document

Table 18 provides the Freescale part numbering nomenclature for the MPC7448 part numbers fully addressed by this document. For information regarding other MPC7448 part numbers, see Section 11.2, "Part Numbers Not Fully Addressed by This Document."

XX	7448	XX	nnnn	L	X
Product Code	Part Identifier	Package	Processor Frequency	Application Modifier	Revision Level
MC PPC <sup>1</sup>	7448	HX = HCTE BGA VS = RoHS LGA	1700	L: 1.3 V +20/–50 mV 0 to 105 °C	C: 2.1; PVR = 0x8004_0201 D: 2.2; PVR = 0x8004_0202
	VU = NUHS		1600	L: 1.25 V ± 50 mV 0 to 105 °C	
			1420	L: 1.2 V ± 50 mV 0 to 105 °C	
			1000	L: 1.15 V ± 50 mV 0 to 105 °C	

### Table 18. Part Numbering Nomenclature

### Notes:

1. The P prefix in a Freescale part number designates a "Pilot Production Prototype" as defined by Freescale SOP 3-13. These parts have only preliminary reliability and characterization data. Before pilot production prototypes may be shipped, written authorization from the customer must be on file in the applicable sales office acknowledging the qualification status and the fact that product changes may still occur as pilot production prototypes are shipped.



### Table 20. Part Numbers Addressed by MC7448TxxnnnnNx Series Hardware Specification Addendum (Document Order No. MPC7448ECS02AD)

XX	7448	т	XX	nnnn	Ν	X
Product Code	Part Identifier	Specificatio n Modifier	Package	Processor Frequency	Application Modifier	Revision Level
MC PPC <sup>1</sup>	7448	T = Extended Temperature	HX = HCTE BGA	1400	N: 1.15 V ± 50 mV - 40 to 105 °C	C: 2.1; PVR = 0x8004_0201 D: 2.2; PVR = 0x8004_0202
		Device		1267 Revision C only	N: 1.1 V ± 50 mV - 40 to 105 °C	
				1267 Revision D only	N: 1.05 V ± 50 mV - 40 to 105 °C	
				1000	N: 1.0 V ± 50 mV - 40 to 105 °C	

Notes:

 The P prefix in a Freescale part number designates a "Pilot Production Prototype" as defined by Freescale SOP 3-13. These parts have only preliminary reliability and characterization data. Before pilot production prototypes can be shipped, written authorization from the customer must be on file in the applicable sales office acknowledging the qualification status and the fact that product changes may still occur as pilot production prototypes are shipped.

### 11.3 Part Marking

Parts are marked as the example shown in Figure 27.



Notes:

AWLYYWW is the test code, where YYWW is the date code (YY = year, WW = work week) MMMMMM is the M00 (mask) number. YWWLAZ is the assembly traceability code.

Figure 27. Part Marking for BGA and LGA Device

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