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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC G4
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.42GHz
Co-Processors/DSP	Multimedia; SIMD
RAM Controllers	-
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	1.5V, 1.8V, 2.5V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	360-CLGA, FCCLGA
Supplier Device Package	360-FCCLGA (25x25)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc7448vs1420ld

2 Features

This section summarizes features of the MPC7448 implementation.

Major features of the MPC7448 are as follows:

- High-performance, superscalar microprocessor
    - Up to four instructions can be fetched from the instruction cache at a time.
    - Up to three instructions plus a branch instruction can be dispatched to the issue queues at a time.
    - Up to 12 instructions can be in the instruction queue (IQ).
    - Up to 16 instructions can be at some stage of execution simultaneously.
    - Single-cycle execution for most instructions
    - One instruction per clock cycle throughput for most instructions
    - Seven-stage pipeline control
- Eleven independent execution units and three register files
    - Branch processing unit (BPU) features static and dynamic branch prediction
        - 128-entry (32-set, four-way set-associative) branch target instruction cache (BTIC), a cache of branch instructions that have been encountered in branch/loop code sequences. If a target instruction is in the BTIC, it is fetched into the instruction queue a cycle sooner than it can be made available from the instruction cache. Typically, a fetch that hits the BTIC provides the first four instructions in the target stream.
        - 2048-entry branch history table (BHT) with 2 bits per entry for four levels of prediction—not taken, strongly not taken, taken, and strongly taken
        - Up to three outstanding speculative branches
        - Branch instructions that do not update the count register (CTR) or link register (LR) are often removed from the instruction stream.
        - Eight-entry link register stack to predict the target address of Branch Conditional to Link Register (**bclr**) instructions
    - Four integer units (IUs) that share 32 GPRs for integer operands
        - Three identical IUs (IU1a, IU1b, and IU1c) can execute all integer instructions except multiply, divide, and move to/from special-purpose register instructions.
        - IU2 executes miscellaneous instructions, including the CR logical operations, integer multiplication and division instructions, and move to/from special-purpose register instructions.
    - Five-stage FPU and 32-entry FPR file
        - Fully IEEE Std. 754™-1985–compliant FPU for both single- and double-precision operations
        - Supports non-IEEE mode for time-critical operations
        - Hardware support for denormalized numbers
        - Thirty-two 64-bit FPRs for single- or double-precision operands

- — Four vector units and 32-entry vector register file (VRs)
    - – Vector permute unit (VPU)
    - – Vector integer unit 1 (VIU1) handles short-latency AltiVec™ integer instructions, such as vector add instructions (for example, **vaddsbs**, **vaddshs**, and **vaddsws**).
    - – Vector integer unit 2 (VIU2) handles longer-latency AltiVec integer instructions, such as vector multiply add instructions (for example, **vmhaddshs**, **vmhraddshs**, and **vmladduhm**).
    - – Vector floating-point unit (VFPU)
- — Three-stage load/store unit (LSU)
    - – Supports integer, floating-point, and vector instruction load/store traffic
    - – Four-entry vector touch queue (VTQ) supports all four architected AltiVec data stream operations
    - – Three-cycle GPR and AltiVec load latency (byte, half word, word, vector) with one-cycle throughput
    - – Four-cycle FPR load latency (single, double) with one-cycle throughput
    - – No additional delay for misaligned access within double-word boundary
    - – A dedicated adder calculates effective addresses (EAs).
    - – Supports store gathering
    - – Performs alignment, normalization, and precision conversion for floating-point data
    - – Executes cache control and TLB instructions
    - – Performs alignment, zero padding, and sign extension for integer data
    - – Supports hits under misses (multiple outstanding misses)
    - – Supports both big- and little-endian modes, including misaligned little-endian accesses
- Three issue queues, FIQ, VIQ, and GIQ, can accept as many as one, two, and three instructions, respectively, in a cycle. Instruction dispatch requires the following:
    - — Instructions can only be dispatched from the three lowest IQ entries—IQ0, IQ1, and IQ2.
    - — A maximum of three instructions can be dispatched to the issue queues per clock cycle.
    - — Space must be available in the CQ for an instruction to dispatch (this includes instructions that are assigned a space in the CQ but not in an issue queue).
- Rename buffers
    - — 16 GPR rename buffers
    - — 16 FPR rename buffers
    - — 16 VR rename buffers
- Dispatch unit
    - — Decode/dispatch stage fully decodes each instruction
- Completion unit
    - — Retires an instruction from the 16-entry completion queue (CQ) when all instructions ahead of it have been completed, the instruction has finished executing, and no exceptions are pending
    - — Guarantees sequential programming model (precise exception model)

- Efficient data flow
  - Although the VR/LSU interface is 128 bits, the L1/L2 bus interface allows up to 256 bits.
  - The L1 data cache is fully pipelined to provide 128 bits/cycle to or from the VRs.
  - The L2 cache is fully pipelined to provide 32 bytes per clock every other cycle to the L1 caches.
  - As many as 16 out-of-order transactions can be present on the MPX bus.
  - Store merging for multiple store misses to the same line. Only coherency action taken (address-only) for store misses merged to all 32 bytes of a cache block (no data tenure needed).
  - Three-entry finished store queue and five-entry completed store queue between the LSU and the L1 data cache
  - Separate additional queues for efficient buffering of outbound data (such as castouts and write-through stores) from the L1 data cache and L2 cache
- Multiprocessing support features include the following:
  - Hardware-enforced, MESI cache coherency protocols for data cache
  - Load/store with reservation instruction pair for atomic memory references, semaphores, and other multiprocessor operations
- Power and thermal management
  - Dynamic frequency switching (DFS) feature allows processor core frequency to be halved or quartered through software to reduce power consumption.
  - The following three power-saving modes are available to the system:
    - Nap—Instruction fetching is halted. Only the clocks for the time base, decrementer, and JTAG logic remain running. The part goes into the doze state to snoop memory operations on the bus and then back to nap using a $\overline{\text{QREQ}}/\overline{\text{QACK}}$ processor-system handshake protocol.
    - Sleep—Power consumption is further reduced by disabling bus snooping, leaving only the PLL in a locked and running state. All internal functional units are disabled.
    - Deep sleep—When the part is in the sleep state, the system can disable the PLL. The system can then disable the SYSCLK source for greater system power savings. Power-on reset procedures for restarting and relocking the PLL must be followed upon exiting the deep sleep state.
  - Instruction cache throttling provides control of instruction fetching to limit device temperature.
  - A new temperature diode that can determine the temperature of the microprocessor
- Performance monitor can be used to help debug system designs and improve software efficiency.
- In-system testability and debugging features through JTAG boundary-scan capability
- Testability
  - LSSD scan design
  - IEEE Std. 1149.1™ JTAG interface

Figure 2 shows the undershoot and overshoot voltage on the MPC7448.
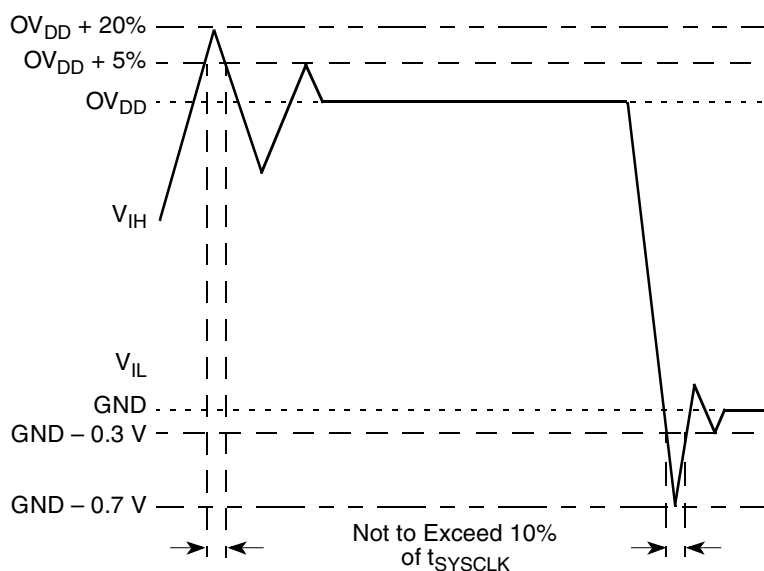
Figure 2. Overshoot/Undershoot Voltage

The MPC7448 provides several I/O voltages to support both compatibility with existing systems and migration to future systems. The MPC7448 core voltage must always be provided at the nominal voltage (see Table 4). The input voltage threshold for each bus is selected by sampling the state of the voltage select pins at the negation of the signal $\overline{\text{HRESET}}$. The output voltage will swing from GND to the maximum voltage applied to the OV_{DD} power pins. Table 3 provides the input threshold voltage settings. Because these settings may change in future products, it is recommended that BVSEL[0:1] be configured using resistor options, jumpers, or some other flexible means, with the capability to reconfigure the termination of this signal in the future, if necessary.

Table 3. Input Threshold Voltage Setting

BVSEL0	BVSEL1	I/O Voltage Mode[1]	Notes
0	0	1.8 V	2, 3
0	1	2.5 V	2, 4
1	0	1.5 V	2
1	1	2.5 V	4

Notes:

1. **Caution:** The I/O voltage mode selected must agree with the OV_{DD} voltages supplied. See Table 4.

2. If used, pull-down resistors should be less than 250 Ω.

3. The pin configuration used to select 1.8V mode on the MPC7448 is not compatible with the pin configuration used to select 1.8V mode on the MPC7447A and earlier devices.

4. The pin configuration used to select 2.5V mode on the MPC7448 is fully compatible with the pin configuration used to select 2.5V mode on the MPC7447A and earlier devices.

Table 6. DC Electrical Specifications (continued)

At recommended operating conditions. See Table 4.

Characteristic		Nominal Bus Voltage [1]	Symbol	Min	Max	Unit	Notes
High-impedance (off-state) leakage current: $V_{in} = OV_{DD}$ $V_{in} = GND$		—	I_{TSI}	—	50 −50	µA	2, 3, 4
Output high voltage @ $I_{OH} = -5$ mA		1.5	V_{OH}	$OV_{DD} - 0.45$	—	V	
		1.8		$OV_{DD} - 0.45$	—		
		2.5		1.8	—		
Output low voltage @ $I_{OL} = 5$ mA		1.5	V_{OL}	—	0.45	V	
		1.8		—	0.45		
		2.5		—	0.6		
Capacitance, $V_{in} = 0$ V, f = 1 MHz	All inputs		C_{in}	—	8.0	pF	5

Notes:

1. Nominal voltages; see Table 4 for recommended operating conditions.
2. All I/O signals are referenced to OV_{DD}.
3. Excludes test signals and IEEE Std. 1149.1 boundary scan (JTAG) signals
4. The leakage is measured for nominal OV_{DD} and V_{DD}, or both OV_{DD} and V_{DD} must vary in the same direction (for example, both OV_{DD} and V_{DD} vary by either +5% or −5%).
5. Capacitance is periodically sampled rather than 100% tested.
6. These pins have internal pull-up resistors.

Table 7 provides the power consumption for the MPC7448 part numbers described by this document; see Section 11.1, "Part Numbers Fully Addressed by This Document," for information regarding which part numbers are described by this document. Freescale also offers MPC7448 part numbers that meet lower power consumption specifications by adhering to lower core voltage and core frequency specifications. For more information on these devices, including references to the MPC7448 Hardware Specification Addenda that describe these devices, see Section 11.2, "Part Numbers Not Fully Addressed by This Document."

The power consumptions provided in Table 7 represent the power consumption of each speed grade when operated at the rated maximum core frequency (see Table 8). Freescale sorts devices by power as well as by core frequency, and power limits for each speed grade are independent of each other. Each device is tested at its maximum core frequency only. (Note that Deep Sleep Mode power consumption is independent of clock frequency.) Operating a device at a frequency lower than its rated maximum is fully supported provided the clock frequencies are within the specifications given in Table 8, and a device operated below its rated maximum will have lower power consumption. However, inferences should not be made about a device's power consumption based on the power specifications of another (lower) speed grade. For example, a 1700 MHz device operated at 1420 MHz may not exhibit the same power consumption as a 1420 MHz device operated at 1420 MHz.

For all MPC7448 devices, the following guidelines on the use of these parameters for system design are suggested. The Full-Power Mode–Typical value represents the sustained power consumption of the device

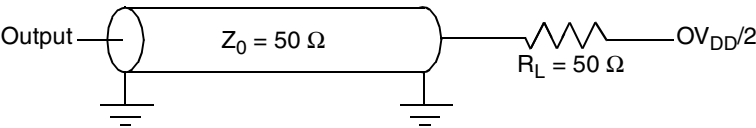Figure 4 provides the AC test load for the MPC7448.

Figure 4. AC Test Load

Figure 5 provides the $\overline{\text{BMODE}}$[0:1] input timing diagram for the MPC7448. These mode select inputs are sampled once before and once after $\overline{\text{HRESET}}$ negation.
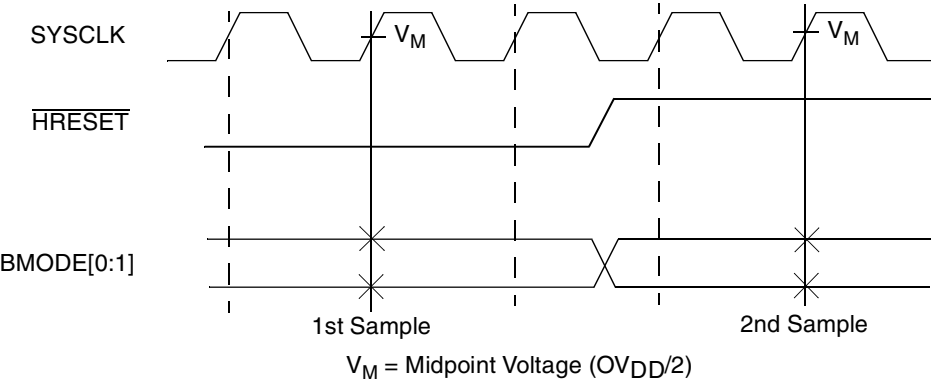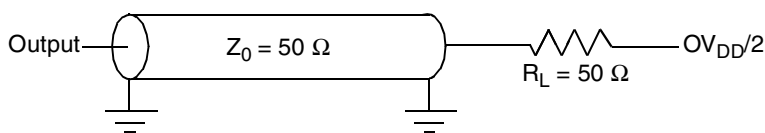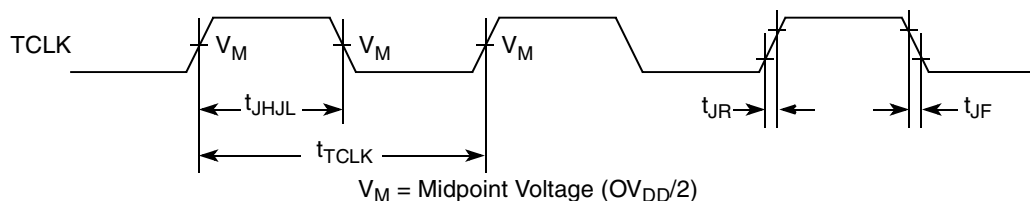

V_M = Midpoint Voltage (OV$_{DD}$/2)

Figure 5. $\overline{\text{BMODE}}$[0:1] Input Sample Timing Diagram

Figure 7 provides the AC test load for TDO and the boundary-scan outputs of the MPC7448.
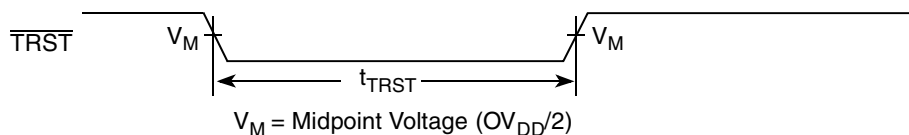

Figure 7. Alternate AC Test Load for the JTAG Interface

Figure 8 provides the JTAG clock input timing diagram.

V_M = Midpoint Voltage ($OV_{DD}/2$)
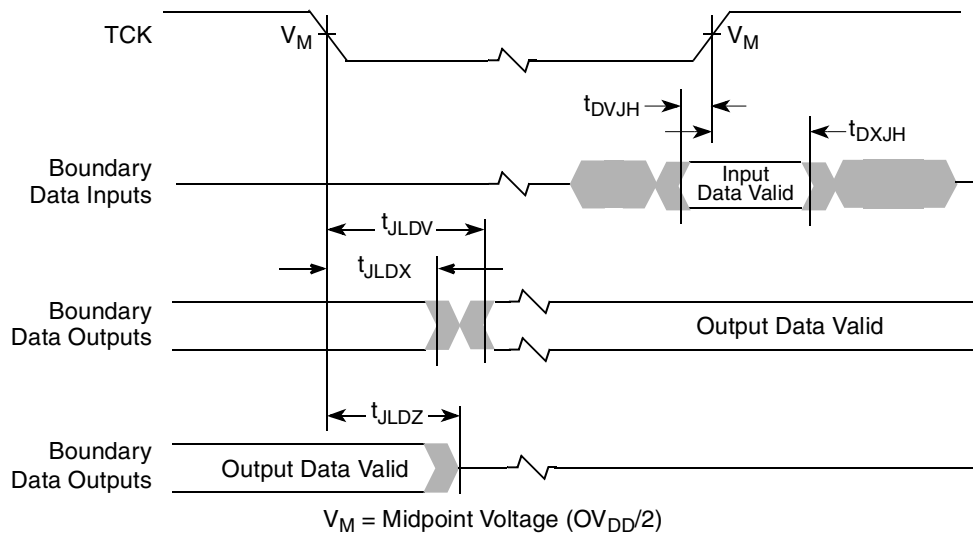
Figure 8. JTAG Clock Input Timing Diagram

Figure 9 provides the $\overline{\text{TRST}}$ timing diagram.

V_M = Midpoint Voltage ($OV_{DD}/2$)

Figure 9. $\overline{\text{TRST}}$ Timing Diagram

Figure 10 provides the boundary-scan timing diagram.

V_M = Midpoint Voltage ($OV_{DD}/2$)

Figure 10. Boundary-Scan Timing Diagram

8.3   Package Parameters for the MPC7448, 360 HCTE LGA

The package parameters are as provided in the following list. The package type is 25×25 mm, 360 pin high coefficient of thermal expansion ceramic land grid array (HCTE).

Package outline	25×25 mm
Interconnects	360 (19×19 ball array – 1)
Pitch	1.27 mm (50 mil)
Minimum module height	1.52 mm
Maximum module height	1.80 mm
Pad diameter	0.89 mm (35 mil)
Coefficient of thermal expansion	12.3 ppm/°C

8.4 Mechanical Dimensions for the MPC7448, 360 HCTE LGA

Figure 13 provides the mechanical dimensions and bottom surface nomenclature for the MPC7448, 360 HCTE LGA package.
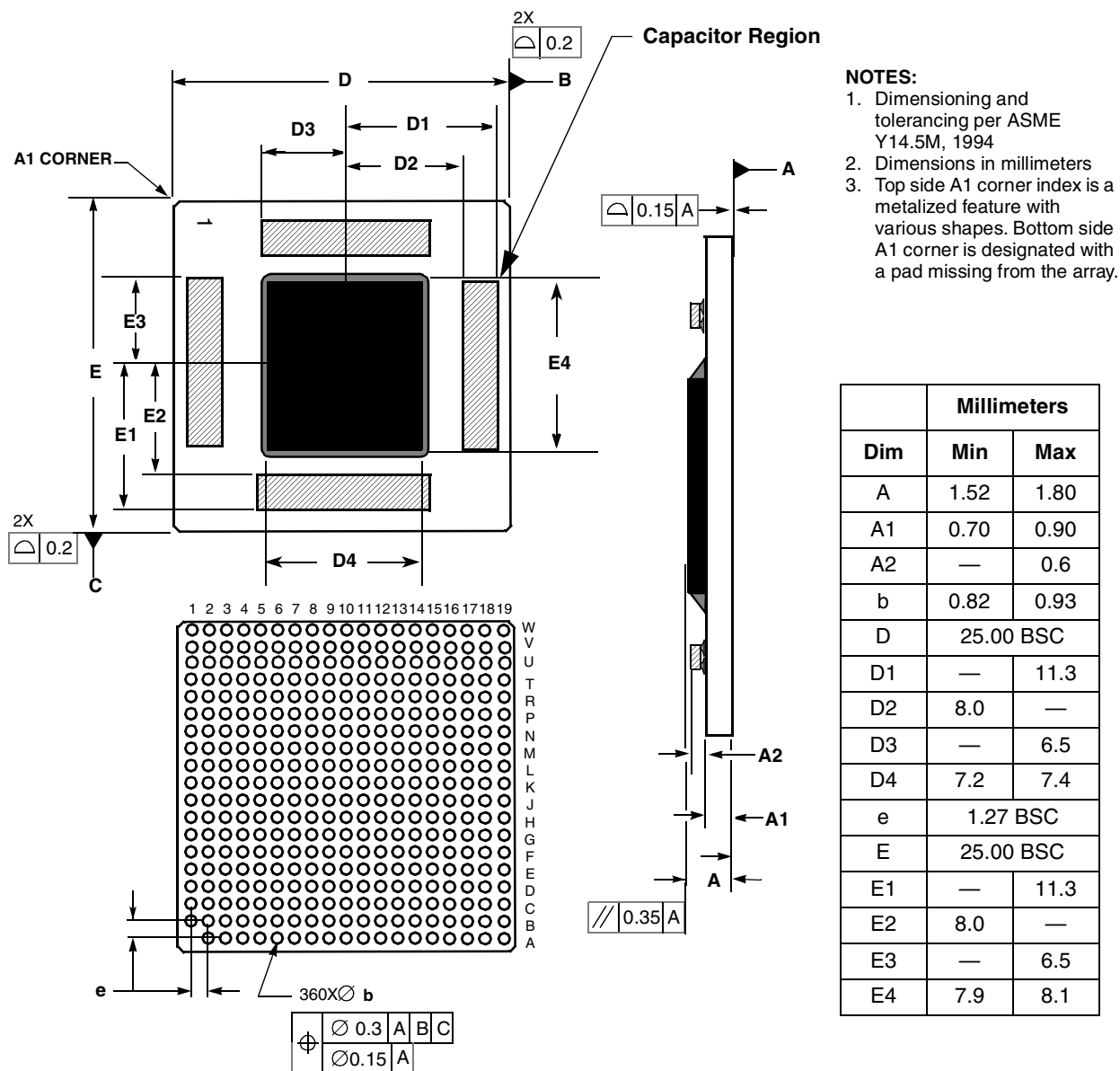
NOTES:
1. Dimensioning and tolerancing per ASME Y14.5M, 1994
2. Dimensions in millimeters
3. Top side A1 corner index is a metalized feature with various shapes. Bottom side A1 corner is designated with a pad missing from the array.

Dim	Millimeters	
	Min	Max
A	1.52	1.80
A1	0.70	0.90
A2	—	0.6
b	0.82	0.93
D	25.00 BSC	
D1	—	11.3
D2	8.0	—
D3	—	6.5
D4	7.2	7.4
e	1.27 BSC	
E	25.00 BSC	
E1	—	11.3
E2	8.0	—
E3	—	6.5
E4	7.9	8.1

Figure 14. Mechanical Dimensions and Bottom Surface Nomenclature for the MPC7448, 360 HCTE LGA Package

9 System Design Information

This section provides system and thermal design requirements and recommendations for successful application of the MPC7448.

9.1 Clocks

The following sections provide more detailed information regarding the clocking of the MPC7448.

9.1.1 PLL Configuration

The MPC7448 PLL is configured by the PLL_CFG[0:5] signals. For a given SYSCLK (bus) frequency, the PLL configuration signals set the internal CPU and VCO frequency of operation. The PLL configuration for the MPC7448 is shown in Table 12. In this example, shaded cells represent settings that, for a given SYSCLK frequency, result in core and/or VCO frequencies that do not comply with Table 8. When enabled, dynamic frequency switching (DFS) also affects the core frequency by halving or quartering the bus-to-core multiplier; see Section 9.7.5, "Dynamic Frequency Switching (DFS)," for more information. Note that when DFS is enabled the resulting core frequency must meet the adjusted minimum core frequency requirements (f_{core_DFS}) described in Table 8. Note that the PLL_CFG[5] is currently used for factory test only and should be tied low, and that the MPC7448 PLL configuration settings are compatible with the MPC7447A PLL configuration settings when PLL_CFG[5] = 0.

Table 12. MPC7448 Microprocessor PLL Configuration Example

PLL_CFG[0:5]	Example Core and VCO Frequency in MHz										
	Bus-to-Core Multiplier [5]	Core-to-VCO Multiplier [5]	Bus (SYSCLK) Frequency								
			33.3 MHz	50 MHz	66.6 MHz	75 MHz	83 MHz	100 MHz	133 MHz	167 MHz	200 MHz
010000	2x [6]	1x									
100000	3x [6]	1x									600
101000	4x [6]	1x								667	800
101100	5x	1x							667	835	1000
100100	5.5x	1x							733	919	1100
110100	6x	1x						600	800	1002	1200
010100	6.5x	1x						650	866	1086	1300
001000	7x	1x						700	931	1169	1400
000100	7.5x	1x					623	750	1000	1253	1500
110000	8x	1x				600	664	800	1064	1336	1600
011000	8.5x	1x				638	706	850	1131	1417	1700
011110	9x	1x			600	675	747	900	1197	1500	
011100	9.5x	1x			633	712	789	950	1264	1583	
101010	10x	1x			667	750	830	1000	1333	1667	
100010	10.5x	1x			700	938	872	1050	1397		

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9.1.2 System Bus Clock (SYSCLK) and Spread Spectrum Sources

Spread spectrum clock sources are an increasingly popular way to control electromagnetic interference emissions (EMI) by spreading the emitted noise to a wider spectrum and reducing the peak noise magnitude in order to meet industry and government requirements. These clock sources intentionally add long-term jitter in order to diffuse the EMI spectral content. The jitter specification given in Table 8 considers short-term (cycle-to-cycle) jitter only and the clock generator's cycle-to-cycle output jitter should meet the MPC7448 input cycle-to-cycle jitter requirement. Frequency modulation and spread are separate concerns, and the MPC7448 is compatible with spread spectrum sources if the recommendations listed in Table 13 are observed.

Table 13. Spread Spectrum Clock Source Recommendations

At recommended operating conditions. See Table 4.

Parameter	Min	Max	Unit	Notes
Frequency modulation	—	50	kHz	1
Frequency spread	—	1.0	%	1, 2

Notes:

1. Guaranteed by design
2. SYSCLK frequencies resulting from frequency spreading, and the resulting core and VCO frequencies, must meet the minimum and maximum specifications given in Table 8.

It is imperative to note that the processor's minimum and maximum SYSCLK, core, and VCO frequencies must not be exceeded regardless of the type of clock source. Therefore, systems in which the processor is operated at its maximum rated core or bus frequency should avoid violating the stated limits by using down-spreading only.

9.2 Power Supply Design and Sequencing

The following sections provide detailed information regarding power supply design for the MPC7448.

9.2.1 Power Supply Sequencing

The MPC7448 requires its power rails and clock to be applied in a specific sequence to ensure proper device operation and to prevent device damage. The power sequencing requirements are as follows:

- AV_{DD} must be delayed with respect to V_{DD} by the RC time constant of the PLL filter circuit described in Section 9.2.2, "PLL Power Supply Filtering". This time constant is nominally 100 µs.
- OV_{DD} may ramp anytime before or after V_{DD} and AV_{DD}.

Additionally, the following requirements exist regarding the application of SYSCLK:

- The voltage at the SYSCLK input must not exceed V_{DD} until V_{DD} has ramped to 0.9 V.
- The voltage at the SYSCLK input must not exceed OV_{DD} by more 20% during transients (see overshoot/undershoot specifications in Figure 2) or 0.3 V DC (see Table 2) at any time.

9.2.4 Decoupling Recommendations

Due to the MPC7448 dynamic power management feature, large address and data buses, and high operating frequencies, the MPC7448 can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the MPC7448 system, and the MPC7448 itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer use sufficient decoupling capacitors, typically one capacitor for every V_{DD} pin, and a similar amount for the OV_{DD} pins, placed as close as possible to the power pins of the MPC7448. It is also recommended that these decoupling capacitors receive their power from separate V_{DD}, OV_{DD}, and GND power planes in the PCB, using short traces to minimize inductance.

These capacitors should have a value of 0.01 or 0.1 µF. Only ceramic surface mount technology (SMT) capacitors should be used to minimize lead inductance. Orientations where connections are made along the length of the part, such as 0204, are preferable but not mandatory. Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993) and contrary to previous recommendations for decoupling Freescale microprocessors, multiple small capacitors of equal value are recommended over using multiple values of capacitance.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V_{DD} and OV_{DD} planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low equivalent series resistance (ESR) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors are 100–330 µF (AVX TPS tantalum or Sanyo OSCON).

9.3 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. Unless otherwise noted, unused active low inputs should be tied to OV_{DD} and unused active high inputs should be connected to GND. All NC (no connect) signals must remain unconnected.

Power and ground connections must be made to all external V_{DD}, OV_{DD}, and GND pins in the MPC7448. For backward compatibility with the MPC7447, MPC7445, and MP7441, or for migrating a system originally designed for one of these devices to the MPC7448, the new power and ground signals (formerly NC, see Table 11) may be left unconnected if the core frequency is 1 GHz or less. Operation above 1 GHz requires that these additional power and ground signals be connected, and it is strongly recommended that all new designs include the additional connections. See also Section 7, "Pinout Listings," for additional information.

The MPC7448 provides VDD_SENSE, OVDD_SENSE, and GND_SENSE pins. These pins connect directly to the power/ground planes in the device package and are intended to allow an external device to measure the voltage present on the V_{DD}, OV_{DD} and GND planes in the device package. The most common use for these signals is as a feedback signal to a power supply regulator to allow it to compensate for board losses and supply the correct voltage at the device. (Note that all voltage parameters are specified at the pins of the device.) If not used for this purpose, it is recommended that these signals be connected to test points that can be used in the event that an accurate measurement of the voltage at the device is needed during system debug. Otherwise, these signals should be connected to the appropriate power/ground planes on the circuit board or left unconnected.

to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must be merged into these signals with logic.

The arrangement shown in Figure 21 allows the COP port to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$, while ensuring that the target can drive $\overline{\text{HRESET}}$ as well. If the JTAG interface and COP header will not be used, $\overline{\text{TRST}}$ should be tied to $\overline{\text{HRESET}}$ through a 0-Ω isolation resistor so that it is asserted when the system reset signal ($\overline{\text{HRESET}}$) is asserted, ensuring that the JTAG scan chain is initialized during power-on. Although Freescale recommends that the COP header be designed into the system as shown in Figure 21, if this is not possible, the isolation resistor will allow future access to $\overline{\text{TRST}}$ in the case where a JTAG interface may need to be wired onto the system in debug situations.

The COP header shown in Figure 21 adds many benefits—breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features are possible through this interface—and can be as inexpensive as an unpopulated footprint for a header to be added when needed.

The COP interface has a standard header for connection to the target system, based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header). The connector typically has pin 14 removed as a connector key.

There is no standardized way to number the COP header shown in Figure 21; consequently, many different pin numbers have been observed from emulator vendors. Some are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom, while still others number the pins counter clockwise from pin 1 (as with an IC). Regardless of the numbering, the signal placement recommended in Figure 21 is common to all known emulators.

The $\overline{\text{QACK}}$ signal shown in Figure 21 is usually connected to the bridge chip or other system control logic in a system and is an input to the MPC7448 informing it that it can go into the quiescent state. Under normal operation this occurs during a low-power mode selection. In order for COP to work, the MPC7448 must see this signal asserted (pulled down). While shown on the COP header, not all emulator products drive this signal. If the product does not, a pull-down resistor can be populated to assert this signal. Additionally, some emulator products implement open-drain type outputs and can only drive $\overline{\text{QACK}}$ asserted; for these tools, a pull-up resistor can be implemented to ensure this signal is negated when it is not being driven by the tool. Note that the pull-up and pull-down resistors on the $\overline{\text{QACK}}$ signal are mutually exclusive and it is never necessary to populate both in a system. To preserve correct power-down operation, $\overline{\text{QACK}}$ should be merged through logic so that it also can be driven by the bridge or system logic.

Figure 21. JTAG Interface Connection
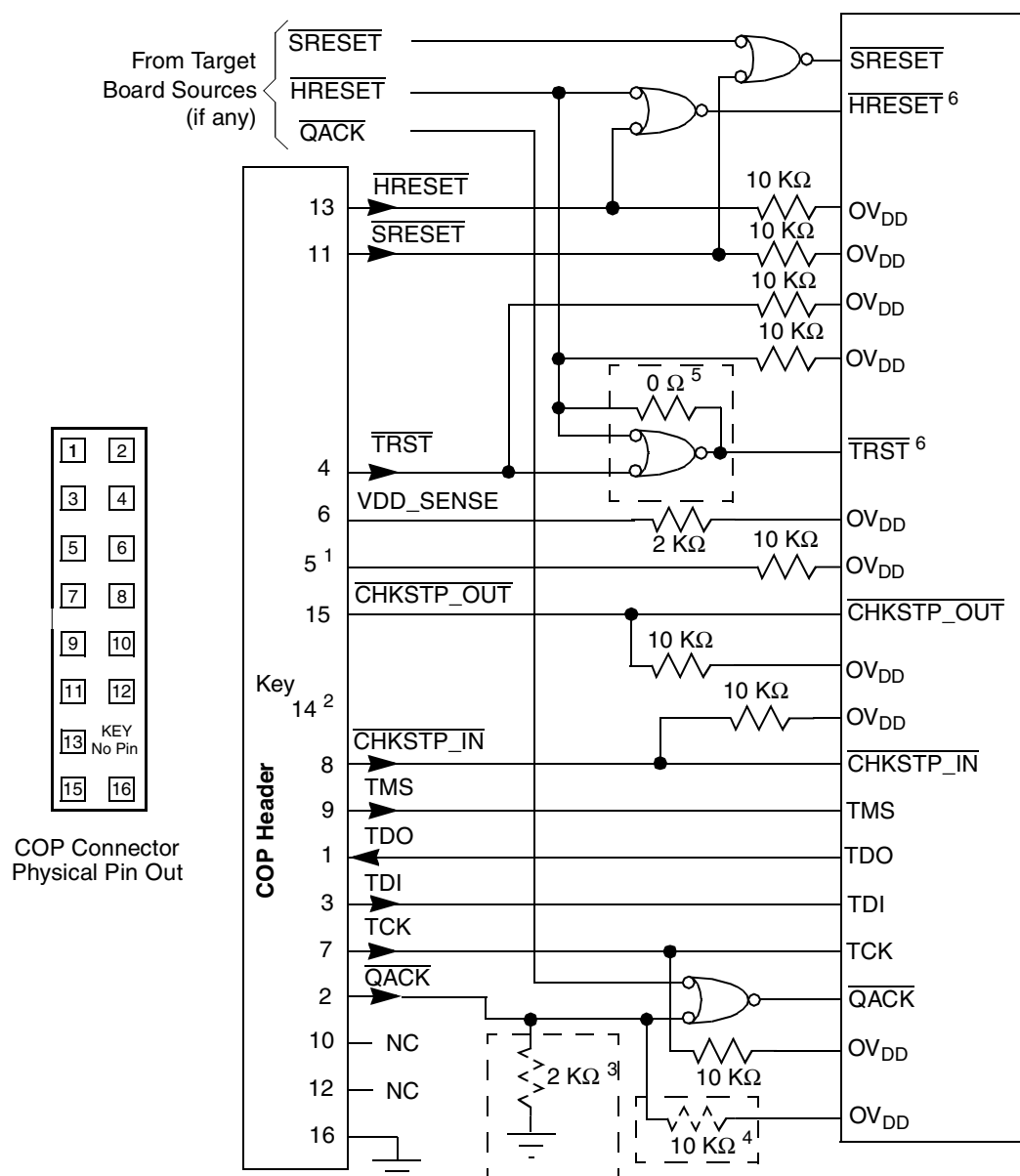
Notes:

1. RUN/$\overline{\text{STOP}}$, normally found on pin 5 of the COP header, is not implemented on the MPC7448. Connect pin 5 of the COP header to OV_{DD} with a 10-KΩ pull-up resistor.

2. Key location; pin 14 is not physically present on the COP header.

3. Component not populated. Populate only if debug tool does not drive $\overline{\text{QACK}}$.

4. Populate only if debug tool uses an open-drain type output and does not actively negate $\overline{\text{QACK}}$.

5. If the JTAG interface is implemented, connect $\overline{\text{HRESET}}$ from the target source to $\overline{\text{TRST}}$ from the COP header though an AND gate to $\overline{\text{TRST}}$ of the part. If the JTAG interface is not implemented, connect $\overline{\text{HRESET}}$ from the target source to $\overline{\text{TRST}}$ of the part through a 0-Ω isolation resistor.

6. The COP port and target board should be able to independently assert $\overline{\text{HRESET}}$ and $\overline{\text{TRST}}$ to the processor in order to fully control the processor as shown above.

of any thermal interface material depends on many factors—thermal performance requirements, manufacturability, service temperature, dielectric properties, cost, and so on.
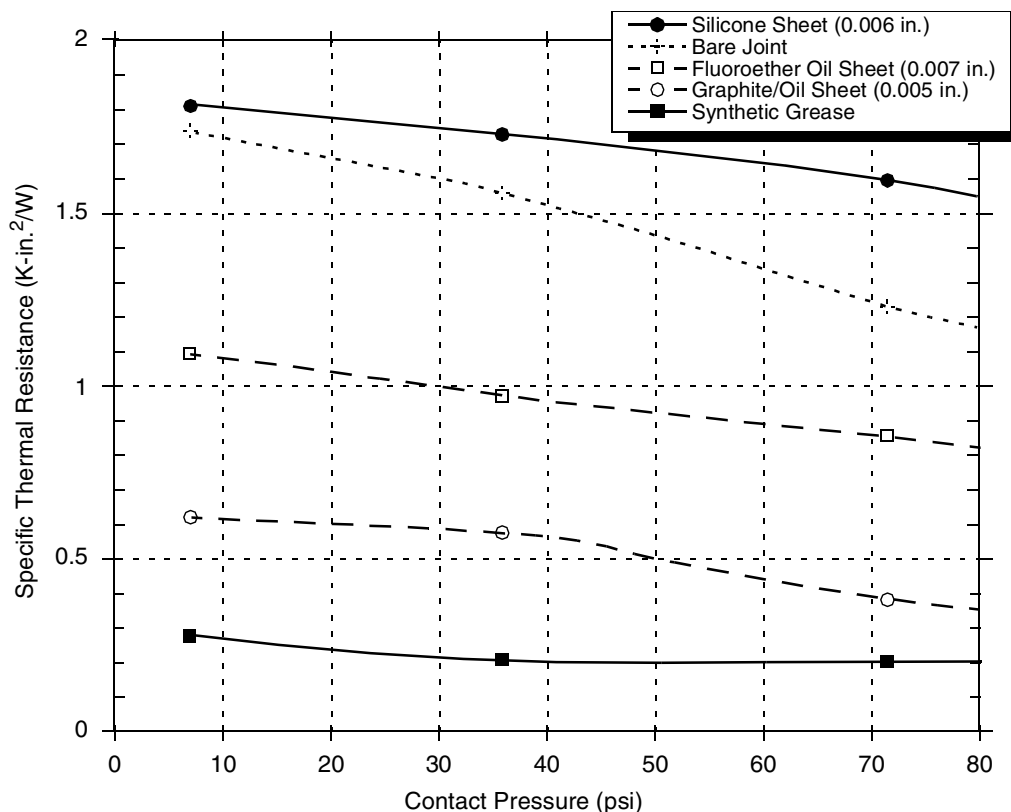
Figure 25. Thermal Performance of Select Thermal Interface Material

The board designer can choose between several types of thermal interfaces. Heat sink adhesive materials should be selected based on high conductivity and mechanical strength to meet equipment shock/vibration requirements. There are several commercially available thermal interfaces and adhesive materials provided by the following vendors:

The Bergquist Company   800-347-4572
18930 West 78th St.
Chanhassen, MN 55317
Internet: www.bergquistcompany.com

Chomerics, Inc.   781-935-4850
77 Dragon Ct.
Woburn, MA 01801
Internet: www.chomerics.com

Dow-Corning Corporation   800-248-2481
Corporate Center
P.O. Box 994.
Midland, MI 48686-0994
Internet: www.dowcorning.com

9.7.4 Temperature Diode

The MPC7448 has a temperature diode on the microprocessor that can be used in conjunction with other system temperature monitoring devices (such as Analog Devices, ADT7461™). These devices use the negative temperature coefficient of a diode operated at a constant current to determine the temperature of the microprocessor and its environment. For proper operation, the monitoring device used should auto-calibrate the device by canceling out the V_{BE} variation of each MPC7448's internal diode.

The following are the specifications of the MPC7448 on-board temperature diode:

$V_f > 0.40$ V

$V_f < 0.90$ V

Operating range 2–300 µA

Diode leakage < 10 nA @ 125°C

Ideality factor over 5–150 µA at 60°C: n = 1.0275 ± 0.9%

Ideality factor is defined as the deviation from the ideal diode equation:

$$I_{fw} = I_s \left[e^{\frac{qV_f}{nKT}} - 1 \right]$$

Another useful equation is:

$$V_H - V_L = n\frac{KT}{q} \left[ln\,\frac{I_H}{I_L} \right] - 1$$

Where:

I_{fw} = Forward current

I_s = Saturation current

V_d = Voltage at diode

V_f = Voltage forward biased

V_H = Diode voltage while I_H is flowing

V_L = Diode voltage while I_L is flowing

I_H = Larger diode bias current

I_L = Smaller diode bias current

q = Charge of electron (1.6 x 10^{-19} C)

n = Ideality factor (normally 1.0)

K = Boltzman's constant (1.38 x 10^{-23} Joules/K)

T = Temperature (Kelvins)

The ratio of I_H to I_L is usually selected to be 10:1. The previous equation simplifies to the following:

$$V_H - V_L = 1.986 \times 10^{-4} \times nT$$

Table 16. Valid Divide Ratio Configurations

DFS mode disabled		DFS divide-by-2 mode enabled (HID1[DFS2] = 1 or $\overline{DFS2}$ = 0)		DFS divide-by-4 mode enabled (HID1[DFS4] = 1 or $\overline{DFS4}$ = 0)	
Bus-to-Core Multiplier Configured by PLL_CFG[0:5] (see Table 12)	HID1[PC0-5] [3]	Bus-to-Core Multiplier	HID1[PC0-5] [3]	Bus-to-Core Multiplier	HID1[PC0-5] [3]
2x [4]	010000	N/A (unchanged) [1]	unchanged [1]	N/A (unchanged) [1]	unchanged [1]
3x [4]	100000	N/A (unchanged) [1]	unchanged [1]	N/A (unchanged) [1]	unchanged [1]
4x [4]	101000	2x [4]	010000	N/A (unchanged) [1]	unchanged [1]
5x	101100	2.5x [4]	010101	N/A (unchanged) [1]	unchanged [1]
5.5x	100100	2.75x [4]	110101 [2]	N/A (unchanged) [1]	unchanged [1]
6x	110100	3x [4]	100000	N/A (unchanged) [1]	unchanged [1]
6.5x	010100	3.25x [4]	100000 [2]	N/A (unchanged) [1]	unchanged [1]
7x	001000	3.5x [4]	110101	N/A (unchanged) [1]	unchanged [1]
7.5x	000100	3.75x [4]	110101 [2]	N/A (unchanged) [1]	unchanged [1]
8x	110000	4x [4]	101000 [4]	2x [4]	010000
8.5x	011000	4.25x [4]	101000 [2]	N/A (unchanged) [1]	unchanged [1]
9x	011110	4.5x [4]	011101	2.25x [4]	010000 [2]
9.5x	011100	4.75x [4]	011101 [2]	N/A (unchanged) [1]	unchanged [1]
10x	101010	5x	101100	2.5x [4]	010101
10.5x	100010	5.25x	101100 [2]	N/A (unchanged) [1]	unchanged [1]
11x	100110	5.5x	100100	2.75x [4]	010101 [2]
11.5x	000000	5.75x	100100 [2]	N/A (unchanged) [1]	unchanged [1]
12x	101110	6x	110100	3x [4]	100000
12.5x	111110	6.25x	110100 [2]	N/A (unchanged) [1]	unchanged [1]
13x	010110	6.5x	010100	3.25x [4]	100000 [2]
13.5x	111000	6.75	010100 [2]	N/A (unchanged) [1]	unchanged [1]
14x	110010	7x	001000	3.5x [4]	110101
15x	000110	7.5x	000100	3.75x [4]	110101 [2]
16x	110110	8x	110000	4x [4]	101000
17x	000010	8.5x	011000	4.25x [4]	101000 [2]
18x	001010	9x	011110	4.5x [4]	011101
20x	001110	10x	101010	5x	101100
21x	010010	10.5x	100010	5.25x	101100 [2]

Table 16. Valid Divide Ratio Configurations (continued)

DFS mode disabled		DFS divide-by-2 mode enabled (HID1[DFS2] = 1 or $\overline{DFS2}$ = 0)		DFS divide-by-4 mode enabled (HID1[DFS4] = 1 or $\overline{DFS4}$ = 0)	
Bus-to-Core Multiplier Configured by PLL_CFG[0:5] (see Table 12)	HID1[PC0-5] [3]	Bus-to-Core Multiplier	HID1[PC0-5] [3]	Bus-to-Core Multiplier	HID1[PC0-5] [3]
24x	011010	12x	101110	6x	110100
28x	111010	14x	110010	7x	001000

Notes:

1. DFS mode is not supported for this combination of DFS mode and PLL_CFG[0:5] setting. As a result, the processor will ignore these settings and remain at the previous multiplier, as reflected by the HID1[PC0-PC5] bits.

2. Though supported by the MPC7448 clock circuitry, multipliers of $n.25x$ and $n.75x$ cannot be expressed as valid PLL configuration codes. As a result, the values displayed in HID1[PC0-PC5] are rounded down to the nearest valid PLL configuration code. However, the actual bus-to-core multiplier is as stated in this table.

3. Note that in the HID1 register of the MPC7448, the PC0, PC1, PC2, PC3, PC4, and PC5 bits are bits 15, 16, 17, 18, 19, and 14 (respectively). See the *MPC7450 RISC Microprocessor Reference Manual* for more information.

4. Special considerations regarding snooped transactions must be observed for bus-to-core multipliers less than 5x. See the *MPC7450 RISC Microprocessor Reference Manual* for more information.

9.7.5.3 Minimum Core Frequency Requirements with DFS

In many systems, enabling DFS can result in very low processor core frequencies. However, care must be taken to ensure that the resulting processor core frequency is within the limits specified in Table 8. Proper operation of the device is not guaranteed at core frequencies below the specified minimum f_{core}.

10 Document Revision History

Table 17 provides a revision history for this hardware specification.

Table 17. Document Revision History

Revision	Date	Substantive Change(s)
4	3/2007	Table 19: Added 800 MHz processor frequency.
3	10/2006	Section 9.7, "Power and Thermal Management Information": Updated contact information. Table 18, Table 20, and Table 19: Added Revision D PVR. Table 19: Added 600 processor frequency, additional product codes, date codes for 1400 processor frequency, and footnotes 1 and 2. Table 20: Added PPC product code and footnote 1. Table 19 and Table 20: Added Revision D information for 1267 processor frequency.

Table 17. Document Revision History (continued)

Revision	Date	Substantive Change(s)
2		Table 6: Added separate input leakage specification for BVSEL0, $\overline{\text{LSSD\_MODE}}$, $\overline{\text{TCK}}$, TDI, TMS, $\overline{\text{TRST}}$ signals to correctly indicate leakage current for signals with internal pull-up resistors.
		Section 5.1: Added paragraph preceding Table 7 and edited notes in Table 7 to clarify core frequencies at which power consumption is measured.
		Section 5.3: Removed voltage derating specifications; this feature has been made redundant by new device offerings and is no longer supported.
		Changed names of "Typical–Nominal" and "Typical–Thermal" power consumption parameters to "Typical" and "Thermal", respectively. (Name change only–no specifications were changed.)
		Table 11: Revised Notes 16, 18, and 19 to reflect current recommendations for connection of SENSE pins.
		Section 9.3: Added paragraph explaining connection recommendations for SENSE pins. (See also Table 11 entry above.)
		Table 19: Updated table to reflect changes in specifications for MC7448xxnnnnNC devices.
		Table 9: Changed all instances of TT[0:3] to TT[0:4]
		Removed mention of these input signals from output valid times and output hold times:
		• AACK, CKSTP_IN, DT[0:3]
		Figure 17: Modified diagram slightly to correctly show constraint on SYSCLK ramping is related to V_{DD} voltage, not AV_{DD} voltage. (Diagram clarification only; no change in power sequencing requirements.)
		Added Table 20 to reflect introduction of extended temperature devices and associated hardware specification addendum.
1		Added 1600 MHz, 1420 MHz, and 1000 MHz devices
		Section 4: corrected die size
		Table 2: Revised Note 4 to consider overshoot/undershoot and combined with Note 5.
		Table 4: Revised operating voltage for 1700 MHz device from ± 50 mV to +20 mV / –50 mV.
		Table 7: Updated and expanded table to include Typical – Nominal power consumption.
		Table 11: Added voltage derating information for 1700 MHz devices; this feature is not supported at this time for other speed grades.
		Added transient specifications for VDD power supply in Section 9.2.3, added Table 15 and Figure 19 and renumbered subsequent tables and figures.
		Moved Decoupling Recommendations from Section 9.4 to Section 9.2.4 and renumbered subsequent sections.
		Section 9.2.1: Revised power sequencing requirements.
		Section 9.7.4: Added thermal diode ideality factor information (previously TBD).
		Table 17: Expanded table to show HID1 register values when DFS modes are enabled.
		Section 11.2: updated to include additional N-spec device speed grades
		Tables 18 and 19: corrected PVR values and added "MC" product code prefix
0		Initial public release.

11 Part Numbering and Marking

Ordering information for the part numbers fully covered by this specification document is provided in Section 11.1, "Part Numbers Fully Addressed by This Document." Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact a local Freescale sales office. In addition to the processor frequency, the part numbering scheme also includes an application modifier that may specify special application conditions. An optional specification modifier may also apply for parts to indicate a specific change in specifications, such as support for an extended temperature range. Finally, each part number contains a revision level code that refers to the die mask revision number. Section 11.2, "Part Numbers Not Fully Addressed by This Document," lists the part numbers that do not fully conform to the specifications of this document. These special part numbers require an additional document called a hardware specification addendum.

11.1 Part Numbers Fully Addressed by This Document

Table 18 provides the Freescale part numbering nomenclature for the MPC7448 part numbers fully addressed by this document. For information regarding other MPC7448 part numbers, see Section 11.2, "Part Numbers Not Fully Addressed by This Document."

Table 18. Part Numbering Nomenclature

xx	**7448**	*xx*	*nnnn*	**L**	*x*
Product Code	**Part Identifier**	**Package**	**Processor Frequency**	**Application Modifier**	**Revision Level**
MC PPC [1]	7448	HX = HCTE BGA VS = RoHS LGA VU = RoHS BGA	1700	L: 1.3 V +20/–50 mV 0 to 105 °C	C: 2.1; PVR = 0x8004_0201 D: 2.2; PVR = 0x8004_0202
			1600	L: 1.25 V ± 50 mV 0 to 105 °C	
			1420	L: 1.2 V ± 50 mV 0 to 105 °C	
			1000	L: 1.15 V ± 50 mV 0 to 105 °C	

Notes:

1. The P prefix in a Freescale part number designates a "Pilot Production Prototype" as defined by Freescale SOP 3-13. These parts have only preliminary reliability and characterization data. Before pilot production prototypes may be shipped, written authorization from the customer must be on file in the applicable sales office acknowledging the qualification status and the fact that product changes may still occur as pilot production prototypes are shipped.