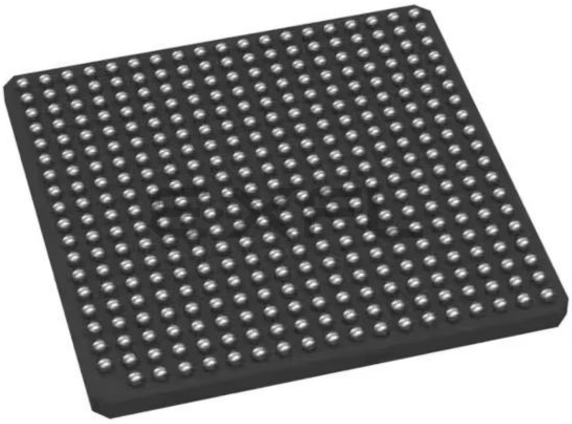

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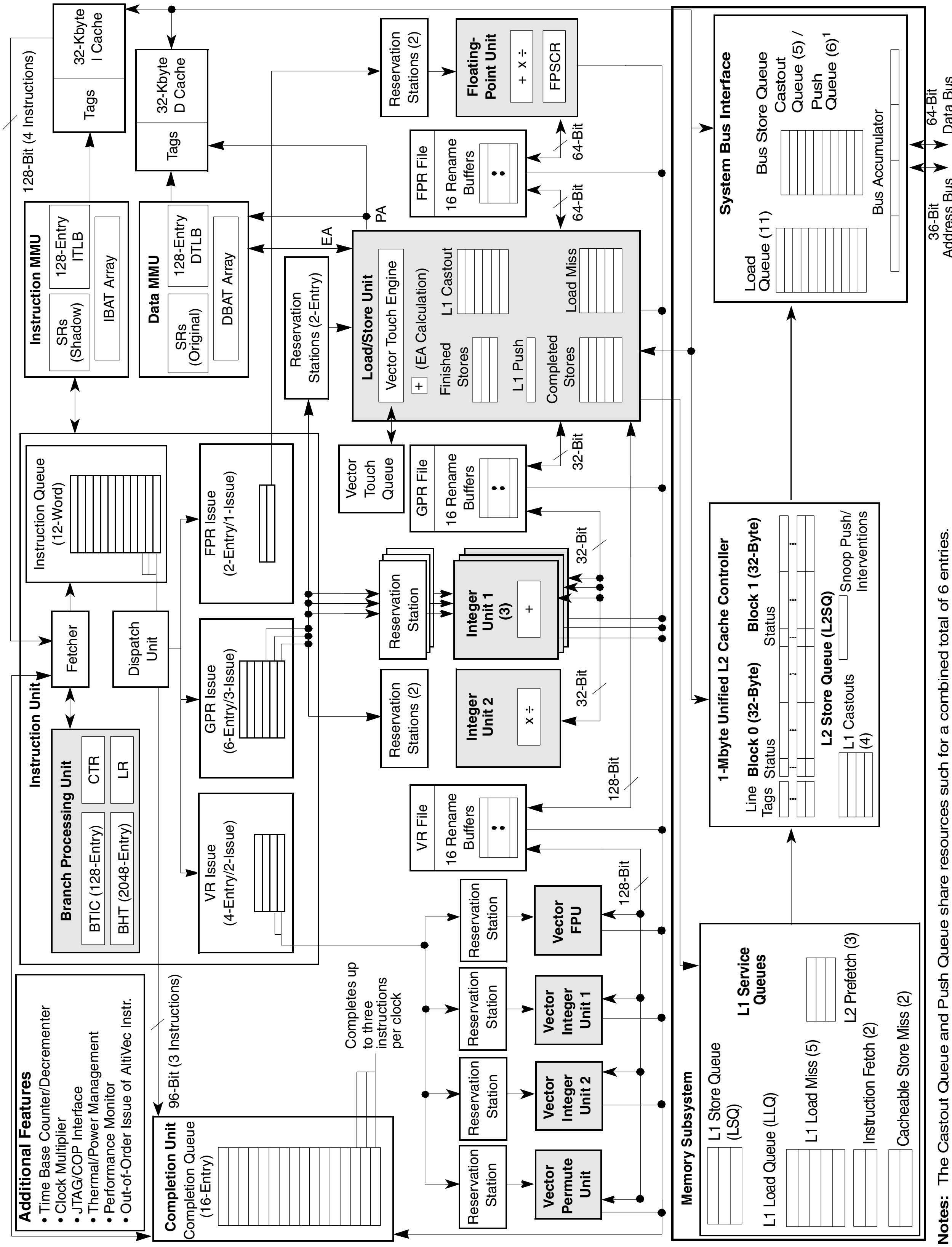
Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC G4
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	667MHz
Co-Processors/DSP	Multimedia; SIMD
RAM Controllers	-
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	1.5V, 1.8V, 2.5V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	360-CLGA, FCCLGA
Supplier Device Package	360-FCCLGA (25x25)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc7448vs667nc



Notes: The Castout Queue and Push Queue share resources such for a combined total of 6 entries. The Castout Queue itself is limited to 5 entries, ensuring 1 entry will be available for a push.

Figure 1. MPC7448 Block Diagram

— Four vector units and 32-entry vector register file (VRs)
  – Vector permute unit (VPU)
  – Vector integer unit 1 (VIU1) handles short-latency AltiVec™ integer instructions, such as vector add instructions (for example, **vaddsbs**, **vaddshs**, and **vaddsws**).
  – Vector integer unit 2 (VIU2) handles longer-latency AltiVec integer instructions, such as vector multiply add instructions (for example, **vmhaddshs**, **vmhraddshs**, and **vmladduhm**).
  – Vector floating-point unit (VFPU)

— Three-stage load/store unit (LSU)
  – Supports integer, floating-point, and vector instruction load/store traffic
  – Four-entry vector touch queue (VTQ) supports all four architected AltiVec data stream operations
  – Three-cycle GPR and AltiVec load latency (byte, half word, word, vector) with one-cycle throughput
  – Four-cycle FPR load latency (single, double) with one-cycle throughput
  – No additional delay for misaligned access within double-word boundary
  – A dedicated adder calculates effective addresses (EAs).
  – Supports store gathering
  – Performs alignment, normalization, and precision conversion for floating-point data
  – Executes cache control and TLB instructions
  – Performs alignment, zero padding, and sign extension for integer data
  – Supports hits under misses (multiple outstanding misses)
  – Supports both big- and little-endian modes, including misaligned little-endian accesses

- Three issue queues, FIQ, VIQ, and GIQ, can accept as many as one, two, and three instructions, respectively, in a cycle. Instruction dispatch requires the following:
  — Instructions can only be dispatched from the three lowest IQ entries—IQ0, IQ1, and IQ2.
  — A maximum of three instructions can be dispatched to the issue queues per clock cycle.
  — Space must be available in the CQ for an instruction to dispatch (this includes instructions that are assigned a space in the CQ but not in an issue queue).
- Rename buffers
  — 16 GPR rename buffers
  — 16 FPR rename buffers
  — 16 VR rename buffers
- Dispatch unit
  — Decode/dispatch stage fully decodes each instruction
- Completion unit
  — Retires an instruction from the 16-entry completion queue (CQ) when all instructions ahead of it have been completed, the instruction has finished executing, and no exceptions are pending
  — Guarantees sequential programming model (precise exception model)

- Efficient data flow
  - — Although the VR/LSU interface is 128 bits, the L1/L2 bus interface allows up to 256 bits.
  - — The L1 data cache is fully pipelined to provide 128 bits/cycle to or from the VRs.
  - — The L2 cache is fully pipelined to provide 32 bytes per clock every other cycle to the L1 caches.
  - — As many as 16 out-of-order transactions can be present on the MPX bus.
  - — Store merging for multiple store misses to the same line. Only coherency action taken (address-only) for store misses merged to all 32 bytes of a cache block (no data tenure needed).
  - — Three-entry finished store queue and five-entry completed store queue between the LSU and the L1 data cache
  - — Separate additional queues for efficient buffering of outbound data (such as castouts and write-through stores) from the L1 data cache and L2 cache
- Multiprocessing support features include the following:
  - — Hardware-enforced, MESI cache coherency protocols for data cache
  - — Load/store with reservation instruction pair for atomic memory references, semaphores, and other multiprocessor operations
- Power and thermal management
  - — Dynamic frequency switching (DFS) feature allows processor core frequency to be halved or quartered through software to reduce power consumption.
  - — The following three power-saving modes are available to the system:
    - – Nap—Instruction fetching is halted. Only the clocks for the time base, decrementer, and JTAG logic remain running. The part goes into the doze state to snoop memory operations on the bus and then back to nap using a $\overline{\text{QREQ}}$/$\overline{\text{QACK}}$ processor-system handshake protocol.
    - – Sleep—Power consumption is further reduced by disabling bus snooping, leaving only the PLL in a locked and running state. All internal functional units are disabled.
    - – Deep sleep—When the part is in the sleep state, the system can disable the PLL. The system can then disable the SYSCLK source for greater system power savings. Power-on reset procedures for restarting and relocking the PLL must be followed upon exiting the deep sleep state.
  - — Instruction cache throttling provides control of instruction fetching to limit device temperature.
  - — A new temperature diode that can determine the temperature of the microprocessor
- Performance monitor can be used to help debug system designs and improve software efficiency.
- In-system testability and debugging features through JTAG boundary-scan capability
- Testability
  - — LSSD scan design
  - — IEEE Std. 1149.1™ JTAG interface

Table 9. Processor Bus AC Timing Specifications[1] (continued)

At recommended operating conditions. See Table 4.

Parameter	Symbol [2]	All Speed Grades		Unit	Notes
		Min	Max		
SYSCLK to output high impedance (all except $\overline{TS}$, $\overline{ARTRY}$, $\overline{SHD0}$, $\overline{SHD1}$)	t_{KHOZ}	—	1.8	ns	5
SYSCLK to $\overline{TS}$ high impedance after precharge	t_{KHTSPZ}	—	1	t_{SYSCLK}	3, 4, 5
Maximum delay to $\overline{ARTRY}$/$\overline{SHD0}$/$\overline{SHD1}$ precharge	t_{KHARP}	—	1	t_{SYSCLK}	3, 5, 6, 7
SYSCLK to $\overline{ARTRY}$/$\overline{SHD0}$/$\overline{SHD1}$ high impedance after precharge	t_{KHARPZ}	—	2	t_{SYSCLK}	3, 5, 6, 7

Notes:

1. All input specifications are measured from the midpoint of the signal in question to the midpoint of the rising edge of the input SYSCLK. All output specifications are measured from the midpoint of the rising edge of SYSCLK to the midpoint of the signal in question. All output timings assume a purely resistive 50-Ω load (see Figure 4). Input and output timings are measured at the pin; time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. The symbology used for timing specifications herein follows the pattern of $t_{(signal)(state)(reference)(state)}$ for inputs and $t_{(reference)(state)(signal)(state)}$ for outputs. For example, t_{IVKH} symbolizes the time input signals (I) reach the valid state (V) relative to the SYSCLK reference (K) going to the high (H) state or input setup time. And t_{KHOV} symbolizes the time from SYSCLK(K) going high (H) until outputs (O) are valid (V) or output valid time. Input hold time can be read as the time that the input signal (I) went invalid (X) with respect to the rising clock edge (KH) (note the position of the reference and its state for inputs) and output hold time can be read as the time from the rising edge (KH) until the output went invalid (OX).
3. t_{sysclk} is the period of the external clock (SYSCLK) in ns. The numbers given in the table must be multiplied by the period of SYSCLK to compute the actual time duration (in ns) of the parameter in question.
4. According to the bus protocol, $\overline{TS}$ is driven only by the currently active bus master. It is asserted low and precharged high before returning to high impedance, as shown in Figure 6. The nominal precharge width for $\overline{TS}$ is t_{SYSCLK}, that is, one clock period. Since no master can assert $\overline{TS}$ on the following clock edge, there is no concern regarding contention with the precharge. Output valid and output hold timing is tested for the signal asserted. Output valid time is tested for precharge.The high-impedance behavior is guaranteed by design.
5. Guaranteed by design and not tested
6. According to the bus protocol, $\overline{ARTRY}$ can be driven by multiple bus masters through the clock period immediately following $\overline{AACK}$. Bus contention is not an issue because any master asserting $\overline{ARTRY}$ will be driving it low. Any master asserting it low in the first clock following $\overline{AACK}$ will then go to high impedance for a fraction of a cycle, then negated for up to an entire cycle (crossing a bus cycle boundary) before being three-stated again. The nominal precharge width for $\overline{ARTRY}$ is 1.0 t_{SYSCLK}; that is, it should be high impedance as shown in Figure 6 before the first opportunity for another master to assert $\overline{ARTRY}$. Output valid and output hold timing is tested for the signal asserted.The high-impedance behavior is guaranteed by design.
7. According to the MPX bus protocol, $\overline{SHD0}$ and $\overline{SHD1}$ can be driven by multiple bus masters beginning two cycles after $\overline{TS}$. Timing is the same as $\overline{ARTRY}$, that is, the signal is high impedance for a fraction of a cycle, then negated for up to an entire cycle (crossing a bus cycle boundary) before being three-stated again. The nominal precharge width for $\overline{SHD0}$ and $\overline{SHD1}$ is 1.0 t_{SYSCLK}. The edges of the precharge vary depending on the programmed ratio of core to bus (PLL configurations).
8. $\overline{BMODE}$[0:1] and BVSEL[0:1] are mode select inputs. $\overline{BMODE}$[0:1] are sampled before and after $\overline{HRESET}$ negation. BVSEL[0:1] are sampled before $\overline{HRESET}$ negation. These parameters represent the input setup and hold times for each sample. These values are guaranteed by design and not tested. $\overline{BMODE}$[0:1] must remain stable after the second sample; BVSEL[0:1] must remain stable after the first (and only) sample. See Figure 5 for sample timing.

Figure 4 provides the AC test load for the MPC7448.

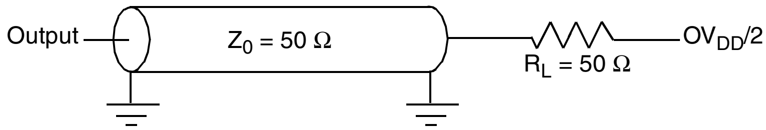


Figure 4. AC Test Load

Figure 5 provides the $\overline{\text{BMODE}}$[0:1] input timing diagram for the MPC7448. These mode select inputs are sampled once before and once after $\overline{\text{HRESET}}$ negation.

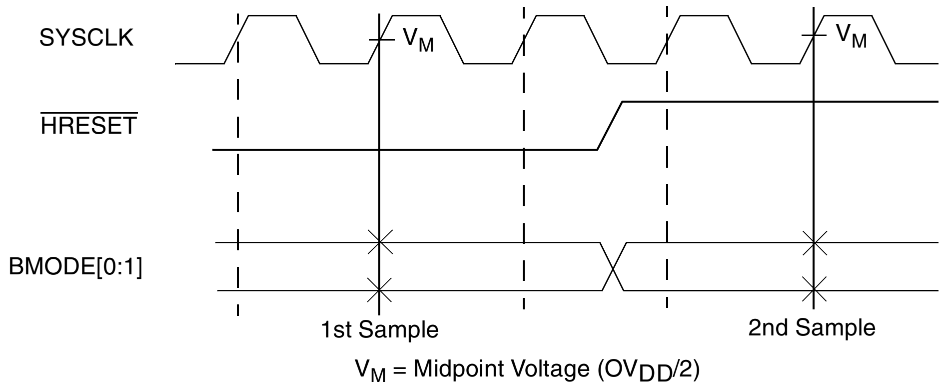


Figure 5. $\overline{\text{BMODE}}$[0:1] Input Sample Timing Diagram

6 Pin Assignments

Figure 12 (in Part A) shows the pinout of the MPC7448, 360 high coefficient of thermal expansion ceramic ball grid array (HCTE) package as viewed from the top surface. Part B shows the side profile of the HCTE package to indicate the direction of the top surface view.

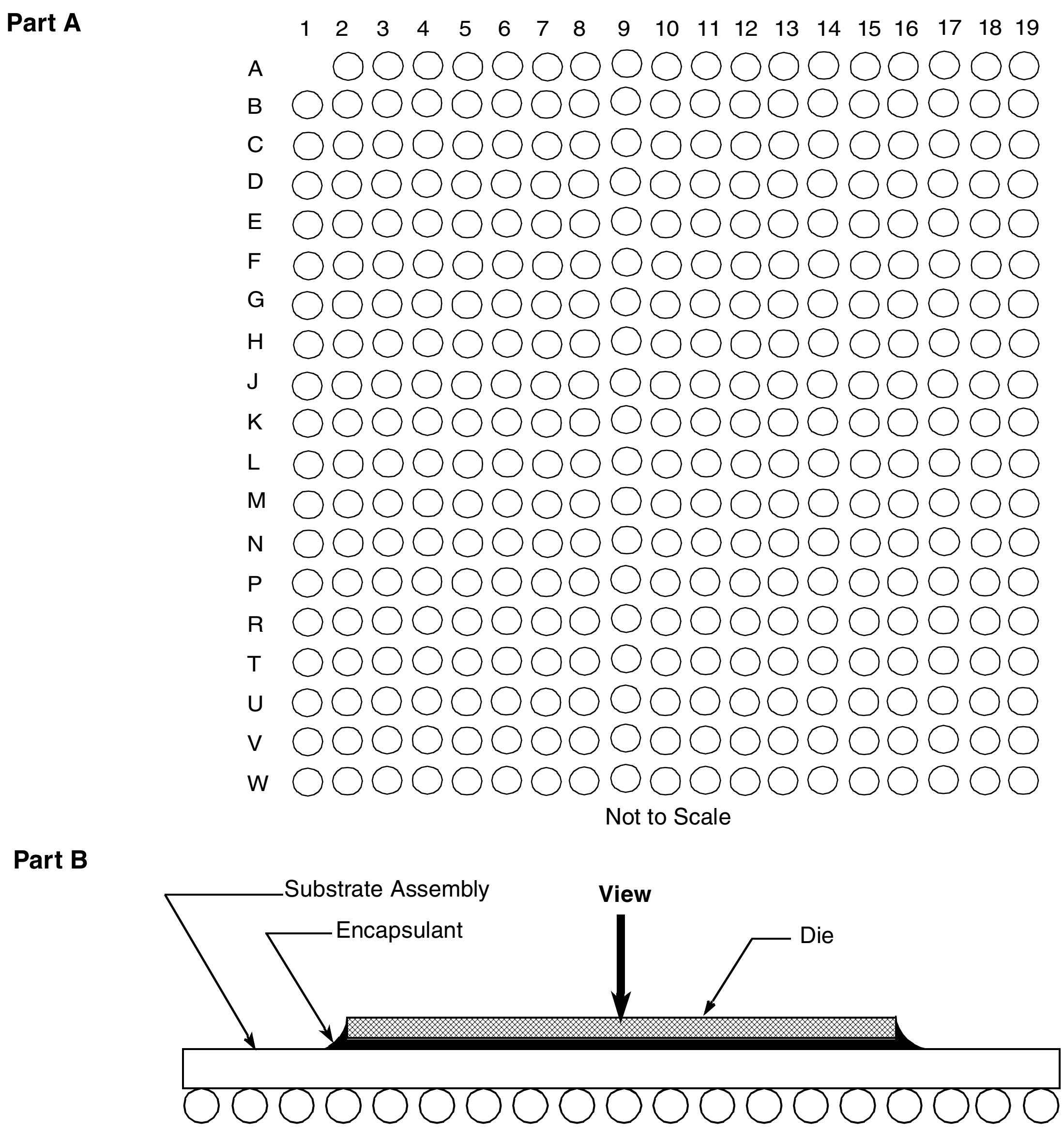


Figure 12. Pinout of the MPC7448, 360 HCTE Package as Viewed from the Top Surface

Table 11. Pinout Listing for the MPC7448, 360 HCTE Package (continued)

Signal Name	Pin Number	Active	I/O	Notes
$\overline{\text{LVRAM}}$	B10	—	—	12, 20, 22
NC (no connect)	A6, A14, A15, B14, B15, C14, C15, C16, C17, C18, C19, D14, D15, D16, D17, D18, D19, E14, E15, F14, F15, G14, G15, H15, H16, J15, J16, J17, J18, J19, K15, K16, K17, K18, K19, L15, L16, L17, L18, L19	—	—	11
$\overline{\text{LSSD\_MODE}}$	E8	Low	Input	6, 12
$\overline{\text{MCP}}$	C9	Low	Input	
OV_{DD}	B4, C2, C12, D5, F2, H3, J5, K2, L5, M3, N6, P2, P8, P11, R4, R13, R16, T6, T9, U2, U12, U16, V4, V7, V10, V14	—	—	
OVDD_SENSE	E18, G18	—	—	16
PLL_CFG[0:4]	B8, C8, C7, D7, A7	High	Input	
PLL_CFG[5]	D10	High	Input	9, 20
$\overline{\text{PMON\_IN}}$	D9	Low	Input	13
$\overline{\text{PMON\_OUT}}$	A9	Low	Output	
$\overline{\text{QACK}}$	G5	Low	Input	
$\overline{\text{QREQ}}$	P4	Low	Output	
$\overline{\text{SHD}}$[0:1]	E4, H5	Low	I/O	3
$\overline{\text{SMI}}$	F9	Low	Input	
$\overline{\text{SRESET}}$	A2	Low	Input	
SYSCLK	A10	—	Input	
$\overline{\text{TA}}$	K6	Low	Input	
TBEN	E1	High	Input	
$\overline{\text{TBST}}$	F11	Low	Output	
TCK	C6	High	Input	
TDI	B9	High	Input	6
TDO	A4	High	Output	
$\overline{\text{TEA}}$	L1	Low	Input	
TEMP_ANODE	N18	—	—	17
TEMP_CATHODE	N19	—	—	17
TMS	F1	High	Input	6
$\overline{\text{TRST}}$	A5	Low	Input	6, 14
$\overline{\text{TS}}$	L4	Low	I/O	3
TSIZ[0:2]	G6, F7, E7	High	Output	
TT[0:4]	E5, E6, F6, E9, C5	High	I/O	
$\overline{\text{WT}}$	D3	Low	Output	
V_{DD}	H8, H10, H12, J7, J9, J11, J13, K8, K10, K12, K14, L7, L9, L11, L13, M8, M10, M12	—	—	
V_{DD}	A13, A16, A18, B17, B19, C13, E13, E16, F12, F17, F19, G11, G16, H14, H17, H19, M14, M16, M18, N15, N17, P16, P18	—	—	15

8 Package Description

The following sections provide the package parameters and mechanical dimensions for the HCTE package.

8.1 Package Parameters for the MPC7448, 360 HCTE BGA

The package parameters are as provided in the following list. The package type is 25 × 25 mm, 360-lead high coefficient of thermal expansion ceramic ball grid array (HCTE).

Package outline	25 × 25 mm
Interconnects	360 (19 × 19 ball array – 1)
Pitch	1.27 mm (50 mil)
Minimum module height	2.32 mm
Maximum module height	2.80 mm
Ball diameter	0.89 mm (35 mil)
Coefficient of thermal expansion	12.3 ppm/°C

8.5 Package Parameters for the MPC7448, 360 HCTE RoHS-Compliant BGA

The package parameters are as provided in the following list. The package type is 25 × 25 mm, 360-lead high coefficient of thermal expansion ceramic ball grid array (HCTE) with RoHS-compliant lead-free spheres.

Package outline	25 × 25 mm
Interconnects	360 (19 × 19 ball array – 1)
Pitch	1.27 mm (50 mil)
Minimum module height	1.92 mm
Maximum module height	2.40 mm
Ball diameter	0.75 mm (30 mil)
Coefficient of thermal expansion	12.3 ppm/°C

Table 12. MPC7448 Microprocessor PLL Configuration Example (continued)

PLL_CFG[0:5]	Example Core and VCO Frequency in MHz										
	Bus-to-Core Multiplier [5]	Core-to-VCO Multiplier [5]	Bus (SYSCLK) Frequency								
			33.3 MHz	50 MHz	66.6 MHz	75 MHz	83 MHz	100 MHz	133 MHz	167 MHz	200 MHz
100110	11x	1x			733	825	913	1100	1467		
000000	11.5x	1x			766	863	955	1150	1533		
101110	12x	1x		600	800	900	996	1200	1600		
111110	12.5x	1x		625	833	938	1038	1250	1667		
010110	13x	1x		650	865	975	1079	1300			
111000	13.5x	1x		675	900	1013	1121	1350			
110010	14x	1x		700	933	1050	1162	1400			
000110	15x	1x		750	1000	1125	1245	1500			
110110	16x	1x		800	1066	1200	1328	1600			
000010	17x	1x		850	1132	1275	1417	1700			
001010	18x	1x	600	900	1200	1350	1500				
001110	20x	1x	667	1000	1332	1500	1666				
010010	21x	1x	700	1050	1399	1575					
011010	24x	1x	800	1200	1600						
111010	28x	1x	933	1400							
001100	PLL bypass		PLL off, SYSCLK clocks core circuitry directly								
111100	PLL off		PLL off, no core clocking occurs								

Notes:

1. PLL_CFG[0:5] settings not listed are reserved.
2. The sample bus-to-core frequencies shown are for reference only. Some PLL configurations may select bus, core, or VCO frequencies which are not useful, not supported, or not tested for by the MPC7448; see Section 5.2.1, "Clock AC Specifications," for valid SYSCLK, core, and VCO frequencies.
3. In PLL-bypass mode, the SYSCLK input signal clocks the internal processor directly and the PLL is disabled. However, the bus interface unit requires a 2x clock to function. Therefore, an additional signal, EXT_QUAL, must be driven at half the frequency of SYSCLK and offset in phase to meet the required input setup t_{IVKH} and hold time t_{IXKH} (see Table 9). The result will be that the processor bus frequency will be one-half SYSCLK, while the internal processor is clocked at SYSCLK frequency. This mode is intended for factory use and emulator tool use only.
   Note: The AC timing specifications given in this document do not apply in PLL-bypass mode.
4. In PLL-off mode, no clocking occurs inside the MPC7448 regardless of the SYSCLK input.
5. Applicable when DFS modes are disabled. These multipliers change when operating in a DFS mode. See Section 9.7.5, "Dynamic Frequency Switching (DFS)" for more information.
6. Bus-to-core multipliers less than 5x require that assertion of AACK be delayed by one or two bus cycles to allow the processor to generate a response to a snooped transaction. See the *MPC7450 RISC Microprocessor Reference Manual* for more information.

9.1.2 System Bus Clock (SYSCLK) and Spread Spectrum Sources

Spread spectrum clock sources are an increasingly popular way to control electromagnetic interference emissions (EMI) by spreading the emitted noise to a wider spectrum and reducing the peak noise magnitude in order to meet industry and government requirements. These clock sources intentionally add long-term jitter in order to diffuse the EMI spectral content. The jitter specification given in Table 8 considers short-term (cycle-to-cycle) jitter only and the clock generator's cycle-to-cycle output jitter should meet the MPC7448 input cycle-to-cycle jitter requirement. Frequency modulation and spread are separate concerns, and the MPC7448 is compatible with spread spectrum sources if the recommendations listed in Table 13 are observed.

Table 13. Spread Spectrum Clock Source Recommendations

At recommended operating conditions. See Table 4.

Parameter	Min	Max	Unit	Notes
Frequency modulation	—	50	kHz	1
Frequency spread	—	1.0	%	1, 2

Notes:
1. Guaranteed by design
2. SYSCLK frequencies resulting from frequency spreading, and the resulting core and VCO frequencies, must meet the minimum and maximum specifications given in Table 8.

It is imperative to note that the processor's minimum and maximum SYSCLK, core, and VCO frequencies must not be exceeded regardless of the type of clock source. Therefore, systems in which the processor is operated at its maximum rated core or bus frequency should avoid violating the stated limits by using down-spreading only.

9.2 Power Supply Design and Sequencing

The following sections provide detailed information regarding power supply design for the MPC7448.

9.2.1 Power Supply Sequencing

The MPC7448 requires its power rails and clock to be applied in a specific sequence to ensure proper device operation and to prevent device damage. The power sequencing requirements are as follows:

- AV_{DD} must be delayed with respect to V_{DD} by the RC time constant of the PLL filter circuit described in Section 9.2.2, "PLL Power Supply Filtering". This time constant is nominally 100 μs.
- OV_{DD} may ramp anytime before or after V_{DD} and AV_{DD}.

Additionally, the following requirements exist regarding the application of SYSCLK:

- The voltage at the SYSCLK input must not exceed V_{DD} until V_{DD} has ramped to 0.9 V.
- The voltage at the SYSCLK input must not exceed OV_{DD} by more 20% during transients (see overshoot/undershoot specifications in Figure 2) or 0.3 V DC (see Table 2) at any time.

These requirements are shown graphically in Figure 16.

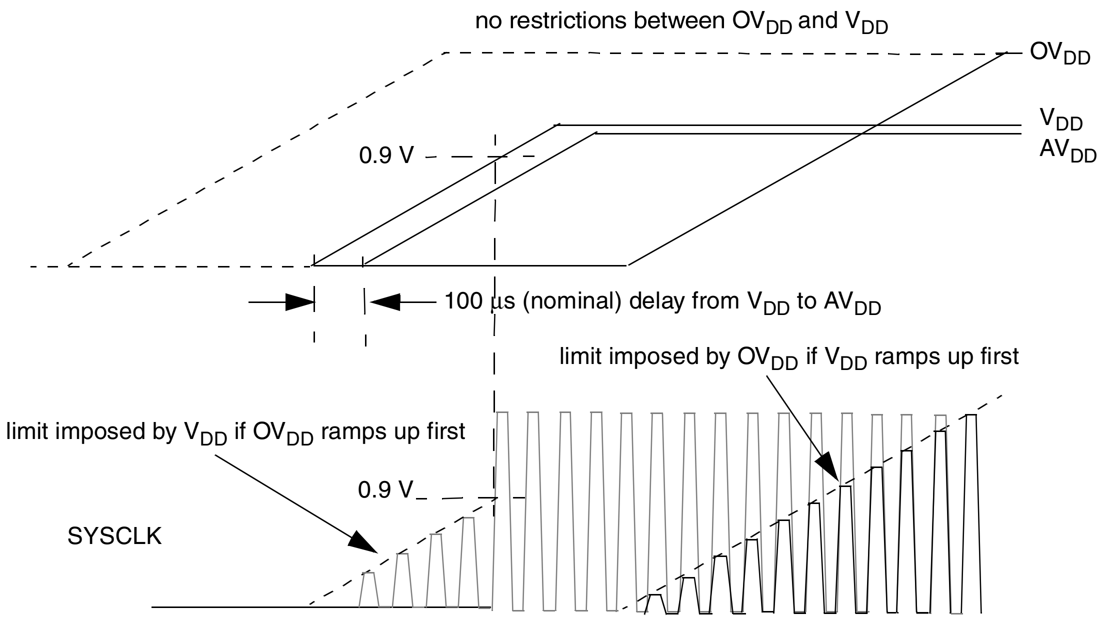


Figure 16. MPC7448 Power Up Sequencing Requirements

Certain stipulations also apply to the manner in which the power rails of the MPC7448 power down, as follows:

- OV_{DD} may ramp down any time before or after V_{DD}.
- The voltage at the SYSCLK input must not exceed V_{DD} once V_{DD} has ramped down below 0.9 V.
- The voltage at the SYSCLK input must not exceed OV_{DD} by more 20% during transients (see overshoot/undershoot specifications in Figure 2) or 0.3 V DC (see Table 2) at any time.

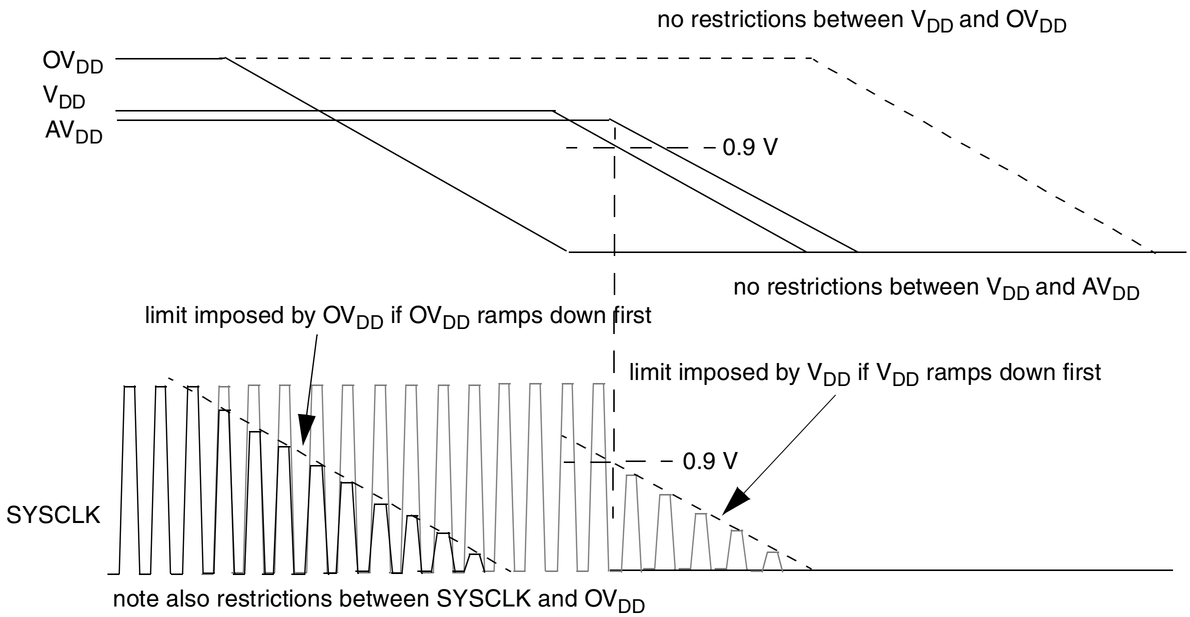


Figure 17. MPC7448 Power Down Sequencing Requirements

There is no requirement regarding AV_{DD} during power down, but it is recommended that AV_{DD} track V_{DD} within the RC time constant of the PLL filter circuit described in Section 9.2.2, "PLL Power Supply Filtering" (nominally 100 µs).

9.2.2 PLL Power Supply Filtering

The AV_{DD} power signal is provided on the MPC7448 to provide power to the clock generation PLL. To ensure stability of the internal clock, the power supplied to the AV_{DD} input signal should be filtered of any noise in the 500-KHz to 10-MHz resonant frequency range of the PLL. The circuit shown in Figure 18 using surface mount capacitors with minimum effective series inductance (ESL) is strongly recommended. In addition to filtering noise from the AV_{DD} input, it also provides the required delay between V_{DD} and AV_{DD} as described in Section 9.2.1, "Power Supply Sequencing."

The circuit should be placed as close as possible to the AV_{DD} pin to minimize noise coupled from nearby circuits. It is often possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of the device footprint.

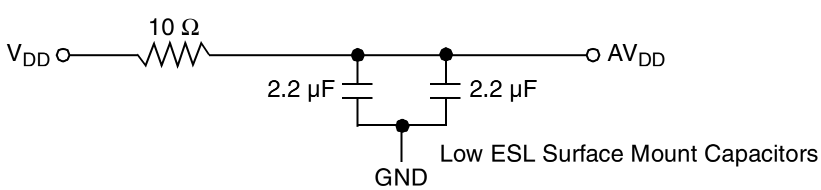


Figure 18. PLL Power Supply Filter Circuit

9.2.4 Decoupling Recommendations

Due to the MPC7448 dynamic power management feature, large address and data buses, and high operating frequencies, the MPC7448 can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the MPC7448 system, and the MPC7448 itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer use sufficient decoupling capacitors, typically one capacitor for every V_{DD} pin, and a similar amount for the OV_{DD} pins, placed as close as possible to the power pins of the MPC7448. It is also recommended that these decoupling capacitors receive their power from separate V_{DD}, OV_{DD}, and GND power planes in the PCB, using short traces to minimize inductance.

These capacitors should have a value of 0.01 or 0.1 µF. Only ceramic surface mount technology (SMT) capacitors should be used to minimize lead inductance. Orientations where connections are made along the length of the part, such as 0204, are preferable but not mandatory. Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993) and contrary to previous recommendations for decoupling Freescale microprocessors, multiple small capacitors of equal value are recommended over using multiple values of capacitance.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V_{DD} and OV_{DD} planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low equivalent series resistance (ESR) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors are 100–330 µF (AVX TPS tantalum or Sanyo OSCON).

9.3 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. Unless otherwise noted, unused active low inputs should be tied to OV_{DD} and unused active high inputs should be connected to GND. All NC (no connect) signals must remain unconnected.

Power and ground connections must be made to all external V_{DD}, OV_{DD}, and GND pins in the MPC7448. For backward compatibility with the MPC7447, MPC7445, and MP7441, or for migrating a system originally designed for one of these devices to the MPC7448, the new power and ground signals (formerly NC, see Table 11) may be left unconnected if the core frequency is 1 GHz or less. Operation above 1 GHz requires that these additional power and ground signals be connected, and it is strongly recommended that all new designs include the additional connections. See also Section 7, "Pinout Listings," for additional information.

The MPC7448 provides VDD_SENSE, OVDD_SENSE, and GND_SENSE pins. These pins connect directly to the power/ground planes in the device package and are intended to allow an external device to measure the voltage present on the V_{DD}, OV_{DD} and GND planes in the device package. The most common use for these signals is as a feedback signal to a power supply regulator to allow it to compensate for board losses and supply the correct voltage at the device. (Note that all voltage parameters are specified at the pins of the device.) If not used for this purpose, it is recommended that these signals be connected to test points that can be used in the event that an accurate measurement of the voltage at the device is needed during system debug. Otherwise, these signals should be connected to the appropriate power/ground planes on the circuit board or left unconnected.

9.4 Output Buffer DC Impedance

The MPC7448 processor bus drivers are characterized over process, voltage, and temperature. To measure Z_0, an external resistor is connected from the chip pad to OV_{DD} or GND. The value of each resistor is varied until the pad voltage is $OV_{DD}/2$. Figure 20 shows the driver impedance measurement.

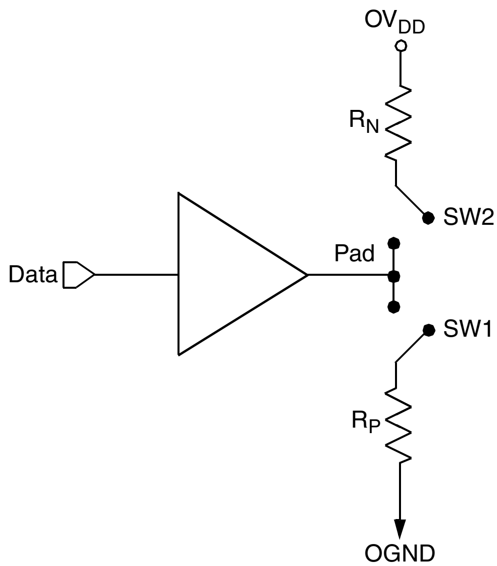


Figure 20. Driver Impedance Measurement

The output impedance is the average of two components—the resistances of the pull-up and pull-down devices. When data is held low, SW2 is closed (SW1 is open), and R_N is trimmed until the voltage at the pad equals $OV_{DD}/2$. R_N then becomes the resistance of the pull-down devices. When data is held high, SW1 is closed (SW2 is open), and R_P is trimmed until the voltage at the pad equals $OV_{DD}/2$. R_P then becomes the resistance of the pull-up devices. R_P and R_N are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N)/2$.

Table 15 summarizes the signal impedance results. The impedance increases with junction temperature and is relatively unaffected by bus voltage.

Table 15. Impedance Characteristics

At recommended operating conditions. See Table 4

Impedance		Processor Bus	Unit
Z_0	Typical	33–42	Ω
	Maximum	31–51	Ω

9.5 Pull-Up/Pull-Down Resistor Requirements

The MPC7448 requires high-resistive (weak: 4.7-KΩ) pull-up resistors on several control pins of the bus interface to maintain the control signals in the negated state after they have been actively negated and released by the MPC7448 or other bus masters. These pins are: $\overline{\text{TS}}$, $\overline{\text{ARTRY}}$, $\overline{\text{SHDO}}$, and $\overline{\text{SHD1}}$.

Some pins designated as being factory test pins must be pulled up to OV_{DD} or down to GND to ensure proper device operation. The pins that must be pulled up to OV_{DD} are $\overline{\text{LSSD\_MODE}}$ and TEST[0:3]; the pins that must be pulled down to GND are L1_TSTCLK and TEST[4]. The $\overline{\text{CKSTP\_IN}}$ signal should to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must be merged into these signals with logic.

The arrangement shown in Figure 21 allows the COP port to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$, while ensuring that the target can drive $\overline{\text{HRESET}}$ as well. If the JTAG interface and COP header will not be used, $\overline{\text{TRST}}$ should be tied to $\overline{\text{HRESET}}$ through a 0-Ω isolation resistor so that it is asserted when the system reset signal ($\overline{\text{HRESET}}$) is asserted, ensuring that the JTAG scan chain is initialized during power-on. Although Freescale recommends that the COP header be designed into the system as shown in Figure 21, if this is not possible, the isolation resistor will allow future access to $\overline{\text{TRST}}$ in the case where a JTAG interface may need to be wired onto the system in debug situations.

The COP header shown in Figure 21 adds many benefits—breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features are possible through this interface—and can be as inexpensive as an unpopulated footprint for a header to be added when needed.

The COP interface has a standard header for connection to the target system, based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header). The connector typically has pin 14 removed as a connector key.

There is no standardized way to number the COP header shown in Figure 21; consequently, many different pin numbers have been observed from emulator vendors. Some are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom, while still others number the pins counter clockwise from pin 1 (as with an IC). Regardless of the numbering, the signal placement recommended in Figure 21 is common to all known emulators.

The $\overline{\text{QACK}}$ signal shown in Figure 21 is usually connected to the bridge chip or other system control logic in a system and is an input to the MPC7448 informing it that it can go into the quiescent state. Under normal operation this occurs during a low-power mode selection. In order for COP to work, the MPC7448 must see this signal asserted (pulled down). While shown on the COP header, not all emulator products drive this signal. If the product does not, a pull-down resistor can be populated to assert this signal. Additionally, some emulator products implement open-drain type outputs and can only drive $\overline{\text{QACK}}$ asserted; for these tools, a pull-up resistor can be implemented to ensure this signal is negated when it is not being driven by the tool. Note that the pull-up and pull-down resistors on the $\overline{\text{QACK}}$ signal are mutually exclusive and it is never necessary to populate both in a system. To preserve correct power-down operation, $\overline{\text{QACK}}$ should be merged through logic so that it also can be driven by the bridge or system logic.

9.7 Power and Thermal Management Information

This section provides thermal management information for the high coefficient of thermal expansion (HCTE) package for air-cooled applications. Proper thermal control design is primarily dependent on the system-level design—the heat sink, airflow, and thermal interface material. The MPC7448 implements several features designed to assist with thermal management, including DFS and the temperature diode. DFS reduces the power consumption of the device by reducing the core frequency; see Section 9.7.5.1, "Power Consumption with DFS Enabled," for specific information regarding power reduction and DFS. The temperature diode allows an external device to monitor the die temperature in order to detect excessive temperature conditions and alert the system; see Section 9.7.4, "Temperature Diode," for more information.

To reduce the die-junction temperature, heat sinks may be attached to the package by several methods—spring clip to holes in the printed-circuit board or package, and mounting clip and screw assembly (see Figure 22); however, due to the potential large mass of the heat sink, attachment through the printed-circuit board is suggested. In any implementation of a heat sink solution, the force on the die should not exceed ten pounds (45 Newtons).

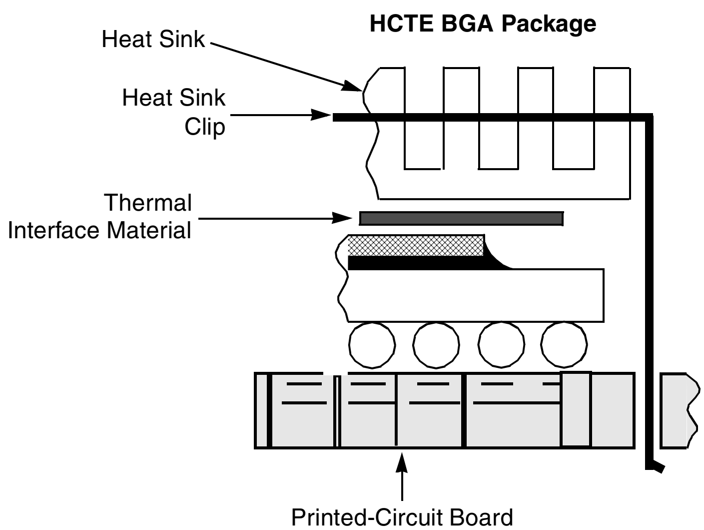


Figure 22. BGA Package Exploded Cross-Sectional View with Several Heat Sink Options

NOTE

A clip on heat sink is not recommended for LGA because there may not be adequate clearance between the device and the circuit board. A through-hole solution is recommended, as shown in Figure 23.

Table 17. Document Revision History (continued)

Revision	Date	Substantive Change(s)
2		Table 6: Added separate input leakage specification for BVSEL0, $\overline{\text{LSSD\_MODE}}$, $\overline{\text{TCK}}$, TDI, TMS, $\overline{\text{TRST}}$ signals to correctly indicate leakage current for signals with internal pull-up resistors. Section 5.1: Added paragraph preceding Table 7 and edited notes in Table 7 to clarify core frequencies at which power consumption is measured. Section 5.3: Removed voltage derating specifications; this feature has been made redundant by new device offerings and is no longer supported. Changed names of “Typical–Nominal” and “Typical–Thermal” power consumption parameters to “Typical” and “Thermal”, respectively. (Name change only–no specifications were changed.) Table 11: Revised Notes 16, 18, and 19 to reflect current recommendations for connection of SENSE pins. Section 9.3: Added paragraph explaining connection recommendations for SENSE pins. (See also Table 11 entry above.) Table 19: Updated table to reflect changes in specifications for MC7448xxnnnnNC devices. Table 9: Changed all instances of TT[0:3] to TT[0:4] Removed mention of these input signals from output valid times and output hold times: • AACK, CKSTP_IN, DT[0:3] Figure 17: Modified diagram slightly to correctly show constraint on SYSCLK ramping is related to V_{DD} voltage, not AV_{DD} voltage. (Diagram clarification only; no change in power sequencing requirements.) Added Table 20 to reflect introduction of extended temperature devices and associated hardware specification addendum.
1		Added 1600 MHz, 1420 MHz, and 1000 MHz devices Section 4: corrected die size Table 2: Revised Note 4 to consider overshoot/undershoot and combined with Note 5. Table 4: Revised operating voltage for 1700 MHz device from ± 50 mV to +20 mV / –50 mV. Table 7: Updated and expanded table to include Typical – Nominal power consumption. Table 11: Added voltage derating information for 1700 MHz devices; this feature is not supported at this time for other speed grades. Added transient specifications for VDD power supply in Section 9.2.3, added Table 15 and Figure 19 and renumbered subsequent tables and figures. Moved Decoupling Recommendations from Section 9.4 to Section 9.2.4 and renumbered subsequent sections. Section 9.2.1: Revised power sequencing requirements. Section 9.7.4: Added thermal diode ideality factor information (previously TBD). Table 17: Expanded table to show HID1 register values when DFS modes are enabled. Section 11.2: updated to include additional N-spec device speed grades Tables 18 and 19: corrected PVR values and added “MC” product code prefix
0		Initial public release.

11.2 Part Numbers Not Fully Addressed by This Document

Parts with application modifiers or revision levels not fully addressed in this specification document are described in separate hardware specification addenda which supplement and supersede this document. As such parts are released, these specifications will be listed in this section.

Table 19. Part Numbers Addressed by MC7448*xxnnnn*N*x* Series Hardware Specification Addendum (Document Order No. MPC7448ECS01AD)

xx	7448	*xx*	*nnnn*	N	*x*
Product Code	**Part Identifier**	**Package**	**Processor Frequency**	**Application Modifier**	**Revision Level**
MC	7448	HX = HCTE BGA VS = RoHS LGA VU = RoHS BGA	1400	N: 1.15 V ± 50 mV 0 to 105 °C (date code 0613 and later) [2]	C: 2.1; PVR = 0x8004_0201 D: 2.2; PVR = 0x8004_0202
MC PPC[1]			1400	N: 1.1 V ± 50 mV 0 to 105 °C (date code 0612 and prior) [2]	
MC PPC[1]			1267 Revision C only	N: 1.1 V ± 50 mV 0 to 105 °C	
MC PPC[1]			1267 Revision D only	N: 1.05 V ± 50 mV 0 to 105 °C	
MC PPC[1]			1250	N: 1.1 V ± 50 mV 0 to 105 °C	
MC PPC[1]			1000 867 800 667 600	N: 1.0 V ± 50 mV 0 to 105 °C	

Notes:
1. The P prefix in a Freescale part number designates a “Pilot Production Prototype” as defined by Freescale SOP 3-13. These parts have only preliminary reliability and characterization data. Before pilot production prototypes can be shipped, written authorization from the customer must be on file in the applicable sales office acknowledging the qualification status and the fact that product changes may still occur as pilot production prototypes are shipped.
2. Core voltage for 1400 MHz devices currently in production (date code of 0613 and later) is 1.15 V ± 50 mV; all such devices have the MC product code. The 1400 MHz devices with date code of 0612 and prior specified core voltage of 1.1 V ± 50 mV; this includes all 1400 MHz devices with the PPC product code. See Section 11.3, “Part Marking,” for information on part marking.

Table 20. Part Numbers Addressed by MC7448T*xxnnnn*N*x* Series Hardware Specification Addendum (Document Order No. MPC7448ECS02AD)

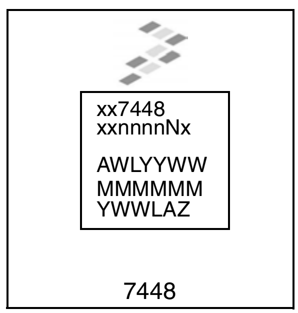
xx	7448	T	*xx*	*nnnn*	N	*x*
Product Code	**Part Identifier**	**Specification Modifier**	**Package**	**Processor Frequency**	**Application Modifier**	**Revision Level**
MC PPC[1]	7448	T = Extended Temperature Device	HX = HCTE BGA	1400	N: 1.15 V ± 50 mV – 40 to 105 °C	C: 2.1; PVR = 0x8004_0201 D: 2.2; PVR = 0x8004_0202
				1267 Revision C only	N: 1.1 V ± 50 mV – 40 to 105 °C	
				1267 Revision D only	N: 1.05 V ± 50 mV – 40 to 105 °C	
				1000	N: 1.0 V ± 50 mV – 40 to 105 °C	

Notes:

1. The P prefix in a Freescale part number designates a “Pilot Production Prototype” as defined by Freescale SOP 3-13. These parts have only preliminary reliability and characterization data. Before pilot production prototypes can be shipped, written authorization from the customer must be on file in the applicable sales office acknowledging the qualification status and the fact that product changes may still occur as pilot production prototypes are shipped.

11.3 Part Marking

Parts are marked as the example shown in Figure 27.



BGA/LGA

Notes:

AWLYYWW is the test code, where YYWW is the date code (YY = year, WW = work week)
MMMMMM is the M00 (mask) number.
YWWLAZ is the assembly traceability code.

Figure 27. Part Marking for BGA and LGA Device