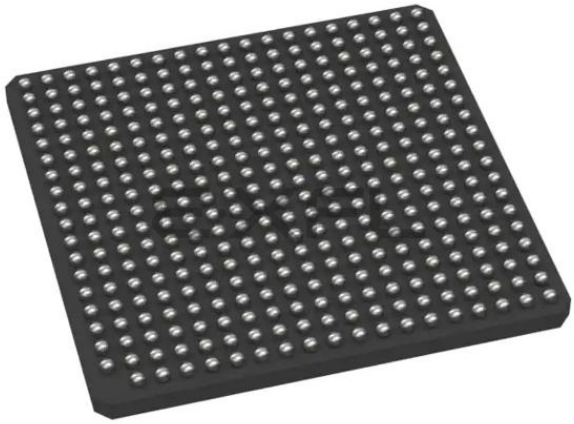

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC G4
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.0GHz
Co-Processors/DSP	Multimedia; SIMD
RAM Controllers	-
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	1.5V, 1.8V, 2.5V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	360-CBGA, FCCBGA
Supplier Device Package	360-FCCBGA (25x25)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc7448vu1000lc

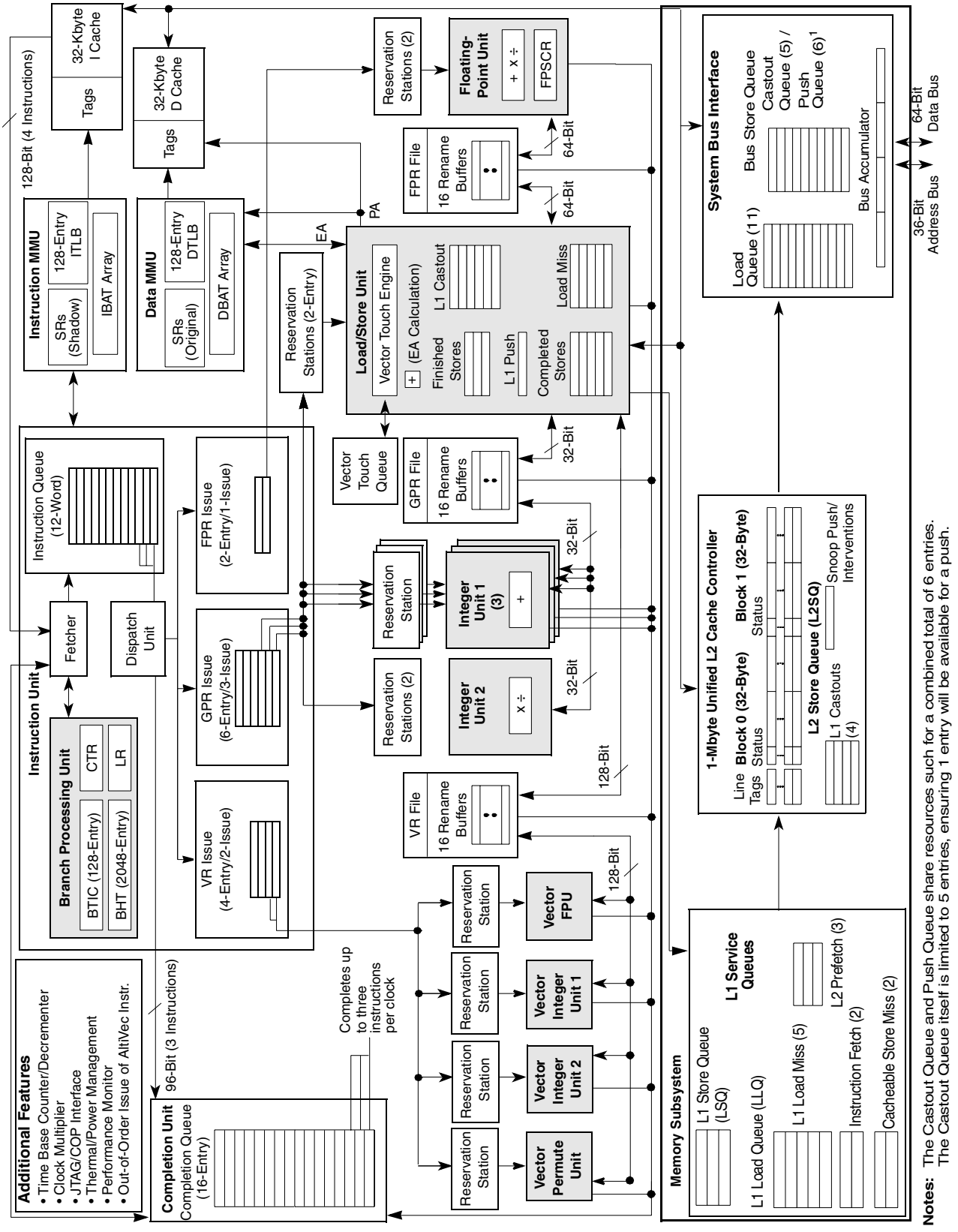


Figure 1. MPC7448 Block Diagram

- Four vector units and 32-entry vector register file (VRs)
  - Vector permute unit (VPU)
  - Vector integer unit 1 (VIU1) handles short-latency AltiVec™ integer instructions, such as vector add instructions (for example, **vaddsbs**, **vaddshs**, and **vaddsws**).
  - Vector integer unit 2 (VIU2) handles longer-latency AltiVec integer instructions, such as vector multiply add instructions (for example, **vmhaddshs**, **vmhraddshs**, and **vmladduhm**).
  - Vector floating-point unit (VFPU)
- Three-stage load/store unit (LSU)
  - Supports integer, floating-point, and vector instruction load/store traffic
  - Four-entry vector touch queue (VTQ) supports all four architected AltiVec data stream operations
  - Three-cycle GPR and AltiVec load latency (byte, half word, word, vector) with one-cycle throughput
  - Four-cycle FPR load latency (single, double) with one-cycle throughput
  - No additional delay for misaligned access within double-word boundary
  - A dedicated adder calculates effective addresses (EAs).
  - Supports store gathering
  - Performs alignment, normalization, and precision conversion for floating-point data
  - Executes cache control and TLB instructions
  - Performs alignment, zero padding, and sign extension for integer data
  - Supports hits under misses (multiple outstanding misses)
  - Supports both big- and little-endian modes, including misaligned little-endian accesses

- Three issue queues, FIQ, VIQ, and GIQ, can accept as many as one, two, and three instructions, respectively, in a cycle. Instruction dispatch requires the following:
  - Instructions can only be dispatched from the three lowest IQ entries—IQ0, IQ1, and IQ2.
  - A maximum of three instructions can be dispatched to the issue queues per clock cycle.
  - Space must be available in the CQ for an instruction to dispatch (this includes instructions that are assigned a space in the CQ but not in an issue queue).
- Rename buffers
  - 16 GPR rename buffers
  - 16 FPR rename buffers
  - 16 VR rename buffers
- Dispatch unit
  - Decode/dispatch stage fully decodes each instruction
- Completion unit
  - Retires an instruction from the 16-entry completion queue (CQ) when all instructions ahead of it have been completed, the instruction has finished executing, and no exceptions are pending
  - Guarantees sequential programming model (precise exception model)

Table 4 provides the recommended operating conditions for the MPC7448 part numbers described by this document; see Section 11.1, “Part Numbers Fully Addressed by This Document,” for more information. See Section 9.2, “Power Supply Design and Sequencing” for power sequencing requirements.

Table 4. Recommended Operating Conditions[1]

Characteristic		Symbol	Recommended Value								Unit	Notes
			1000 MHz		1420 MHz		1600 MHz		1700 MHz			
			Min	Max	Min	Max	Min	Max	Min	Max		
Core supply voltage		V_{DD}	1.15 V ± 50 mV		1.2 V ± 50 mV		1.25 V ± 50 mV		1.3 V +20/ – 50 mV		V	3, 4, 5
PLL supply voltage		AV_{DD}	1.15 V ± 50 mV		1.2 V ± 50 mV		1.25 V ± 50 mV		1.3 V +20/ – 50 mV		V	2, 3, 4
Processor bus supply voltage	I/O Voltage Mode = 1.5 V	OV_{DD}	1.5 V ± 5%		1.5 V ± 5%		1.5 V ± 5%		1.5 V ± 5%		V	4
	I/O Voltage Mode = 1.8 V		1.8 V ± 5%		1.8 V ± 5%		1.8 V ± 5%		1.8 V ± 5%			4
	I/O Voltage Mode = 2.5 V		2.5 V ± 5%		2.5 V ± 5%		2.5 V ± 5%		2.5 V ± 5%			4
Input voltage	Processor bus	V_{in}	GND	OV_{DD}	GND	OV_{DD}	GND	OV_{DD}	GND	OV_{DD}	V	
	JTAG signals	V_{in}	GND	OV_{DD}	GND	OV_{DD}	GND	OV_{DD}	GND	OV_{DD}		
Die-junction temperature		T_j	0	105	0	105	0	105	0	105	•C	6

Notes:

1. These are the recommended and tested operating conditions.
2. This voltage is the input to the filter discussed in Section 9.2.2, “PLL Power Supply Filtering,” and not necessarily the voltage at the AV_{DD} pin, which may be reduced from V_{DD} by the filter.
3. Some early devices supported voltage and frequency derating whereby VDD (and AVDD) could be reduced to reduce power consumption. This feature has been superseded and is no longer supported. See Section 5.3, “Voltage and Frequency Derating,” for more information.
4. **Caution**: Power sequencing requirements must be met; see Section 9.2, “Power Supply Design and Sequencing”.
5. **Caution**: See Section 9.2.3, “Transient Specifications” for information regarding transients on this power supply.
6. For information on extended temperature devices, see Section 11.2, “Part Numbers Not Fully Addressed by This Document.”

Table 5 provides the package thermal characteristics for the MPC7448. For more information regarding thermal management, see Section 9.7, "Power and Thermal Management Information."

Table 5. Package Thermal Characteristics[1]

Characteristic	Symbol	Value	Unit	Notes
Junction-to-ambient thermal resistance, natural convection, single-layer (1s) board	$R_{\theta JA}$	26	•C/W	2, 3
Junction-to-ambient thermal resistance, natural convection, four-layer (2s2p) board	$R_{\theta JMA}$	19	•C/W	2, 4
Junction-to-ambient thermal resistance, 200 ft/min airflow, single-layer (1s) board	$R_{\theta JMA}$	22	•C/W	2, 4
Junction-to-ambient thermal resistance, 200 ft/min airflow, four-layer (2s2p) board	$R_{\theta JMA}$	16	•C/W	2, 4
Junction-to-board thermal resistance	$R_{\theta JB}$	11	•C/W	5
Junction-to-case thermal resistance	$R_{\theta JC}$	< 0.1	•C/W	6

Notes:

1. Refer to Section 9.7, "Power and Thermal Management Information," for details about thermal management.
2. Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, airflow, power dissipation of other components on the board, and board thermal resistance.
3. Per JEDEC JESD51-2 with the single-layer board horizontal
4. Per JEDEC JESD51-6 with the board horizontal
5. Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
6. This is the thermal resistance between die and case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the calculated case temperature. The actual value of $R_{\theta JC}$ for the part is less than 0.1°C/W.

Table 6 provides the DC electrical characteristics for the MPC7448.

Table 6. DC Electrical Specifications

At recommended operating conditions. See Table 4.

Characteristic	Nominal Bus Voltage [1]	Symbol	Min	Max	Unit	Notes
Input high voltage (all inputs)	1.5	V_{IH}	$OV_{DD} \times 0.65$	$OV_{DD} + 0.3$	V	2
	1.8		$OV_{DD} \times 0.65$	$OV_{DD} + 0.3$		
	2.5		1.7	$OV_{DD} + 0.3$		
Input low voltage (all inputs)	1.5	V_{IL}	–0.3	$OV_{DD} \times 0.35$	V	2
	1.8		–0.3	$OV_{DD} \times 0.35$		
	2.5		–0.3	0.7		
Input leakage current, all signals except BVSEL0, LSSD_MODE, TCK, TDI, TMS, TRST: $V_{in} = OV_{DD}$ V_{in} = GND	—	I_{in}	—	 50 – 50	µA	2, 3
Input leakage current, BVSEL0, LSSD_MODE, TCK, TDI, TMS, TRST: $V_{in} = OV_{DD}$ V_{in} = GND	—	I_{in}	—	 50 – 2000	µA	2, 6

when running a typical benchmark at temperatures in a typical system. The Full-Power Mode–Thermal value is intended to represent the sustained power consumption of the device when running a typical code sequence at high temperature and is recommended to be used as the basis for designing a thermal solution; see Section 9.7, "Power and Thermal Management Information" for more information on thermal solutions. The Full-Power Mode–Maximum value is recommended to be used for power supply design because this represents the maximum peak power draw of the device that a power supply must be capable of sourcing without voltage droop. For information on power consumption when dynamic frequency switching is enabled, see Section 9.7.5, "Dynamic Frequency Switching (DFS)."

Table 7. Power Consumption for MPC7448 at Maximum Rated Frequency

	Die Junction Temperature (T_j)	Maximum Processor Core Frequency (Speed Grade, MHz)				Unit	Notes
		1000 MHz	1420 MHz	1600 MHz	1700 MHz		
Full-Power Mode							
Typical	65 •C	15.0	19.0	20.0	21.0	W	1, 2
Thermal	105 •C	18.6	23.3	24.4	25.6	W	1, 5
Maximum	105 •C	21.6	27.1	28.4	29.8	W	1, 3
Nap Mode							
Typical	105 •C	11.1	11.8	13.0	13.0	W	1, 6
Sleep Mode							
Typical	105 •C	10.8	11.4	12.5	12.5	W	1, 6
Deep Sleep Mode (PLL Disabled)							
Typical	105 •C	10.4	11.0	12.0	12.0	W	1, 6

Notes:

1. These values specify the power consumption for the core power supply (V_{DD}) at nominal voltage and apply to all valid processor bus frequencies and configurations. The values do not include I/O supply power (OV_{DD}) or PLL supply power (AV_{DD}). OV_{DD} power is system dependent but is typically < 5% of V_{DD} power. Worst case power consumption for AV_{DD} < 13 mW. Freescale also offers MPC7448 part numbers that meet lower power consumption specifications; for more information on these devices, see Section 11.2, "Part Numbers Not Fully Addressed by This Document."
2. Typical power consumption is an average value measured with the processor operating at its rated maximum processor core frequency (except for Deep Sleep Mode), at nominal recommended V_{DD} (see Table 4) and 65°C while running the Dhrystone 2.1 benchmark and achieving 2.3 Dhrystone MIPs/MHz. This parameter is not 100% tested but periodically sampled.b
3. Maximum power consumption is the average measured with the processor operating at its rated maximum processor core frequency, at nominal V_{DD} and maximum operating junction temperature (see Table 4) while running an entirely cache-resident, contrived sequence of instructions to keep all the execution units maximally busy.
4. Doze mode is not a user-definable state; it is an intermediate state between full-power and either nap or sleep mode. As a result, power consumption for this mode is not tested.
5. Thermal power consumption is an average value measured at the nominal recommended V_{DD} (see Table 4) and 105 °C while running the Dhrystone 2.1 benchmark and achieving 2.3 Dhrystone MIPs/MHz. This parameter is not 100% tested but periodically sampled.
6. Typical power consumption for these modes is measured at the nominal recommended V_{DD} (see Table 4) and 105 °C in the mode described. This parameter is not 100% tested but is periodically sampled.

Figure 4 provides the AC test load for the MPC7448.

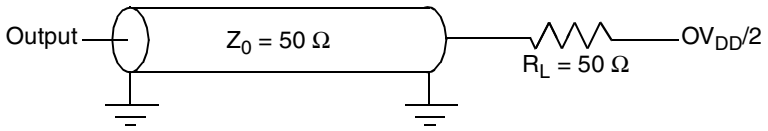


Figure 4. AC Test Load

Figure 5 provides the $\overline{\text{BMODE}}$[0:1] input timing diagram for the MPC7448. These mode select inputs are sampled once before and once after $\overline{\text{HRESET}}$ negation.

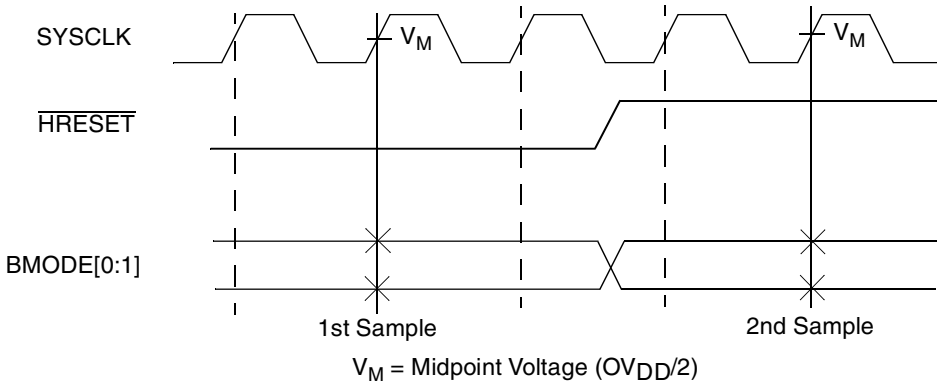


Figure 5. $\overline{\text{BMODE}}$[0:1] Input Sample Timing Diagram

Figure 11 provides the test access port timing diagram.

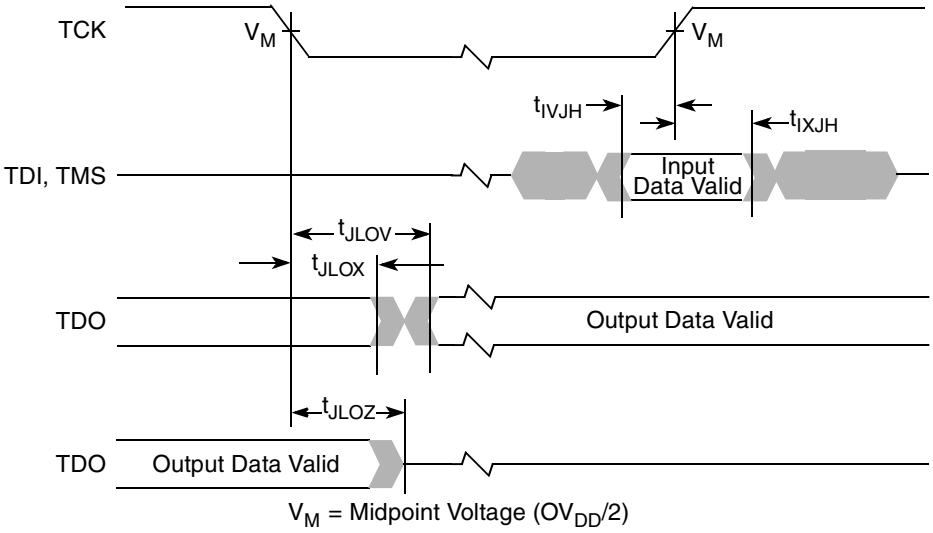


Figure 11. Test Access Port Timing Diagram

5.3 Voltage and Frequency Derating

Voltage and frequency derating is no longer supported for part numbers described by this document beginning with datecode 0613. (See Section 11, “Part Numbering and Marking,” for information on date code markings.) It is supported by some MPC7448 part numbers which target low-power applications; see Section 11.2, “Part Numbers Not Fully Addressed by This Document” and the referenced MPC7448 Hardware Specification Addenda for more information on these low-power devices. For those devices which previously supported this feature, information has been archived in the *Chip Errata for the MPC7448* (document order no. MPC7448CE).

Table 11. Pinout Listing for the MPC7448, 360 HCTE Package

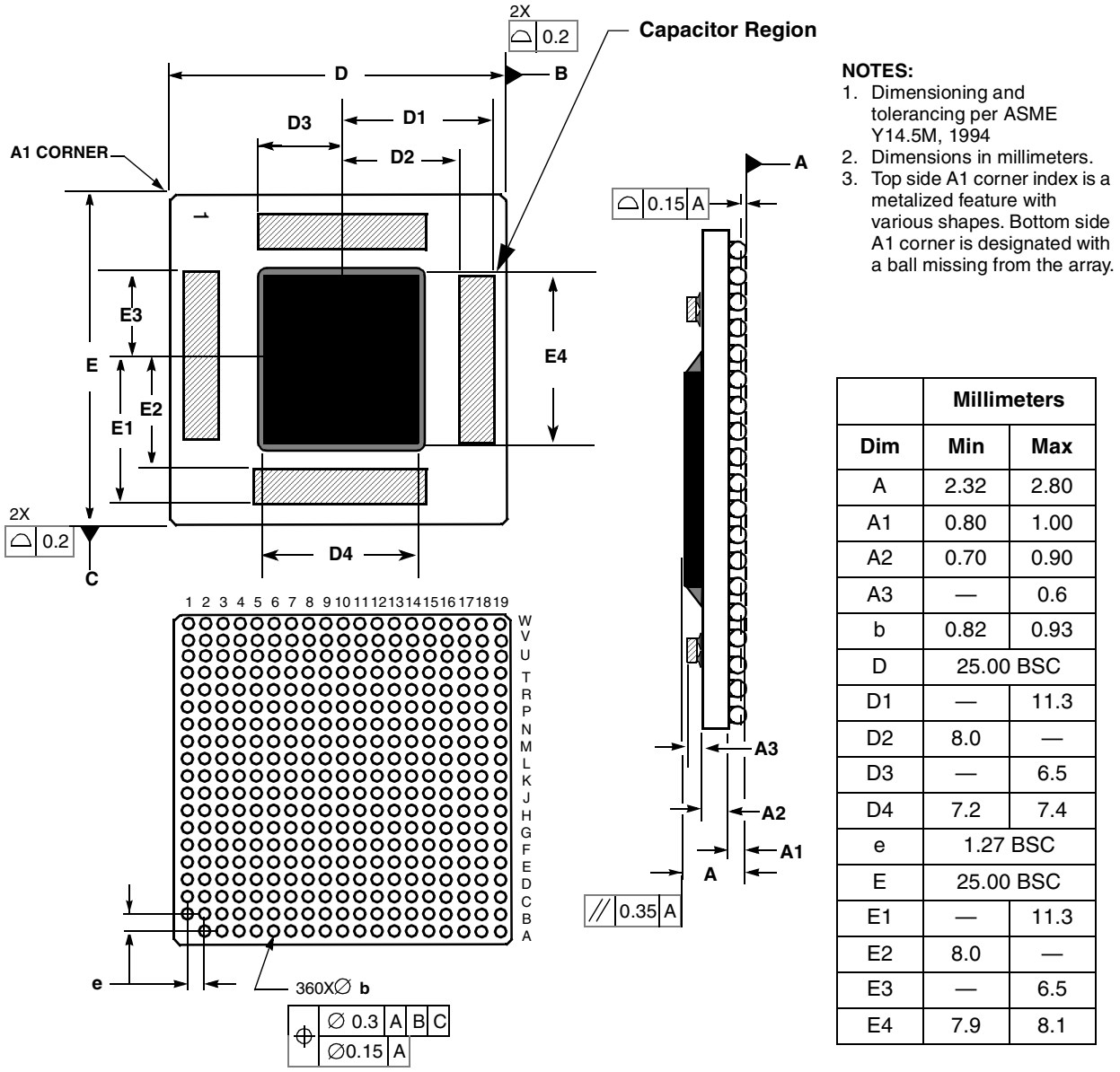
Signal Name	Pin Number	Active	I/O	Notes
A[0:35]	E11, H1, C11, G3, F10, L2, D11, D1, C10, G2, D12, L3, G4, T2, F4, V1, J4, R2, K5, W2, J2, K4, N4, J3, M5, P5, N3, T1, V2, U1, N5, W1, B12, C4, G10, B11	High	I/O	2
$\overline{\text{AACK}}$	R1	Low	Input	
AP[0:4]	C1, E3, H6, F5, G7	High	I/O	2
$\overline{\text{ARTRY}}$	N2	Low	I/O	3
AV_{DD}	A8	—	Input	
$\overline{\text{BG}}$	M1	Low	Input	
$\overline{\text{BMODE0}}$	G9	Low	Input	4
$\overline{\text{BMODE1}}$	F8	Low	Input	5
$\overline{\text{BR}}$	D2	Low	Output	
BVSEL0	B7	High	Input	1, 6
BVSEL1	E10	High	Input	1, 20
$\overline{\text{CI}}$	J1	Low	Output	
$\overline{\text{CKSTP\_IN}}$	A3	Low	Input	
$\overline{\text{CKSTP\_OUT}}$	B1	Low	Output	
CLK_OUT	H2	High	Output	
D[0:63]	R15, W15, T14, V16, W16, T15, U15, P14, V13, W13, T13, P13, U14, W14, R12, T12, W12, V12, N11, N10, R11, U11, W11, T11, R10, N9, P10, U10, R9, W10, U9, V9, W5, U6, T5, U5, W7, R6, P7, V6, P17, R19, V18, R18, V19, T19, U19, W19, U18, W17, W18, T16, T18, T17, W3, V17, U4, U8, U7, R7, P6, R8, W8, T8	High	I/O	
$\overline{\text{DBG}}$	M2	Low	Input	
$\overline{\text{DFS2}}$	A12	Low	Input	20, 21
$\overline{\text{DFS4}}$	B6	Low	Input	12, 20, 21
DP[0:7]	T3, W4, T4, W9, M6, V3, N8, W6	High	I/O	
$\overline{\text{DRDY}}$	R3	Low	Output	7
DTI[0:3]	G1, K1, P1, N1	High	Input	8
EXT_QUAL	A11	High	Input	9
$\overline{\text{GBL}}$	E2	Low	I/O	
GND	B5, C3, D6, D13, E17, F3, G17, H4, H7, H9, H11, H13, J6, J8, J10, J12, K7, K3, K9, K11, K13, L6, L8, L10, L12, M4, M7, M9, M11, M13, N7, P3, P9, P12, R5, R14, R17, T7, T10, U3, U13, U17, V5, V8, V11, V15	—	—	
GND	A17, A19, B13, B16, B18, E12, E19, F13, F16, F18, G19, H18, J14, L14, M15, M17, M19, N14, N16, P15, P19	—	—	15
GND_SENSE	G12, N13	—	—	19
$\overline{\text{HIT}}$	B2	Low	Output	7
$\overline{\text{HRESET}}$	D8	Low	Input	
$\overline{\text{INT}}$	D4	Low	Input	
L1_TSTCLK	G8	High	Input	9
L2_TSTCLK	B3	High	Input	10

Table 11. Pinout Listing for the MPC7448, 360 HCTE Package (continued)

Signal Name	Pin Number	Active	I/O	Notes
$\overline{\text{LVRAM}}$	B10	—	—	12, 20, 22
NC (no connect)	A6, A14, A15, B14, B15, C14, C15, C16, C17, C18, C19, D14, D15, D16, D17, D18, D19, E14, E15, F14, F15, G14, G15, H15, H16, J15, J16, J17, J18, J19, K15, K16, K17, K18, K19, L15, L16, L17, L18, L19	—	—	11
$\overline{\text{LSSD\_MODE}}$	E8	Low	Input	6, 12
$\overline{\text{MCP}}$	C9	Low	Input	
OV_{DD}	B4, C2, C12, D5, F2, H3, J5, K2, L5, M3, N6, P2, P8, P11, R4, R13, R16, T6, T9, U2, U12, U16, V4, V7, V10, V14	—	—	
OVDD_SENSE	E18, G18	—	—	16
PLL_CFG[0:4]	B8, C8, C7, D7, A7	High	Input	
PLL_CFG[5]	D10	High	Input	9, 20
$\overline{\text{PMON\_IN}}$	D9	Low	Input	13
$\overline{\text{PMON\_OUT}}$	A9	Low	Output	
$\overline{\text{QACK}}$	G5	Low	Input	
$\overline{\text{QREQ}}$	P4	Low	Output	
$\overline{\text{SHD}}$[0:1]	E4, H5	Low	I/O	3
$\overline{\text{SMI}}$	F9	Low	Input	
$\overline{\text{SRESET}}$	A2	Low	Input	
SYSCLK	A10	—	Input	
$\overline{\text{TA}}$	K6	Low	Input	
TBEN	E1	High	Input	
$\overline{\text{TBST}}$	F11	Low	Output	
TCK	C6	High	Input	
TDI	B9	High	Input	6
TDO	A4	High	Output	
$\overline{\text{TEA}}$	L1	Low	Input	
TEMP_ANODE	N18	—	—	17
TEMP_CATHODE	N19	—	—	17
TMS	F1	High	Input	6
$\overline{\text{TRST}}$	A5	Low	Input	6, 14
$\overline{\text{TS}}$	L4	Low	I/O	3
TSIZ[0:2]	G6, F7, E7	High	Output	
TT[0:4]	E5, E6, F6, E9, C5	High	I/O	
$\overline{\text{WT}}$	D3	Low	Output	
V_{DD}	H8, H10, H12, J7, J9, J11, J13, K8, K10, K12, K14, L7, L9, L11, L13, M8, M10, M12	—	—	
V_{DD}	A13, A16, A18, B17, B19, C13, E13, E16, F12, F17, F19, G11, G16, H14, H17, H19, M14, M16, M18, N15, N17, P16, P18	—	—	15

8.2 Mechanical Dimensions for the MPC7448, 360 HCTE BGA

Figure 13 provides the mechanical dimensions and bottom surface nomenclature for the MPC7448, 360 HCTE BGA package.



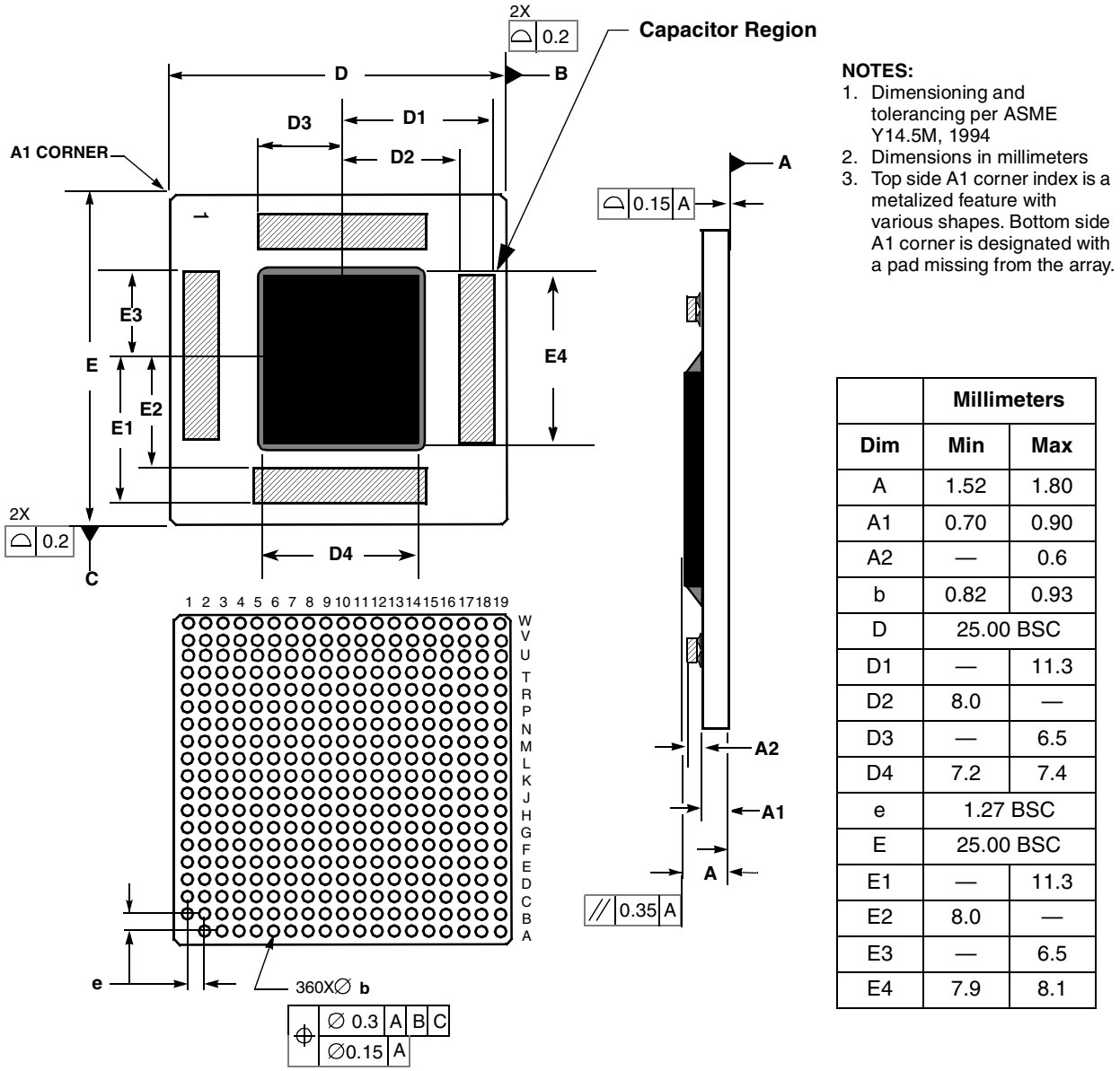
NOTES:
1. Dimensioning and tolerancing per ASME Y14.5M, 1994
2. Dimensions in millimeters.
3. Top side A1 corner index is a metalized feature with various shapes. Bottom side A1 corner is designated with a ball missing from the array.

	Millimeters	
Dim	Min	Max
A	2.32	2.80
A1	0.80	1.00
A2	0.70	0.90
A3	—	0.6
b	0.82	0.93
D	25.00 BSC	
D1	—	11.3
D2	8.0	—
D3	—	6.5
D4	7.2	7.4
e	1.27 BSC	
E	25.00 BSC	
E1	—	11.3
E2	8.0	—
E3	—	6.5
E4	7.9	8.1

Figure 13. Mechanical Dimensions and Bottom Surface Nomenclature for the MPC7448, 360 HCTE BGA Package

8.4 Mechanical Dimensions for the MPC7448, 360 HCTE LGA

Figure 13 provides the mechanical dimensions and bottom surface nomenclature for the MPC7448, 360 HCTE LGA package.



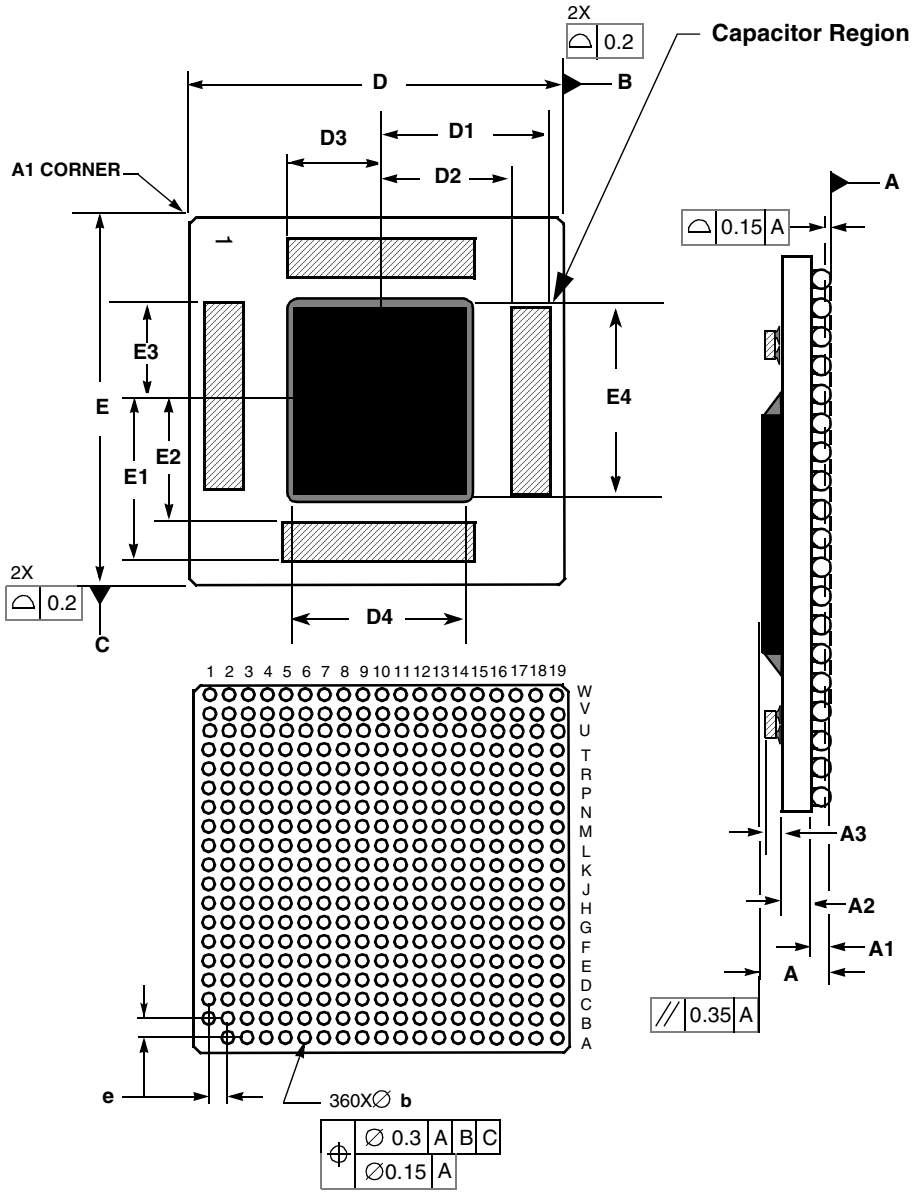
NOTES:
1. Dimensioning and tolerancing per ASME Y14.5M, 1994
2. Dimensions in millimeters
3. Top side A1 corner index is a metalized feature with various shapes. Bottom side A1 corner is designated with a pad missing from the array.

	Millimeters	
Dim	Min	Max
A	1.52	1.80
A1	0.70	0.90
A2	—	0.6
b	0.82	0.93
D	25.00 BSC	
D1	—	11.3
D2	8.0	—
D3	—	6.5
D4	7.2	7.4
e	1.27 BSC	
E	25.00 BSC	
E1	—	11.3
E2	8.0	—
E3	—	6.5
E4	7.9	8.1

Figure 14. Mechanical Dimensions and Bottom Surface Nomenclature for the MPC7448, 360 HCTE LGA Package

8.6 Mechanical Dimensions for the MPC7448, 360 HCTE RoHS-Compliant BGA

Figure 13 provides the mechanical dimensions and bottom surface nomenclature for the MPC7448, 360 HCTE BGA package with RoHS-compliant lead-free spheres.



NOTES:
1. Dimensioning and tolerancing per ASME Y14.5M, 1994
2. Dimensions in millimeters.
3. Top side A1 corner index is a metalized feature with various shapes. Bottom side A1 corner is designated with a ball missing from the array.
4. Dimension A1 represents the collapsed sphere diameter.

	Millimeters	
Dim	**Min**	**Max**
A	1.92	2.40
A1 [4]	0.40	0.60
A2	0.70	0.90
A3	—	0.6
b	0.60	0.90
D	25.00 BSC	
D1	—	11.3
D2	8.0	—
D3	—	6.5
D4	7.2	7.4
e	1.27 BSC	
E	25.00 BSC	
E1	—	11.3
E2	8.0	—
E3	—	6.5
E4	7.9	8.1

Figure 15. Mechanical Dimensions and Bottom Surface Nomenclature for the MPC7448, 360 HCTE RoHS-Compliant BGA Package

9 System Design Information

This section provides system and thermal design requirements and recommendations for successful application of the MPC7448.

9.1 Clocks

The following sections provide more detailed information regarding the clocking of the MPC7448.

9.1.1 PLL Configuration

The MPC7448 PLL is configured by the PLL_CFG[0:5] signals. For a given SYSCLK (bus) frequency, the PLL configuration signals set the internal CPU and VCO frequency of operation. The PLL configuration for the MPC7448 is shown in Table 12. In this example, shaded cells represent settings that, for a given SYSCLK frequency, result in core and/or VCO frequencies that do not comply with Table 8. When enabled, dynamic frequency switching (DFS) also affects the core frequency by halving or quartering the bus-to-core multiplier; see Section 9.7.5, "Dynamic Frequency Switching (DFS)," for more information. Note that when DFS is enabled the resulting core frequency must meet the adjusted minimum core frequency requirements (f_{core_DFS}) described in Table 8. Note that the PLL_CFG[5] is currently used for factory test only and should be tied low, and that the MPC7448 PLL configuration settings are compatible with the MPC7447A PLL configuration settings when PLL_CFG[5] = 0.

Table 12. MPC7448 Microprocessor PLL Configuration Example

PLL_CFG[0:5]	Example Core and VCO Frequency in MHz									
	Bus-to-Core Multiplier [5]	Core-to-VCO Multiplier [5]	Bus (SYSCLK) Frequency							
			33.3 MHz	50 MHz	66.6 MHz	75 MHz	83 MHz	100 MHz	133 MHz	167 MHz	200 MHz
010000	2x [6]	1x									
100000	3x [6]	1x									600
101000	4x [6]	1x								667	800
101100	5x	1x							667	835	1000
100100	5.5x	1x							733	919	1100
110100	6x	1x						600	800	1002	1200
010100	6.5x	1x						650	866	1086	1300
001000	7x	1x						700	931	1169	1400
000100	7.5x	1x					623	750	1000	1253	1500
110000	8x	1x				600	664	800	1064	1336	1600
011000	8.5x	1x				638	706	850	1131	1417	1700
011110	9x	1x			600	675	747	900	1197	1500	
011100	9.5x	1x			633	712	789	950	1264	1583	
101010	10x	1x			667	750	830	1000	1333	1667	
100010	10.5x	1x			700	938	872	1050	1397		

9.2.3 Transient Specifications

The ensure the long-term reliability of the device, the MPC7448 requires that transients on the core power rail (V_{DD}) be constrained. The recommended operating voltage specifications provided in Table 4 are DC specifications. That is, the device may be operated continuously with V_{DD} within the specified range without adversely affecting the device's reliability. Excursions above the stated recommended operation range, including overshoot during power-up, can impact the long-term reliability of the device. Excursions are described by their amplitude and duration. Duration is defined as the time period during which the V_{DD} power plane, as measured at the VDD_SENSE pins, will be within a specific voltage range, expressed as percentage of the total time the device will be powered up over the device lifetime. In practice, the period over which transients are measured can be any arbitrary period of time that accurately represents the expected range of processor and system activity. The voltage ranges and durations for normal operation and transients are described in Table 14.

Table 14. VDD Power Supply Transient Specifications

At recommended operating temperatures. See Table 4.

Voltage Region	Voltage Range (V)		Permitted Duration [1]	Notes
	Min	Max		
Normal	V_{DD} minimum	V_{DD} maximum	100%	2
Low Transient	V_{DD} maximum	1.35 V	10%	2, 3
High Transient	1.35 V	1.40 V	0.2%	4

Notes:
1. Permitted duration is defined as the percentage of the total time the device is powered on that the V_{DD} power supply voltage may exist within the specified voltage range.
2. See Table 4 for nominal V_{DD} specifications.
3. To simplify measurement, excursions into the High Transient region are included in this duration.
4. Excursions above the absolute maximum rating of 1.4 V are not permitted; see Table 2.

Note that, to simplify transient measurements, the duration of the excursion into the High Transient region is also included in the Low Transient duration, so that only the time the voltage is above each threshold must be considered. Figure 19 shows an example of measuring voltage transients.

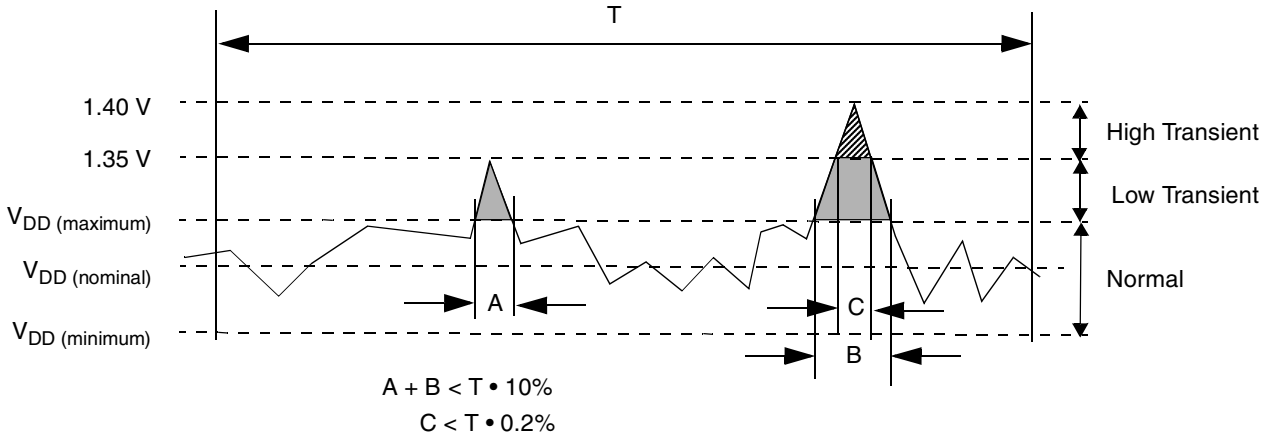


Figure 19. Voltage Transient Example

9.2.4 Decoupling Recommendations

Due to the MPC7448 dynamic power management feature, large address and data buses, and high operating frequencies, the MPC7448 can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the MPC7448 system, and the MPC7448 itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer use sufficient decoupling capacitors, typically one capacitor for every V_{DD} pin, and a similar amount for the OV_{DD} pins, placed as close as possible to the power pins of the MPC7448. It is also recommended that these decoupling capacitors receive their power from separate V_{DD}, OV_{DD}, and GND power planes in the PCB, using short traces to minimize inductance.

These capacitors should have a value of 0.01 or 0.1 µF. Only ceramic surface mount technology (SMT) capacitors should be used to minimize lead inductance. Orientations where connections are made along the length of the part, such as 0204, are preferable but not mandatory. Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993) and contrary to previous recommendations for decoupling Freescale microprocessors, multiple small capacitors of equal value are recommended over using multiple values of capacitance.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V_{DD} and OV_{DD} planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low equivalent series resistance (ESR) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors are 100–330 µF (AVX TPS tantalum or Sanyo OSCON).

9.3 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. Unless otherwise noted, unused active low inputs should be tied to OV_{DD} and unused active high inputs should be connected to GND. All NC (no connect) signals must remain unconnected.

Power and ground connections must be made to all external V_{DD}, OV_{DD}, and GND pins in the MPC7448. For backward compatibility with the MPC7447, MPC7445, and MP7441, or for migrating a system originally designed for one of these devices to the MPC7448, the new power and ground signals (formerly NC, see Table 11) may be left unconnected if the core frequency is 1 GHz or less. Operation above 1 GHz requires that these additional power and ground signals be connected, and it is strongly recommended that all new designs include the additional connections. See also Section 7, “Pinout Listings,” for additional information.

The MPC7448 provides VDD_SENSE, OVDD_SENSE, and GND_SENSE pins. These pins connect directly to the power/ground planes in the device package and are intended to allow an external device to measure the voltage present on the V_{DD}, OV_{DD} and GND planes in the device package. The most common use for these signals is as a feedback signal to a power supply regulator to allow it to compensate for board losses and supply the correct voltage at the device. (Note that all voltage parameters are specified at the pins of the device.) If not used for this purpose, it is recommended that these signals be connected to test points that can be used in the event that an accurate measurement of the voltage at the device is needed during system debug. Otherwise, these signals should be connected to the appropriate power/ground planes on the circuit board or left unconnected.

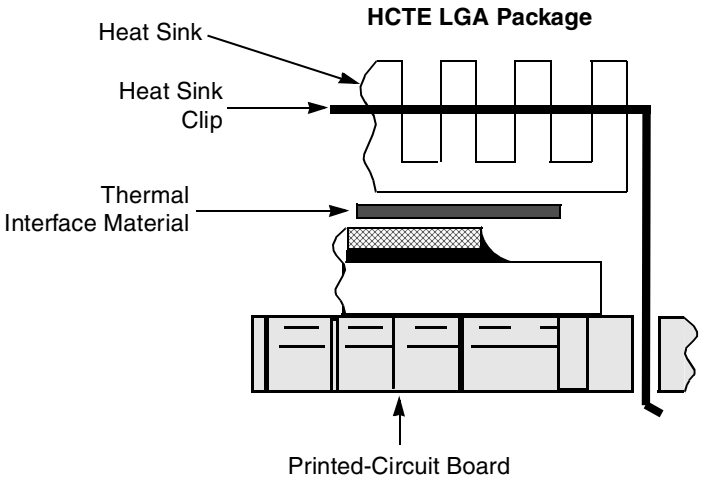


Figure 23. LGA Package Exploded Cross-Sectional View with Several Heat Sink Options

There are several commercially-available heat sinks for the MPC7448 provided by the following vendors:

Aavid Thermalloy 80 Commercial St. Concord, NH 03301 Internet: www.aavidthermalloy.com	603-224-9988
Alpha Novatech 473 Sapena Ct. #12 Santa Clara, CA 95054 Internet: www.alphanovatech.com	408-567-8082
Calgreg Thermal Solutions 60 Alhambra Road, Suite 1 Warwick, RI 02886 Internet: www.calgregthermalsolutions.com	888-732-6100
International Electronic Research Corporation (IERC) 413 North Moss St. Burbank, CA 91502 Internet: www.ctscorp.com	818-842-7277
Tyco Electronics Chip Coolers™ P.O. Box 3668 Harrisburg, PA 17105-3668 Internet: www.tycoelectronics.com	800-522-6752
Wakefield Engineering 33 Bridge St. Pelham, NH 03076 Internet: www.wakefield.com	603-635-2800

Ultimately, the final selection of an appropriate heat sink depends on many factors, such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost.

Solving for T, the equation becomes:

$$nT = \frac{V_H - V_L}{1.986 \times 10^{-4}}$$

9.7.5 Dynamic Frequency Switching (DFS)

The DFS feature in the MPC7448 adds the ability to divide the processor-to-system bus ratio by two or four during normal functional operation. Divide-by-two mode is enabled by setting the HID1[DFS2] bit in software or by asserting the $\overline{\text{DFS2}}$ pin via hardware. The MPC7448 can be returned for full speed by clearing HID1[DFS2] or negating $\overline{\text{DFS2}}$. Similarly, divide-by-four mode is enabled by setting HID1[DFS4] in software or by asserting the $\overline{\text{DFS4}}$ pin. In all cases, the frequency change occurs in 1 clock cycle and no idle waiting period is required to switch between modes. Note that asserting either $\overline{\text{DFS2}}$ or $\overline{\text{DFS4}}$ overrides software control of DFS, and that asserting both $\overline{\text{DFS2}}$ and $\overline{\text{DFS4}}$ disables DFS completely, including software control. Additional information regarding DFS can be found in the *MPC7450 RISC Microprocessor Family Reference Manual.* Note that minimum core frequency requirements must be observed when enabling DFS, and the resulting core frequency must meet the requirements for f_{core_DFS} given in Table 8.

9.7.5.1 Power Consumption with DFS Enabled

Power consumption with DFS enabled can be approximated using the following formula:

$$P_{DFS} = \left[\frac{f_{DFS}}{f}\ (P - P_{DS})\right] + P_{DS}$$

Where:

P_{DFS} = Power consumption with DFS enabled
f_{DFS} = Core frequency with DFS enabled
f = Core frequency prior to enabling DFS
P = Power consumption prior to enabling DFS (see Table 7)
P_{DS} = Deep sleep mode power consumption (see Table 7)

The above is an approximation only. Power consumption with DFS enabled is not tested or guaranteed.

9.7.5.2 Bus-to-Core Multiplier Constraints with DFS

DFS is not available for all bus-to-core multipliers as configured by PLL_CFG[0:5] during hard reset. The complete listing is shown in Table 16. Shaded cells represent DFS modes that are not available for a particular PLL_CFG[0:5] setting. Should software or hardware attempt to transition to a multiplier that is not supported, the device will remain at its current multiplier. For example, if a transition from DFS-disabled to an unsupported divide-by-2 or divide-by-4 setting is attempted, the bus-to-core multiplier will remain at the setting configured by the PLL_CFG[0:5] pins. In the case of an attempted transition from a supported divide-by-2 mode to an unsupported divide-by-4 mode, the device will remain in divide-by-2 mode. In all cases, the HID1[PC0-5] bits will correctly reflect the current bus-to-core frequency multiplier.

Table 16. Valid Divide Ratio Configurations

DFS mode disabled		DFS divide-by-2 mode enabled (HID1[DFS2] = 1 or $\overline{\text{DFS2}}$ = 0)		DFS divide-by-4 mode enabled (HID1[DFS4] = 1 or $\overline{\text{DFS4}}$ = 0)	
Bus-to-Core Multiplier Configured by PLL_CFG[0:5] (see Table 12)	HID1[PC0-5] [3]	Bus-to-Core Multiplier	HID1[PC0-5] [3]	Bus-to-Core Multiplier	HID1[PC0-5] [3]
2x [4]	010000	N/A (unchanged) [1]	unchanged [1]	N/A (unchanged) [1]	unchanged [1]
3x [4]	100000	N/A (unchanged) [1]	unchanged [1]	N/A (unchanged) [1]	unchanged [1]
4x [4]	101000	2x [4]	010000	N/A (unchanged) [1]	unchanged [1]
5x	101100	2.5x [4]	010101	N/A (unchanged) [1]	unchanged [1]
5.5x	100100	2.75x [4]	110101 [2]	N/A (unchanged) [1]	unchanged [1]
6x	110100	3x [4]	100000	N/A (unchanged) [1]	unchanged [1]
6.5x	010100	3.25x [4]	100000 [2]	N/A (unchanged) [1]	unchanged [1]
7x	001000	3.5x [4]	110101	N/A (unchanged) [1]	unchanged [1]
7.5x	000100	3.75x [4]	110101 [2]	N/A (unchanged) [1]	unchanged [1]
8x	110000	4x [4]	101000 [4]	2x [4]	010000
8.5x	011000	4.25x [4]	101000 [2]	N/A (unchanged) [1]	unchanged [1]
9x	011110	4.5x [4]	011101	2.25x [4]	010000 [2]
9.5x	011100	4.75x [4]	011101 [2]	N/A (unchanged) [1]	unchanged [1]
10x	101010	5x	101100	2.5x [4]	010101
10.5x	100010	5.25x	101100 [2]	N/A (unchanged) [1]	unchanged [1]
11x	100110	5.5x	100100	2.75x [4]	010101 [2]
11.5x	000000	5.75x	100100 [2]	N/A (unchanged) [1]	unchanged [1]
12x	101110	6x	110100	3x [4]	100000
12.5x	111110	6.25x	110100 [2]	N/A (unchanged) [1]	unchanged [1]
13x	010110	6.5x	010100	3.25x [4]	100000 [2]
13.5x	111000	6.75	010100 [2]	N/A (unchanged) [1]	unchanged [1]
14x	110010	7x	001000	3.5x [4]	110101
15x	000110	7.5x	000100	3.75x [4]	110101 [2]
16x	110110	8x	110000	4x [4]	101000
17x	000010	8.5x	011000	4.25x [4]	101000 [2]
18x	001010	9x	011110	4.5x [4]	011101
20x	001110	10x	101010	5x	101100
21x	010010	10.5x	100010	5.25x	101100 [2]

Table 17. Document Revision History (continued)

Revision	Date	Substantive Change(s)
2		Table 6: Added separate input leakage specification for BVSEL0, $\overline{\text{LSSD\_MODE}}$, $\overline{\text{TCK}}$, TDI, TMS, $\overline{\text{TRST}}$ signals to correctly indicate leakage current for signals with internal pull-up resistors. Section 5.1: Added paragraph preceding Table 7 and edited notes in Table 7 to clarify core frequencies at which power consumption is measured. Section 5.3: Removed voltage derating specifications; this feature has been made redundant by new device offerings and is no longer supported. Changed names of “Typical–Nominal” and “Typical–Thermal” power consumption parameters to “Typical” and “Thermal”, respectively. (Name change only–no specifications were changed.) Table 11: Revised Notes 16, 18, and 19 to reflect current recommendations for connection of SENSE pins. Section 9.3: Added paragraph explaining connection recommendations for SENSE pins. (See also Table 11 entry above.) Table 19: Updated table to reflect changes in specifications for MC7448xxnnnnNC devices. Table 9: Changed all instances of TT[0:3] to TT[0:4] Removed mention of these input signals from output valid times and output hold times: • AACK, CKSTP_IN, DT[0:3] Figure 17: Modified diagram slightly to correctly show constraint on SYSCLK ramping is related to V_{DD} voltage, not AV_{DD} voltage. (Diagram clarification only; no change in power sequencing requirements.) Added Table 20 to reflect introduction of extended temperature devices and associated hardware specification addendum.
1		Added 1600 MHz, 1420 MHz, and 1000 MHz devices Section 4: corrected die size Table 2: Revised Note 4 to consider overshoot/undershoot and combined with Note 5. Table 4: Revised operating voltage for 1700 MHz device from ± 50 mV to +20 mV / –50 mV. Table 7: Updated and expanded table to include Typical – Nominal power consumption. Table 11: Added voltage derating information for 1700 MHz devices; this feature is not supported at this time for other speed grades. Added transient specifications for VDD power supply in Section 9.2.3, added Table 15 and Figure 19 and renumbered subsequent tables and figures. Moved Decoupling Recommendations from Section 9.4 to Section 9.2.4 and renumbered subsequent sections. Section 9.2.1: Revised power sequencing requirements. Section 9.7.4: Added thermal diode ideality factor information (previously TBD). Table 17: Expanded table to show HID1 register values when DFS modes are enabled. Section 11.2: updated to include additional N-spec device speed grades Tables 18 and 19: corrected PVR values and added “MC” product code prefix
0		Initial public release.

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