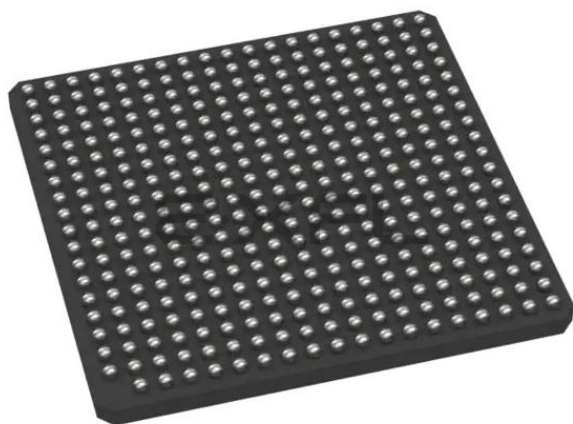




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Understanding [Embedded - Microprocessors](#)

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC G4
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.42GHz
Co-Processors/DSP	Multimedia; SIMD
RAM Controllers	-
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	1.5V, 1.8V, 2.5V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	360-CBGA, FCCBGA
Supplier Device Package	360-FCCBGA (25x25)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc7448vu1420ld

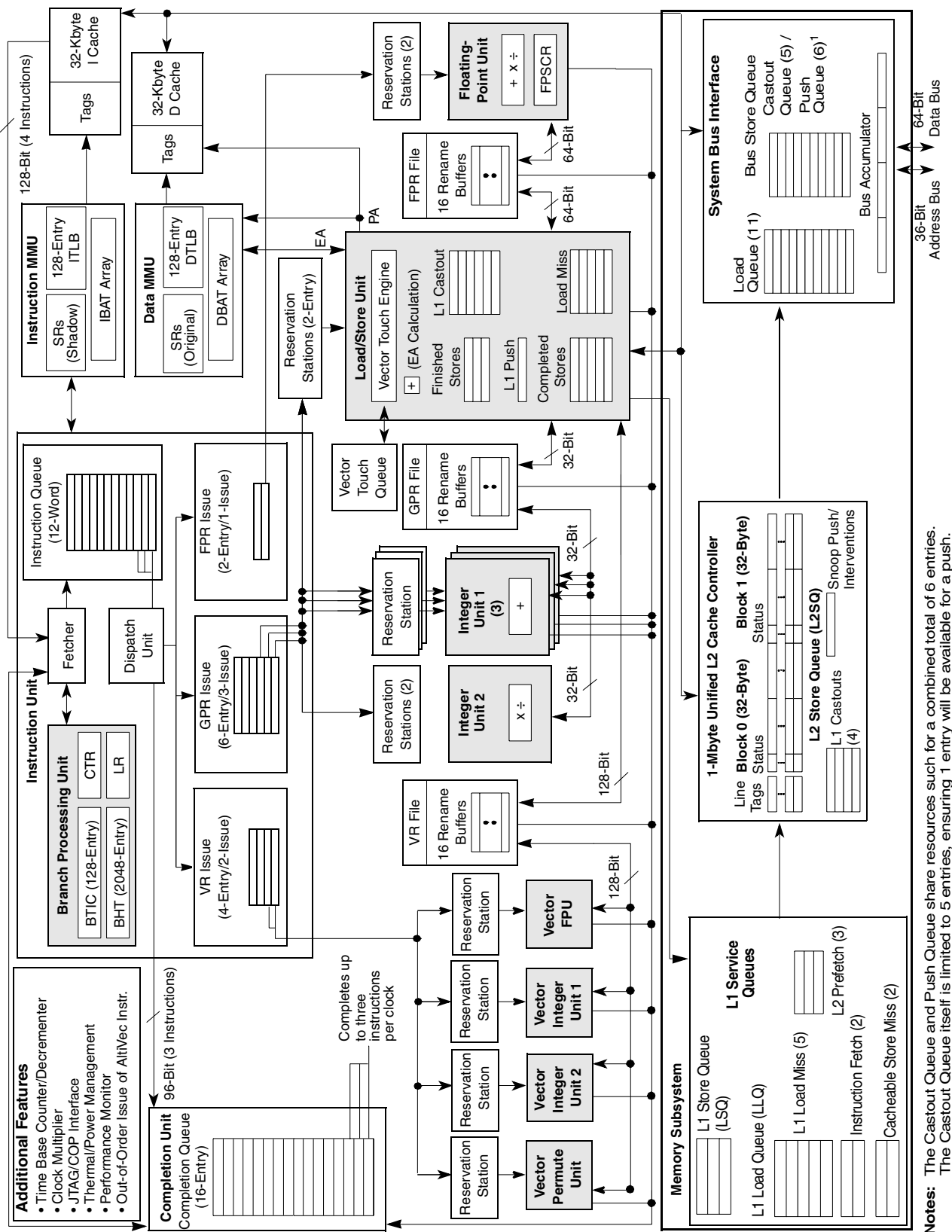


Figure 1. MPC7448 Block Diagram

- Monitors all dispatched instructions and retires them in order
- Tracks unresolved branches and flushes instructions after a mispredicted branch
- Retires as many as three instructions per clock cycle
- Separate on-chip L1 instruction and data caches (Harvard architecture)
 - 32-Kbyte, eight-way set-associative instruction and data caches
 - Pseudo least-recently-used (PLRU) replacement algorithm
 - 32-byte (eight-word) L1 cache block
 - Physically indexed/physical tags
 - Cache write-back or write-through operation programmable on a per-page or per-block basis
 - Instruction cache can provide four instructions per clock cycle; data cache can provide four words per clock cycle
 - Caches can be disabled in software.
 - Caches can be locked in software.
 - MESI data cache coherency maintained in hardware
 - Separate copy of data cache tags for efficient snooping
 - Parity support on cache
 - No snooping of instruction cache except for **icbi** instruction
 - Data cache supports AltiVec LRU and transient instructions
 - Critical double- and/or quad-word forwarding is performed as needed. Critical quad-word forwarding is used for AltiVec loads and instruction fetches. Other accesses use critical double-word forwarding.
- Level 2 (L2) cache interface
 - On-chip, 1-Mbyte, eight-way set-associative unified instruction and data cache
 - Cache write-back or write-through operation programmable on a per-page or per-block basis
 - Parity support on cache tags
 - ECC or parity support on data
 - Error injection allows testing of error recovery software
- Separate memory management units (MMUs) for instructions and data
 - 52-bit virtual address, 32- or 36-bit physical address
 - Address translation for 4-Kbyte pages, variable-sized blocks, and 256-Mbyte segments
 - Memory programmable as write-back/write-through, caching-inhibited/caching-allowed, and memory coherency enforced/memory coherency not enforced on a page or block basis
 - Separate IBATs and DBATs (eight each) also defined as SPRs
 - Separate instruction and data translation lookaside buffers (TLBs)
 - Both TLBs are 128-entry, two-way set-associative and use an LRU replacement algorithm.
 - TLBs are hardware- or software-reloadable (that is, a page table search is performed in hardware or by system software on a TLB miss).

4 General Parameters

The following list summarizes the general parameters of the MPC7448:

Technology	90 nm CMOS SOI, nine-layer metal	
Die size	8.0 mm × 7.3 mm	
Transistor count	90 million	
Logic design	Mixed static and dynamic	
Packages	Surface mount 360 ceramic ball grid array (HCTE)	
	Surface mount 360 ceramic land grid array (HCTE)	
	Surface mount 360 ceramic ball grid array with lead-free spheres (HCTE)	
Core power supply	1.30 V	(1700 MHz device)
	1.25 V	(1600 MHz device)
	1.20 V	(1420 MHz device)
	1.15 V	(1000 MHz device)
I/O power supply	1.5 V, 1.8 V, or 2.5 V	

5 Electrical and Thermal Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC7448.

5.1 DC Electrical Characteristics

The tables in this section describe the MPC7448 DC electrical characteristics. [Table 2](#) provides the absolute maximum ratings. See [Section 9.2, “Power Supply Design and Sequencing,”](#) for power sequencing requirements.

Table 2. Absolute Maximum Ratings ¹

Characteristic		Symbol	Maximum Value	Unit	Notes
Core supply voltage		V_{DD}	−0.3 to 1.4	V	2
PLL supply voltage		AV_{DD}	−0.3 to 1.4	V	2
Processor bus supply voltage	I/O Voltage Mode = 1.5 V	OV_{DD}	−0.3 to 1.8	V	3
	I/O Voltage Mode = 1.8 V		−0.3 to 2.2		3
	I/O Voltage Mode = 2.5 V		−0.3 to 3.0		3
Input voltage	Processor bus	V_{in}	−0.3 to $OV_{DD} + 0.3$	V	4
	JTAG signals	V_{in}	−0.3 to $OV_{DD} + 0.3$	V	
Storage temperature range		T_{stg}	− 55 to 150	°C	

Notes:

- Functional and tested operating conditions are given in [Table 4](#). Absolute maximum ratings are stress ratings only and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
- See [Section 9.2, “Power Supply Design and Sequencing,”](#) for power sequencing requirements.
- Bus must be configured in the corresponding I/O voltage mode; see [Table 3](#).
- Caution:** V_{in} must not exceed OV_{DD} by more than 0.3 V at any time including during power-on reset except as allowed by the overshoot specifications. V_{in} may overshoot/undershoot to a voltage and for a maximum duration as shown in [Figure 2](#).

Table 4 provides the recommended operating conditions for the MPC7448 part numbers described by this document; see [Section 11.1, “Part Numbers Fully Addressed by This Document,”](#) for more information. See [Section 9.2, “Power Supply Design and Sequencing”](#) for power sequencing requirements.

Table 4. Recommended Operating Conditions¹

Characteristic		Symbol	Recommended Value								Unit	Notes
			1000 MHz		1420 MHz		1600 MHz		1700 MHz			
			Min	Max	Min	Max	Min	Max	Min	Max		
Core supply voltage		V _{DD}	1.15 V ± 50 mV		1.2 V ± 50 mV		1.25 V ± 50 mV		1.3 V +20/ – 50 mV		V	3, 4, 5
PLL supply voltage		AV _{DD}	1.15 V ± 50 mV		1.2 V ± 50 mV		1.25 V ± 50 mV		1.3 V +20/ – 50 mV		V	2, 3, 4
Processor bus supply voltage	I/O Voltage Mode = 1.5 V	OV _{DD}	1.5 V ± 5%		1.5 V ± 5%		1.5 V ± 5%		1.5 V ± 5%		V	4
	I/O Voltage Mode = 1.8 V		1.8 V ± 5%		1.8 V ± 5%		1.8 V ± 5%		4			
	I/O Voltage Mode = 2.5 V		2.5 V ± 5%		2.5 V ± 5%		2.5 V ± 5%		4			
Input voltage	Processor bus	V _{in}	GND	OV _{DD}	GND	OV _{DD}	GND	OV _{DD}	GND	OV _{DD}	V	
	JTAG signals	V _{in}	GND	OV _{DD}	GND	OV _{DD}	GND	OV _{DD}	GND	OV _{DD}		
Die-junction temperature		T _j	0	105	0	105	0	105	0	105	•C	6

Notes:

1. These are the recommended and tested operating conditions.
2. This voltage is the input to the filter discussed in [Section 9.2.2, “PLL Power Supply Filtering,”](#) and not necessarily the voltage at the AV_{DD} pin, which may be reduced from V_{DD} by the filter.
3. Some early devices supported voltage and frequency derating whereby VDD (and AVDD) could be reduced to reduce power consumption. This feature has been superseded and is no longer supported. See [Section 5.3, “Voltage and Frequency Derating,”](#) for more information.
4. **Caution:** Power sequencing requirements must be met; see [Section 9.2, “Power Supply Design and Sequencing”](#).
5. **Caution:** See [Section 9.2.3, “Transient Specifications”](#) for information regarding transients on this power supply.
6. For information on extended temperature devices, see [Section 11.2, “Part Numbers Not Fully Addressed by This Document.”](#)

5.2 AC Electrical Characteristics

This section provides the AC electrical characteristics for the MPC7448. After fabrication, functional parts are sorted by maximum processor core frequency as shown in [Section 5.2.1, “Clock AC Specifications,”](#) and tested for conformance to the AC specifications for that frequency. The processor core frequency, determined by the bus (SYSCLK) frequency and the settings of the PLL_CFG[0:5] signals, can be dynamically modified using dynamic frequency switching (DFS). Parts are sold by maximum processor core frequency; see [Section 11, “Part Numbering and Marking,”](#) for information on ordering parts. DFS is described in [Section 9.7.5, “Dynamic Frequency Switching \(DFS\).”](#)

5.2.1 Clock AC Specifications

[Table 8](#) provides the clock AC timing specifications as defined in [Figure 3](#) and represents the tested operating frequencies of the devices. The maximum system bus frequency, f_{SYSCLK} , given in [Table 8](#), is considered a practical maximum in a typical single-processor system. This does not exclude multi-processor systems, but these typically require considerably more design effort to achieve the maximum rated bus frequency. The actual maximum SYSCLK frequency for any application of the MPC7448 will be a function of the AC timings of the microprocessor(s), the AC timings for the system controller, bus loading, circuit board topology, trace lengths, and so forth, and may be less than the value given in [Table 8](#).

Table 8. Clock AC Timing Specifications

At recommended operating conditions. See [Table 4](#).

Characteristic		Symbol	Maximum Processor Core Frequency (Speed Grade)								Unit	Notes
			1000 MHz		1420 MHz		1600 MHz		1700 MHz			
			Min	Max	Min	Max	Min	Max	Min	Max		
Processor core frequency	DFS mode disabled	f _{core}	600	1000	600	1420	600	1600	600	1700	MHz	1, 8
	DFS mode enabled	f _{core—DF}	300	500	300	710	300	800	300	850		9
VCO frequency		f _{VCO}	600	1000	600	1420	600	800	600	1700	MHz	1, 10
SYSCLK frequency		f _{SYSCLK}	33	200	33	200	33	200	33	200	MHz	1, 2, 8
SYSCLK cycle time		t _{SYSCLK}	5.0	30	5.0	30	5.0	30	5.0	30	ns	2
SYSCLK rise and fall time		t _{KR} , t _{KF}	—	0.5	—	0.5	—	0.5	—	0.5	ns	3
SYSCLK duty cycle measured at OV _{DD} /2		t _{KHKL} / t _{SYSCLK}	40	60	40	60	40	60	40	60	%	4
SYSCLK cycle-to-cycle jitter			—	150	—	150	—	150	—	150	ps	5, 6
Internal PLL relock time			—	100	—	100	—	100	—	100	μs	7

Notes:

- Caution:** The SYSCLK frequency and PLL_CFG[0:5] settings must be chosen such that the resulting SYSCLK (bus) frequency, processor core frequency, and PLL (VCO) frequency do not exceed their respective maximum or minimum operating frequencies. Refer to the PLL_CFG[0:5] signal description in [Section 9.1.1, "PLL Configuration,"](#) for valid PLL_CFG[0:5] settings.
- Actual maximum system bus frequency is system-dependent. See [Section 5.2.1, "Clock AC Specifications."](#)
- Rise and fall times for the SYSCLK input measured from 0.4 to 1.4 V
- Timing is guaranteed by design and characterization.
- Guaranteed by design
- The SYSCLK driver's closed loop jitter bandwidth should be less than 1.5 MHz at –3 dB.
- Relock timing is guaranteed by design and characterization. PLL-relock time is the maximum amount of time required for PLL lock after a stable V_{DD} and SYSCLK are reached during the power-on reset sequence. This specification also applies when the PLL has been disabled and subsequently re-enabled during sleep mode. Also note that $\overline{HRESET}$ must be held asserted for a minimum of 255 bus clocks after the PLL-relock time during the power-on reset sequence.
- This reflects the maximum and minimum core frequencies when the dynamic frequency switching feature (DFS) is disabled. f_{core_DFS} provides the maximum and minimum core frequencies when operating in a DFS mode.
- This specification supports the Dynamic Frequency Switching (DFS) feature and is applicable only when one of the DFS modes (divide-by-2 or divide-by-4) is enabled. When DFS is disabled, the core frequency must conform to the maximum and minimum frequencies stated for f_{core} .
- Use of the DFS feature does not affect VCO frequency.

Figure 6 provides the input/output timing diagram for the MPC7448.

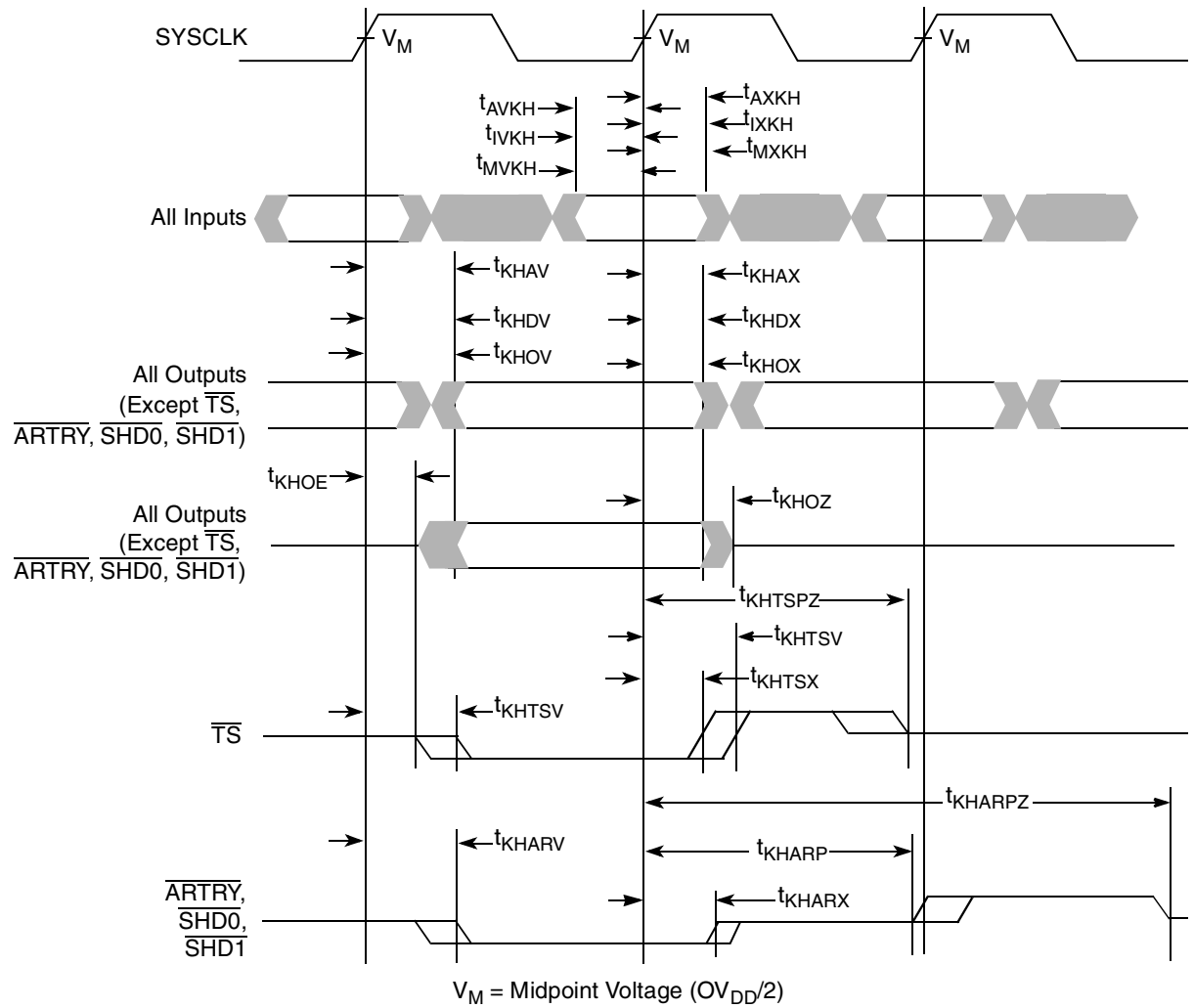


Figure 6. Input/Output Timing Diagram

Figure 7 provides the AC test load for TDO and the boundary-scan outputs of the MPC7448.

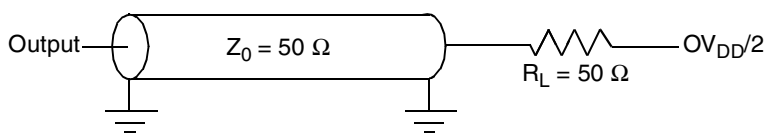


Figure 7. Alternate AC Test Load for the JTAG Interface

Figure 8 provides the JTAG clock input timing diagram.

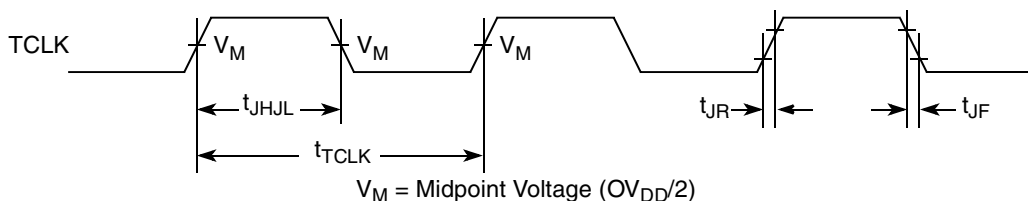


Figure 8. JTAG Clock Input Timing Diagram

Figure 9 provides the $\overline{\text{TRST}}$ timing diagram.

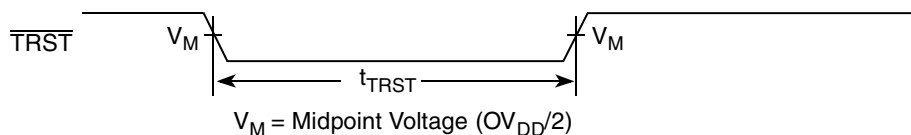


Figure 9. $\overline{\text{TRST}}$ Timing Diagram

Figure 10 provides the boundary-scan timing diagram.

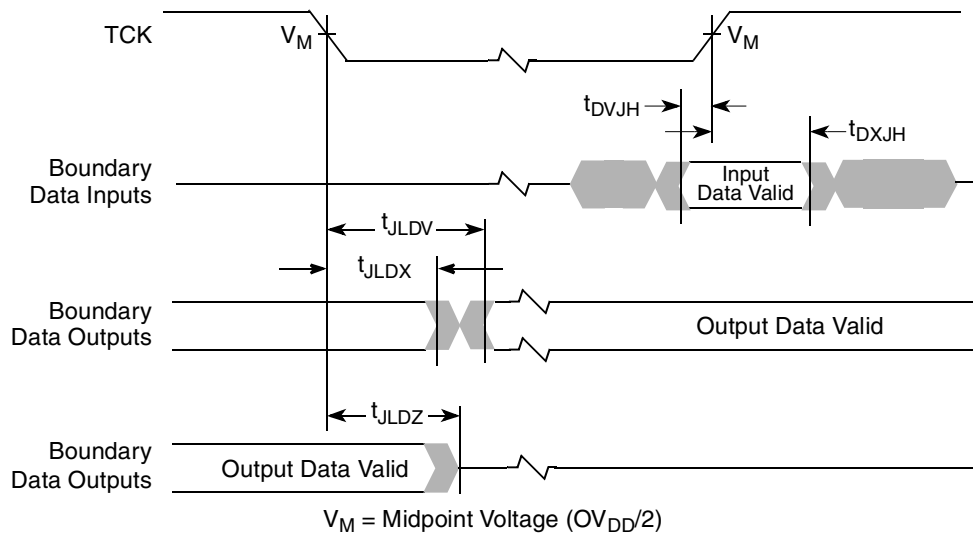


Figure 10. Boundary-Scan Timing Diagram

6 Pin Assignments

Figure 12 (in Part A) shows the pinout of the MPC7448, 360 high coefficient of thermal expansion ceramic ball grid array (HCTE) package as viewed from the top surface. Part B shows the side profile of the HCTE package to indicate the direction of the top surface view.

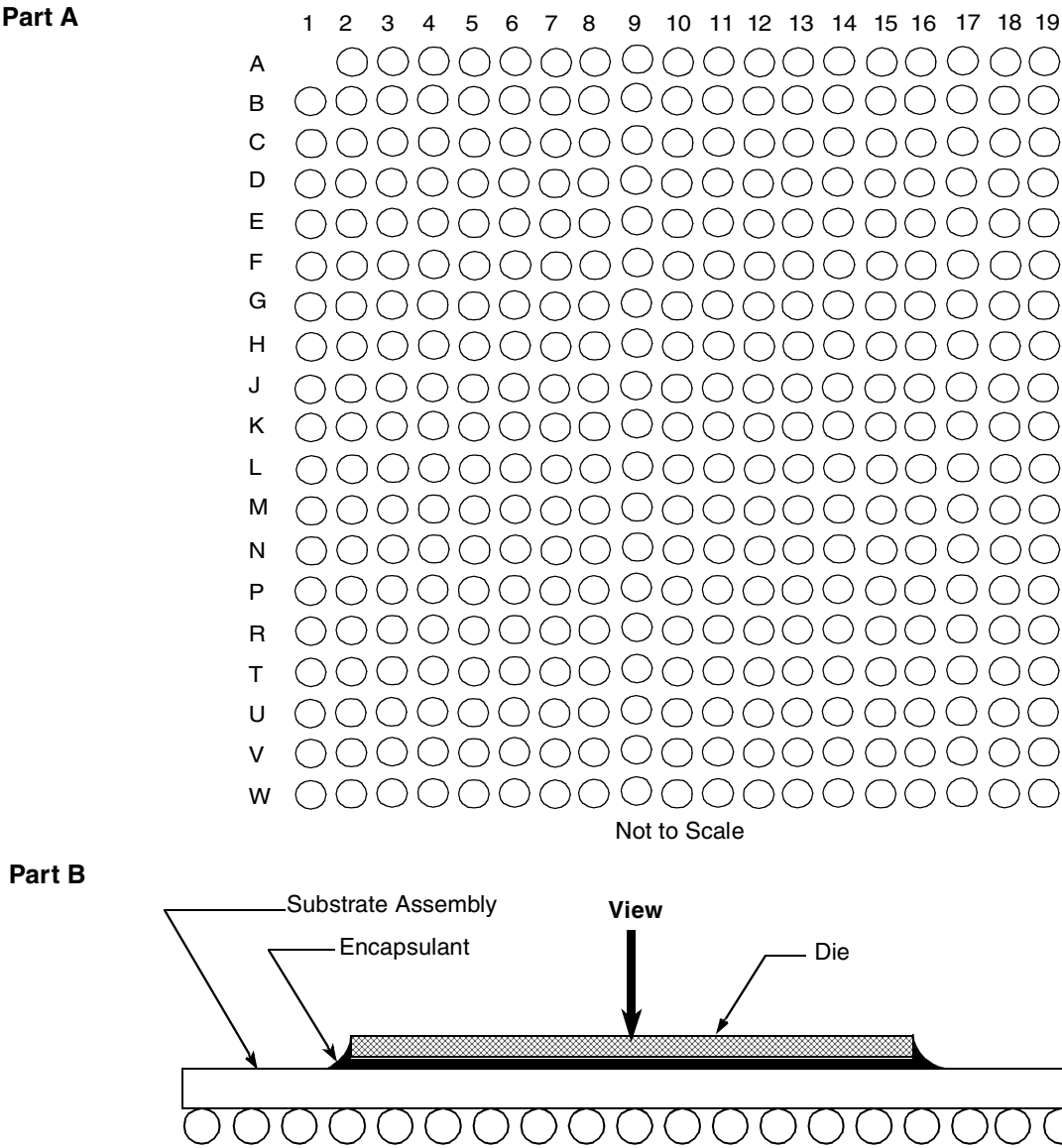


Figure 12. Pinout of the MPC7448, 360 HCTE Package as Viewed from the Top Surface

Table 11. Pinout Listing for the MPC7448, 360 HCTE Package (continued)

Signal Name	Pin Number	Active	I/O	Notes
VDD_SENSE	G13, N12	—	—	18

Notes:

1. OV_{DD} supplies power to the processor bus, JTAG, and all control signals, and is configurable. (V_{DD} supplies power to the processor core, and AV_{DD} supplies power to the PLL after filtering from V_{DD}). To program the I/O voltage, see [Table 3](#). If used, the pull-down resistor should be less than 250 Ω . Because these settings may change in future products, it is recommended BVSEL[0:1] be configured using resistor options, jumpers, or some other flexible means, with the capability to reconfigure the termination of this signal in the future if necessary. For actual recommended value of V_{in} or supply voltages see [Table 4](#).
2. Unused address pins must be pulled down to GND and corresponding address parity pins pulled up to OV_{DD} .
3. These pins require weak pull-up resistors (for example, 4.7 K Ω) to maintain the control signals in the negated state after they have been actively negated and released by the MPC7448 and other bus masters.
4. This signal selects between MPX bus mode (asserted) and 60x bus mode (negated) and will be sampled at $\overline{HRESET}$ going high.
5. This signal must be negated during reset, by pull-up resistor to OV_{DD} or negation by $\neg\overline{HRESET}$ (inverse of $\overline{HRESET}$), to ensure proper operation.
6. Internal pull up on die.
7. Not used in 60x bus mode.
8. These signals must be pulled down to GND if unused, or if the MPC7448 is in 60x bus mode.
9. These input signals are for factory use only and must be pulled down to GND for normal machine operation.
10. This test signal is recommended to be tied to $\overline{HRESET}$; however, other configurations will not adversely affect performance.
11. These signals are for factory use only and must be left unconnected for normal machine operation. Some pins that were NCs on the MPC7447, MPC7445, and MPC7441 have now been defined for other purposes.
12. These input signals are for factory use only and must be pulled up to OV_{DD} for normal machine operation.
13. This pin can externally cause a performance monitor event. Counting of the event is enabled through software.
14. This signal must be asserted during reset, by pull down to GND or assertion by $\overline{HRESET}$, to ensure proper operation.
15. These pins were NCs on the MPC7447, MPC7445, and MPC7441. See [Section 9.3, "Connection Recommendations,"](#) for more information.
16. These pins were OV_{DD} pins on the MPC7447, MPC7445, and MPC7441. These pins are internally connected to OV_{DD} and are intended to allow an external device (such as a power supply) to detect the I/O voltage level present inside the device package. If unused, it is recommended they be connected to test points to facilitate system debug; otherwise, they may be connected directly to OV_{DD} or left unconnected.
17. These pins provide connectivity to the on-chip temperature diode that can be used to determine the die junction temperature of the processor. These pins may be left unterminated if unused.
18. These pins are internally connected to V_{DD} and are intended to allow an external device (such as a power supply) to detect the processor core voltage level present inside the device package. If unused, it is recommended they be connected to test points to facilitate system debug; otherwise, they may be connected directly to V_{DD} or left unconnected.
19. These pins are internally connected to GND and are intended to allow an external device to detect the processor ground voltage level present inside the device package. If unused, it is recommended they be connected to test points to facilitate system debug; otherwise, they may be connected directly to GND or left unconnected.
20. These pins were in the TEST[0:4] factory test pin group on the MPC7447A, MPC7447, MPC7445, and MPC7441. They have been assigned new functions on the MPC7448.
21. These pins can be used to enable the supported dynamic frequency switching (DFS) modes via hardware. If both are pulled down, DFS mode is disabled completely and cannot be enabled via software. If unused, they should be pulled up to OV_{DD} to allow software control of DFS. See the *MPC7450 RISC Microprocessor Family Reference Manual* for more information.
22. This pin is provided to allow operation of the L2 cache at low core voltages and is for factory use only. See the *MPC7450 RISC Microprocessor Family Reference Manual* for more information.

8.3 Package Parameters for the MPC7448, 360 HCTE LGA

The package parameters are as provided in the following list. The package type is 25 × 25 mm, 360 pin high coefficient of thermal expansion ceramic land grid array (HCTE).

Package outline	25 × 25 mm
Interconnects	360 (19 × 19 ball array – 1)
Pitch	1.27 mm (50 mil)
Minimum module height	1.52 mm
Maximum module height	1.80 mm
Pad diameter	0.89 mm (35 mil)
Coefficient of thermal expansion	12.3 ppm/°C

8.5 Package Parameters for the MPC7448, 360 HCTE RoHS-Compliant BGA

The package parameters are as provided in the following list. The package type is 25 × 25 mm, 360-lead high coefficient of thermal expansion ceramic ball grid array (HCTE) with RoHS-compliant lead-free spheres.

Package outline	25 × 25 mm
Interconnects	360 (19 × 19 ball array – 1)
Pitch	1.27 mm (50 mil)
Minimum module height	1.92 mm
Maximum module height	2.40 mm
Ball diameter	0.75 mm (30 mil)
Coefficient of thermal expansion	12.3 ppm/°C

8.6 Mechanical Dimensions for the MPC7448, 360 HCTE RoHS-Compliant BGA

Figure 13 provides the mechanical dimensions and bottom surface nomenclature for the MPC7448, 360 HCTE BGA package with RoHS-compliant lead-free spheres.

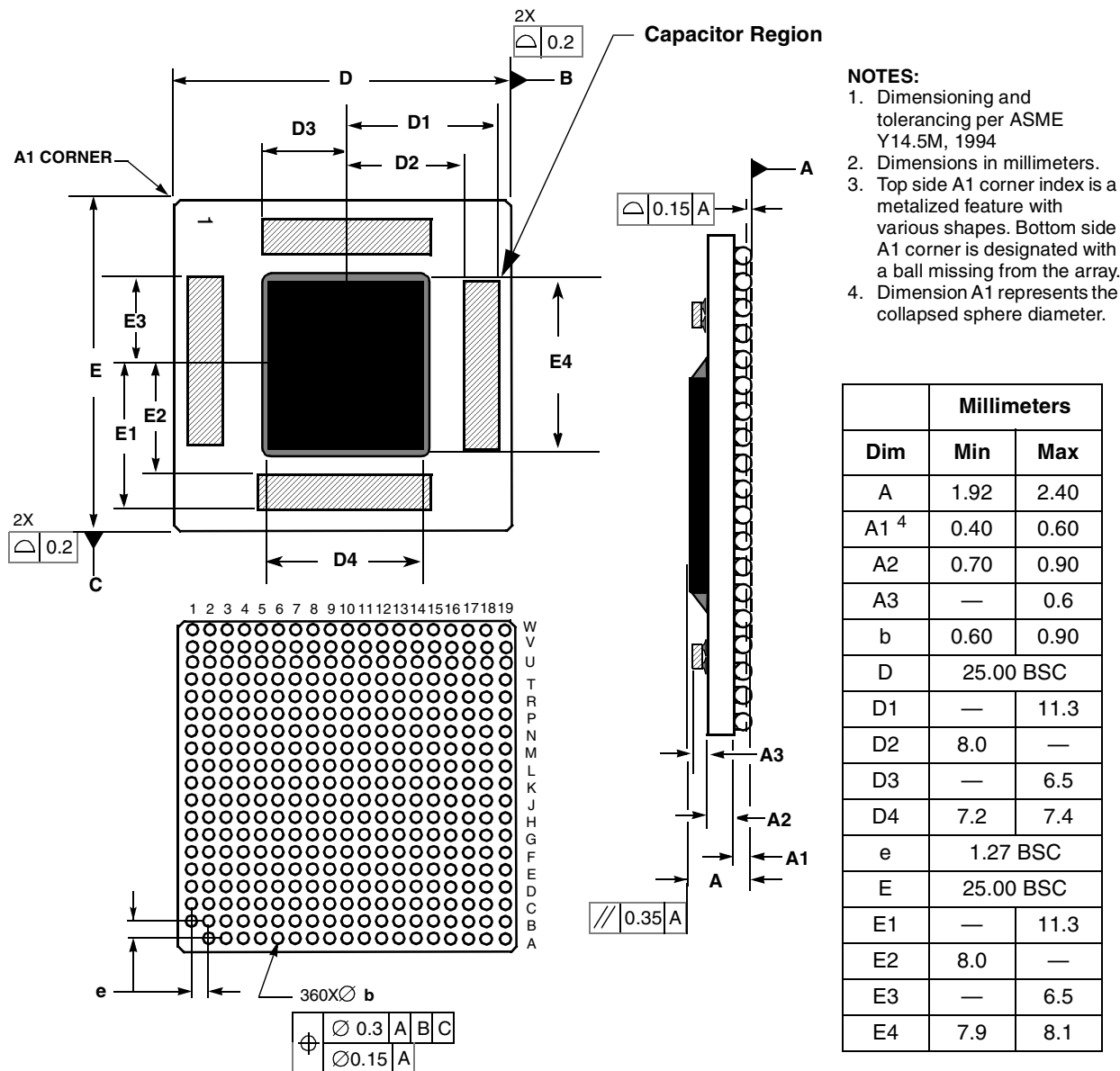


Figure 15. Mechanical Dimensions and Bottom Surface Nomenclature for the MPC7448, 360 HCTE RoHS-Compliant BGA Package

9.1.2 System Bus Clock (SYSCLK) and Spread Spectrum Sources

Spread spectrum clock sources are an increasingly popular way to control electromagnetic interference emissions (EMI) by spreading the emitted noise to a wider spectrum and reducing the peak noise magnitude in order to meet industry and government requirements. These clock sources intentionally add long-term jitter in order to diffuse the EMI spectral content. The jitter specification given in [Table 8](#) considers short-term (cycle-to-cycle) jitter only and the clock generator's cycle-to-cycle output jitter should meet the MPC7448 input cycle-to-cycle jitter requirement. Frequency modulation and spread are separate concerns, and the MPC7448 is compatible with spread spectrum sources if the recommendations listed in [Table 13](#) are observed.

Table 13. Spread Spectrum Clock Source Recommendations

At recommended operating conditions. See [Table 4](#).

Parameter	Min	Max	Unit	Notes
Frequency modulation	—	50	kHz	1
Frequency spread	—	1.0	%	1, 2

Notes:

1. Guaranteed by design
2. SYSCLK frequencies resulting from frequency spreading, and the resulting core and VCO frequencies, must meet the minimum and maximum specifications given in [Table 8](#).

It is imperative to note that the processor's minimum and maximum SYSCLK, core, and VCO frequencies must not be exceeded regardless of the type of clock source. Therefore, systems in which the processor is operated at its maximum rated core or bus frequency should avoid violating the stated limits by using down-spreading only.

9.2 Power Supply Design and Sequencing

The following sections provide detailed information regarding power supply design for the MPC7448.

9.2.1 Power Supply Sequencing

The MPC7448 requires its power rails and clock to be applied in a specific sequence to ensure proper device operation and to prevent device damage. The power sequencing requirements are as follows:

- AV_{DD} must be delayed with respect to V_{DD} by the RC time constant of the PLL filter circuit described in [Section 9.2.2, "PLL Power Supply Filtering"](#). This time constant is nominally 100 μ s.
- OV_{DD} may ramp anytime before or after V_{DD} and AV_{DD} .

Additionally, the following requirements exist regarding the application of SYSCLK:

- The voltage at the SYSCLK input must not exceed V_{DD} until V_{DD} has ramped to 0.9 V.
- The voltage at the SYSCLK input must not exceed OV_{DD} by more 20% during transients (see overshoot/undershoot specifications in [Figure 2](#)) or 0.3 V DC (see [Table 2](#)) at any time.

9.2.4 Decoupling Recommendations

Due to the MPC7448 dynamic power management feature, large address and data buses, and high operating frequencies, the MPC7448 can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the MPC7448 system, and the MPC7448 itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer use sufficient decoupling capacitors, typically one capacitor for every V_{DD} pin, and a similar amount for the OV_{DD} pins, placed as close as possible to the power pins of the MPC7448. It is also recommended that these decoupling capacitors receive their power from separate V_{DD} , OV_{DD} , and GND power planes in the PCB, using short traces to minimize inductance.

These capacitors should have a value of 0.01 or 0.1 μF . Only ceramic surface mount technology (SMT) capacitors should be used to minimize lead inductance. Orientations where connections are made along the length of the part, such as 0204, are preferable but not mandatory. Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993) and contrary to previous recommendations for decoupling Freescale microprocessors, multiple small capacitors of equal value are recommended over using multiple values of capacitance.

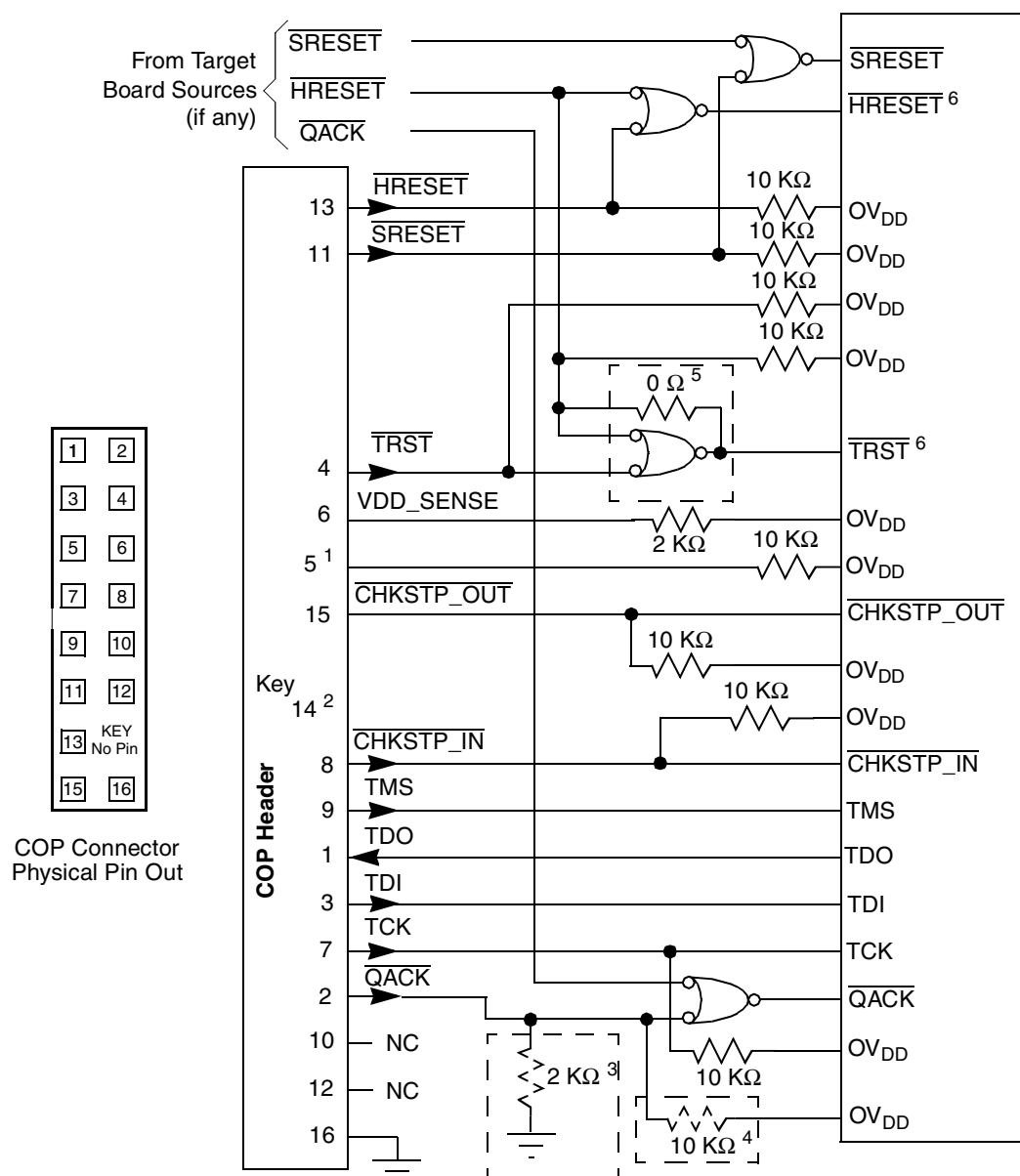
In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V_{DD} and OV_{DD} planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low equivalent series resistance (ESR) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors are 100–330 μF (AVX TPS tantalum or Sanyo OSCON).

9.3 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. Unless otherwise noted, unused active low inputs should be tied to OV_{DD} and unused active high inputs should be connected to GND. All NC (no connect) signals must remain unconnected.

Power and ground connections must be made to all external V_{DD} , OV_{DD} , and GND pins in the MPC7448. For backward compatibility with the MPC7447, MPC7445, and MP7441, or for migrating a system originally designed for one of these devices to the MPC7448, the new power and ground signals (formerly NC, see [Table 11](#)) may be left unconnected if the core frequency is 1 GHz or less. Operation above 1 GHz requires that these additional power and ground signals be connected, and it is strongly recommended that all new designs include the additional connections. See also [Section 7, “Pinout Listings,”](#) for additional information.

The MPC7448 provides VDD_SENSE , $OVDD_SENSE$, and GND_SENSE pins. These pins connect directly to the power/ground planes in the device package and are intended to allow an external device to measure the voltage present on the V_{DD} , OV_{DD} and GND planes in the device package. The most common use for these signals is as a feedback signal to a power supply regulator to allow it to compensate for board losses and supply the correct voltage at the device. (Note that all voltage parameters are specified at the pins of the device.) If not used for this purpose, it is recommended that these signals be connected to test points that can be used in the event that an accurate measurement of the voltage at the device is needed during system debug. Otherwise, these signals should be connected to the appropriate power/ground planes on the circuit board or left unconnected.



Notes:

1. RUN/STOP, normally found on pin 5 of the COP header, is not implemented on the MPC7448. Connect pin 5 of the COP header to OV_{DD} with a 10-KΩ pull-up resistor.
2. Key location; pin 14 is not physically present on the COP header.
3. Component not populated. Populate only if debug tool does not drive $\overline{QACK}$.
4. Populate only if debug tool uses an open-drain type output and does not actively negate $\overline{QACK}$.
5. If the JTAG interface is implemented, connect $\overline{HRESET}$ from the target source to $\overline{TRST}$ from the COP header through an AND gate to $\overline{TRST}$ of the part. If the JTAG interface is not implemented, connect $\overline{HRESET}$ from the target source to $\overline{TRST}$ of the part through a 0-Ω isolation resistor.
6. The COP port and target board should be able to independently assert $\overline{HRESET}$ and $\overline{TRST}$ to the processor in order to fully control the processor as shown above.

Figure 21. JTAG Interface Connection

Due to the complexity and variety of system-level boundary conditions for today's microelectronic equipment, the combined effects of the heat transfer mechanisms (radiation, convection, and conduction) may vary widely. For these reasons, we recommend using conjugate heat transfer models for the board as well as system-level designs.

For system thermal modeling, the MPC7448 thermal model is shown in Figure 26. Four volumes represent this device. Two of the volumes, solder ball-air and substrate, are modeled using the package outline size of the package. The other two, die and bump-underfill, have the same size as the die. The silicon die should be modeled $8.0 \times 7.3 \times 0.86 \text{ mm}^3$ with the heat source applied as a uniform source at the bottom of the volume. The bump and underfill layer is modeled as $8.0 \times 7.3 \times 0.07 \text{ mm}^3$ collapsed in the z-direction with a thermal conductivity of $5.0 \text{ W/(m} \cdot \text{K)}$ in the z-direction. The substrate volume is $25 \times 25 \times 1.14 \text{ mm}^3$ and has $9.9 \text{ W/(m} \cdot \text{K)}$ isotropic conductivity in the xy-plane and $2.95 \text{ W/(m} \cdot \text{K)}$ in the direction of the z-axis. The solder ball and air layer are modeled with the same horizontal dimensions as the substrate and is 0.8 mm thick. For the LGA package the solder and air layer is 0.1 mm thick, but the material properties are the same. It can also be modeled as a collapsed volume using orthotropic material properties: $0.034 \text{ W/(m} \cdot \text{K)}$ in the xy-plane direction and $11.2 \text{ W/(m} \cdot \text{K)}$ in the direction of the z-axis.

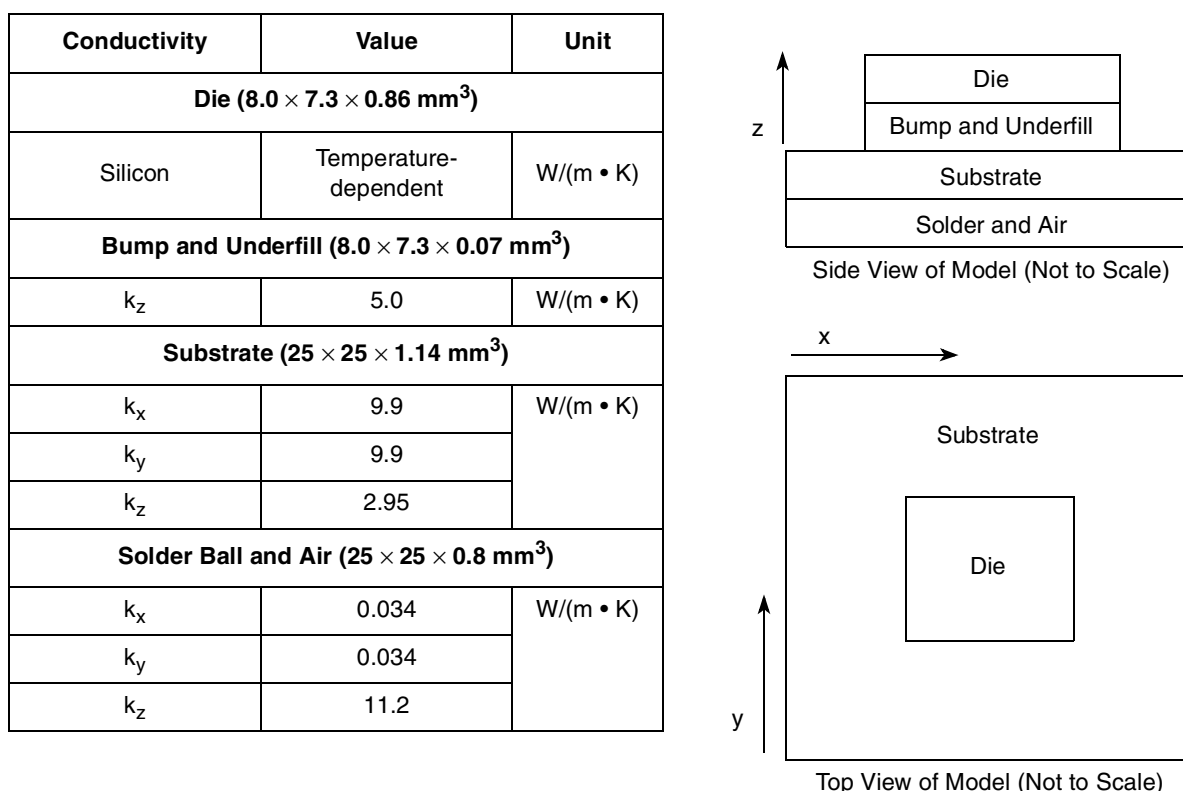


Figure 26. Recommended Thermal Model of MPC7448

Solving for T, the equation becomes:

$$nT = \frac{V_H - V_L}{1.986 \times 10^{-4}}$$

9.7.5 Dynamic Frequency Switching (DFS)

The DFS feature in the MPC7448 adds the ability to divide the processor-to-system bus ratio by two or four during normal functional operation. Divide-by-two mode is enabled by setting the HID1[DFS2] bit in software or by asserting the $\overline{\text{DFS2}}$ pin via hardware. The MPC7448 can be returned for full speed by clearing HID1[DFS2] or negating $\overline{\text{DFS2}}$. Similarly, divide-by-four mode is enabled by setting HID1[DFS4] in software or by asserting the $\overline{\text{DFS4}}$ pin. In all cases, the frequency change occurs in 1 clock cycle and no idle waiting period is required to switch between modes. Note that asserting either $\overline{\text{DFS2}}$ or $\overline{\text{DFS4}}$ overrides software control of DFS, and that asserting both $\overline{\text{DFS2}}$ and $\overline{\text{DFS4}}$ disables DFS completely, including software control. Additional information regarding DFS can be found in the *MPC7450 RISC Microprocessor Family Reference Manual*. Note that minimum core frequency requirements must be observed when enabling DFS, and the resulting core frequency must meet the requirements for $f_{\text{core_DFS}}$ given in [Table 8](#).

9.7.5.1 Power Consumption with DFS Enabled

Power consumption with DFS enabled can be approximated using the following formula:

$$P_{\text{DFS}} = \left[\frac{f_{\text{DFS}}}{f} (P - P_{\text{DS}}) \right] + P_{\text{DS}}$$

Where:

P_{DFS} = Power consumption with DFS enabled

f_{DFS} = Core frequency with DFS enabled

f = Core frequency prior to enabling DFS

P = Power consumption prior to enabling DFS (see [Table 7](#))

P_{DS} = Deep sleep mode power consumption (see [Table 7](#))

The above is an approximation only. Power consumption with DFS enabled is not tested or guaranteed.

9.7.5.2 Bus-to-Core Multiplier Constraints with DFS

DFS is not available for all bus-to-core multipliers as configured by PLL_CFG[0:5] during hard reset. The complete listing is shown in [Table 16](#). Shaded cells represent DFS modes that are not available for a particular PLL_CFG[0:5] setting. Should software or hardware attempt to transition to a multiplier that is not supported, the device will remain at its current multiplier. For example, if a transition from DFS-disabled to an unsupported divide-by-2 or divide-by-4 setting is attempted, the bus-to-core multiplier will remain at the setting configured by the PLL_CFG[0:5] pins. In the case of an attempted transition from a supported divide-by-2 mode to an unsupported divide-by-4 mode, the device will remain in divide-by-2 mode. In all cases, the HID1[PC0-5] bits will correctly reflect the current bus-to-core frequency multiplier.

11 Part Numbering and Marking

Ordering information for the part numbers fully covered by this specification document is provided in [Section 11.1, “Part Numbers Fully Addressed by This Document.”](#) Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact a local Freescale sales office. In addition to the processor frequency, the part numbering scheme also includes an application modifier that may specify special application conditions. An optional specification modifier may also apply for parts to indicate a specific change in specifications, such as support for an extended temperature range. Finally, each part number contains a revision level code that refers to the die mask revision number. [Section 11.2, “Part Numbers Not Fully Addressed by This Document,”](#) lists the part numbers that do not fully conform to the specifications of this document. These special part numbers require an additional document called a hardware specification addendum.

11.1 Part Numbers Fully Addressed by This Document

[Table 18](#) provides the Freescale part numbering nomenclature for the MPC7448 part numbers fully addressed by this document. For information regarding other MPC7448 part numbers, see [Section 11.2, “Part Numbers Not Fully Addressed by This Document.”](#)

Table 18. Part Numbering Nomenclature

xx	7448	xx	nnnn	L	x
Product Code	Part Identifier	Package	Processor Frequency	Application Modifier	Revision Level
MC PPC ¹	7448	HX = HCTE BGA VS = RoHS LGA VU = RoHS BGA	1700	L: 1.3 V +20/–50 mV 0 to 105 °C	C: 2.1; PVR = 0x8004_0201 D: 2.2; PVR = 0x8004_0202
			1600	L: 1.25 V ± 50 mV 0 to 105 °C	
			1420	L: 1.2 V ± 50 mV 0 to 105 °C	
			1000	L: 1.15 V ± 50 mV 0 to 105 °C	

Notes:

1. The P prefix in a Freescale part number designates a “Pilot Production Prototype” as defined by Freescale SOP 3-13. These parts have only preliminary reliability and characterization data. Before pilot production prototypes may be shipped, written authorization from the customer must be on file in the applicable sales office acknowledging the qualification status and the fact that product changes may still occur as pilot production prototypes are shipped.

11.2 Part Numbers Not Fully Addressed by This Document

Parts with application modifiers or revision levels not fully addressed in this specification document are described in separate hardware specification addenda which supplement and supersede this document. As such parts are released, these specifications will be listed in this section.

Table 19. Part Numbers Addressed by MC7448xxnnnnNx Series Hardware Specification Addendum (Document Order No. MPC7448ECS01AD)

xx	7448	xx	nnnn	N	x
Product Code	Part Identifier	Package	Processor Frequency	Application Modifier	Revision Level
MC	7448	HX = HCTE BGA VS = RoHS LGA VU = RoHS BGA	1400	N: 1.15 V ± 50 mV 0 to 105 °C (date code 0613 and later) ²	C: 2.1; PVR = 0x8004_0201 D: 2.2; PVR = 0x8004_0202
MC PPC ¹			1400	N: 1.1 V ± 50 mV 0 to 105 °C (date code 0612 and prior) ²	
MC PPC ¹			1267 Revision C only	N: 1.1 V ± 50 mV 0 to 105 °C	
MC PPC ¹			1267 Revision D only	N: 1.05 V ± 50 mV 0 to 105 °C	
MC PPC ¹			1250	N: 1.1 V ± 50 mV 0 to 105 °C	
MC PPC ¹			1000 867 800 667 600	N: 1.0 V ± 50 mV 0 to 105 °C	

Notes:

1. The P prefix in a Freescale part number designates a "Pilot Production Prototype" as defined by Freescale SOP 3-13. These parts have only preliminary reliability and characterization data. Before pilot production prototypes can be shipped, written authorization from the customer must be on file in the applicable sales office acknowledging the qualification status and the fact that product changes may still occur as pilot production prototypes are shipped.
2. Core voltage for 1400 MHz devices currently in production (date code of 0613 and later) is 1.15 V ± 50 mV; all such devices have the MC product code. The 1400 MHz devices with date code of 0612 and prior specified core voltage of 1.1 V ± 50 mV; this includes all 1400 MHz devices with the PPC product code. See [Section 11.3, "Part Marking,"](#) for information on part marking.