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Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC G4
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.6GHz
Co-Processors/DSP	Multimedia; SIMD
RAM Controllers	-
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	1.5V, 1.8V, 2.5V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	360-CBGA, FCCBGA
Supplier Device Package	360-FCCBGA (25x25)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc7448vu1600lc

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



2 Features

This section summarizes features of the MPC7448 implementation.

Major features of the MPC7448 are as follows:

- High-performance, superscalar microprocessor
 - Up to four instructions can be fetched from the instruction cache at a time.
 - Up to three instructions plus a branch instruction can be dispatched to the issue queues at a time.
 - Up to 12 instructions can be in the instruction queue (IQ).
 - Up to 16 instructions can be at some stage of execution simultaneously.
 - Single-cycle execution for most instructions
 - One instruction per clock cycle throughput for most instructions
 - Seven-stage pipeline control
- Eleven independent execution units and three register files
 - Branch processing unit (BPU) features static and dynamic branch prediction
 - 128-entry (32-set, four-way set-associative) branch target instruction cache (BTIC), a cache of branch instructions that have been encountered in branch/loop code sequences. If a target instruction is in the BTIC, it is fetched into the instruction queue a cycle sooner than it can be made available from the instruction cache. Typically, a fetch that hits the BTIC provides the first four instructions in the target stream.
 - 2048-entry branch history table (BHT) with 2 bits per entry for four levels of prediction—not taken, strongly not taken, taken, and strongly taken
 - Up to three outstanding speculative branches
 - Branch instructions that do not update the count register (CTR) or link register (LR) are often removed from the instruction stream.
 - Eight-entry link register stack to predict the target address of Branch Conditional to Link Register (bclr) instructions
 - Four integer units (IUs) that share 32 GPRs for integer operands
 - Three identical IUs (IU1a, IU1b, and IU1c) can execute all integer instructions except multiply, divide, and move to/from special-purpose register instructions.
 - IU2 executes miscellaneous instructions, including the CR logical operations, integer multiplication and division instructions, and move to/from special-purpose register instructions.
 - Five-stage FPU and 32-entry FPR file
 - Fully IEEE Std. 754TM-1985–compliant FPU for both single- and double-precision operations
 - Supports non-IEEE mode for time-critical operations
 - Hardware support for denormalized numbers
 - Thirty-two 64-bit FPRs for single- or double-precision operands

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Features

— Four vector units and 32-entry vector register file (VRs)

- Vector permute unit (VPU)
- − Vector integer unit 1 (VIU1) handles short-latency AltiVecTM integer instructions, such as vector add instructions (for example, vaddsbs, vaddsbs, and vaddsws).
- Vector integer unit 2 (VIU2) handles longer-latency AltiVec integer instructions, such as vector multiply add instructions (for example, vmhaddshs, vmhraddshs, and vmladduhm).
- Vector floating-point unit (VFPU)
- Three-stage load/store unit (LSU)
 - Supports integer, floating-point, and vector instruction load/store traffic
 - Four-entry vector touch queue (VTQ) supports all four architected AltiVec data stream operations
 - Three-cycle GPR and AltiVec load latency (byte, half word, word, vector) with one-cycle throughput
 - Four-cycle FPR load latency (single, double) with one-cycle throughput
 - No additional delay for misaligned access within double-word boundary
 - A dedicated adder calculates effective addresses (EAs).
 - Supports store gathering
 - Performs alignment, normalization, and precision conversion for floating-point data
 - Executes cache control and TLB instructions
 - Performs alignment, zero padding, and sign extension for integer data
 - Supports hits under misses (multiple outstanding misses)
 - Supports both big- and little-endian modes, including misaligned little-endian accesses
- Three issue queues, FIQ, VIQ, and GIQ, can accept as many as one, two, and three instructions, respectively, in a cycle. Instruction dispatch requires the following:
 - Instructions can only be dispatched from the three lowest IQ entries—IQ0, IQ1, and IQ2.
 - A maximum of three instructions can be dispatched to the issue queues per clock cycle.
 - Space must be available in the CQ for an instruction to dispatch (this includes instructions that are assigned a space in the CQ but not in an issue queue).
- Rename buffers
 - 16 GPR rename buffers
 - 16 FPR rename buffers
 - 16 VR rename buffers
- Dispatch unit
 - Decode/dispatch stage fully decodes each instruction
- Completion unit
 - Retires an instruction from the 16-entry completion queue (CQ) when all instructions ahead of it have been completed, the instruction has finished executing, and no exceptions are pending
 - Guarantees sequential programming model (precise exception model)



Features

- Efficient data flow
 - Although the VR/LSU interface is 128 bits, the L1/L2 bus interface allows up to 256 bits.
 - The L1 data cache is fully pipelined to provide 128 bits/cycle to or from the VRs.
 - The L2 cache is fully pipelined to provide 32 bytes per clock every other cycle to the L1 caches.
 - As many as 16 out-of-order transactions can be present on the MPX bus.
 - Store merging for multiple store misses to the same line. Only coherency action taken (address-only) for store misses merged to all 32 bytes of a cache block (no data tenure needed).
 - Three-entry finished store queue and five-entry completed store queue between the LSU and the L1 data cache
 - Separate additional queues for efficient buffering of outbound data (such as castouts and write-through stores) from the L1 data cache and L2 cache
- Multiprocessing support features include the following:
 - Hardware-enforced, MESI cache coherency protocols for data cache
 - Load/store with reservation instruction pair for atomic memory references, semaphores, and other multiprocessor operations
- Power and thermal management
 - Dynamic frequency switching (DFS) feature allows processor core frequency to be halved or quartered through software to reduce power consumption.
 - The following three power-saving modes are available to the system:
 - Nap—Instruction fetching is halted. Only the clocks for the time base, decrementer, and JTAG logic remain running. The part goes into the doze state to snoop memory operations on the bus and then back to nap using a <u>QREQ</u>/<u>QACK</u> processor-system handshake protocol.
 - Sleep—Power consumption is further reduced by disabling bus snooping, leaving only the PLL in a locked and running state. All internal functional units are disabled.
 - Deep sleep—When the part is in the sleep state, the system can disable the PLL. The system
 can then disable the SYSCLK source for greater system power savings. Power-on reset
 procedures for restarting and relocking the PLL must be followed upon exiting the deep
 sleep state.
 - Instruction cache throttling provides control of instruction fetching to limit device temperature.
 - A new temperature diode that can determine the temperature of the microprocessor
- Performance monitor can be used to help debug system designs and improve software efficiency.
- In-system testability and debugging features through JTAG boundary-scan capability
- Testability
 - LSSD scan design
 - IEEE Std. 1149.1TM JTAG interface





- Reliability and serviceability
 - Parity checking on system bus
 - Parity checking on the L1 caches and L2 data tags
 - ECC or parity checking on L2 data

3 Comparison with the MPC7447A, MPC7447, MPC7445, and MPC7441

Table 1 compares the key features of the MPC7448 with the key features of the earlier MPC7447A, MPC7447, MPC7445, and MPC7441. All are based on the MPC7450 RISC microprocessor and are architecturally very similar. The MPC7448 is identical to the MPC7447A, but the MPC7448 supports 1 Mbyte of L2 cache with ECC and the use of dynamic frequency switching (DFS) with more bus-to-core ratios.

Microarchitectural Specs	MPC7448	MPC7447A	MPC7447	MPC7445	MPC7441			
Basic Pipeline Functions								
Logic inversions per cycle 18								
Pipeline stages up to execute			5					
Total pipeline stages (minimum)			7					
Pipeline maximum instruction throughput		:	3 + branch					
Pipeline Re	esources							
Instruction buffer size			12					
Completion buffer size			16					
Renames (integer, float, vector)			16, 16, 16					
Maximum Executi	ion Through	nput						
SFX			3					
Vector	2 (any 2 of 4 units)							
Scalar floating-point	1							
Out-of-Order Window Siz	e in Execut	ion Queues						
SFX integer units		1 en	try $ imes$ 3 queu	ies				
Vector units	In order, 4 queues							
Scalar floating-point unit			In order					
Branch Processi	ng Resourc	es						
Prediction structures		BTIC,	BHT, link s	tack				
BTIC size, associativity	128-entry, 4-way							
BHT size	2K-entry							
Link stack depth	8							
Unresolved branches supported	3							
Branch taken penalty (BTIC hit)	1							
Minimum misprediction penalty	6							

Table 1. Microarchitecture Comparison

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Electrical and Thermal Characteristics

Figure 2 shows the undershoot and overshoot voltage on the MPC7448.



Figure 2. Overshoot/Undershoot Voltage

The MPC7448 provides several I/O voltages to support both compatibility with existing systems and migration to future systems. The MPC7448 core voltage must always be provided at the nominal voltage (see Table 4). The input voltage threshold for each bus is selected by sampling the state of the voltage select pins at the negation of the signal HRESET. The output voltage will swing from GND to the maximum voltage applied to the OV_{DD} power pins. Table 3 provides the input threshold voltage settings. Because these settings may change in future products, it is recommended that BVSEL[0:1] be configured using resistor options, jumpers, or some other flexible means, with the capability to reconfigure the termination of this signal in the future, if necessary.

BVSEL0	BVSEL1	I/O Voltage Mode ¹	Notes
0	0	1.8 V	2, 3
0	1	2.5 V	2, 4
1	0	1.5 V	2
1	1	2.5 V	4

Table 3. Input Threshold Voltage Setting

Notes:

- 1. **Caution:** The I/O voltage mode selected must agree with the OV_{DD} voltages supplied. See Table 4.
- 2. If used, pull-down resistors should be less than 250 $\Omega.$
- 3. The pin configuration used to select 1.8V mode on the MPC7448 is not compatible with the pin configuration used to select 1.8V mode on the MPC7447A and earlier devices.
- 4. The pin configuration used to select 2.5V mode on the MPC7448 is fully compatible with the pin configuration used to select 2.5V mode on the MPC7447A and earlier devices.



Table 6. DC Electrical Specifications (continued)

At recommended operating conditions. See Table 4.

Characteristic		Nominal Bus Voltage ¹	Symbol	Min	Max	Unit	Notes
$\label{eq:high-impedance} \begin{array}{l} \text{High-impedance (off-stat}\\ V_{in} = OV_{DD}\\ V_{in} = GND \end{array}$	_	I _{TSI}	_	50 - 50	μA	2, 3, 4	
Output high voltage @ Ic	1.5	V _{OH}	OV _{DD} - 0.45	_	V		
	1.8		OV _{DD} - 0.45	_			
	2.5		1.8	_			
Output low voltage @ IO	_ = 5 mA	1.5	V _{OL}	—	0.45	V	
		1.8		_	0.45		
		2.5		—	0.6		
Capacitance, V _{in} = 0 V, f = 1 MHz	All inputs		C _{in}	—	8.0	pF	5

Notes:

1. Nominal voltages; see Table 4 for recommended operating conditions.

2. All I/O signals are referenced to OV_{DD}.

3. Excludes test signals and IEEE Std. 1149.1 boundary scan (JTAG) signals

4. The leakage is measured for nominal OV_{DD} and V_{DD} , or both OV_{DD} and V_{DD} must vary in the same direction (for example, both OV_{DD} and V_{DD} vary by either +5% or -5%).

5. Capacitance is periodically sampled rather than 100% tested.

6. These pins have internal pull-up resistors.

Table 7 provides the power consumption for the MPC7448 part numbers described by this document; see Section 11.1, "Part Numbers Fully Addressed by This Document," for information regarding which part numbers are described by this document. Freescale also offers MPC7448 part numbers that meet lower power consumption specifications by adhering to lower core voltage and core frequency specifications. For more information on these devices, including references to the MPC7448 Hardware Specification Addenda that describe these devices, see Section 11.2, "Part Numbers Not Fully Addressed by This Document."

The power consumptions provided in Table 7 represent the power consumption of each speed grade when operated at the rated maximum core frequency (see Table 8). Freescale sorts devices by power as well as by core frequency, and power limits for each speed grade are independent of each other. Each device is tested at its maximum core frequency only. (Note that Deep Sleep Mode power consumption is independent of clock frequency.) Operating a device at a frequency lower than its rated maximum is fully supported provided the clock frequencies are within the specifications given in Table 8, and a device operated below its rated maximum will have lower power consumption. However, inferences should not be made about a device's power consumption based on the power specifications of another (lower) speed grade. For example, a 1700 MHz device operated at 1420 MHz may not exhibit the same power consumption as a 1420 MHz device operated at 1420 MHz.

For all MPC7448 devices, the following guidelines on the use of these parameters for system design are suggested. The Full-Power Mode–Typical value represents the sustained power consumption of the device

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5.2 AC Electrical Characteristics

This section provides the AC electrical characteristics for the MPC7448. After fabrication, functional parts are sorted by maximum processor core frequency as shown in Section 5.2.1, "Clock AC Specifications," and tested for conformance to the AC specifications for that frequency. The processor core frequency, determined by the bus (SYSCLK) frequency and the settings of the PLL_CFG[0:5] signals, can be dynamically modified using dynamic frequency switching (DFS). Parts are sold by maximum processor core frequency; see Section 11, "Part Numbering and Marking," for information on ordering parts. DFS is described in Section 9.7.5, "Dynamic Frequency Switching (DFS)."

5.2.1 Clock AC Specifications

Table 8 provides the clock AC timing specifications as defined in Figure 3 and represents the tested operating frequencies of the devices. The maximum system bus frequency, f_{SYSCLK}, given in Table 8, is considered a practical maximum in a typical single-processor system. This does not exclude multi-processor systems, but these typically require considerably more design effort to achieve the maximum rated bus frequency. The actual maximum SYSCLK frequency for any application of the MPC7448 will be a function of the AC timings of the microprocessor(s), the AC timings for the system controller, bus loading, circuit board topology, trace lengths, and so forth, and may be less than the value given in Table 8.



Electrical and Thermal Characteristics

Table 9. Processor Bus AC Timing Specifications¹ (continued)

At recommended operating conditions. See Table 4.

Parameter	Symbol 2	All Spee	d Grades	Unit	Notes
Falanetei	Symbol	Min	Мах	Unit	
SYSCLK to output high impedance (all except \overline{TS} , \overline{ARTRY} , SHD0, $\overline{SHD1}$)	^t кноz	—	1.8	ns	5
SYSCLK to \overline{TS} high impedance after precharge	t _{KHTSPZ}	_	1	t _{SYSCLK}	3, 4, 5
Maximum delay to ARTRY/SHD0/SHD1 precharge	t _{KHARP}	_	1	t _{SYSCLK}	3, 5, 6, 7
SYSCLK to ARTRY/SHD0/SHD1 high impedance after precharge	t _{KHARPZ}	_	2	t _{SYSCLK}	3, 5, 6, 7

Notes:

- All input specifications are measured from the midpoint of the signal in question to the midpoint of the rising edge of the input SYSCLK. All output specifications are measured from the midpoint of the rising edge of SYSCLK to the midpoint of the signal in question. All output timings assume a purely resistive 50-Ω load (see Figure 4). Input and output timings are measured at the pin; time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
- 2. The symbology used for timing specifications herein follows the pattern of t_{(signal)(state)(reference)(state)} for inputs and t_{(reference)(state)(signal)(state)} for outputs. For example, t_{IVKH} symbolizes the time input signals (I) reach the valid state (V) relative to the SYSCLK reference (K) going to the high (H) state or input setup time. And t_{KHOV} symbolizes the time from SYSCLK(K) going high (H) until outputs (O) are valid (V) or output valid time. Input hold time can be read as the time that the input signal (I) went invalid (X) with respect to the rising clock edge (KH) (note the position of the reference and its state for inputs) and output hold time can be read as the time from the rising edge (KH) until the output went invalid (OX).
- 3. t_{sysclk} is the period of the external clock (SYSCLK) in ns. The numbers given in the table must be multiplied by the period of SYSCLK to compute the actual time duration (in ns) of the parameter in question.
- 4. According to the bus protocol, TS is driven only by the currently active bus master. It is asserted low and precharged high before returning to high impedance, as shown in Figure 6. The nominal precharge width for TS is t_{SYSCLK}, that is, one clock period. Since no master can assert TS on the following clock edge, there is no concern regarding contention with the precharge. Output valid and output hold timing is tested for the signal asserted. Output valid time is tested for precharge. The high-impedance behavior is guaranteed by design.
- 5. Guaranteed by design and not tested
- 6. According to the bus protocol, ARTRY can be driven by multiple bus masters through the clock period immediately following AACK. Bus contention is not an issue because any master asserting ARTRY will be driving it low. Any master asserting it low in the first clock following AACK will then go to high impedance for a fraction of a cycle, then negated for up to an entire cycle (crossing a bus cycle boundary) before being three-stated again. The nominal precharge width for ARTRY is 1.0 t_{SYSCLK}; that is, it should be high impedance as shown in Figure 6 before the first opportunity for another master to assert ARTRY. Output valid and output hold timing is tested for the signal asserted. The high-impedance behavior is guaranteed by design.
- 7. According to the MPX bus protocol, SHD0 and SHD1 can be driven by multiple bus masters beginning two cycles after TS. Timing is the same as ARTRY, that is, the signal is high impedance for a fraction of a cycle, then negated for up to an entire cycle (crossing a bus cycle boundary) before being three-stated again. The nominal precharge width for SHD0 and SHD1 is 1.0 t_{SYSCLK}. The edges of the precharge vary depending on the programmed ratio of core to bus (PLL configurations).
- BMODE[0:1] and BVSEL[0:1] are mode select inputs. BMODE[0:1] are sampled before and after HRESET negation. BVSEL[0:1] are sampled before HRESET negation. These parameters represent the input setup and hold times for each sample. These values are guaranteed by design and not tested. BMODE[0:1] must remain stable after the second sample; BVSEL[0:1] must remain stable after the first (and only) sample. See Figure 5 for sample timing.



Figure 4 provides the AC test load for the MPC7448.



Figure 5 provides the BMODE[0:1] input timing diagram for the MPC7448. These mode select inputs are sampled once before and once after HRESET negation.



Figure 5. BMODE[0:1] Input Sample Timing Diagram



5.2.3 IEEE Std. 1149.1 AC Timing Specifications

Table 10 provides the IEEE Std. 1149.1 (JTAG) AC timing specifications as defined in Figure 8 through Figure 11.

Table 10. JTAG AC Timing Specifications (Independent of SYSCLK)¹

At recommended operating conditions. See Table 4.

Parameter	Symbol	Min	Мах	Unit	Notes
TCK frequency of operation	f _{TCLK}	0	33.3	MHz	
TCK cycle time	t _{TCLK}	30	—	ns	
TCK clock pulse width measured at 1.4 V	t _{JHJL}	15	—	ns	
TCK rise and fall times	$t_{\rm JR}$ and $t_{\rm JF}$	—	2	ns	
TRST assert time	t _{TRST}	25	—	ns	2
Input setup times: Boundary-scan data TMS, TDI	t _{DVJH} t _{IVJH}	4 0	_	ns	3
Input hold times: Boundary-scan data TMS, TDI	^t DXJH t _{IXJH}	20 25		ns	3
Valid times: Boundary-scan data TDO	t _{JLDV} t _{JLOV}	4 4	20 25	ns	4
Output hold times: Boundary-scan data TDO	t _{JLDX} t _{JLOX}	30 30	—	ns	4
TCK to output high impedance: Boundary-scan data TDO	t _{JLDZ} t _{JLOZ}	3 3	19 9	ns	4, 5

Notes:

 All outputs are measured from the midpoint voltage of the falling/rising edge of TCLK to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load (see Figure 7). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.

2. TRST is an asynchronous level sensitive signal. The time is for test purposes only.

3. Non-JTAG signal input timing with respect to TCK.

4. Non-JTAG signal output timing with respect to TCK.

5. Guaranteed by design and characterization.



7 Pinout Listings

Table 11 provides the pinout listing for the MPC7448, 360 HCTE package. The pinouts of the MPC7448 and MPC7447A are compatible, but the requirements regarding the use of the additional power and ground pins have changed. The MPC7448 requires these pins be connected to the appropriate power or ground plane to achieve high core frequencies; see Section 9.3, "Connection Recommendations," for additional information. As a result, these pins should be connected in all new designs.

Additionally, the MPC7448 may be populated on a board designed for a MPC7447 (or MPC7445 or MPC7441), provided the core voltage can be made to match the requirements in Table 4 and all pins defined as 'no connect' for the MPC7447 are unterminated, as required by the *MPC7457 RISC Microprocessor Hardware Specifications*. The MPC7448 uses pins previously marked 'no connect' for the temperature diode pins and for additional power and ground connections. The additional power and ground pins are required to achieve high core frequencies and core frequency will be limited if they are not connected; see Section 9.3, "Connection Recommendations," for additional information. Because these 'no connect' pins in the MPC7447 360 pin package are not driven in functional mode, an MPC7447 can be populated in an MPC7448 board.

NOTE

Caution must be exercised when performing boundary scan test operations on a board designed for an MPC7448, but populated with an MPC7447 or earlier device. This is because in the MPC7447 it is possible to drive the latches associated with the former 'no connect' pins in the MPC7447, potentially causing contention on those pins. To prevent this, ensure that these pins are not connected on the board or, if they are connected, ensure that the states of internal MPC7447 latches do not cause these pins to be driven during board testing.

For the MPC7448, pins that were defined as the TEST[0:4] factory test signal group on the MPC7447A and earlier devices have been assigned new functions. For most of these, the termination recommendations for the TEST[0:4] pins of the MPC7447A are compatible with the MPC7448 and will allow correct operation with no performance loss. The exception is BVSEL1 (TEST3 on the MPC7447A and earlier devices), which may require a different termination depending which I/O voltage mode is desired; see Table 3 for more information.

NOTE

This pinout is not compatible with the MPC750, MPC7400, or MPC7410 360 BGA package.



Package Description

8.2 Mechanical Dimensions for the MPC7448, 360 HCTE BGA

Figure 13 provides the mechanical dimensions and bottom surface nomenclature for the MPC7448, 360 HCTE BGA package.



Figure 13. Mechanical Dimensions and Bottom Surface Nomenclature for the MPC7448, 360 HCTE BGA Package



8.5 Package Parameters for the MPC7448, 360 HCTE RoHS-Compliant BGA

The package parameters are as provided in the following list. The package type is 25×25 mm, 360-lead high coefficient of thermal expansion ceramic ball grid array (HCTE) with RoHS-compliant lead-free spheres.

Package outline	$25 \times 25 \text{ mm}$				
Interconnects	360 (19 × 19 ball array – 1)				
Pitch	1.27 mm (50 mil)				
Minimum module height	1.92 mm				
Maximum module height	2.40 mm				
Ball diameter	0.75 mm (30 mil)				
Coefficient of thermal expansion12.3 ppm/°C					





9 System Design Information

This section provides system and thermal design requirements and recommendations for successful application of the MPC7448.

9.1 Clocks

The following sections provide more detailed information regarding the clocking of the MPC7448.

9.1.1 PLL Configuration

The MPC7448 PLL is configured by the PLL_CFG[0:5] signals. For a given SYSCLK (bus) frequency, the PLL configuration signals set the internal CPU and VCO frequency of operation. The PLL configuration for the MPC7448 is shown in Table 12. In this example, shaded cells represent settings that, for a given SYSCLK frequency, result in core and/or VCO frequencies that do not comply with Table 8. When enabled, dynamic frequency switching (DFS) also affects the core frequency by halving or quartering the bus-to-core multiplier; see Section 9.7.5, "Dynamic Frequency Switching (DFS)," for more information. Note that when DFS is enabled the resulting core frequency must meet the adjusted minimum core frequency requirements (f_{core_DFS}) described in Table 8. Note that the PLL_CFG[5] is currently used for factory test only and should be tied low, and that the MPC7448 PLL configuration settings are compatible with the MPC7447A PLL configuration settings when PLL_CFG[5] = 0.

	Example Core and VCO Frequency in MHz										
PLL_CFG[0:5]	Bus-to-Core Multiplier ⁵	Core-to-VCO Multiplier ⁵	Bus (SYSCLK) Frequency								
			33.3 MHz	50 MHz	66.6 MHz	75 MHz	83 MHz	100 MHz	133 MHz	167 MHz	200 MHz
010000	2x ⁶	1x									
100000	3x ⁶	1x									600
101000	4x ⁶	1x								667	800
101100	5x	1x							667	835	1000
100100	5.5x	1x							733	919	1100
110100	6x	1x						600	800	1002	1200
010100	6.5x	1x						650	866	1086	1300
001000	7x	1x						700	931	1169	1400
000100	7.5x	1x					623	750	1000	1253	1500
110000	8x	1x				600	664	800	1064	1336	1600
011000	8.5x	1x				638	706	850	1131	1417	1700
011110	9x	1x			600	675	747	900	1197	1500	
011100	9.5x	1x			633	712	789	950	1264	1583	
101010	10x	1x			667	750	830	1000	1333	1667	
100010	10.5x	1x			700	938	872	1050	1397		

Table 12. MPC7448 Microprocessor PLL Configuration Example



9.2.4 Decoupling Recommendations

Due to the MPC7448 dynamic power management feature, large address and data buses, and high operating frequencies, the MPC7448 can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the MPC7448 system, and the MPC7448 itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer use sufficient decoupling capacitors, typically one capacitor for every V_{DD} pin, and a similar amount for the OV_{DD} pins, placed as close as possible to the power pins of the MPC7448. It is also recommended that these decoupling capacitors receive their power from separate V_{DD} , OV_{DD}, and GND power planes in the PCB, using short traces to minimize inductance.

These capacitors should have a value of 0.01 or 0.1 μ F. Only ceramic surface mount technology (SMT) capacitors should be used to minimize lead inductance. Orientations where connections are made along the length of the part, such as 0204, are preferable but not mandatory. Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993) and contrary to previous recommendations for decoupling Freescale microprocessors, multiple small capacitors of equal value are recommended over using multiple values of capacitance.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V_{DD} and OV_{DD} planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low equivalent series resistance (ESR) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors are 100–330 μ F (AVX TPS tantalum or Sanyo OSCON).

9.3 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. Unless otherwise noted, unused active low inputs should be tied to OV_{DD} and unused active high inputs should be connected to GND. All NC (no connect) signals must remain unconnected.

Power and ground connections must be made to all external V_{DD} , OV_{DD} , and GND pins in the MPC7448. For backward compatibility with the MPC7447, MPC7445, and MP7441, or for migrating a system originally designed for one of these devices to the MPC7448, the new power and ground signals (formerly NC, see Table 11) may be left unconnected if the core frequency is 1 GHz or less. Operation above 1 GHz requires that these additional power and ground signals be connected, and it is strongly recommended that all new designs include the additional connections. See also Section 7, "Pinout Listings," for additional information.

The MPC7448 provides VDD_SENSE, OVDD_SENSE, and GND_SENSE pins. These pins connect directly to the power/ground planes in the device package and are intended to allow an external device to measure the voltage present on the V_{DD} , OV_{DD} and GND planes in the device package. The most common use for these signals is as a feedback signal to a power supply regulator to allow it to compensate for board losses and supply the correct voltage at the device. (Note that all voltage parameters are specified at the pins of the device.) If not used for this purpose, it is recommended that these signals be connected to test points that can be used in the event that an accurate measurement of the voltage at the device is needed during system debug. Otherwise, these signals should be connected to the appropriate power/ground planes on the circuit board or left unconnected.



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9.4 Output Buffer DC Impedance

The MPC7448 processor bus drivers are characterized over process, voltage, and temperature. To measure Z_0 , an external resistor is connected from the chip pad to OV_{DD} or GND. The value of each resistor is varied until the pad voltage is $OV_{DD}/2$. Figure 20 shows the driver impedance measurement.



Figure 20. Driver Impedance Measurement

The output impedance is the average of two components—the resistances of the pull-up and pull-down devices. When data is held low, SW2 is closed (SW1 is open), and R_N is trimmed until the voltage at the pad equals $OV_{DD}/2$. R_N then becomes the resistance of the pull-down devices. When data is held high, SW1 is closed (SW2 is open), and R_P is trimmed until the voltage at the pad equals $OV_{DD}/2$. R_P then becomes the resistance of the pull-down devices to each other in value. Then, $Z_0 = (R_P + R_N)/2$.

Table 15 summarizes the signal impedance results. The impedance increases with junction temperature and is relatively unaffected by bus voltage.

At recommended operating conditions. See Table 4						
Impedance Processor Bus Unit						
Z ₀	Typical	33–42	Ω			
	Maximum	31–51	Ω			

Table 15. Impedance Characteristics

9.5 Pull-Up/Pull-Down Resistor Requirements

The MPC7448 requires high-resistive (weak: 4.7-K Ω) pull-up resistors on several control pins of the bus interface to maintain the control signals in the negated state after they have been actively negated and released by the MPC7448 or other bus masters. These pins are: TS, ARTRY, SHDO, and SHD1.

Some pins designated as being factory test pins must be pulled up to OV_{DD} or down to GND to ensure proper device operation. The pins that must be pulled up to OV_{DD} are LSSD_MODE and TEST[0:3]; the pins that must be pulled down to GND are L1_TSTCLK and TEST[4]. The CKSTP_IN signal should



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Notes:

- 1. RUN/STOP, normally found on pin 5 of the COP header, is not implemented on the MPC7448. Connect pin 5 of the COP header to OV_{DD} with a 10-K Ω pull-up resistor.
- 2. Key location; pin 14 is not physically present on the COP header.
- 3. Component not populated. Populate only if debug tool does not drive QACK.
- 4. Populate only if debug tool uses an open-drain type output and does not actively negate QACK.
- 5. If the JTAG interface is implemented, connect $\overline{\text{HRESET}}$ from the target source to $\overline{\text{TRST}}$ from the COP header though an AND gate to $\overline{\text{TRST}}$ of the part. If the JTAG interface is not implemented, connect $\overline{\text{HRESET}}$ from the target source to $\overline{\text{TRST}}$ of the part through a 0- Ω isolation resistor.
- 6. The COP port and target board should be able to independently assert HRESET and TRST to the processor in order to fully control the processor as shown above.

Figure 21. JTAG Interface Connection

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9.7.1 Internal Package Conduction Resistance

For the exposed-die packaging technology described in Table 5, the intrinsic conduction thermal resistance paths are as follows:

- The die junction-to-case thermal resistance (the case is actually the top of the exposed silicon die)
- The die junction-to-board thermal resistance

Figure 24 depicts the primary heat transfer path for a package with an attached heat sink mounted to a printed-circuit board.



Figure 24. C4 Package with Heat Sink Mounted to a Printed-Circuit Board

Heat generated on the active side of the chip is conducted through the silicon, through the heat sink attach material (or thermal interface material), and, finally, to the heat sink, where it is removed by forced-air convection.

Because the silicon thermal resistance is quite small, the temperature drop in the silicon may be neglected for a first-order analysis. Thus, the thermal interface material and the heat sink conduction/convective thermal resistances are the dominant terms.

9.7.2 Thermal Interface Materials

A thermal interface material is recommended at the package lid-to-heat sink interface to minimize the thermal contact resistance. For those applications where the heat sink is attached by spring clip mechanism, Figure 25 shows the thermal performance of three thin-sheet thermal-interface materials (silicone, graphite/oil, fluoroether oil), a bare joint, and a joint with thermal grease as a function of contact pressure. As shown, the performance of these thermal interface materials improves with increasing contact pressure. The use of thermal grease significantly reduces the interface thermal resistance. That is, the bare joint results in a thermal resistance approximately seven times greater than the thermal grease joint.

Often, heat sinks are attached to the package by means of a spring clip to holes in the printed-circuit board (see Figure 22). Therefore, synthetic grease offers the best thermal performance due to the low interface pressure and is recommended due to the high power dissipation of the MPC7448. Of course, the selection



of any thermal interface material depends on many factors—thermal performance requirements, manufacturability, service temperature, dielectric properties, cost, and so on.



Figure 25. Thermal Performance of Select Thermal Interface Material

The board designer can choose between several types of thermal interfaces. Heat sink adhesive materials should be selected based on high conductivity and mechanical strength to meet equipment shock/vibration requirements. There are several commercially available thermal interfaces and adhesive materials provided by the following vendors:

The Bergquist Company	800-347-4572
18930 West 78 th St.	
Chanhassen, MN 55317	
Internet: www.bergquistcompany.com	
Chomerics, Inc.	781-935-4850
77 Dragon Ct.	
Woburn, MA 01801	
Internet: www.chomerics.com	
Dow-Corning Corporation	800-248-2481
Corporate Center	
P.O. Box 994.	
Midland, MI 48686-0994	
Internet: www.dowcorning.com	

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Home Page: www.freescale.com

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USA/Europe or Locations Not Listed:

Freescale Semiconductor Technical Information Center, CH370 1300 N. Alma School Road Chandler, Arizona 85224 1-800-521-6274 480-768-2130 support@freescale.com

Europe, Middle East, and Africa:

Freescale Halbleiter Deutschland GmbH Technical Information Center Schatzbogen 7 81829 Muenchen, Germany +44 1296 380 456 (English) +46 8 52200080 (English) +49 89 92103 559 (German) +33 1 69 35 48 48 (French) support@freescale.com

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