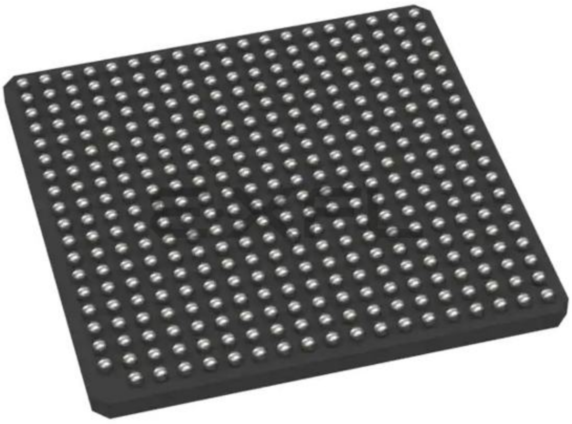

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC G4
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.7GHz
Co-Processors/DSP	Multimedia; SIMD
RAM Controllers	-
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	1.5V, 1.8V, 2.5V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	360-CBGA, FCCBGA
Supplier Device Package	360-FCCBGA (25x25)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc7448vu1700lc

2 Features

This section summarizes features of the MPC7448 implementation.

Major features of the MPC7448 are as follows:

- High-performance, superscalar microprocessor
  - Up to four instructions can be fetched from the instruction cache at a time.
  - Up to three instructions plus a branch instruction can be dispatched to the issue queues at a time.
  - Up to 12 instructions can be in the instruction queue (IQ).
  - Up to 16 instructions can be at some stage of execution simultaneously.
  - Single-cycle execution for most instructions
  - One instruction per clock cycle throughput for most instructions
  - Seven-stage pipeline control
- Eleven independent execution units and three register files
  - Branch processing unit (BPU) features static and dynamic branch prediction
    - 128-entry (32-set, four-way set-associative) branch target instruction cache (BTIC), a cache of branch instructions that have been encountered in branch/loop code sequences. If a target instruction is in the BTIC, it is fetched into the instruction queue a cycle sooner than it can be made available from the instruction cache. Typically, a fetch that hits the BTIC provides the first four instructions in the target stream.
    - 2048-entry branch history table (BHT) with 2 bits per entry for four levels of prediction—not taken, strongly not taken, taken, and strongly taken
    - Up to three outstanding speculative branches
    - Branch instructions that do not update the count register (CTR) or link register (LR) are often removed from the instruction stream.
    - Eight-entry link register stack to predict the target address of Branch Conditional to Link Register (**bclr**) instructions
  - Four integer units (IUs) that share 32 GPRs for integer operands
    - Three identical IUs (IU1a, IU1b, and IU1c) can execute all integer instructions except multiply, divide, and move to/from special-purpose register instructions.
    - IU2 executes miscellaneous instructions, including the CR logical operations, integer multiplication and division instructions, and move to/from special-purpose register instructions.
  - Five-stage FPU and 32-entry FPR file
    - Fully IEEE Std. 754™-1985–compliant FPU for both single- and double-precision operations
    - Supports non-IEEE mode for time-critical operations
    - Hardware support for denormalized numbers
    - Thirty-two 64-bit FPRs for single- or double-precision operands

- Four vector units and 32-entry vector register file (VRs)
  - Vector permute unit (VPU)
  - Vector integer unit 1 (VIU1) handles short-latency AltiVec™ integer instructions, such as vector add instructions (for example, **vaddsbs**, **vaddshs**, and **vaddsws**).
  - Vector integer unit 2 (VIU2) handles longer-latency AltiVec integer instructions, such as vector multiply add instructions (for example, **vmhaddshs**, **vmhraddshs**, and **vmladduhm**).
  - Vector floating-point unit (VFPU)
- Three-stage load/store unit (LSU)
  - Supports integer, floating-point, and vector instruction load/store traffic
  - Four-entry vector touch queue (VTQ) supports all four architected AltiVec data stream operations
  - Three-cycle GPR and AltiVec load latency (byte, half word, word, vector) with one-cycle throughput
  - Four-cycle FPR load latency (single, double) with one-cycle throughput
  - No additional delay for misaligned access within double-word boundary
  - A dedicated adder calculates effective addresses (EAs).
  - Supports store gathering
  - Performs alignment, normalization, and precision conversion for floating-point data
  - Executes cache control and TLB instructions
  - Performs alignment, zero padding, and sign extension for integer data
  - Supports hits under misses (multiple outstanding misses)
  - Supports both big- and little-endian modes, including misaligned little-endian accesses

- Three issue queues, FIQ, VIQ, and GIQ, can accept as many as one, two, and three instructions, respectively, in a cycle. Instruction dispatch requires the following:
  - Instructions can only be dispatched from the three lowest IQ entries—IQ0, IQ1, and IQ2.
  - A maximum of three instructions can be dispatched to the issue queues per clock cycle.
  - Space must be available in the CQ for an instruction to dispatch (this includes instructions that are assigned a space in the CQ but not in an issue queue).
- Rename buffers
  - 16 GPR rename buffers
  - 16 FPR rename buffers
  - 16 VR rename buffers
- Dispatch unit
  - Decode/dispatch stage fully decodes each instruction
- Completion unit
  - Retires an instruction from the 16-entry completion queue (CQ) when all instructions ahead of it have been completed, the instruction has finished executing, and no exceptions are pending
  - Guarantees sequential programming model (precise exception model)

- Monitors all dispatched instructions and retires them in order
  - Tracks unresolved branches and flushes instructions after a mispredicted branch
  - Retires as many as three instructions per clock cycle
- Separate on-chip L1 instruction and data caches (Harvard architecture)
  - 32-Kbyte, eight-way set-associative instruction and data caches
  - Pseudo least-recently-used (PLRU) replacement algorithm
  - 32-byte (eight-word) L1 cache block
  - Physically indexed/physical tags
  - Cache write-back or write-through operation programmable on a per-page or per-block basis
  - Instruction cache can provide four instructions per clock cycle; data cache can provide four words per clock cycle
  - Caches can be disabled in software.
  - Caches can be locked in software.
  - MESI data cache coherency maintained in hardware
  - Separate copy of data cache tags for efficient snooping
  - Parity support on cache
  - No snooping of instruction cache except for **icbi** instruction
  - Data cache supports AltiVec LRU and transient instructions
  - Critical double- and/or quad-word forwarding is performed as needed. Critical quad-word forwarding is used for AltiVec loads and instruction fetches. Other accesses use critical double-word forwarding.
- Level 2 (L2) cache interface
  - On-chip, 1-Mbyte, eight-way set-associative unified instruction and data cache
  - Cache write-back or write-through operation programmable on a per-page or per-block basis
  - Parity support on cache tags
  - ECC or parity support on data
  - Error injection allows testing of error recovery software
- Separate memory management units (MMUs) for instructions and data
  - 52-bit virtual address, 32- or 36-bit physical address
  - Address translation for 4-Kbyte pages, variable-sized blocks, and 256-Mbyte segments
  - Memory programmable as write-back/write-through, caching-inhibited/caching-allowed, and memory coherency enforced/memory coherency not enforced on a page or block basis
  - Separate IBATs and DBATs (eight each) also defined as SPRs
  - Separate instruction and data translation lookaside buffers (TLBs)
    - Both TLBs are 128-entry, two-way set-associative and use an LRU replacement algorithm.
    - TLBs are hardware- or software-reloadable (that is, a page table search is performed in hardware or by system software on a TLB miss).

- Efficient data flow
  - — Although the VR/LSU interface is 128 bits, the L1/L2 bus interface allows up to 256 bits.
  - — The L1 data cache is fully pipelined to provide 128 bits/cycle to or from the VRs.
  - — The L2 cache is fully pipelined to provide 32 bytes per clock every other cycle to the L1 caches.
  - — As many as 16 out-of-order transactions can be present on the MPX bus.
  - — Store merging for multiple store misses to the same line. Only coherency action taken (address-only) for store misses merged to all 32 bytes of a cache block (no data tenure needed).
  - — Three-entry finished store queue and five-entry completed store queue between the LSU and the L1 data cache
  - — Separate additional queues for efficient buffering of outbound data (such as castouts and write-through stores) from the L1 data cache and L2 cache
- Multiprocessing support features include the following:
  - — Hardware-enforced, MESI cache coherency protocols for data cache
  - — Load/store with reservation instruction pair for atomic memory references, semaphores, and other multiprocessor operations
- Power and thermal management
  - — Dynamic frequency switching (DFS) feature allows processor core frequency to be halved or quartered through software to reduce power consumption.
  - — The following three power-saving modes are available to the system:
    - – Nap—Instruction fetching is halted. Only the clocks for the time base, decrementer, and JTAG logic remain running. The part goes into the doze state to snoop memory operations on the bus and then back to nap using a $\overline{\text{QREQ}}$/$\overline{\text{QACK}}$ processor-system handshake protocol.
    - – Sleep—Power consumption is further reduced by disabling bus snooping, leaving only the PLL in a locked and running state. All internal functional units are disabled.
    - – Deep sleep—When the part is in the sleep state, the system can disable the PLL. The system can then disable the SYSCLK source for greater system power savings. Power-on reset procedures for restarting and relocking the PLL must be followed upon exiting the deep sleep state.
  - — Instruction cache throttling provides control of instruction fetching to limit device temperature.
  - — A new temperature diode that can determine the temperature of the microprocessor
- Performance monitor can be used to help debug system designs and improve software efficiency.
- In-system testability and debugging features through JTAG boundary-scan capability
- Testability
  - — LSSD scan design
  - — IEEE Std. 1149.1™ JTAG interface

Table 4 provides the recommended operating conditions for the MPC7448 part numbers described by this document; see Section 11.1, “Part Numbers Fully Addressed by This Document,” for more information. See Section 9.2, “Power Supply Design and Sequencing” for power sequencing requirements.

Table 4. Recommended Operating Conditions[1]

Characteristic		Symbol	Recommended Value								Unit	Notes
			1000 MHz		1420 MHz		1600 MHz		1700 MHz			
			Min	Max	Min	Max	Min	Max	Min	Max		
Core supply voltage		V_{DD}	1.15 V ± 50 mV		1.2 V ± 50 mV		1.25 V ± 50 mV		1.3 V +20/ – 50 mV		V	3, 4, 5
PLL supply voltage		AV_{DD}	1.15 V ± 50 mV		1.2 V ± 50 mV		1.25 V ± 50 mV		1.3 V +20/ – 50 mV		V	2, 3, 4
Processor bus supply voltage	I/O Voltage Mode = 1.5 V	OV_{DD}	1.5 V ± 5%		1.5 V ± 5%		1.5 V ± 5%		1.5 V ± 5%		V	4
	I/O Voltage Mode = 1.8 V		1.8 V ± 5%		1.8 V ± 5%		1.8 V ± 5%		1.8 V ± 5%			4
	I/O Voltage Mode = 2.5 V		2.5 V ± 5%		2.5 V ± 5%		2.5 V ± 5%		2.5 V ± 5%			4
Input voltage	Processor bus	V_{in}	GND	OV_{DD}	GND	OV_{DD}	GND	OV_{DD}	GND	OV_{DD}	V	
	JTAG signals	V_{in}	GND	OV_{DD}	GND	OV_{DD}	GND	OV_{DD}	GND	OV_{DD}		
Die-junction temperature		T_j	0	105	0	105	0	105	0	105	•C	6

Notes:

1. These are the recommended and tested operating conditions.
2. This voltage is the input to the filter discussed in Section 9.2.2, “PLL Power Supply Filtering,” and not necessarily the voltage at the AV_{DD} pin, which may be reduced from V_{DD} by the filter.
3. Some early devices supported voltage and frequency derating whereby VDD (and AVDD) could be reduced to reduce power consumption. This feature has been superseded and is no longer supported. See Section 5.3, “Voltage and Frequency Derating,” for more information.
4. **Caution**: Power sequencing requirements must be met; see Section 9.2, “Power Supply Design and Sequencing”.
5. **Caution**: See Section 9.2.3, “Transient Specifications” for information regarding transients on this power supply.
6. For information on extended temperature devices, see Section 11.2, “Part Numbers Not Fully Addressed by This Document.”

Table 5 provides the package thermal characteristics for the MPC7448. For more information regarding thermal management, see Section 9.7, “Power and Thermal Management Information.”

Table 5. Package Thermal Characteristics[1]

Characteristic	Symbol	Value	Unit	Notes
Junction-to-ambient thermal resistance, natural convection, single-layer (1s) board	$R_{\theta JA}$	26	•C/W	2, 3
Junction-to-ambient thermal resistance, natural convection, four-layer (2s2p) board	$R_{\theta JMA}$	19	•C/W	2, 4
Junction-to-ambient thermal resistance, 200 ft/min airflow, single-layer (1s) board	$R_{\theta JMA}$	22	•C/W	2, 4
Junction-to-ambient thermal resistance, 200 ft/min airflow, four-layer (2s2p) board	$R_{\theta JMA}$	16	•C/W	2, 4
Junction-to-board thermal resistance	$R_{\theta JB}$	11	•C/W	5
Junction-to-case thermal resistance	$R_{\theta JC}$	< 0.1	•C/W	6

Notes:

1. Refer to Section 9.7, “Power and Thermal Management Information,” for details about thermal management.
2. Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, airflow, power dissipation of other components on the board, and board thermal resistance.
3. Per JEDEC JESD51-2 with the single-layer board horizontal
4. Per JEDEC JESD51-6 with the board horizontal
5. Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
6. This is the thermal resistance between die and case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the calculated case temperature. The actual value of $R_{\theta JC}$ for the part is less than 0.1°C/W.

Table 6 provides the DC electrical characteristics for the MPC7448.

Table 6. DC Electrical Specifications

At recommended operating conditions. See Table 4.

Characteristic	Nominal Bus Voltage[1]	Symbol	Min	Max	Unit	Notes
Input high voltage (all inputs)	1.5	V_{IH}	$OV_{DD} \times 0.65$	$OV_{DD} + 0.3$	V	2
	1.8		$OV_{DD} \times 0.65$	$OV_{DD} + 0.3$		
	2.5		1.7	$OV_{DD} + 0.3$		
Input low voltage (all inputs)	1.5	V_{IL}	–0.3	$OV_{DD} \times 0.35$	V	2
	1.8		–0.3	$OV_{DD} \times 0.35$		
	2.5		–0.3	0.7		
Input leakage current, all signals except BVSEL0, $\overline{\text{LSSD\_MODE}}$, $\overline{\text{TCK}}$, TDI, TMS, $\overline{\text{TRST}}$: $V_{in} = OV_{DD}$ $V_{in} = GND$	—	I_{in}	—	 50 – 50	μA	2, 3
Input leakage current, BVSEL0, $\overline{\text{LSSD\_MODE}}$, $\overline{\text{TCK}}$, TDI, TMS, $\overline{\text{TRST}}$: $V_{in} = OV_{DD}$ $V_{in} = GND$	—	I_{in}	—	 50 – 2000	μA	2, 6

Table 6. DC Electrical Specifications (continued)

At recommended operating conditions. See Table 4.

Characteristic		Nominal Bus Voltage [1]	Symbol	Min	Max	Unit	Notes
High-impedance (off-state) leakage current: $V_{in} = OV_{DD}$ $V_{in} = GND$		—	I_{TSI}	—	 50 – 50	μA	2, 3, 4
Output high voltage @ $I_{OH} = –5$ mA		1.5	V_{OH}	$OV_{DD} – 0.45$	—	V	
		1.8		$OV_{DD} – 0.45$	—		
		2.5		1.8	—		
Output low voltage @ $I_{OL} = 5$ mA		1.5	V_{OL}	—	0.45	V	
		1.8		—	0.45		
		2.5		—	0.6		
Capacitance, $V_{in} = 0$ V, f = 1 MHz	All inputs		C_{in}	—	8.0	pF	5

Notes:

1. Nominal voltages; see Table 4 for recommended operating conditions.
2. All I/O signals are referenced to OV_{DD}.
3. Excludes test signals and IEEE Std. 1149.1 boundary scan (JTAG) signals
4. The leakage is measured for nominal OV_{DD} and V_{DD}, or both OV_{DD} and V_{DD} must vary in the same direction (for example, both OV_{DD} and V_{DD} vary by either +5% or –5%).
5. Capacitance is periodically sampled rather than 100% tested.
6. These pins have internal pull-up resistors.

Table 7 provides the power consumption for the MPC7448 part numbers described by this document; see Section 11.1, "Part Numbers Fully Addressed by This Document," for information regarding which part numbers are described by this document. Freescale also offers MPC7448 part numbers that meet lower power consumption specifications by adhering to lower core voltage and core frequency specifications. For more information on these devices, including references to the MPC7448 Hardware Specification Addenda that describe these devices, see Section 11.2, "Part Numbers Not Fully Addressed by This Document."

The power consumptions provided in Table 7 represent the power consumption of each speed grade when operated at the rated maximum core frequency (see Table 8). Freescale sorts devices by power as well as by core frequency, and power limits for each speed grade are independent of each other. Each device is tested at its maximum core frequency only. (Note that Deep Sleep Mode power consumption is independent of clock frequency.) Operating a device at a frequency lower than its rated maximum is fully supported provided the clock frequencies are within the specifications given in Table 8, and a device operated below its rated maximum will have lower power consumption. However, inferences should not be made about a device's power consumption based on the power specifications of another (lower) speed grade. For example, a 1700 MHz device operated at 1420 MHz may not exhibit the same power consumption as a 1420 MHz device operated at 1420 MHz.

For all MPC7448 devices, the following guidelines on the use of these parameters for system design are suggested. The Full-Power Mode–Typical value represents the sustained power consumption of the device

Figure 4 provides the AC test load for the MPC7448.

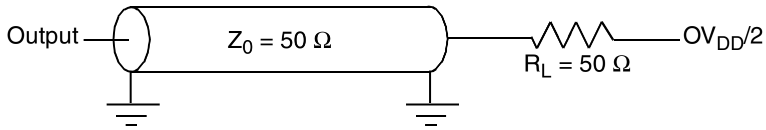


Figure 4. AC Test Load

Figure 5 provides the $\overline{\text{BMODE}}$[0:1] input timing diagram for the MPC7448. These mode select inputs are sampled once before and once after $\overline{\text{HRESET}}$ negation.

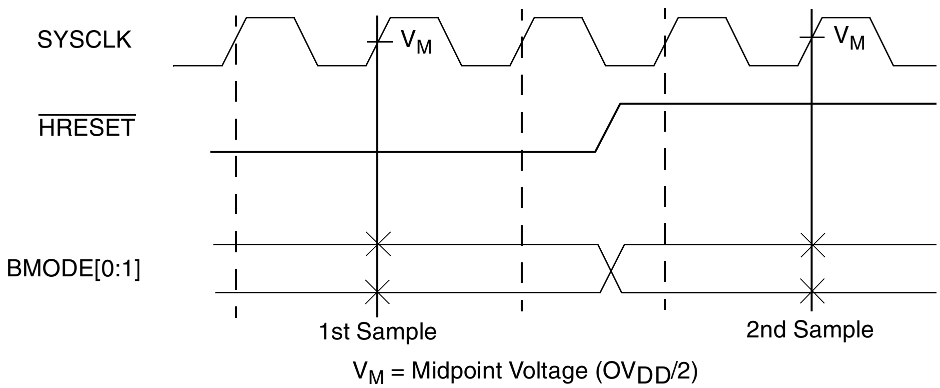


Figure 5. $\overline{\text{BMODE}}$[0:1] Input Sample Timing Diagram

Figure 11 provides the test access port timing diagram.

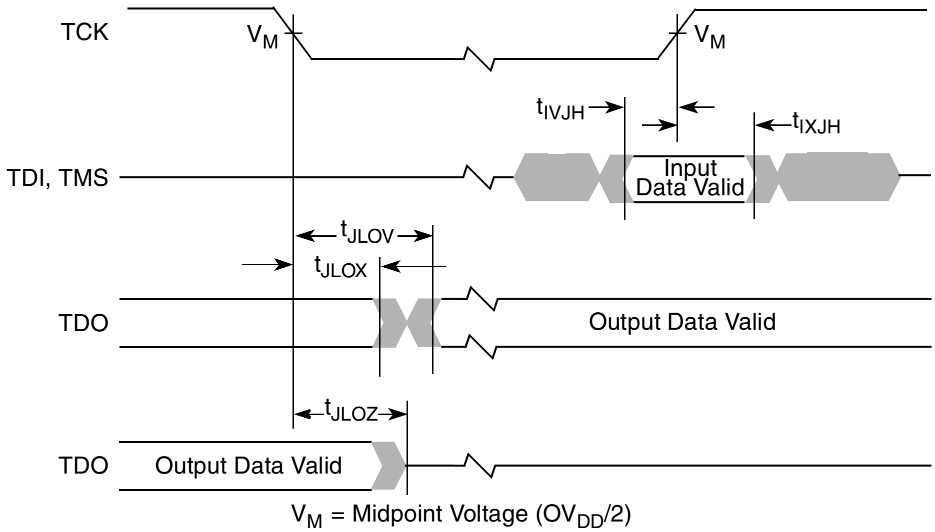


Figure 11. Test Access Port Timing Diagram

5.3 Voltage and Frequency Derating

Voltage and frequency derating is no longer supported for part numbers described by this document beginning with datecode 0613. (See Section 11, "Part Numbering and Marking," for information on date code markings.) It is supported by some MPC7448 part numbers which target low-power applications; see Section 11.2, "Part Numbers Not Fully Addressed by This Document" and the referenced MPC7448 Hardware Specification Addenda for more information on these low-power devices. For those devices which previously supported this feature, information has been archived in the *Chip Errata for the MPC7448* (document order no. MPC7448CE).

7 Pinout Listings

Table 11 provides the pinout listing for the MPC7448, 360 HCTE package. The pinouts of the MPC7448 and MPC7447A are compatible, but the requirements regarding the use of the additional power and ground pins have changed. The MPC7448 requires these pins be connected to the appropriate power or ground plane to achieve high core frequencies; see Section 9.3, "Connection Recommendations," for additional information. As a result, these pins should be connected in all new designs.

Additionally, the MPC7448 may be populated on a board designed for a MPC7447 (or MPC7445 or MPC7441), provided the core voltage can be made to match the requirements in Table 4 and all pins defined as 'no connect' for the MPC7447 are unterminated, as required by the *MPC7457 RISC Microprocessor Hardware Specifications*. The MPC7448 uses pins previously marked 'no connect' for the temperature diode pins and for additional power and ground connections. The additional power and ground pins are required to achieve high core frequencies and core frequency will be limited if they are not connected; see Section 9.3, "Connection Recommendations," for additional information. Because these 'no connect' pins in the MPC7447 360 pin package are not driven in functional mode, an MPC7447 can be populated in an MPC7448 board.

NOTE

Caution must be exercised when performing boundary scan test operations on a board designed for an MPC7448, but populated with an MPC7447 or earlier device. This is because in the MPC7447 it is possible to drive the latches associated with the former 'no connect' pins in the MPC7447, potentially causing contention on those pins. To prevent this, ensure that these pins are not connected on the board or, if they are connected, ensure that the states of internal MPC7447 latches do not cause these pins to be driven during board testing.

For the MPC7448, pins that were defined as the TEST[0:4] factory test signal group on the MPC7447A and earlier devices have been assigned new functions. For most of these, the termination recommendations for the TEST[0:4] pins of the MPC7447A are compatible with the MPC7448 and will allow correct operation with no performance loss. The exception is BVSEL1 (TEST3 on the MPC7447A and earlier devices), which may require a different termination depending which I/O voltage mode is desired; see Table 3 for more information.

NOTE

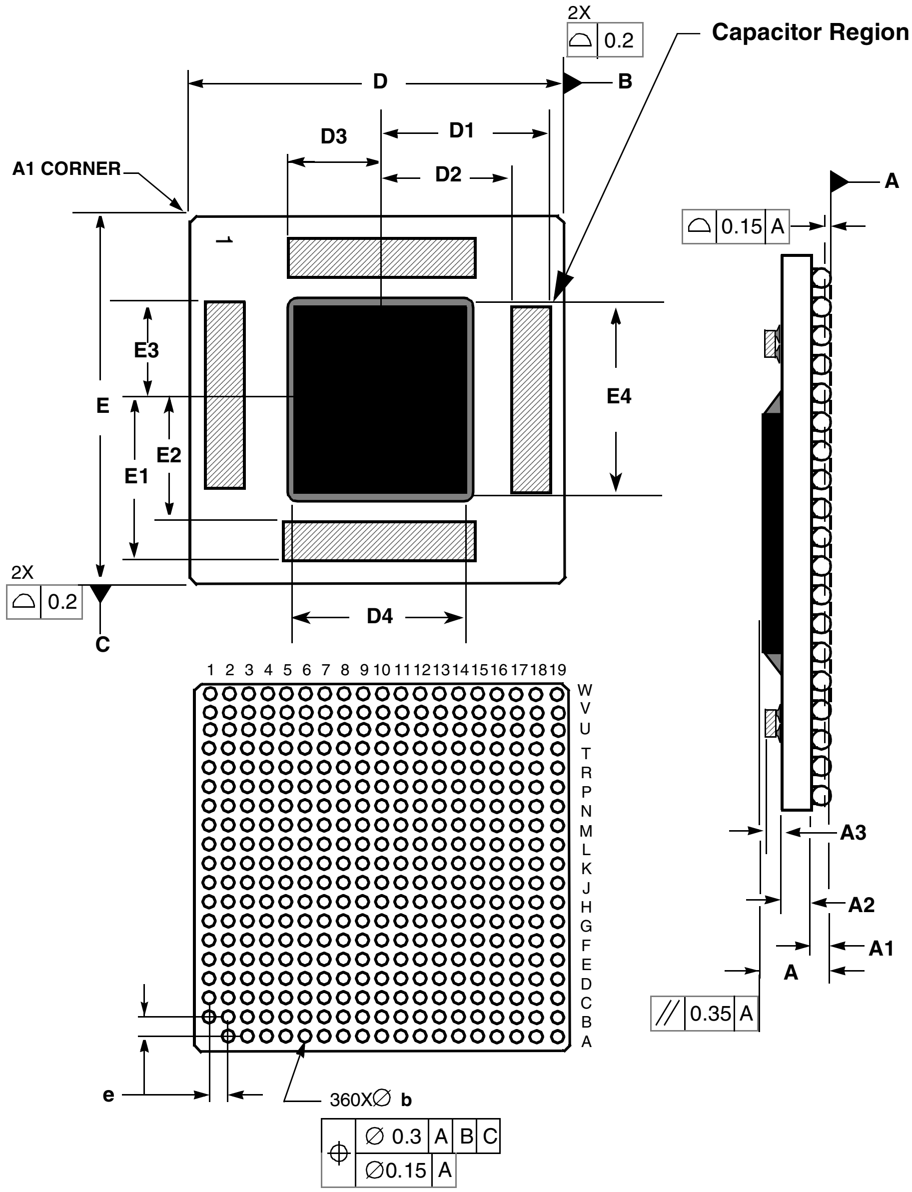
This pinout is not compatible with the MPC750, MPC7400, or MPC7410 360 BGA package.

Table 11. Pinout Listing for the MPC7448, 360 HCTE Package

Signal Name	Pin Number	Active	I/O	Notes
A[0:35]	E11, H1, C11, G3, F10, L2, D11, D1, C10, G2, D12, L3, G4, T2, F4, V1, J4, R2, K5, W2, J2, K4, N4, J3, M5, P5, N3, T1, V2, U1, N5, W1, B12, C4, G10, B11	High	I/O	2
$\overline{\text{AACK}}$	R1	Low	Input	
AP[0:4]	C1, E3, H6, F5, G7	High	I/O	2
$\overline{\text{ARTRY}}$	N2	Low	I/O	3
AV_{DD}	A8	—	Input	
$\overline{\text{BG}}$	M1	Low	Input	
$\overline{\text{BMODE0}}$	G9	Low	Input	4
$\overline{\text{BMODE1}}$	F8	Low	Input	5
$\overline{\text{BR}}$	D2	Low	Output	
BVSEL0	B7	High	Input	1, 6
BVSEL1	E10	High	Input	1, 20
$\overline{\text{CI}}$	J1	Low	Output	
$\overline{\text{CKSTP\_IN}}$	A3	Low	Input	
$\overline{\text{CKSTP\_OUT}}$	B1	Low	Output	
CLK_OUT	H2	High	Output	
D[0:63]	R15, W15, T14, V16, W16, T15, U15, P14, V13, W13, T13, P13, U14, W14, R12, T12, W12, V12, N11, N10, R11, U11, W11, T11, R10, N9, P10, U10, R9, W10, U9, V9, W5, U6, T5, U5, W7, R6, P7, V6, P17, R19, V18, R18, V19, T19, U19, W19, U18, W17, W18, T16, T18, T17, W3, V17, U4, U8, U7, R7, P6, R8, W8, T8	High	I/O	
$\overline{\text{DBG}}$	M2	Low	Input	
$\overline{\text{DFS2}}$	A12	Low	Input	20, 21
$\overline{\text{DFS4}}$	B6	Low	Input	12, 20, 21
DP[0:7]	T3, W4, T4, W9, M6, V3, N8, W6	High	I/O	
$\overline{\text{DRDY}}$	R3	Low	Output	7
DTI[0:3]	G1, K1, P1, N1	High	Input	8
EXT_QUAL	A11	High	Input	9
$\overline{\text{GBL}}$	E2	Low	I/O	
GND	B5, C3, D6, D13, E17, F3, G17, H4, H7, H9, H11, H13, J6, J8, J10, J12, K7, K3, K9, K11, K13, L6, L8, L10, L12, M4, M7, M9, M11, M13, N7, P3, P9, P12, R5, R14, R17, T7, T10, U3, U13, U17, V5, V8, V11, V15	—	—	
GND	A17, A19, B13, B16, B18, E12, E19, F13, F16, F18, G19, H18, J14, L14, M15, M17, M19, N14, N16, P15, P19	—	—	15
GND_SENSE	G12, N13	—	—	19
$\overline{\text{HIT}}$	B2	Low	Output	7
$\overline{\text{HRESET}}$	D8	Low	Input	
$\overline{\text{INT}}$	D4	Low	Input	
L1_TSTCLK	G8	High	Input	9
L2_TSTCLK	B3	High	Input	10

8.2 Mechanical Dimensions for the MPC7448, 360 HCTE BGA

Figure 13 provides the mechanical dimensions and bottom surface nomenclature for the MPC7448, 360 HCTE BGA package.



NOTES:
1. Dimensioning and tolerancing per ASME Y14.5M, 1994
2. Dimensions in millimeters.
3. Top side A1 corner index is a metalized feature with various shapes. Bottom side A1 corner is designated with a ball missing from the array.

	Millimeters	
Dim	Min	Max
A	2.32	2.80
A1	0.80	1.00
A2	0.70	0.90
A3	—	0.6
b	0.82	0.93
D	25.00 BSC	
D1	—	11.3
D2	8.0	—
D3	—	6.5
D4	7.2	7.4
e	1.27 BSC	
E	25.00 BSC	
E1	—	11.3
E2	8.0	—
E3	—	6.5
E4	7.9	8.1

Figure 13. Mechanical Dimensions and Bottom Surface Nomenclature for the MPC7448, 360 HCTE BGA Package

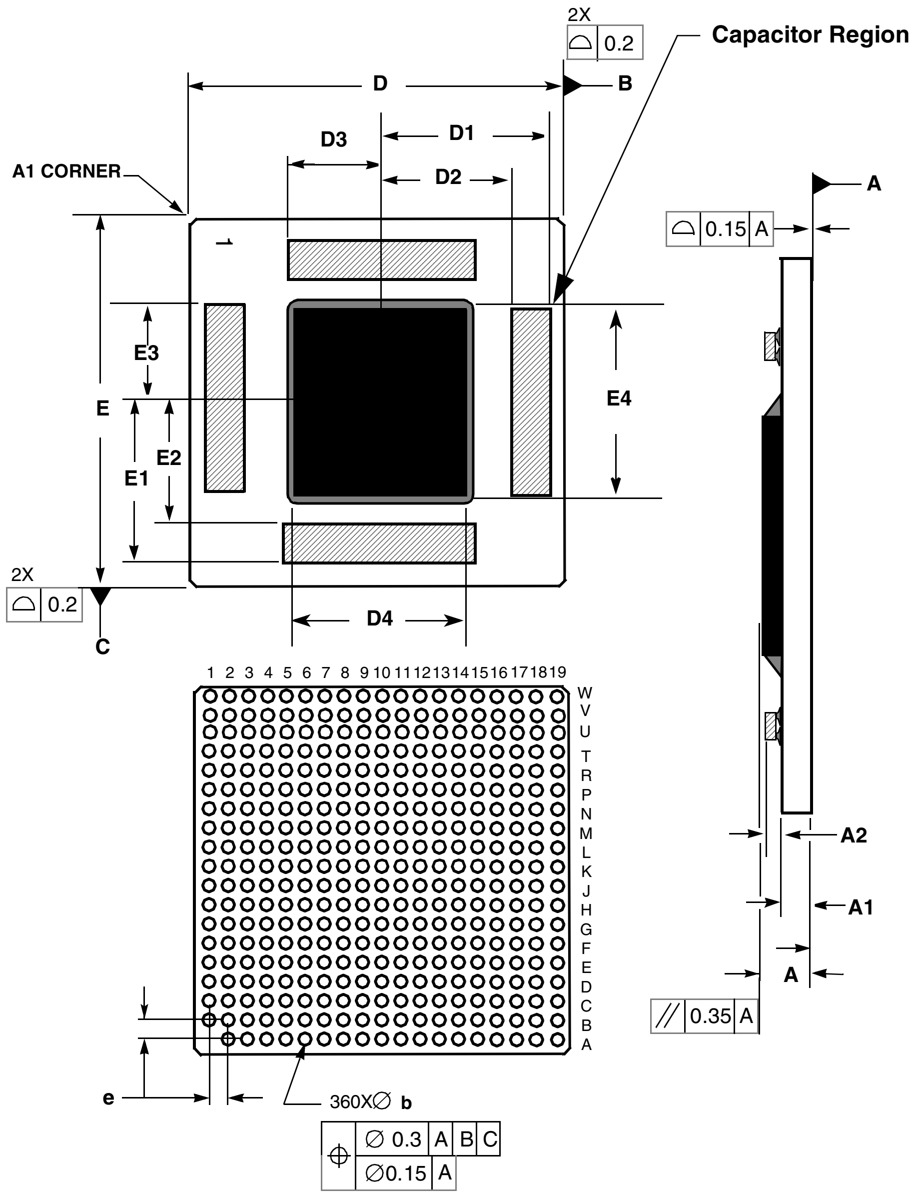
8.3 Package Parameters for the MPC7448, 360 HCTE LGA

The package parameters are as provided in the following list. The package type is 25 × 25 mm, 360 pin high coefficient of thermal expansion ceramic land grid array (HCTE).

Package outline	25 × 25 mm
Interconnects	360 (19 × 19 ball array – 1)
Pitch	1.27 mm (50 mil)
Minimum module height	1.52 mm
Maximum module height	1.80 mm
Pad diameter	0.89 mm (35 mil)
Coefficient of thermal expansion	12.3 ppm/°C

8.4 Mechanical Dimensions for the MPC7448, 360 HCTE LGA

Figure 13 provides the mechanical dimensions and bottom surface nomenclature for the MPC7448, 360 HCTE LGA package.



NOTES:
1. Dimensioning and tolerancing per ASME Y14.5M, 1994
2. Dimensions in millimeters
3. Top side A1 corner index is a metalized feature with various shapes. Bottom side A1 corner is designated with a pad missing from the array.

	Millimeters	
Dim	**Min**	**Max**
A	1.52	1.80
A1	0.70	0.90
A2	—	0.6
b	0.82	0.93
D	25.00 BSC	
D1	—	11.3
D2	8.0	—
D3	—	6.5
D4	7.2	7.4
e	1.27 BSC	
E	25.00 BSC	
E1	—	11.3
E2	8.0	—
E3	—	6.5
E4	7.9	8.1

Figure 14. Mechanical Dimensions and Bottom Surface Nomenclature for the MPC7448, 360 HCTE LGA Package

9 System Design Information

This section provides system and thermal design requirements and recommendations for successful application of the MPC7448.

9.1 Clocks

The following sections provide more detailed information regarding the clocking of the MPC7448.

9.1.1 PLL Configuration

The MPC7448 PLL is configured by the PLL_CFG[0:5] signals. For a given SYSCLK (bus) frequency, the PLL configuration signals set the internal CPU and VCO frequency of operation. The PLL configuration for the MPC7448 is shown in Table 12. In this example, shaded cells represent settings that, for a given SYSCLK frequency, result in core and/or VCO frequencies that do not comply with Table 8. When enabled, dynamic frequency switching (DFS) also affects the core frequency by halving or quartering the bus-to-core multiplier; see Section 9.7.5, "Dynamic Frequency Switching (DFS)," for more information. Note that when DFS is enabled the resulting core frequency must meet the adjusted minimum core frequency requirements (f_{core_DFS}) described in Table 8. Note that the PLL_CFG[5] is currently used for factory test only and should be tied low, and that the MPC7448 PLL configuration settings are compatible with the MPC7447A PLL configuration settings when PLL_CFG[5] = 0.

Table 12. MPC7448 Microprocessor PLL Configuration Example

PLL_CFG[0:5]	Example Core and VCO Frequency in MHz										
	Bus-to-Core Multiplier [5]	Core-to-VCO Multiplier [5]	Bus (SYSCLK) Frequency								
			33.3 MHz	50 MHz	66.6 MHz	75 MHz	83 MHz	100 MHz	133 MHz	167 MHz	200 MHz
010000	2x [6]	1x									
100000	3x [6]	1x									600
101000	4x [6]	1x								667	800
101100	5x	1x							667	835	1000
100100	5.5x	1x							733	919	1100
110100	6x	1x						600	800	1002	1200
010100	6.5x	1x						650	866	1086	1300
001000	7x	1x						700	931	1169	1400
000100	7.5x	1x					623	750	1000	1253	1500
110000	8x	1x				600	664	800	1064	1336	1600
011000	8.5x	1x				638	706	850	1131	1417	1700
011110	9x	1x			600	675	747	900	1197	1500	
011100	9.5x	1x			633	712	789	950	1264	1583	
101010	10x	1x			667	750	830	1000	1333	1667	
100010	10.5x	1x			700	938	872	1050	1397		

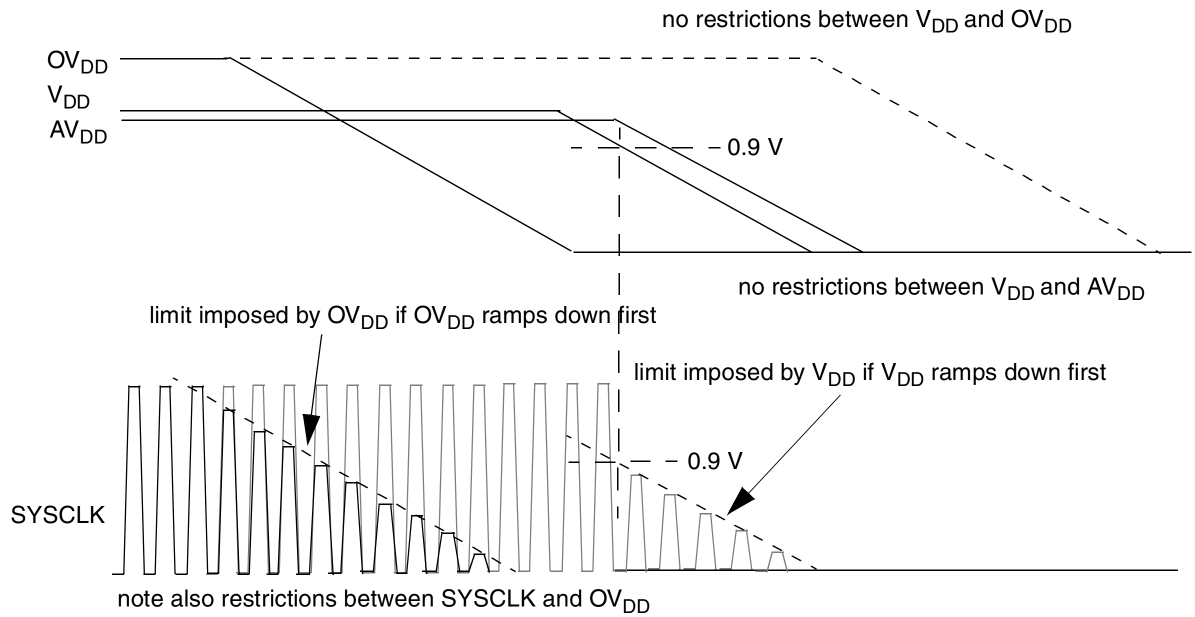


Figure 17. MPC7448 Power Down Sequencing Requirements

There is no requirement regarding AV_{DD} during power down, but it is recommended that AV_{DD} track V_{DD} within the RC time constant of the PLL filter circuit described in Section 9.2.2, "PLL Power Supply Filtering" (nominally 100 µs).

9.2.2 PLL Power Supply Filtering

The AV_{DD} power signal is provided on the MPC7448 to provide power to the clock generation PLL. To ensure stability of the internal clock, the power supplied to the AV_{DD} input signal should be filtered of any noise in the 500-KHz to 10-MHz resonant frequency range of the PLL. The circuit shown in Figure 18 using surface mount capacitors with minimum effective series inductance (ESL) is strongly recommended. In addition to filtering noise from the AV_{DD} input, it also provides the required delay between V_{DD} and AV_{DD} as described in Section 9.2.1, "Power Supply Sequencing."

The circuit should be placed as close as possible to the AV_{DD} pin to minimize noise coupled from nearby circuits. It is often possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of the device footprint.

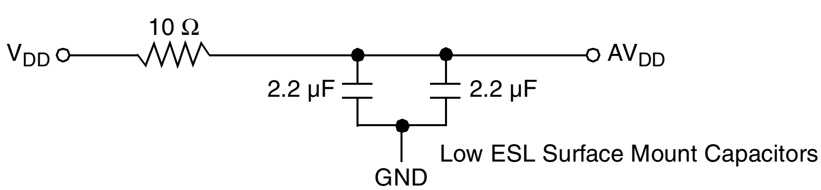


Figure 18. PLL Power Supply Filter Circuit

9.4 Output Buffer DC Impedance

The MPC7448 processor bus drivers are characterized over process, voltage, and temperature. To measure Z_0, an external resistor is connected from the chip pad to OV_{DD} or GND. The value of each resistor is varied until the pad voltage is $OV_{DD}/2$. Figure 20 shows the driver impedance measurement.

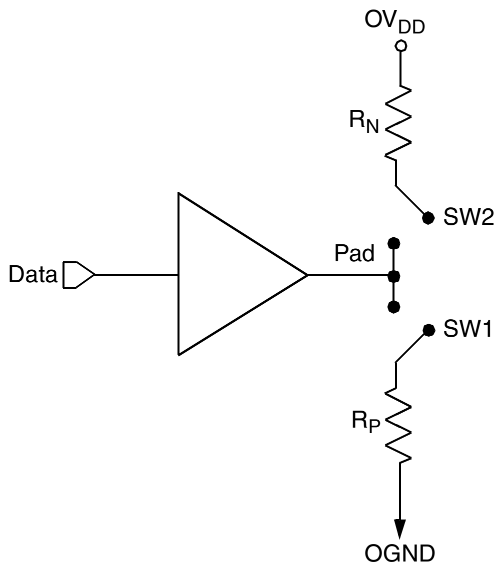


Figure 20. Driver Impedance Measurement

The output impedance is the average of two components—the resistances of the pull-up and pull-down devices. When data is held low, SW2 is closed (SW1 is open), and R_N is trimmed until the voltage at the pad equals $OV_{DD}/2$. R_N then becomes the resistance of the pull-down devices. When data is held high, SW1 is closed (SW2 is open), and R_P is trimmed until the voltage at the pad equals $OV_{DD}/2$. R_P then becomes the resistance of the pull-up devices. R_P and R_N are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N)/2$.

Table 15 summarizes the signal impedance results. The impedance increases with junction temperature and is relatively unaffected by bus voltage.

Table 15. Impedance Characteristics

At recommended operating conditions. See Table 4

Impedance		Processor Bus	Unit
Z_0	Typical	33–42	Ω
	Maximum	31–51	Ω

9.5 Pull-Up/Pull-Down Resistor Requirements

The MPC7448 requires high-resistive (weak: 4.7-KΩ) pull-up resistors on several control pins of the bus interface to maintain the control signals in the negated state after they have been actively negated and released by the MPC7448 or other bus masters. These pins are: $\overline{\text{TS}}$, $\overline{\text{ARTRY}}$, $\overline{\text{SHDO}}$, and $\overline{\text{SHD1}}$.

Some pins designated as being factory test pins must be pulled up to OV_{DD} or down to GND to ensure proper device operation. The pins that must be pulled up to OV_{DD} are $\overline{\text{LSSD\_MODE}}$ and TEST[0:3]; the pins that must be pulled down to GND are L1_TSTCLK and TEST[4]. The $\overline{\text{CKSTP\_IN}}$ signal should to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must be merged into these signals with logic.

The arrangement shown in Figure 21 allows the COP port to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$, while ensuring that the target can drive $\overline{\text{HRESET}}$ as well. If the JTAG interface and COP header will not be used, $\overline{\text{TRST}}$ should be tied to $\overline{\text{HRESET}}$ through a 0-Ω isolation resistor so that it is asserted when the system reset signal ($\overline{\text{HRESET}}$) is asserted, ensuring that the JTAG scan chain is initialized during power-on. Although Freescale recommends that the COP header be designed into the system as shown in Figure 21, if this is not possible, the isolation resistor will allow future access to $\overline{\text{TRST}}$ in the case where a JTAG interface may need to be wired onto the system in debug situations.

The COP header shown in Figure 21 adds many benefits—breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features are possible through this interface—and can be as inexpensive as an unpopulated footprint for a header to be added when needed.

The COP interface has a standard header for connection to the target system, based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header). The connector typically has pin 14 removed as a connector key.

There is no standardized way to number the COP header shown in Figure 21; consequently, many different pin numbers have been observed from emulator vendors. Some are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom, while still others number the pins counter clockwise from pin 1 (as with an IC). Regardless of the numbering, the signal placement recommended in Figure 21 is common to all known emulators.

The $\overline{\text{QACK}}$ signal shown in Figure 21 is usually connected to the bridge chip or other system control logic in a system and is an input to the MPC7448 informing it that it can go into the quiescent state. Under normal operation this occurs during a low-power mode selection. In order for COP to work, the MPC7448 must see this signal asserted (pulled down). While shown on the COP header, not all emulator products drive this signal. If the product does not, a pull-down resistor can be populated to assert this signal. Additionally, some emulator products implement open-drain type outputs and can only drive $\overline{\text{QACK}}$ asserted; for these tools, a pull-up resistor can be implemented to ensure this signal is negated when it is not being driven by the tool. Note that the pull-up and pull-down resistors on the $\overline{\text{QACK}}$ signal are mutually exclusive and it is never necessary to populate both in a system. To preserve correct power-down operation, $\overline{\text{QACK}}$ should be merged through logic so that it also can be driven by the bridge or system logic.

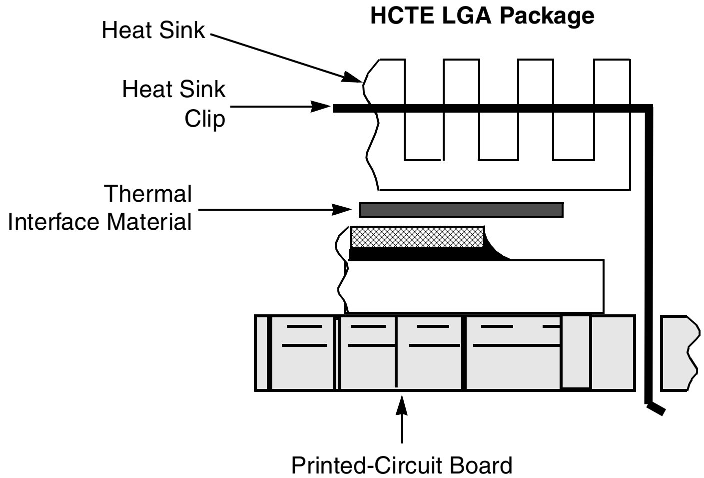


Figure 23. LGA Package Exploded Cross-Sectional View with Several Heat Sink Options

There are several commercially-available heat sinks for the MPC7448 provided by the following vendors:

Aavid Thermalloy 80 Commercial St. Concord, NH 03301 Internet: www.aavidthermalloy.com	603-224-9988
Alpha Novatech 473 Sapena Ct. #12 Santa Clara, CA 95054 Internet: www.alphanovatech.com	408-567-8082
Calgreg Thermal Solutions 60 Alhambra Road, Suite 1 Warwick, RI 02886 Internet: www.calgregthermalsolutions.com	888-732-6100
International Electronic Research Corporation (IERC) 413 North Moss St. Burbank, CA 91502 Internet: www.ctscorp.com	818-842-7277
Tyco Electronics Chip Coolers™ P.O. Box 3668 Harrisburg, PA 17105-3668 Internet: www.tycoelectronics.com	800-522-6752
Wakefield Engineering 33 Bridge St. Pelham, NH 03076 Internet: www.wakefield.com	603-635-2800

Ultimately, the final selection of an appropriate heat sink depends on many factors, such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost.

9.7.4 Temperature Diode

The MPC7448 has a temperature diode on the microprocessor that can be used in conjunction with other system temperature monitoring devices (such as Analog Devices, ADT7461™). These devices use the negative temperature coefficient of a diode operated at a constant current to determine the temperature of the microprocessor and its environment. For proper operation, the monitoring device used should auto-calibrate the device by canceling out the V_{BE} variation of each MPC7448's internal diode.

The following are the specifications of the MPC7448 on-board temperature diode:

$V_f > 0.40$ V

$V_f < 0.90$ V

Operating range 2–300 µA

Diode leakage < 10 nA @ 125°C

Ideality factor over 5–150 µA at 60°C: n = 1.0275 ± 0.9%

Ideality factor is defined as the deviation from the ideal diode equation:

$$I_{fw} = I_s \left[e^{\frac{qV_f}{nKT}} - 1 \right]$$

Another useful equation is:

$$V_H - V_L = n\frac{KT}{q}\left[\ln\frac{I_H}{I_L} \right] - 1$$

Where:

- I_{fw} = Forward current
- I_s = Saturation current
- V_d = Voltage at diode
- V_f = Voltage forward biased
- V_H = Diode voltage while I_H is flowing
- V_L = Diode voltage while I_L is flowing
- I_H = Larger diode bias current
- I_L = Smaller diode bias current
- q = Charge of electron (1.6×10^{-19} C)
- n = Ideality factor (normally 1.0)
- K = Boltzman's constant (1.38×10^{-23} Joules/K)
- T = Temperature (Kelvins)

The ratio of I_H to I_L is usually selected to be 10:1. The previous equation simplifies to the following:

$$V_H - V_L = 1.986 \times 10^{-4} \times nT$$