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Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC G4
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	667MHz
Co-Processors/DSP	Multimedia; SIMD
RAM Controllers	-
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	1.5V, 1.8V, 2.5V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	360-CBGA, FCCBGA
Supplier Device Package	360-FCCBGA (25x25)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc7448vu667nc

Table 6. DC Electrical Specifications (continued)

 At recommended operating conditions. See [Table 4](#).

Characteristic		Nominal Bus Voltage ¹	Symbol	Min	Max	Unit	Notes
High-impedance (off-state) leakage current: $V_{in} = OV_{DD}$ $V_{in} = GND$		—	I_{TSI}	—	50 – 50	μA	2, 3, 4
Output high voltage @ $I_{OH} = -5$ mA		1.5	V_{OH}	$OV_{DD} - 0.45$	—	V	
		1.8		$OV_{DD} - 0.45$	—		
		2.5		1.8	—		
Output low voltage @ $I_{OL} = 5$ mA		1.5	V_{OL}	—	0.45	V	
		1.8		—	0.45		
		2.5		—	0.6		
Capacitance, $V_{in} = 0$ V, $f = 1$ MHz	All inputs		C_{in}	—	8.0	pF	5

Notes:

1. Nominal voltages; see [Table 4](#) for recommended operating conditions.
2. All I/O signals are referenced to OV_{DD} .
3. Excludes test signals and IEEE Std. 1149.1 boundary scan (JTAG) signals
4. The leakage is measured for nominal OV_{DD} and V_{DD} , or both OV_{DD} and V_{DD} must vary in the same direction (for example, both OV_{DD} and V_{DD} vary by either +5% or –5%).
5. Capacitance is periodically sampled rather than 100% tested.
6. These pins have internal pull-up resistors.

[Table 7](#) provides the power consumption for the MPC7448 part numbers described by this document; see [Section 11.1, “Part Numbers Fully Addressed by This Document,”](#) for information regarding which part numbers are described by this document. Freescale also offers MPC7448 part numbers that meet lower power consumption specifications by adhering to lower core voltage and core frequency specifications. For more information on these devices, including references to the MPC7448 Hardware Specification Addenda that describe these devices, see [Section 11.2, “Part Numbers Not Fully Addressed by This Document.”](#)

The power consumptions provided in [Table 7](#) represent the power consumption of each speed grade when operated at the rated maximum core frequency (see [Table 8](#)). Freescale sorts devices by power as well as by core frequency, and power limits for each speed grade are independent of each other. Each device is tested at its maximum core frequency only. (Note that Deep Sleep Mode power consumption is independent of clock frequency.) Operating a device at a frequency lower than its rated maximum is fully supported provided the clock frequencies are within the specifications given in [Table 8](#), and a device operated below its rated maximum will have lower power consumption. However, inferences should not be made about a device’s power consumption based on the power specifications of another (lower) speed grade. For example, a 1700 MHz device operated at 1420 MHz may not exhibit the same power consumption as a 1420 MHz device operated at 1420 MHz.

For all MPC7448 devices, the following guidelines on the use of these parameters for system design are suggested. The Full-Power Mode–Typical value represents the sustained power consumption of the device

when running a typical benchmark at temperatures in a typical system. The Full-Power Mode–Thermal value is intended to represent the sustained power consumption of the device when running a typical code sequence at high temperature and is recommended to be used as the basis for designing a thermal solution; see [Section 9.7, “Power and Thermal Management Information”](#) for more information on thermal solutions. The Full-Power Mode–Maximum value is recommended to be used for power supply design because this represents the maximum peak power draw of the device that a power supply must be capable of sourcing without voltage droop. For information on power consumption when dynamic frequency switching is enabled, see [Section 9.7.5, “Dynamic Frequency Switching \(DFS\)”](#).

Table 7. Power Consumption for MPC7448 at Maximum Rated Frequency

	Die Junction Temperature (T _j)	Maximum Processor Core Frequency (Speed Grade, MHz)				Unit	Notes
		1000 MHz	1420 MHz	1600 MHz	1700 MHz		
Full-Power Mode							
Typical	65 °C	15.0	19.0	20.0	21.0	W	1, 2
Thermal	105 °C	18.6	23.3	24.4	25.6	W	1, 5
Maximum	105 °C	21.6	27.1	28.4	29.8	W	1, 3
Nap Mode							
Typical	105 °C	11.1	11.8	13.0	13.0	W	1, 6
Sleep Mode							
Typical	105 °C	10.8	11.4	12.5	12.5	W	1, 6
Deep Sleep Mode (PLL Disabled)							
Typical	105 °C	10.4	11.0	12.0	12.0	W	1, 6

Notes:

1. These values specify the power consumption for the core power supply (V_{DD}) at nominal voltage and apply to all valid processor bus frequencies and configurations. The values do not include I/O supply power (OV_{DD}) or PLL supply power (AV_{DD}). OV_{DD} power is system dependent but is typically < 5% of V_{DD} power. Worst case power consumption for AV_{DD} < 13 mW. Freescale also offers MPC7448 part numbers that meet lower power consumption specifications; for more information on these devices, see [Section 11.2, “Part Numbers Not Fully Addressed by This Document.”](#)
2. Typical power consumption is an average value measured with the processor operating at its rated maximum processor core frequency (except for Deep Sleep Mode), at nominal recommended V_{DD} (see [Table 4](#)) and 65°C while running the Dhrystone 2.1 benchmark and achieving 2.3 Dhrystone MIPs/MHz. This parameter is not 100% tested but periodically sampled.
3. Maximum power consumption is the average measured with the processor operating at its rated maximum processor core frequency, at nominal V_{DD} and maximum operating junction temperature (see [Table 4](#)) while running an entirely cache-resident, contrived sequence of instructions to keep all the execution units maximally busy.
4. Doze mode is not a user-definable state; it is an intermediate state between full-power and either nap or sleep mode. As a result, power consumption for this mode is not tested.
5. Thermal power consumption is an average value measured at the nominal recommended V_{DD} (see [Table 4](#)) and 105 °C while running the Dhrystone 2.1 benchmark and achieving 2.3 Dhrystone MIPs/MHz. This parameter is not 100% tested but periodically sampled.
6. Typical power consumption for these modes is measured at the nominal recommended V_{DD} (see [Table 4](#)) and 105 °C in the mode described. This parameter is not 100% tested but is periodically sampled.

Table 9. Processor Bus AC Timing Specifications¹ (continued)

At recommended operating conditions. See [Table 4](#).

Parameter	Symbol ²	All Speed Grades		Unit	Notes
		Min	Max		
SYSClk to output high impedance (all except \overline{TS} , \overline{ARTRY} , $\overline{SHD0}$, $\overline{SHD1}$)	t_{KHOZ}	—	1.8	ns	5
SYSClk to \overline{TS} high impedance after precharge	t_{KHTSPZ}	—	1	t_{SYSClk}	3, 4, 5
Maximum delay to $\overline{ARTRY}/\overline{SHD0}/\overline{SHD1}$ precharge	t_{KHARP}	—	1	t_{SYSClk}	3, 5, 6, 7
SYSClk to $\overline{ARTRY}/\overline{SHD0}/\overline{SHD1}$ high impedance after precharge	t_{KHARPZ}	—	2	t_{SYSClk}	3, 5, 6, 7

Notes:

- All input specifications are measured from the midpoint of the signal in question to the midpoint of the rising edge of the input SYSClk. All output specifications are measured from the midpoint of the rising edge of SYSClk to the midpoint of the signal in question. All output timings assume a purely resistive 50-Ω load (see [Figure 4](#)). Input and output timings are measured at the pin; time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
- The symbology used for timing specifications herein follows the pattern of $t_{(signal)(state)(reference)(state)}$ for inputs and $t_{(reference)(state)(signal)(state)}$ for outputs. For example, t_{VKH} symbolizes the time input signals (I) reach the valid state (V) relative to the SYSClk reference (K) going to the high (H) state or input setup time. And t_{KHOV} symbolizes the time from SYSClk(K) going high (H) until outputs (O) are valid (V) or output valid time. Input hold time can be read as the time that the input signal (I) went invalid (X) with respect to the rising clock edge (KH) (note the position of the reference and its state for inputs) and output hold time can be read as the time from the rising edge (KH) until the output went invalid (OX).
- t_{SYSClk} is the period of the external clock (SYSClk) in ns. The numbers given in the table must be multiplied by the period of SYSClk to compute the actual time duration (in ns) of the parameter in question.
- According to the bus protocol, \overline{TS} is driven only by the currently active bus master. It is asserted low and precharged high before returning to high impedance, as shown in [Figure 6](#). The nominal precharge width for \overline{TS} is t_{SYSClk} , that is, one clock period. Since no master can assert \overline{TS} on the following clock edge, there is no concern regarding contention with the precharge. Output valid and output hold timing is tested for the signal asserted. Output valid time is tested for precharge. The high-impedance behavior is guaranteed by design.
- Guaranteed by design and not tested
- According to the bus protocol, \overline{ARTRY} can be driven by multiple bus masters through the clock period immediately following \overline{AACK} . Bus contention is not an issue because any master asserting \overline{ARTRY} will be driving it low. Any master asserting it low in the first clock following \overline{AACK} will then go to high impedance for a fraction of a cycle, then negated for up to an entire cycle (crossing a bus cycle boundary) before being three-stated again. The nominal precharge width for \overline{ARTRY} is $1.0 t_{SYSClk}$; that is, it should be high impedance as shown in [Figure 6](#) before the first opportunity for another master to assert \overline{ARTRY} . Output valid and output hold timing is tested for the signal asserted. The high-impedance behavior is guaranteed by design.
- According to the MPX bus protocol, $\overline{SHD0}$ and $\overline{SHD1}$ can be driven by multiple bus masters beginning two cycles after \overline{TS} . Timing is the same as \overline{ARTRY} , that is, the signal is high impedance for a fraction of a cycle, then negated for up to an entire cycle (crossing a bus cycle boundary) before being three-stated again. The nominal precharge width for $\overline{SHD0}$ and $\overline{SHD1}$ is $1.0 t_{SYSClk}$. The edges of the precharge vary depending on the programmed ratio of core to bus (PLL configurations).
- $\overline{BMODE}[0:1]$ and $BVSEL[0:1]$ are mode select inputs. $\overline{BMODE}[0:1]$ are sampled before and after \overline{HRESET} negation. $BVSEL[0:1]$ are sampled before \overline{HRESET} negation. These parameters represent the input setup and hold times for each sample. These values are guaranteed by design and not tested. $\overline{BMODE}[0:1]$ must remain stable after the second sample; $BVSEL[0:1]$ must remain stable after the first (and only) sample. See [Figure 5](#) for sample timing.

Figure 11 provides the test access port timing diagram.

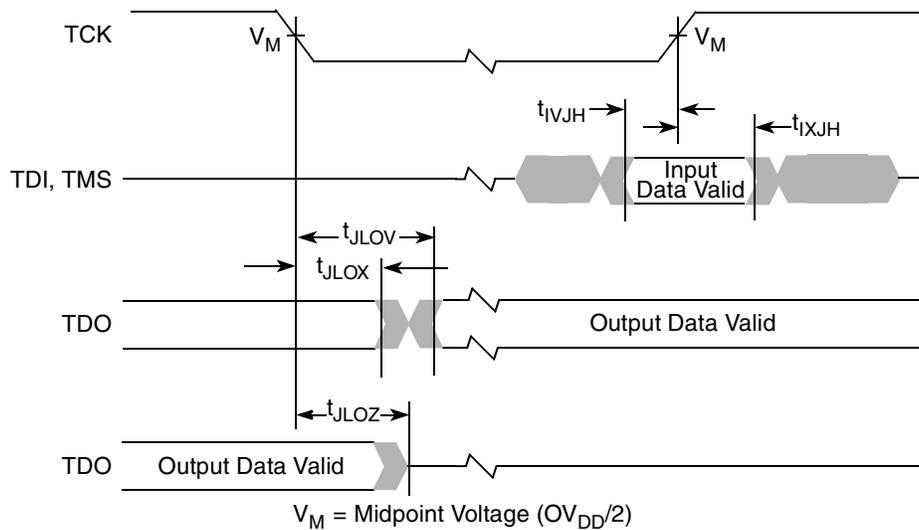


Figure 11. Test Access Port Timing Diagram

5.3 Voltage and Frequency Derating

Voltage and frequency derating is no longer supported for part numbers described by this document beginning with datecode 0613. (See [Section 11, “Part Numbering and Marking,”](#) for information on date code markings.) It is supported by some MPC7448 part numbers which target low-power applications; see [Section 11.2, “Part Numbers Not Fully Addressed by This Document”](#) and the referenced MPC7448 Hardware Specification Addenda for more information on these low-power devices. For those devices which previously supported this feature, information has been archived in the *Chip Errata for the MPC7448* (document order no. MPC7448CE).

7 Pinout Listings

Table 11 provides the pinout listing for the MPC7448, 360 HCTE package. The pinouts of the MPC7448 and MPC7447A are compatible, but the requirements regarding the use of the additional power and ground pins have changed. The MPC7448 requires these pins be connected to the appropriate power or ground plane to achieve high core frequencies; see Section 9.3, “Connection Recommendations,” for additional information. As a result, these pins should be connected in all new designs.

Additionally, the MPC7448 may be populated on a board designed for a MPC7447 (or MPC7445 or MPC7441), provided the core voltage can be made to match the requirements in Table 4 and all pins defined as ‘no connect’ for the MPC7447 are unterminated, as required by the *MPC7457 RISC Microprocessor Hardware Specifications*. The MPC7448 uses pins previously marked ‘no connect’ for the temperature diode pins and for additional power and ground connections. The additional power and ground pins are required to achieve high core frequencies and core frequency will be limited if they are not connected; see Section 9.3, “Connection Recommendations,” for additional information. Because these ‘no connect’ pins in the MPC7447 360 pin package are not driven in functional mode, an MPC7447 can be populated in an MPC7448 board.

NOTE

Caution must be exercised when performing boundary scan test operations on a board designed for an MPC7448, but populated with an MPC7447 or earlier device. This is because in the MPC7447 it is possible to drive the latches associated with the former ‘no connect’ pins in the MPC7447, potentially causing contention on those pins. To prevent this, ensure that these pins are not connected on the board or, if they are connected, ensure that the states of internal MPC7447 latches do not cause these pins to be driven during board testing.

For the MPC7448, pins that were defined as the TEST[0:4] factory test signal group on the MPC7447A and earlier devices have been assigned new functions. For most of these, the termination recommendations for the TEST[0:4] pins of the MPC7447A are compatible with the MPC7448 and will allow correct operation with no performance loss. The exception is BVSEL1 (TEST3 on the MPC7447A and earlier devices), which may require a different termination depending which I/O voltage mode is desired; see Table 3 for more information.

NOTE

This pinout is not compatible with the MPC750, MPC7400, or MPC7410 360 BGA package.

Table 11. Pinout Listing for the MPC7448, 360 HCTE Package (continued)

Signal Name	Pin Number	Active	I/O	Notes
$\overline{\text{LVRAM}}$	B10	—	—	12, 20, 22
NC (no connect)	A6, A14, A15, B14, B15, C14, C15, C16, C17, C18, C19, D14, D15, D16, D17, D18, D19, E14, E15, F14, F15, G14, G15, H15, H16, J15, J16, J17, J18, J19, K15, K16, K17, K18, K19, L15, L16, L17, L18, L19	—	—	11
$\overline{\text{LSSD_MODE}}$	E8	Low	Input	6, 12
$\overline{\text{MCP}}$	C9	Low	Input	
OV_{DD}	B4, C2, C12, D5, F2, H3, J5, K2, L5, M3, N6, P2, P8, P11, R4, R13, R16, T6, T9, U2, U12, U16, V4, V7, V10, V14	—	—	
OVDD_SENSE	E18, G18	—	—	16
$\text{PLL_CFG}[0:4]$	B8, C8, C7, D7, A7	High	Input	
$\text{PLL_CFG}[5]$	D10	High	Input	9, 20
$\overline{\text{PMON_IN}}$	D9	Low	Input	13
$\overline{\text{PMON_OUT}}$	A9	Low	Output	
$\overline{\text{QACK}}$	G5	Low	Input	
$\overline{\text{QREQ}}$	P4	Low	Output	
$\overline{\text{SHD}}[0:1]$	E4, H5	Low	I/O	3
$\overline{\text{SMI}}$	F9	Low	Input	
$\overline{\text{SRESET}}$	A2	Low	Input	
SYSCLK	A10	—	Input	
$\overline{\text{TA}}$	K6	Low	Input	
TBEN	E1	High	Input	
$\overline{\text{TBST}}$	F11	Low	Output	
TCK	C6	High	Input	
TDI	B9	High	Input	6
TDO	A4	High	Output	
$\overline{\text{TEA}}$	L1	Low	Input	
TEMP_ANODE	N18	—	—	17
TEMP_CATHODE	N19	—	—	17
TMS	F1	High	Input	6
$\overline{\text{TRST}}$	A5	Low	Input	6, 14
$\overline{\text{TS}}$	L4	Low	I/O	3
$\text{TSIZ}[0:2]$	G6, F7, E7	High	Output	
$\text{TT}[0:4]$	E5, E6, F6, E9, C5	High	I/O	
$\overline{\text{WT}}$	D3	Low	Output	
V_{DD}	H8, H10, H12, J7, J9, J11, J13, K8, K10, K12, K14, L7, L9, L11, L13, M8, M10, M12	—	—	
V_{DD}	A13, A16, A18, B17, B19, C13, E13, E16, F12, F17, F19, G11, G16, H14, H17, H19, M14, M16, M18, N15, N17, P16, P18	—	—	15

8 Package Description

The following sections provide the package parameters and mechanical dimensions for the HCTE package.

8.1 Package Parameters for the MPC7448, 360 HCTE BGA

The package parameters are as provided in the following list. The package type is 25 × 25 mm, 360-lead high coefficient of thermal expansion ceramic ball grid array (HCTE).

Package outline	25 × 25 mm
Interconnects	360 (19 × 19 ball array – 1)
Pitch	1.27 mm (50 mil)
Minimum module height	2.32 mm
Maximum module height	2.80 mm
Ball diameter	0.89 mm (35 mil)
Coefficient of thermal expansion	12.3 ppm/°C

8.4 Mechanical Dimensions for the MPC7448, 360 HCTE LGA

Figure 13 provides the mechanical dimensions and bottom surface nomenclature for the MPC7448, 360 HCTE LGA package.

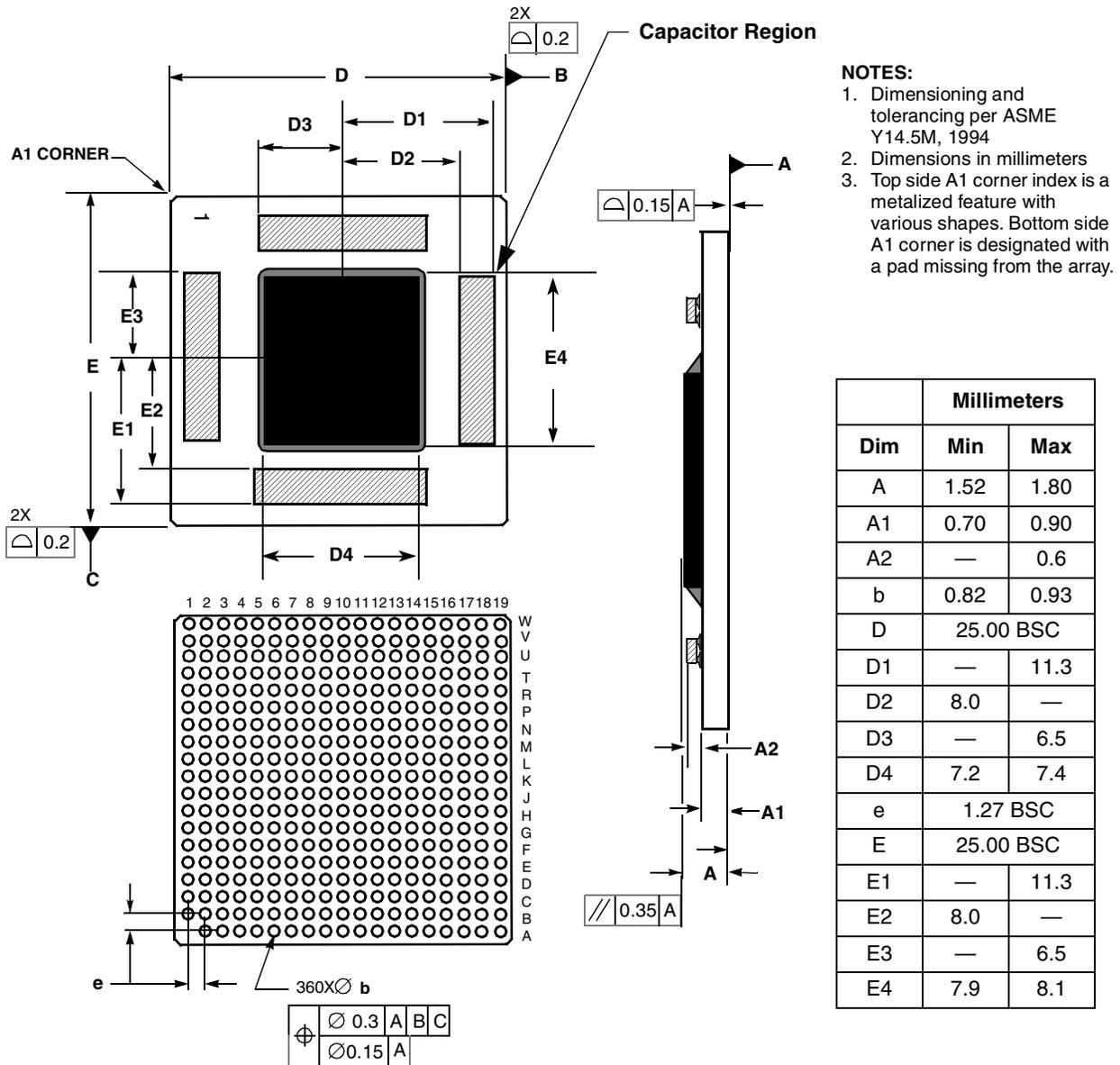


Figure 14. Mechanical Dimensions and Bottom Surface Nomenclature for the MPC7448, 360 HCTE LGA Package

8.6 Mechanical Dimensions for the MPC7448, 360 HCTE RoHS-Compliant BGA

Figure 13 provides the mechanical dimensions and bottom surface nomenclature for the MPC7448, 360 HCTE BGA package with RoHS-compliant lead-free spheres.

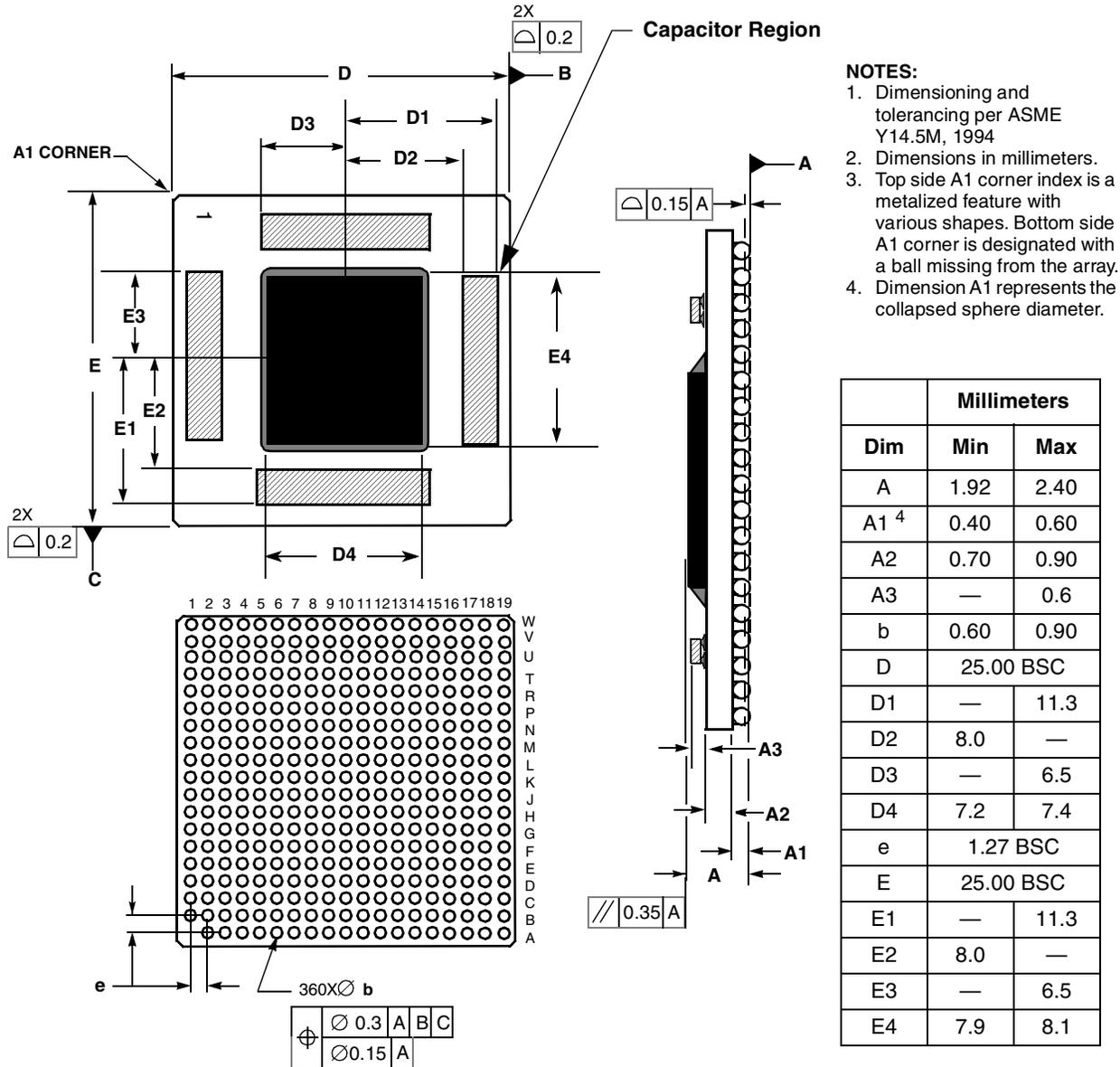


Figure 15. Mechanical Dimensions and Bottom Surface Nomenclature for the MPC7448, 360 HCTE RoHS-Compliant BGA Package

9 System Design Information

This section provides system and thermal design requirements and recommendations for successful application of the MPC7448.

9.1 Clocks

The following sections provide more detailed information regarding the clocking of the MPC7448.

9.1.1 PLL Configuration

The MPC7448 PLL is configured by the PLL_CFG[0:5] signals. For a given SYSCLK (bus) frequency, the PLL configuration signals set the internal CPU and VCO frequency of operation. The PLL configuration for the MPC7448 is shown in Table 12. In this example, shaded cells represent settings that, for a given SYSCLK frequency, result in core and/or VCO frequencies that do not comply with Table 8. When enabled, dynamic frequency switching (DFS) also affects the core frequency by halving or quartering the bus-to-core multiplier; see Section 9.7.5, “Dynamic Frequency Switching (DFS),” for more information. Note that when DFS is enabled the resulting core frequency must meet the adjusted minimum core frequency requirements ($f_{\text{core_DFS}}$) described in Table 8. Note that the PLL_CFG[5] is currently used for factory test only and should be tied low, and that the MPC7448 PLL configuration settings are compatible with the MPC7447A PLL configuration settings when PLL_CFG[5] = 0.

Table 12. MPC7448 Microprocessor PLL Configuration Example

PLL_CFG[0:5]	Example Core and VCO Frequency in MHz											
	Bus-to-Core Multiplier ⁵	Core-to-VCO Multiplier ⁵	Bus (SYSCLK) Frequency									
			33.3 MHz	50 MHz	66.6 MHz	75 MHz	83 MHz	100 MHz	133 MHz	167 MHz	200 MHz	
010000	2x ⁶	1x										
100000	3x ⁶	1x										600
101000	4x ⁶	1x									667	800
101100	5x	1x								667	835	1000
100100	5.5x	1x								733	919	1100
110100	6x	1x							600	800	1002	1200
010100	6.5x	1x							650	866	1086	1300
001000	7x	1x							700	931	1169	1400
000100	7.5x	1x						623	750	1000	1253	1500
110000	8x	1x				600	664	800	1064	1336	1600	
011000	8.5x	1x				638	706	850	1131	1417	1700	
011110	9x	1x			600	675	747	900	1197	1500		
011100	9.5x	1x			633	712	789	950	1264	1583		
101010	10x	1x			667	750	830	1000	1333	1667		
100010	10.5x	1x			700	938	872	1050	1397			

9.1.2 System Bus Clock (SYSCLK) and Spread Spectrum Sources

Spread spectrum clock sources are an increasingly popular way to control electromagnetic interference emissions (EMI) by spreading the emitted noise to a wider spectrum and reducing the peak noise magnitude in order to meet industry and government requirements. These clock sources intentionally add long-term jitter in order to diffuse the EMI spectral content. The jitter specification given in [Table 8](#) considers short-term (cycle-to-cycle) jitter only and the clock generator's cycle-to-cycle output jitter should meet the MPC7448 input cycle-to-cycle jitter requirement. Frequency modulation and spread are separate concerns, and the MPC7448 is compatible with spread spectrum sources if the recommendations listed in [Table 13](#) are observed.

Table 13. Spread Spectrum Clock Source Recommendations

At recommended operating conditions. See [Table 4](#).

Parameter	Min	Max	Unit	Notes
Frequency modulation	—	50	kHz	1
Frequency spread	—	1.0	%	1, 2

Notes:

1. Guaranteed by design
2. SYSCLK frequencies resulting from frequency spreading, and the resulting core and VCO frequencies, must meet the minimum and maximum specifications given in [Table 8](#).

It is imperative to note that the processor's minimum and maximum SYSCLK, core, and VCO frequencies must not be exceeded regardless of the type of clock source. Therefore, systems in which the processor is operated at its maximum rated core or bus frequency should avoid violating the stated limits by using down-spreading only.

9.2 Power Supply Design and Sequencing

The following sections provide detailed information regarding power supply design for the MPC7448.

9.2.1 Power Supply Sequencing

The MPC7448 requires its power rails and clock to be applied in a specific sequence to ensure proper device operation and to prevent device damage. The power sequencing requirements are as follows:

- AV_{DD} must be delayed with respect to V_{DD} by the RC time constant of the PLL filter circuit described in [Section 9.2.2, "PLL Power Supply Filtering"](#). This time constant is nominally 100 μ s.
- OV_{DD} may ramp anytime before or after V_{DD} and AV_{DD} .

Additionally, the following requirements exist regarding the application of SYSCLK:

- The voltage at the SYSCLK input must not exceed V_{DD} until V_{DD} has ramped to 0.9 V.
- The voltage at the SYSCLK input must not exceed OV_{DD} by more 20% during transients (see overshoot/undershoot specifications in [Figure 2](#)) or 0.3 V DC (see [Table 2](#)) at any time.

These requirements are shown graphically in [Figure 16](#).

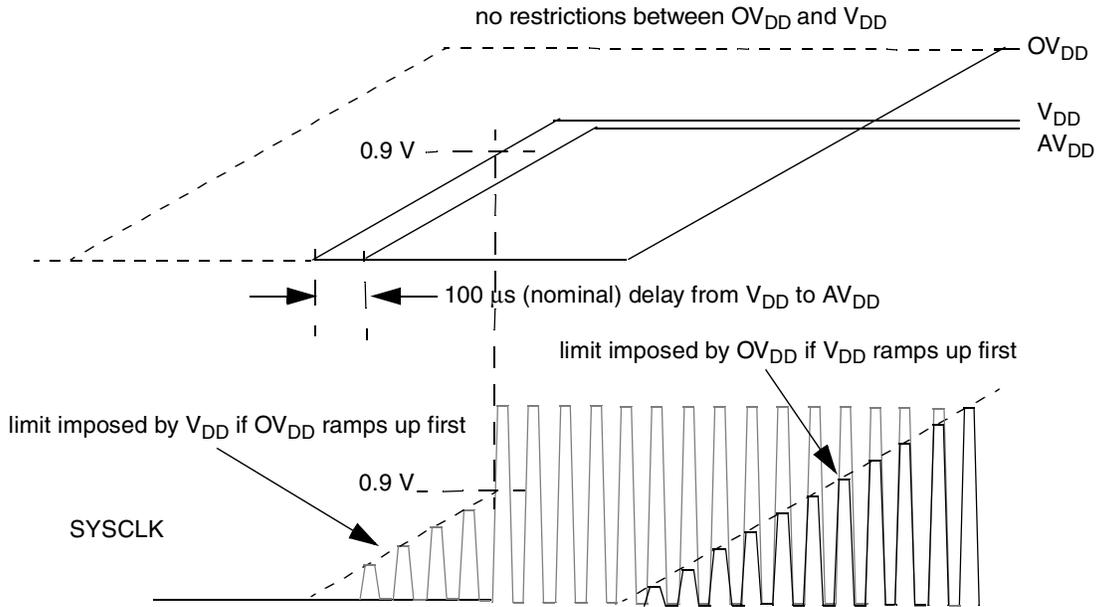


Figure 16. MPC7448 Power Up Sequencing Requirements

Certain stipulations also apply to the manner in which the power rails of the MPC7448 power down, as follows:

- OV_{DD} may ramp down any time before or after V_{DD} .
- The voltage at the SYSCLK input must not exceed V_{DD} once V_{DD} has ramped down below 0.9 V.
- The voltage at the SYSCLK input must not exceed OV_{DD} by more 20% during transients (see overshoot/undershoot specifications in [Figure 2](#)) or 0.3 V DC (see [Table 2](#)) at any time.

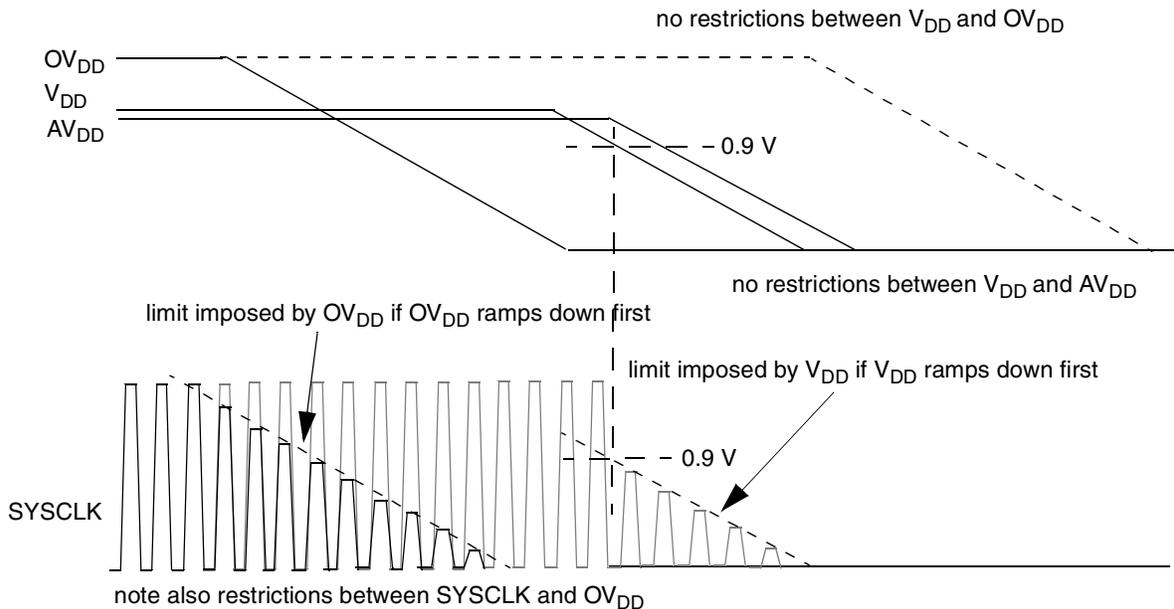


Figure 17. MPC7448 Power Down Sequencing Requirements

There is no requirement regarding AV_{DD} during power down, but it is recommended that AV_{DD} track V_{DD} within the RC time constant of the PLL filter circuit described in [Section 9.2.2, “PLL Power Supply Filtering”](#) (nominally 100 μ s).

9.2.2 PLL Power Supply Filtering

The AV_{DD} power signal is provided on the MPC7448 to provide power to the clock generation PLL. To ensure stability of the internal clock, the power supplied to the AV_{DD} input signal should be filtered of any noise in the 500-KHz to 10-MHz resonant frequency range of the PLL. The circuit shown in [Figure 18](#) using surface mount capacitors with minimum effective series inductance (ESL) is strongly recommended. In addition to filtering noise from the AV_{DD} input, it also provides the required delay between V_{DD} and AV_{DD} as described in [Section 9.2.1, “Power Supply Sequencing.”](#)

The circuit should be placed as close as possible to the AV_{DD} pin to minimize noise coupled from nearby circuits. It is often possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of the device footprint.

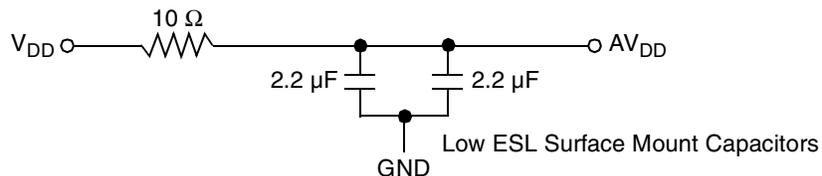


Figure 18. PLL Power Supply Filter Circuit

9.2.3 Transient Specifications

To ensure the long-term reliability of the device, the MPC7448 requires that transients on the core power rail (V_{DD}) be constrained. The recommended operating voltage specifications provided in [Table 4](#) are DC specifications. That is, the device may be operated continuously with V_{DD} within the specified range without adversely affecting the device's reliability. Excursions above the stated recommended operation range, including overshoot during power-up, can impact the long-term reliability of the device. Excursions are described by their amplitude and duration. Duration is defined as the time period during which the V_{DD} power plane, as measured at the VDD_SENSE pins, will be within a specific voltage range, expressed as percentage of the total time the device will be powered up over the device lifetime. In practice, the period over which transients are measured can be any arbitrary period of time that accurately represents the expected range of processor and system activity. The voltage ranges and durations for normal operation and transients are described in [Table 14](#).

Table 14. VDD Power Supply Transient Specifications

At recommended operating temperatures. See [Table 4](#).

Voltage Region	Voltage Range (V)		Permitted Duration ¹	Notes
	Min	Max		
Normal	V_{DD} minimum	V_{DD} maximum	100%	2
Low Transient	V_{DD} maximum	1.35 V	10%	2, 3
High Transient	1.35 V	1.40 V	0.2%	4

Notes:

1. Permitted duration is defined as the percentage of the total time the device is powered on that the V_{DD} power supply voltage may exist within the specified voltage range.
2. See [Table 4](#) for nominal V_{DD} specifications.
3. To simplify measurement, excursions into the High Transient region are included in this duration.
4. Excursions above the absolute maximum rating of 1.4 V are not permitted; see [Table 2](#).

Note that, to simplify transient measurements, the duration of the excursion into the High Transient region is also included in the Low Transient duration, so that only the time the voltage is above each threshold must be considered. [Figure 19](#) shows an example of measuring voltage transients.

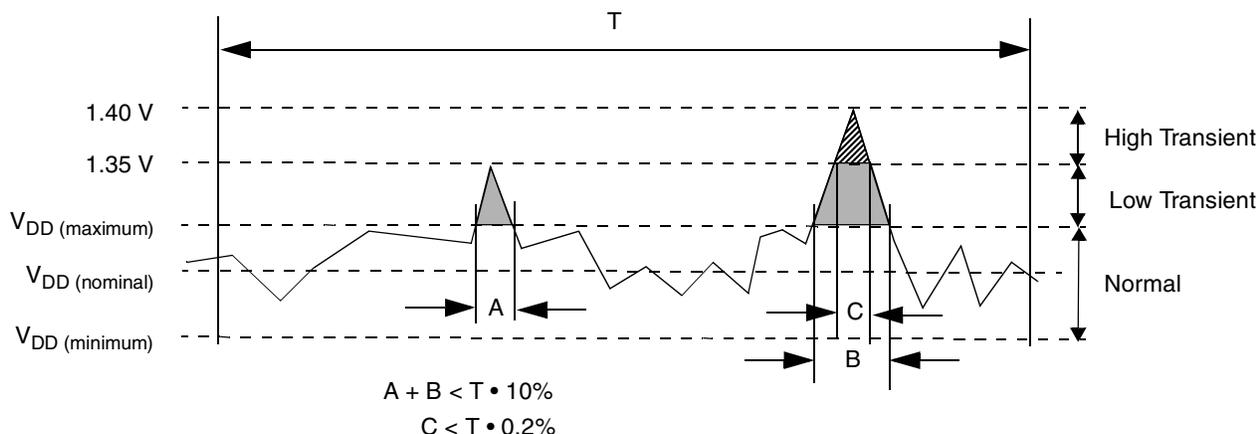


Figure 19. Voltage Transient Example

9.7.1 Internal Package Conduction Resistance

For the exposed-die packaging technology described in Table 5, the intrinsic conduction thermal resistance paths are as follows:

- The die junction-to-case thermal resistance (the case is actually the top of the exposed silicon die)
- The die junction-to-board thermal resistance

Figure 24 depicts the primary heat transfer path for a package with an attached heat sink mounted to a printed-circuit board.

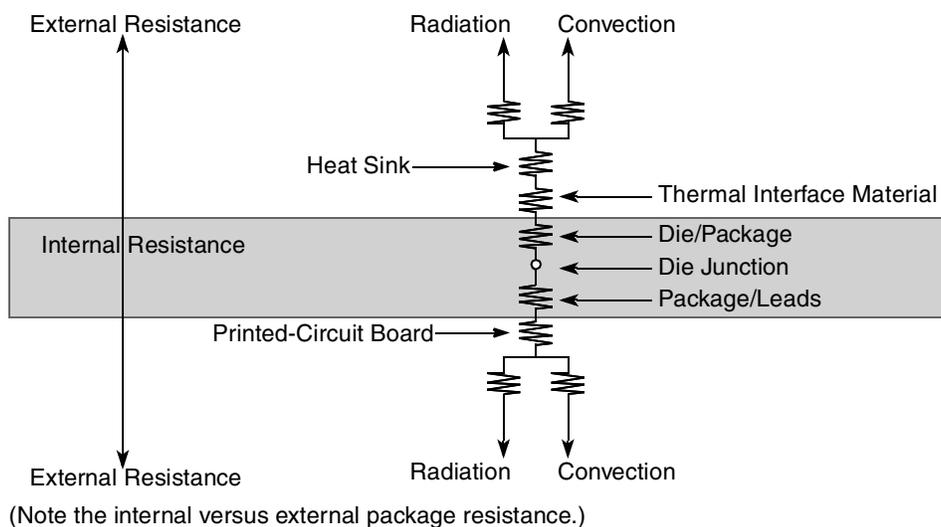


Figure 24. C4 Package with Heat Sink Mounted to a Printed-Circuit Board

Heat generated on the active side of the chip is conducted through the silicon, through the heat sink attach material (or thermal interface material), and, finally, to the heat sink, where it is removed by forced-air convection.

Because the silicon thermal resistance is quite small, the temperature drop in the silicon may be neglected for a first-order analysis. Thus, the thermal interface material and the heat sink conduction/convective thermal resistances are the dominant terms.

9.7.2 Thermal Interface Materials

A thermal interface material is recommended at the package lid-to-heat sink interface to minimize the thermal contact resistance. For those applications where the heat sink is attached by spring clip mechanism, Figure 25 shows the thermal performance of three thin-sheet thermal-interface materials (silicone, graphite/oil, fluoroether oil), a bare joint, and a joint with thermal grease as a function of contact pressure. As shown, the performance of these thermal interface materials improves with increasing contact pressure. The use of thermal grease significantly reduces the interface thermal resistance. That is, the bare joint results in a thermal resistance approximately seven times greater than the thermal grease joint.

Often, heat sinks are attached to the package by means of a spring clip to holes in the printed-circuit board (see Figure 22). Therefore, synthetic grease offers the best thermal performance due to the low interface pressure and is recommended due to the high power dissipation of the MPC7448. Of course, the selection

Due to the complexity and variety of system-level boundary conditions for today's microelectronic equipment, the combined effects of the heat transfer mechanisms (radiation, convection, and conduction) may vary widely. For these reasons, we recommend using conjugate heat transfer models for the board as well as system-level designs.

For system thermal modeling, the MPC7448 thermal model is shown in Figure 26. Four volumes represent this device. Two of the volumes, solder ball-air and substrate, are modeled using the package outline size of the package. The other two, die and bump-underfill, have the same size as the die. The silicon die should be modeled $8.0 \times 7.3 \times 0.86 \text{ mm}^3$ with the heat source applied as a uniform source at the bottom of the volume. The bump and underfill layer is modeled as $8.0 \times 7.3 \times 0.07 \text{ mm}^3$ collapsed in the z-direction with a thermal conductivity of $5.0 \text{ W}/(\text{m} \cdot \text{K})$ in the z-direction. The substrate volume is $25 \times 25 \times 1.14 \text{ mm}^3$ and has $9.9 \text{ W}/(\text{m} \cdot \text{K})$ isotropic conductivity in the xy-plane and $2.95 \text{ W}/(\text{m} \cdot \text{K})$ in the direction of the z-axis. The solder ball and air layer are modeled with the same horizontal dimensions as the substrate and is 0.8 mm thick. For the LGA package the solder and air layer is 0.1 mm thick, but the material properties are the same. It can also be modeled as a collapsed volume using orthotropic material properties: $0.034 \text{ W}/(\text{m} \cdot \text{K})$ in the xy-plane direction and $11.2 \text{ W}/(\text{m} \cdot \text{K})$ in the direction of the z-axis.

Conductivity	Value	Unit
Die ($8.0 \times 7.3 \times 0.86 \text{ mm}^3$)		
Silicon	Temperature-dependent	$\text{W}/(\text{m} \cdot \text{K})$
Bump and Underfill ($8.0 \times 7.3 \times 0.07 \text{ mm}^3$)		
k_z	5.0	$\text{W}/(\text{m} \cdot \text{K})$
Substrate ($25 \times 25 \times 1.14 \text{ mm}^3$)		
k_x	9.9	$\text{W}/(\text{m} \cdot \text{K})$
k_y	9.9	
k_z	2.95	
Solder Ball and Air ($25 \times 25 \times 0.8 \text{ mm}^3$)		
k_x	0.034	$\text{W}/(\text{m} \cdot \text{K})$
k_y	0.034	
k_z	11.2	

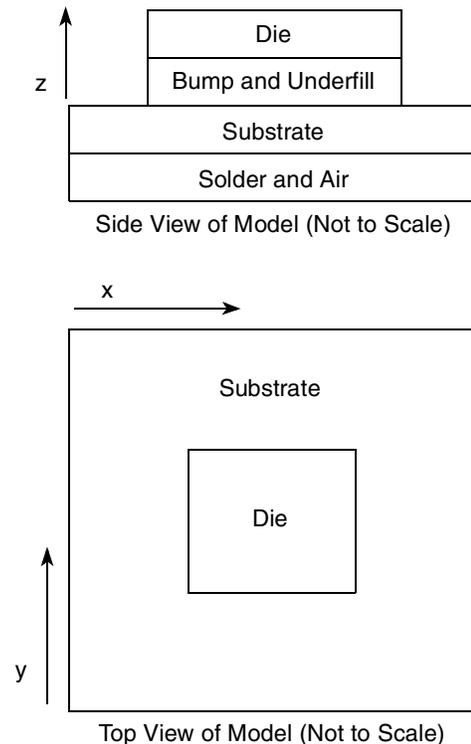


Figure 26. Recommended Thermal Model of MPC7448

Solving for T, the equation becomes:

$$nT = \frac{V_H - V_L}{1.986 \times 10^{-4}}$$

9.7.5 Dynamic Frequency Switching (DFS)

The DFS feature in the MPC7448 adds the ability to divide the processor-to-system bus ratio by two or four during normal functional operation. Divide-by-two mode is enabled by setting the HID1[DFS2] bit in software or by asserting the $\overline{\text{DFS2}}$ pin via hardware. The MPC7448 can be returned for full speed by clearing HID1[DFS2] or negating $\overline{\text{DFS2}}$. Similarly, divide-by-four mode is enabled by setting HID1[DFS4] in software or by asserting the $\overline{\text{DFS4}}$ pin. In all cases, the frequency change occurs in 1 clock cycle and no idle waiting period is required to switch between modes. Note that asserting either $\overline{\text{DFS2}}$ or $\overline{\text{DFS4}}$ overrides software control of DFS, and that asserting both $\overline{\text{DFS2}}$ and $\overline{\text{DFS4}}$ disables DFS completely, including software control. Additional information regarding DFS can be found in the *MPC7450 RISC Microprocessor Family Reference Manual*. Note that minimum core frequency requirements must be observed when enabling DFS, and the resulting core frequency must meet the requirements for $f_{\text{core_DFS}}$ given in [Table 8](#).

9.7.5.1 Power Consumption with DFS Enabled

Power consumption with DFS enabled can be approximated using the following formula:

$$P_{\text{DFS}} = \left[\frac{f_{\text{DFS}}}{f} (P - P_{\text{DS}}) \right] + P_{\text{DS}}$$

Where:

P_{DFS} = Power consumption with DFS enabled

f_{DFS} = Core frequency with DFS enabled

f = Core frequency prior to enabling DFS

P = Power consumption prior to enabling DFS (see [Table 7](#))

P_{DS} = Deep sleep mode power consumption (see [Table 7](#))

The above is an approximation only. Power consumption with DFS enabled is not tested or guaranteed.

9.7.5.2 Bus-to-Core Multiplier Constraints with DFS

DFS is not available for all bus-to-core multipliers as configured by PLL_CFG[0:5] during hard reset. The complete listing is shown in [Table 16](#). Shaded cells represent DFS modes that are not available for a particular PLL_CFG[0:5] setting. Should software or hardware attempt to transition to a multiplier that is not supported, the device will remain at its current multiplier. For example, if a transition from DFS-disabled to an unsupported divide-by-2 or divide-by-4 setting is attempted, the bus-to-core multiplier will remain at the setting configured by the PLL_CFG[0:5] pins. In the case of an attempted transition from a supported divide-by-2 mode to an unsupported divide-by-4 mode, the device will remain in divide-by-2 mode. In all cases, the HID1[PC0-5] bits will correctly reflect the current bus-to-core frequency multiplier.

Table 17. Document Revision History (continued)

Revision	Date	Substantive Change(s)
2		<p>Table 6: Added separate input leakage specification for $\overline{\text{BVSEL0}}$, $\overline{\text{LSSD_MODE}}$, $\overline{\text{TCK}}$, $\overline{\text{TDI}}$, $\overline{\text{TMS}}$, $\overline{\text{TRST}}$ signals to correctly indicate leakage current for signals with internal pull-up resistors.</p> <p>Section 5.1: Added paragraph preceding Table 7 and edited notes in Table 7 to clarify core frequencies at which power consumption is measured.</p> <p>Section 5.3: Removed voltage derating specifications; this feature has been made redundant by new device offerings and is no longer supported.</p> <p>Changed names of “Typical–Nominal” and “Typical–Thermal” power consumption parameters to “Typical” and “Thermal”, respectively. (Name change only—no specifications were changed.)</p> <p>Table 11: Revised Notes 16, 18, and 19 to reflect current recommendations for connection of SENSE pins.</p> <p>Section 9.3: Added paragraph explaining connection recommendations for SENSE pins. (See also Table 11 entry above.)</p> <p>Table 19: Updated table to reflect changes in specifications for MC7448xxnnnnNC devices.</p> <p>Table 9: Changed all instances of TT[0:3] to TT[0:4]</p> <p>Removed mention of these input signals from output valid times and output hold times:</p> <ul style="list-style-type: none"> • AACK, CKSTP_IN, DT[0:3] <p>Figure 17: Modified diagram slightly to correctly show constraint on SYSCLK ramping is related to V_{DD} voltage, not AV_{DD} voltage. (Diagram clarification only; no change in power sequencing requirements.)</p> <p>Added Table 20 to reflect introduction of extended temperature devices and associated hardware specification addendum.</p>
1		<p>Added 1600 MHz, 1420 MHz, and 1000 MHz devices</p> <p>Section 4: corrected die size</p> <p>Table 2: Revised Note 4 to consider overshoot/undershoot and combined with Note 5.</p> <p>Table 4: Revised operating voltage for 1700 MHz device from ± 50 mV to +20 mV / –50 mV.</p> <p>Table 7: Updated and expanded table to include Typical – Nominal power consumption.</p> <p>Table 11: Added voltage derating information for 1700 MHz devices; this feature is not supported at this time for other speed grades.</p> <p>Added transient specifications for VDD power supply in Section 9.2.3, added Table 15 and Figure 19 and renumbered subsequent tables and figures.</p> <p>Moved Decoupling Recommendations from Section 9.4 to Section 9.2.4 and renumbered subsequent sections.</p> <p>Section 9.2.1: Revised power sequencing requirements.</p> <p>Section 9.7.4: Added thermal diode ideality factor information (previously TBD).</p> <p>Table 17: Expanded table to show HID1 register values when DFS modes are enabled.</p> <p>Section 11.2: updated to include additional N-spec device speed grades</p> <p>Tables 18 and 19: corrected PVR values and added “MC” product code prefix</p>
0		Initial public release.

11.2 Part Numbers Not Fully Addressed by This Document

Parts with application modifiers or revision levels not fully addressed in this specification document are described in separate hardware specification addenda which supplement and supersede this document. As such parts are released, these specifications will be listed in this section.

Table 19. Part Numbers Addressed by MC7448xxnnnnNx Series Hardware Specification Addendum (Document Order No. MPC7448ECS01AD)

xx	7448	xx	nnnn	N	x
Product Code	Part Identifier	Package	Processor Frequency	Application Modifier	Revision Level
MC	7448	HX = HCTE BGA VS = RoHS LGA VU = RoHS BGA	1400	N: 1.15 V ± 50 mV 0 to 105 °C (date code 0613 and later) ²	C: 2.1; PVR = 0x8004_0201 D: 2.2; PVR = 0x8004_0202
MC PPC ¹			1400	N: 1.1 V ± 50 mV 0 to 105 °C (date code 0612 and prior) ²	
MC PPC ¹			1267 Revision C only	N: 1.1 V ± 50 mV 0 to 105 °C	
MC PPC ¹			1267 Revision D only	N: 1.05 V ± 50 mV 0 to 105 °C	
MC PPC ¹			1250	N: 1.1 V ± 50 mV 0 to 105 °C	
MC PPC ¹			1000 867 800 667 600	N: 1.0 V ± 50 mV 0 to 105 °C	

Notes:

1. The P prefix in a Freescale part number designates a “Pilot Production Prototype” as defined by Freescale SOP 3-13. These parts have only preliminary reliability and characterization data. Before pilot production prototypes can be shipped, written authorization from the customer must be on file in the applicable sales office acknowledging the qualification status and the fact that product changes may still occur as pilot production prototypes are shipped.
2. Core voltage for 1400 MHz devices currently in production (date code of 0613 and later) is 1.15 V ± 50 mV; all such devices have the MC product code. The 1400 MHz devices with date code of 0612 and prior specified core voltage of 1.1 V ± 50 mV; this includes all 1400 MHz devices with the PPC product code. See [Section 11.3, “Part Marking,”](#) for information on part marking.

**Table 20. Part Numbers Addressed by MC7448TxxnnnnNx Series Hardware Specification Addendum
(Document Order No. MPC7448ECS02AD)**

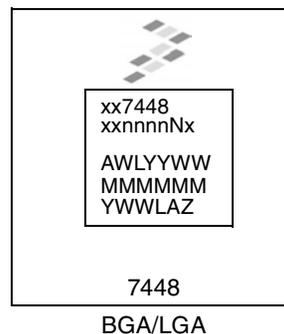
xx	7448	T	xx	nnnn	N	x
Product Code	Part Identifier	Specification Modifier	Package	Processor Frequency	Application Modifier	Revision Level
MC PPC ¹	7448	T = Extended Temperature Device	HX = HCTE BGA	1400	N: 1.15 V ± 50 mV – 40 to 105 °C	C: 2.1; PVR = 0x8004_0201 D: 2.2; PVR = 0x8004_0202
				1267 Revision C only	N: 1.1 V ± 50 mV – 40 to 105 °C	
				1267 Revision D only	N: 1.05 V ± 50 mV – 40 to 105 °C	
				1000	N: 1.0 V ± 50 mV – 40 to 105 °C	

Notes:

- The P prefix in a Freescale part number designates a “Pilot Production Prototype” as defined by Freescale SOP 3-13. These parts have only preliminary reliability and characterization data. Before pilot production prototypes can be shipped, written authorization from the customer must be on file in the applicable sales office acknowledging the qualification status and the fact that product changes may still occur as pilot production prototypes are shipped.

11.3 Part Marking

Parts are marked as the example shown in [Figure 27](#).



Notes:

- AWLYYWW is the test code, where YYWW is the date code (YY = year, WW = work week)
- MMMMMM is the M00 (mask) number.
- YWWLAZ is the assembly traceability code.

Figure 27. Part Marking for BGA and LGA Device