Infineon Technologies - MB91F585MHPMC-GTE1 Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	FR81S
Core Size	32-Bit Single-Core
Speed	128MHz
Connectivity	CANbus, CSIO, I²C, LINbus, SPI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	-
Program Memory Size	576KB (576K x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	56K x 8
Voltage - Supply (Vcc/Vdd)	3.7V ~ 5.5V
Data Converters	A/D 23x12b; D/A 1x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb91f585mhpmc-gte1

- DMA controller
  - Up to 8 channels can be started simultaneously.
  - 2 transfer factors (Internal peripheral request and software)
- External interrupt input

MB91F583AM/F584AM/F585AM: 8 channels
MB91F583AS/F584AS/F585AS: 7 channels
Level ("H" / "L") or edge detection (rising or falling) enabled

- Multi-function serial communication (built-in transmission/reception FIFO memory)

MB91F583AM/F584AM/F585AM: 4 channels
MB91F583AS/F584AS/F585AS: 2 channels

  - UART (Asynchronous serial interface)
    - Full-duplex double buffering system, 64-byte transmission FIFO memory, 64-byte reception FIFO memory
    - Parity or no parity is selectable.
    - Built-in dedicated baud rate generator
    - An external clock can be used as the transfer clock
    - Parity, frame, and overrun error detection functions provided
    - DMA transfer supported
  - CSIO (Synchronous serial interface)
    - Full-duplex double buffering system, 64-byte transmission FIFO memory, 64-byte reception FIFO memory
    - SPI supported; master and slave systems supported; 5 to 16, 20, 24, 32-bit data length can be set.
    - Built-in dedicated baud rate generator (Master operation)
    - An external clock can be entered. (Slave operation)
    - Overrun error detection function is provided.
    - Built-in chip selection function
    - DMA transfer supported
  - LIN interface (v2.1)
    - Full-duplex double buffering system, 64-byte transmission FIFO memory, 64-byte reception FIFO memory
    - LIN protocol revision2.1 supported.
    - Master and slave systems supported
    - Framing error and overrun error detection
    - LIN sync break generation and detection; LIN sync delimiter generation
    - Built-in dedicated baud rate generator
    - An external clock can be adjusted by the reload counter.
    - DMA transfer supported
  - I^2C
    - MB91F583AM/F584AM/F585AM: Supported for 3 channels: ch.0,ch.2,and ch.3

      MB91F583AS/F584AS/F585AS: Supported for 1 channel: ch.0
    - Full-duplex double buffering system, 64-byte transmission FIFO memory, 64-byte reception FIFO memory
    - Standard mode (Max. 100 kbps) / high-speed mode (Max. 400 kbps) supported
    - DMA transfer supported (for transmission only)
- CAN controller (CAN)

MB91F583AM/F584AM/F585AM: 2 channels
MB91F583AS/F584AS/F585AS: 1 channel

  - Transfer speed: Up to 1Mbps
  - 64-transmission/reception message buffering
- FlexRay controller

MB91F583AMG/F584AMG/F585AMG/F583AMJ/F584AMJ/F585AMJ/
F583ASG/F584ASG/F585ASG/F583ASJ/F584ASJ/F585ASJ: 1 unit (ch.A/ch.B)

  - FlexRay Specifications Version 2.1 supported
  - Up to 128 message buffers
  - 8K bytes of message RAM
  - Variable length of message buffers
  - Each message buffer can be allocated as a part of reception buffer, transmission buffer or reception FIFO memory
  - Host access to the message buffer via input and output buffers
  - Filtering for slot counter, cycle counter and channels
  - Maskable interrupts are supported
- PPG: 16 bits × 6 channels
- Reload timer: 16 bits × 4 channels
- A/D converter (successive approximation type)
  - 12-bit resolution

    MB91F583AM/F584AM/F585AM: 3 units (23 channels)
    MB91F583AS/F584AS/F585AS: 3 units (17 channels)
  - Conversion time: 1 μs
- Free-run timer

16 bits × 6 channels (1 channel can be selected for input capture, and 1 channel for output compare.)

- Input capture: 16 bits × 4 channels (linked to the free-run timer)
- Output compare: 16 bits × 7 channels (linked to the free-run timer)
- Waveform generator: 2 units (7 channels)
- 10-bit D/A converter: 1 channel
- Calibration: The hardware watchdog for CR oscillation drive

The CR oscillation frequency can be trimmed.

MB91580AS Series Product Lineup Comparison

■ Memory size

Items	MB91F583ASG MB91F583ASH MB91F583ASJ MB91F583ASK	MB91F584ASG MB91F584ASH MB91F584ASJ MB91F584ASK	MB91F585ASG MB91F585ASH MB91F585ASJ MB91F585ASK
Flash memory capacity (program)	256+64 Kbytes	384+64 Kbytes	512+64 Kbytes
Flash memory capacity (work)	64 Kbytes		
RAM capacity (main)	32 Kbytes	48 Kbytes	48 Kbytes
RAM capacity (backup)	8 Kbytes		

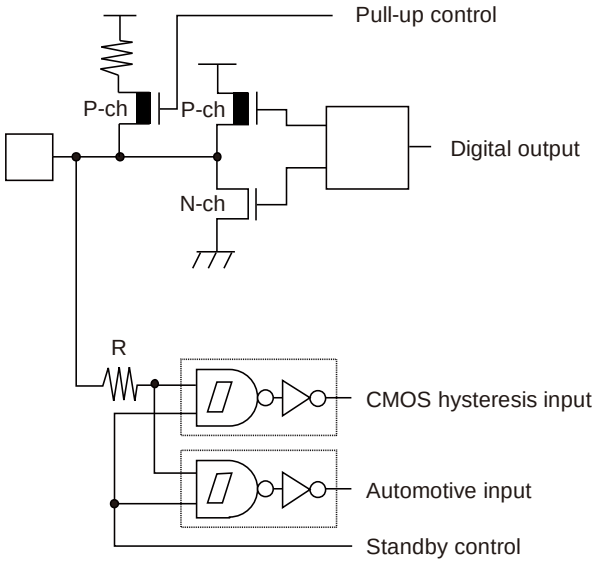
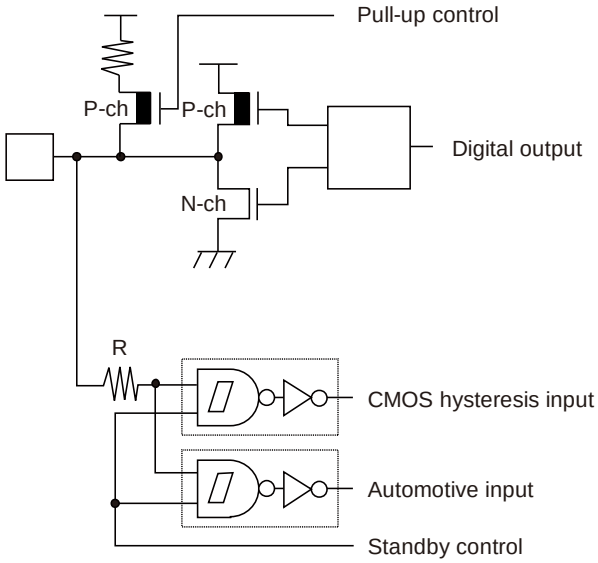
■ Function

Items	MB91F583ASG MB91F584ASG MB91F585ASG	MB91F583ASH MB91F584ASH MB91F585ASH	MB91F583ASJ MB91F584ASJ MB91F585ASJ	MB91F583ASK MB91F584ASK MB91F585ASK
System clock	On-chip PLL clock multiplication system (Up to 32 times of multiplication) Minimum instruction execution time: 7.81ns (128MHz, source oscillation 4MHz × 32 times of multiplication)			
CR oscillation	Provided			
Oscillation stop feature during standby	Provided	Provided	Not provided	Not provided
External bus interface	Not provided			
DMA transfer	8 channels			
16-bit base timer	2 channels			
Free-run timer	6 channels			
Input capture	4 channels			
Output compare	7 channels			
Waveform generator	2 units (7 channels)			
16-bit reload timer	4 channels			
PPG	6 channels			
External interrupt	7 channels			
A/D converter	3 units (17 channels)			
R/D converter	Not provided			
D/A converter	Provided			
Up/ down counter	2 channels			
Multi-function serial interface	2 channels			
CAN	64msb × 1 channel (ch.0)			
FlexRay	128msb × 1unit (ch.A / ch.B)	Not provided	128msb × 1unit (ch.A / ch.B)	Not provided
Software watchdog	Provided			
Hardware watchdog	Provided			
CRC generation	2 channels			

3. Pin Description

MB91F583AM/F584AM/F585AM

Pin No.	Pin name	I/O circuit type*	Function
83	X0	A	Main clock oscillation input pin
84	X1		Main clock oscillation output pin
67	NMIX	B	Interrupt input pin without mask
88	RSTX	B	External reset input pin
81	MD0	C	Mode pin 0 (with high-voltage control)
82	MD1	C	Mode pin 1 (with high-voltage control)
2	P000	D	General-purpose I/O port
4	P001	D	General-purpose I/O port
7	P002	D	General-purpose I/O port
9	P003	D	General-purpose I/O port
11	P004	D	General-purpose I/O port
13	P005	D	General-purpose I/O port
15	P006	D	General-purpose I/O port
17	P007	D	General-purpose I/O port
19	P010	F	General-purpose I/O port
	IN0		16-bit input capture ch.0 external pulse input pin
	AN0		ADC analog 0 input pin
20	P011	F	General-purpose I/O port
	IN1		16-bit input capture ch.1 external pulse input pin
	AN1		ADC analog 1 input pin
21	P012	F	General-purpose I/O port
	IN2		16-bit input capture ch.2 external pulse input pin
	AN2		ADC analog 2 input pin
22	P013	F	General-purpose I/O port
	IN3		16-bit input capture ch.3 external pulse input pin
	AN3		ADC analog 3 input pin
23	P014	F	General-purpose I/O port
	TRG1		PPG ch.4, ch.5 external trigger
	AN4		ADC analog 4 input pin
24	P015	F	General-purpose I/O port
	AN5		ADC analog 5 input pin
27	P016	G	General-purpose I/O port
	AN6		ADC analog 6 input pin
	INT6		INT6 external interrupt input pin

Type	Circuit	Remarks
D		■ General-purpose I/O port ■ CMOS level output I_{OH}=-2/-5mA, I_{OL}=2/5mA ■ With 50kΩ pull-up resistor control ■ CMOS hysteresis input (0.7Vcc/0.3Vcc) ■ Automotive input (0.8Vcc/0.5Vcc)
E		■ General-purpose I/O port ■ CMOS level output I_{OH}=-2/-5mA, I_{OL}=2/5mA ■ With 50 kΩ pull-up resistor control ■ CMOS hysteresis input (0.7Vcc/0.3Vcc) During standby, the input value retains the previous value. ■ Automotive input (0.8Vcc/0.5Vcc) During standby, the input value retains the previous value.

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
000880_H	WRAR00[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				Wild register [S]
000884_H	WRDR00[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000888_H	WRAR01[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
$00088C_H$	WRDR01[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000890_H	WRAR02[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
000894_H	WRDR02[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000898_H	WRAR03[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
$00089C_H$	WRDR03[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0008A0_H$	WRAR04[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
$0008A4_H$	WRDR04[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0008A8_H$	WRAR05[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
$0008AC_H$	WRDR05[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0008B0_H$	WRAR06[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
$0008B4_H$	WRDR06[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0008B8_H$	WRAR07[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
$0008BC_H$	WRDR07[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0008C0_H$	WRAR08[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
$0008C4_H$	WRDR08[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0008C8_H$	WRAR09[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
$0008CC_H$	WRDR09[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
001278$_H$	ADTCD10[R] B,H,W 10--0000 00000000		ADTCD11[R] B,H,W 10--0000 00000000		12-bit A/D converter
00127C$_H$	ADTCD12[R] B,H,W 10--0000 00000000		ADTCD13[R] B,H,W 10--0000 00000000		
001280$_H$	ADTCD14[R] B,H,W 10--0000 00000000		-		
001284$_H$	ADTCD16[R] B,H,W 10--0000 00000000		ADTCD17[R] B,H,W 10--0000 00000000		
001288$_H$	ADTCD18[R] B,H,W 10--0000 00000000		ADTCD19[R] B,H,W 10--0000 00000000		
00128C$_H$	ADTCD20[R] B,H,W 10--0000 00000000		ADTCD21[R] B,H,W 10--0000 00000000		
001290$_H$	ADTCD22[R] B,H,W 10--0000 00000000		ADTCD23[R] B,H,W 10--0000 00000000		
001294$_H$	-	-	-	-	
001298$_H$	-	-	-	-	
00129C$_H$	-	-	-	-	
0012A0$_H$	-	-	-	-	
0012A4$_H$	ADCS0[R/W] B,H,W 0------- --------		ADCH0[R] B,H,W -----000	ADMD0[R/W] B,H,W ----0000	
0012A8$_H$	ADCS1[R/W] B,H,W 0------- --------		ADCH1[R] B,H,W -----000	ADMD1[R/W] B,H,W ----0000	
0012AC$_H$	ADCS2[R/W] B,H,W 0------- --------		ADCH2[R] B,H,W -----000	ADMD2[R/W] B,H,W ----0000	
0012B0$_H$	MTRCSR[R/W] B,H,W -------0	-	-	-	Motor control extension function
0012B4$_H$	RTOSEL0[R/W] B,H,W --000000	RTOSEL1[R/W] B,H,W -------0	-	-	
0012B8$_H$ | 0012FC$_H$	-	-	-	-	Reserved
001300$_H$	-	-	-	-	Reserved
001304$_H$	-	-	-	-	
001308$_H$	-	-	-	-	
00130C$_H$	-	-	-	-	
001310$_H$	-	-	-	-	
001314$_H$	-	-	-	-	
001318$_H$	-	-	-	-	
00131C$_H$	-	-	-	-	
001320$_H$	-	-	-	-	
001324$_H$	-		-		

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
$002028_{H,}$ $00202C_{H}$	-		-		CAN 0 64msb
$002030_{H,}$ 002034_{H}	Reserved (IF1 data mirror)				
$002038_{H,}$ $00203C_{H}$	-		-		
002040_{H}	IF2CREQ0[R/W] B,H,W 0------- 00000001		IF2CMSK0[R/W] B,H,W -------- 00000000		
002044_{H}	IF2MSK20[R/W] B,H,W 11-11111 11111111		IF2MSK10[R/W] B,H,W 11111111 11111111		
002048_{H}	IF2ARB20[R/W] B,H,W 00000000 00000000		IF2ARB10[R/W] B,H,W 00000000 00000000		
$00204C_{H}$	IF2MCTR0[R/W] B,H,W 00000000 0---0000		-		
002050_{H}	IF2DTA10[R/W] B,H,W 00000000 00000000		IF2DTA20[R/W] B,H,W 00000000 00000000		
002054_{H}	IF2DTB10[R/W] B,H,W 00000000 00000000		IF2DTB20[R/W] B,H,W 00000000 00000000		
$002058_{H,}$ $00205C_{H}$	-		-		
$002060_{H,}$ 002064_{H}	Reserved (IF2 data mirror)				
002068_{H} | $00207C_{H}$	-		-		
002080_{H}	TREQR20[R] B,H,W 00000000 00000000		TREQR10[R] B,H,W 00000000 00000000		
002084_{H}	TREQR40[R] B,H,W 00000000 00000000		TREQR30[R] B,H,W 00000000 00000000		
002088_{H}	-		-		
$00208C_{H}$	-		-		
002090_{H}	NEWDT20[R] B,H,W 00000000 00000000		NEWDT10[R] B,H,W 00000000 00000000		
002094_{H}	NEWDT40[R] B,H,W 00000000 00000000		NEWDT30[R] B,H,W 00000000 00000000		
002098_{H}	-		-		
$00209C_{H}$	-		-		
$0020A0_{H}$	INTPND20[R] B,H,W 00000000 00000000		INTPND10[R] B,H,W 00000000 00000000		
$0020A4_{H}$	INTPND40[R] B,H,W 00000000 00000000		INTPND30[R] B,H,W 00000000 00000000		
$0020A8_{H}$	-		-		
$0020AC_{H}$	-		-		

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
000120_H	IRPR0H[R] B,H,W 00------	IRPR0L[R] B,H,W 00------	IRPR1H[R] B,H,W 00------	IRPR1L[R] B,H,W --------	Interrupt request batch read register
000124_H	IRPR2H[R] B,H,W --------	IRPR2L[R] B,H,W *5 0000----	IRPR3H[R] B,H,W 00------	IRPR3L[R] B,H,W 00------	
000128_H	IRPR4H[R] B,H,W 00------	IRPR4L[R] B,H,W 000000--	IRPR5H[R] B,H,W 00------	IRPR5L[R] B,H,W 00------	
$00012C_H$	IRPR6H[R] B,H,W 0000----	IRPR6L[R] B,H,W 00------	IRPR7H[R] B,H,W 00------	IRPR7L[R] B,H,W --------	
000130_H	IRPR8H[R] B,H,W --------	IRPR8L[R] B,H,W 00------	IRPR9H[R] B,H,W 00------	IRPR9L[R] B,H,W 00------	
000134_H	IRPR10H[R] B,H,W 00------	IRPR10L[R] B,H,W 00------	IRPR11H[R] B,H,W 00------	IRPR11L[R] B,H,W 0000000-	
000138_H	IRPR12H[R] B,H,W 0000000-	IRPR12L[R] B,H,W 00000000	IRPR13H[R] B,H,W 0000000-	IRPR13L[R] B,H,W ---00---	
$00013C_H$	IRPR14H[R] B,H,W 00------	IRPR14L[R] B,H,W 00------	IRPR15H[R] B,H,W 00000000	IRPR15L[R] B,H,W 0000----	
000140_H	IRPR16H[R] B,H,W 00------	IRPR16L[R] B,H,W --------	IRPR17H[R] B,H,W --------	IRPR17L[R] B,H,W --------	
000144_H	IRPR18H[R]B,H,W --------	IRPR18L[R]B,H,W 000000--	-	-	
000148_H | $0001FC_H$	-	-	-	-	Reserved
000200_H	PCN0[R/W] B,H,W 00000000 000000-0		PCSR0[W] H,W XXXXXXXX XXXXXXXX		PPG0
000204_H	PDUT0[W] H,W XXXXXXXX XXXXXXXX		PTMR0[R] H,W 11111111 11111111		
000208_H	PCN1[R/W] B,H,W 00000000 000000-0		PCSR1[W] H,W XXXXXXXX XXXXXXXX		PPG1
$00020C_H$	PDUT1[W] H,W XXXXXXXX XXXXXXXX		PTMR1[R] H,W 11111111 11111111		
000210_H	PCN2[R/W] B,H,W 00000000 000000-0		PCSR2[W] H,W XXXXXXXX XXXXXXXX		PPG2
000214_H	PDUT2[W] H,W XXXXXXXX XXXXXXXX		PTMR2[R] H,W 11111111 11111111		
000218_H	PCN3[R/W] B,H,W 00000000 000000-0		PCSR3[W] H,W XXXXXXXX XXXXXXXX		PPG3
$00021C_H$	PDUT3[W] H,W XXXXXXXX XXXXXXXX		PTMR3[R] H,W 11111111 11111111		

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
0004E8$_H$	PLL2DIVM[R/W] B,H,W ----0000	PLL2DIVN[R/W] B,H,W -0000000	PLL2DIVG[R/W] B,H,W ----0000	PLL2MULG[R/W] B,H,W 00000000	FlexRay clock control *5
0004EC$_H$	PLL2CTRL[R/W] B,H,W ----0000	PLL2DIVK[R/W] B,H,W -------0	CLKR2[R/W] B,H,W 000--000	-	
0004F0$_H$ | 0004FC$_H$	-	-	-	-	Reserved
000500$_H$	-				Reserved
000504$_H$	-				Reserved
000508$_H$ | 00050C$_H$	-	-	-	-	Reserved
000510$_H$	CSELR[R/W] B,H,W -0----00	CMONR[R] B,H,W -01---00	MTMCR[R/W] B,H,W 00001111	-	Clock control [S]
000514$_H$	PLLCR[R/W] B,H,W 00-00000 11110000		CSTBR[R/W] B,H,W ----0000	PTMCR[R/W] B,H,W 00------	
000518$_H$	-	-	CPUAR[R/W] B,H,W 0---XXXX	-	Reset [S]
00051C$_H$	-		-	-	Reserved [S]
000520$_H$	CCPSSELR[R/W] B,H,W -------0	-	-	CCPSDIVR[R/W] B,H,W -000-000	Clock control 2
000524$_H$	-	CCPLLFBR[R/W] B,H,W -0000000	CCSSFBR0[R/W] B,H,W --000000	CCSSFBR1[R/W] B,H,W ---00000	
000528$_H$	-	CCSSCCR0[R/W] B,H,W ----0000	CCSSCCR1[R/W] B,H,W 000----- --------		
00052C$_H$	-	CCCGRCR0[R/W] B,H,W 00----00	CCCGRCR1[R/W] B,H,W 00000000	CCCGRCR2[R/W] B,H,W 00000000	
000530$_H$	-	-	CCPMUCR0[R/W] B,H,W 0-----00	CCPMUCR1[R/W] B,H,W 0--00000	
000534$_H$	-	-	-	-	
000538$_H$	-	-	-	-	
00053C$_H$	-	-	-	-	
000540$_H$ | 00054C$_H$	-	-	-	-	Reserved
000550$_H$	EIRR0[R/W] B,H,W -XXXXXXX	ENIR0[R/W] B,H,W -0000000	ELVR0[R/W] B,H,W --000000 00000000		External interrupt (INT0 to 6)

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
001234$_H$	ADTCS8[R/W] B,H,W 00000000 0010-000		ADTCS9[R/W] B,H,W 00000000 0010-000		12-bit A/D converter
001238$_H$	ADTCS10[R/W] B,H,W 00000000 0010-000		ADTCS11[R/W] B,H,W 00000000 0010-000		
00123C$_H$	ADTCS12[R/W] B,H,W 00000000 0010-000		ADTCS13[R/W] B,H,W 00000000 0010-000		
001240$_H$	ADTCS14[R/W] B,H,W 00000000 0010-000		-		
001244$_H$	-		-		
001248$_H$	-		ADTCS19[R/W] B,H,W 00000000 00100000		
00124C$_H$	ADTCS20[R/W] B,H,W 00000000 00100000		-		
001250$_H$	-		-		
001254$_H$	-	-	-	-	
001258$_H$	-	-	-	-	
00125C$_H$	-	-	-	-	
001260$_H$	-	-	-	-	
001264$_H$	ADTCD0[R] B,H,W 10--0000 00000000		ADTCD1[R] B,H,W 10--0000 00000000		
001268$_H$	ADTCD2[R] B,H,W 10--0000 00000000		ADTCD3[R] B,H,W 10--0000 00000000		
00126C$_H$	ADTCD4[R] B,H,W 10--0000 00000000		ADTCD5[R] B,H,W 10--0000 00000000		
001270$_H$	ADTCD6[R] B,H,W 10--0000 00000000		ADTCD7[R] B,H,W 10--0000 00000000		
001274$_H$	ADTCD8[R] B,H,W 10--0000 00000000		ADTCD9[R] B,H,W 10--0000 00000000		
001278$_H$	ADTCD10[R] B,H,W 10--0000 00000000		ADTCD11[R] B,H,W 10--0000 00000000		
00127C$_H$	ADTCD12[R] B,H,W 10--0000 00000000		ADTCD13[R] B,H,W 10--0000 00000000		
001280$_H$	ADTCD14[R] B,H,W 10--0000 00000000		-		
001284$_H$	-		-		
001288$_H$	-		ADTCD19[R] B,H,W 10--0000 00000000		
00128C$_H$	ADTCD20[R] B,H,W 10--0000 00000000		-		
001290$_H$	-		-		
001294$_H$	-	-	-	-	
001298$_H$	-	-	-	-	

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
003100_H	BUSDIGSR0[R/W] H,W 00000000 0-----00		BUSDIGSR1[R/W] H,W 00000000 0-----00		Bus diagnosis
003104_H	BUSDIGSR2[R/W] H,W 00000000 0-----00		BUSTSTR0[R/W] H,W 00--0000 00000000		
003108_H	BUSADR0[R] W 00000000 00000000 00000000 00000000				
$00310C_H$	BUSADR1[R] W 00000000 00000000 00000000 00000000				
003110_H	BUSADR2[R] W 00000000 00000000 00000000 00000000				
003114_H	-		BUSDIGSR3[R/W] H,W 00000000 0-----00		
003118_H	BUSDIGSR4[R/W] H,W 00000000 0-----00		BUSTSTR1[R/W] H,W 00--0000 00000000		
$00311C_H$	-				
003120_H	BUSADR3[R] W 00000000 00000000 00000000 00000000				
003124_H	BUSADR4[R] W 00000000 00000000 00000000 00000000				
003128_H | $003FFC_H$	-	-	-	-	Reserved
004000_H | $005FFC_H$	Backup RAM				Backup RAM area
006000_H | $00CFFC_H$	-	-	-	-	Reserved
$00D000_H$	CIF0[R] W 00000100 11111111 01011011 11111111				FlexRay CIF [*5]
$00D004_H$	CIF1[R/W] W 00000000 -------0 -0000000 --------				
$00D008_H$ | $00D00C_H$	-	-	-	-	Reserved
$00D010_H$	-				FlexRay GIF [*5]
$00D014_H$	-				
$00D018_H$	-	-	-	-	
$00D01C_H$	LCK[R/W] W -------- -------- -------- 00000000				

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
$00D140_H$	ESID5[R] W -------- -------- 00----00 00000000				FlexRay GTU [*5]
$00D144_H$	ESID6[R] W -------- -------- 00----00 00000000				
$00D148_H$	ESID7[R] W -------- -------- 00----00 00000000				
$00D14C_H$	ESID8[R] W -------- -------- 00----00 00000000				
$00D150_H$	ESID9[R] W -------- -------- 00----00 00000000				
$00D154_H$	ESID10[R] W -------- -------- 00----00 00000000				
$00D158_H$	ESID11[R] W -------- -------- 00----00 00000000				
$00D15C_H$	ESID12[R] W -------- -------- 00----00 00000000				
$00D160_H$	ESID13[R] W -------- -------- 00----00 00000000				
$00D164_H$	ESID14[R] W -------- -------- 00----00 00000000				
$00D168_H$	ESID15[R] W -------- -------- 00----00 00000000				
$00D16C_H$	-				
$00D170_H$	OSID1[R] W -------- -------- 00----00 00000000				
$00D174_H$	OSID2[R] W -------- -------- 00----00 00000000				
$00D178_H$	OSID3[R] W -------- -------- 00----00 00000000				
$00D17C_H$	OSID4[R] W -------- -------- 00----00 00000000				
$00D180_H$	OSID5[R] W -------- -------- 00----00 00000000				
$00D184_H$	OSID6[R] W -------- -------- 00----00 00000000				
$00D188_H$	OSID7[R] W -------- -------- 00----00 00000000				
$00D18C_H$	OSID8[R] W -------- -------- 00----00 00000000				
$00D190_H$	OSID9[R] W -------- -------- 00----00 00000000				
$00D194_H$	OSID10[R] W -------- -------- 00----00 00000000				

Interrupt factor	Interrupt number		Interrupt level	Offset	TBR default address	RN*1	Interrupt request batch read target
	Decimal	Hexa decimal					
ICU 0 (fetching) / ICU 1 (fetching)	45	2D	ICR29	348_H	$000FFF48_H$	29	○
ICU 2 (fetching) / ICU 3 (fetching)	46	2E	ICR30	344_H	$000FFF44_H$	30	○
*4	47	2F	ICR31	340_H	$000FFF40_H$	-	-
*4	48	30	ICR32	$33C_H$	$000FFF3C_H$	-	-
OCU 0 (match) / OCU 1 (match)	49	31	ICR33	338_H	$000FFF38_H$	33	○
OCU 2 (match) / OCU 3 (match)	50	32	ICR34	334_H	$000FFF34_H$	34	○
OCU 4 (match) / OCU 5 (match)	51	33	ICR35	330_H	$000FFF30_H$	35	○
OCU 6 (match) / OCU 7 (match)	52	34	ICR36	$32C_H$	$000FFF2C_H$	36	○
OCU 8 (match) / OCU 9 (match)	53	35	ICR37	328_H	$000FFF28_H$	37	○
OCU 10 (match) / OCU 11 (match)	54	36	ICR38	324_H	$000FFF24_H$	38	○
WG dead timer underflow 0 / 1 / 2 WG dead timer reload 0 / 1 / 2 WG DTTI 0	55	37	ICR39	320_H	$000FFF20_H$	39	○
WG dead timer underflow 3 / 4 / 5 WG dead timer reload 3 / 4 / 5 WG DTTI 1	56	38	ICR40	$31C_H$	$000FFF1C_H$	40	○
AD converter 0 / 1 / 2 / 3 / 4 / 5 / 6 / 7	57	39	ICR41	318_H	$000FFF18_H$	41	○
AD converter 8 / 9 / 10 / 11 / 12 / 13 / 14	58	3A	ICR42	314_H	$000FFF14_H$	42	○
AD converter 19 / 20	59	3B	ICR43	310_H	$000FFF10_H$	43	○
Base timer 0 IRQ 0/ base timer 0 IRQ 1	60	3C	ICR44	$30C_H$	$000FFF0C_H$	44	○
Base timer 1 IRQ 0/ base timer 1 IRQ 1	61	3D	ICR45	308_H	$000FFF08_H$	45	○
DMAC 0 / 1 / 2 / 3 / 4 / 5 / 6 / 7	62	3E	ICR46	304_H	$000FFF04_H$	-	○
Delay interrupt	63	3F	ICR47	300_H	$000FFF00_H$	-	-
System reserved	64	40	-	$2FC_H$	$000FFEFC_H$	-	-
System reserved	65	41	-	$2F8_H$	$000FFEF8_H$	-	-
Used with the INT instruction.	66 | 255	42 | FF	-	$2F4_H$ | 000_H	$000FFEF4_H$ | $000FFC00_H$	-	-

(T_A: Recommended operating conditions, Vcc=5.0V±10%, V_{SS}= AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"L" level output voltage	V_{OL1}	P000 to P007*, P010 to P017, P020 to P027, P030 to P037, P040 to P047, P050 to P056, P060 to P066*, P070 to P072, P080 to P087*, P090 to P092*, P093, P094, P095 to P097*, P100 to P102*	Vcc=4.5V I_{OL}=2.0mA	0	-	0.4	V	
	V_{OL2}	P021 to P023, P025 to P027	Vcc=4.5V I_{OL}=4.0mA	0	-	0.4	V	When FlexRay is selected
	V_{OL3}	P000 to P007*, P010 to P017, P020, P024, P030 to P037, P040 to P047, P050 to P056, P060 to P066*, P070 to P072, P080 to P087*, P090 to P092*, P093, P094, P095 to P097*, P100 to P102*	Vcc=4.5V I_{OL}=5.0mA	0	-	0.4	V	
	V_{OL4}	P040, P041, P063*, P064*, P080*, P081*, P083*,P084*	Vcc=4.5V I_{OL}=3.0mA	0	-	0.4	V	I^2C shared pin (when I^2C is selected)
	V_{OL5}	DEBUGIF	Vcc=2.7V I_{OL}=25.0mA	0	-	0.25	V	

*: Only available with MB91F583AM/F584AM/F585AM

(T_A: Recommended operating conditions, Vcc=5.0V±10%, V_{SS}= AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input Leak Current	I_{IL}	All input pins	Vcc= AV_{CC}=5.5V $V_{SS} < V_I < V_{CC}$	-5	-	+5	µA	
Pull-up resistance	R_{UP1}	RSTX, NMIX	-	25	-	100	kΩ	
	R_{UP2}	P000 to P007*, P010 to P017, P020 to P027, P030 to P037, P040 to P047, P050 to P056, P060 to P066*, P070 to P072, P080 to P087*, P090 to P092*, P093, P094, P095 to P097*, P100 to P102*	When pull-up resistance is selected	25	-	100	kΩ	
Input Capacitor	C_{IN}	Other thanVCC, VSS, AVCC, AVSS, C	-	-	5	15	pF	

*: Only available with MB91F583AM/F584AM/F585AM

Normal synchronous transfer (SCR:SPI=0) and serial clock output signal detect level "L" (SMR:SCINV=1)

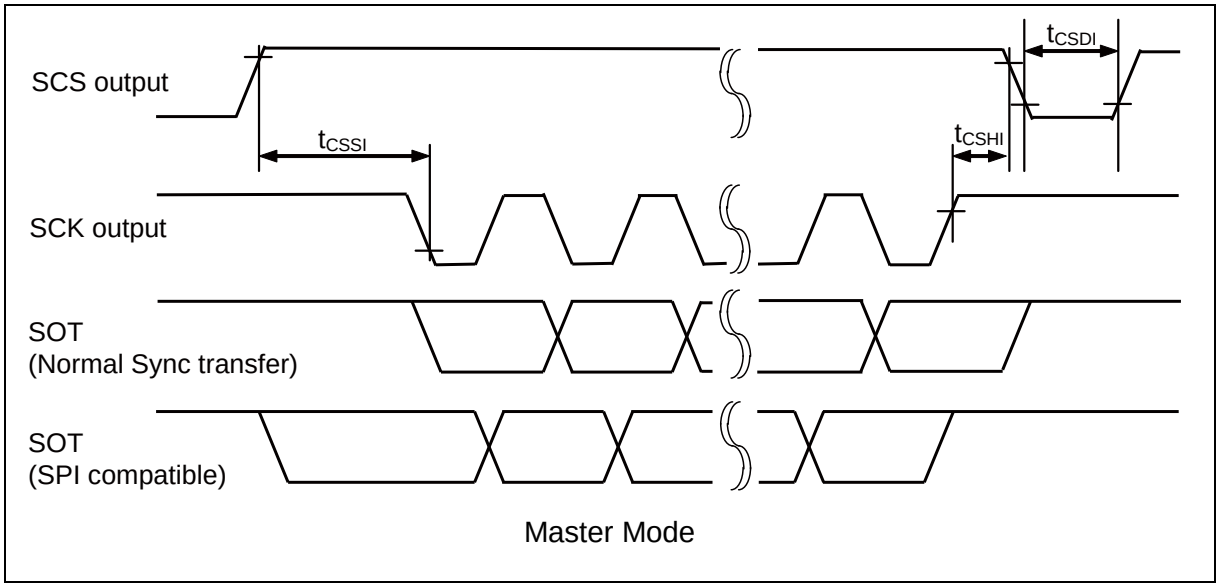
(T_A: Recommended operating conditions, V_{CC} =5.0V±10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK0_0, SCK0_1*, SCK1, SCK2*, SCK3*	Master mode C_L=50pF	$4t_{CPP}$	-	ns	
SCK ↑ ⇒ SOT delay time	t_{SHOVI}	SCK0_0, SCK0_1*, SCK1, SCK2*, SCK3*, SOT0_0, SOT0_1*, SOT1, SOT2*, SOT3*		-30	+30	ns	
Valid SIN ⇒ SCK ↓ setup time	t_{IVSLI}	SCK0_0, SCK0_1*, SCK1, SCK2*, SCK3*, SIN0_0, SIN0_1*, SIN1, SIN2*, SIN3*		30	-	ns	
SCK ↓ ⇒ Valid SIN hold time	t_{SLIXI}			0	-	ns	
Serial clock "H"pulse width	t_{SHSL}	SCK0_0, SCK0_1*, SCK1, SCK2*, SCK3*	Slave mode C_L=50pF	t_{CPP}+10	-	ns	
Serial clock "L"pulse width	t_{SLSH}			$2t_{CPP}$-10	-	ns	
SCK ↑ ⇒ SOT delay time	t_{SHOVE}	SCK0_0, SCK0_1*, SCK1, SCK2*, SCK3*, SOT0_0, SOT0_1*, SOT1, SOT2*, SOT3*		-	30	ns	
Valid SIN ⇒ SCK ↓ setup time	t_{IVSLE}	SCK0_0, SCK0_1*, SCK1, SCK2*, SCK3*, SIN0_0, SIN0_1*, SIN1, SIN2*, SIN3*		10	-	ns	
SCK ↓ ⇒ Valid SIN hold time	t_{SLIXE}			20	-	ns	
SCK fall time	t_F	SCK0_0, SCK0_1*, SCK1, SCK2*, SCK3*		-	5	ns	
SCK rise time	t_R	SCK0_0, SCK0_1*, SCK1, SCK2*, SCK3*		-	5	ns	

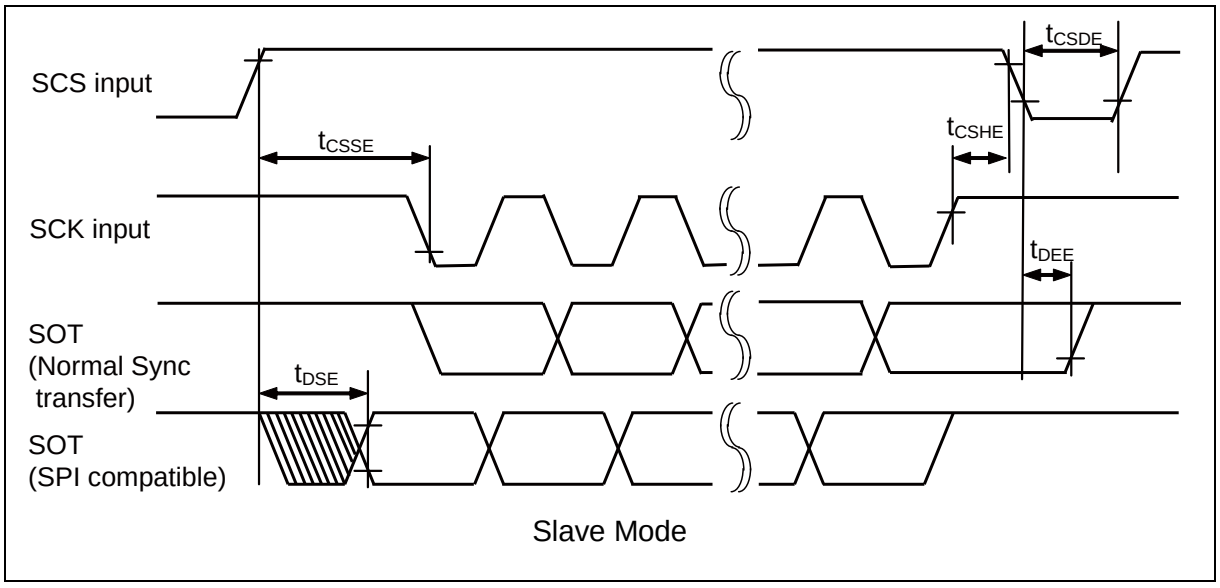
*: Only available with MB91F583AM/F584AM/F585AM

Notes:

- This is the AC characteristic in CLK synchronized mode.
- C_L is the load capacitance applied to pins during testing.
- The maximum baud rate is limited by the internal operation clock used and other parameters. See Hardware Manual for details.



Master Mode



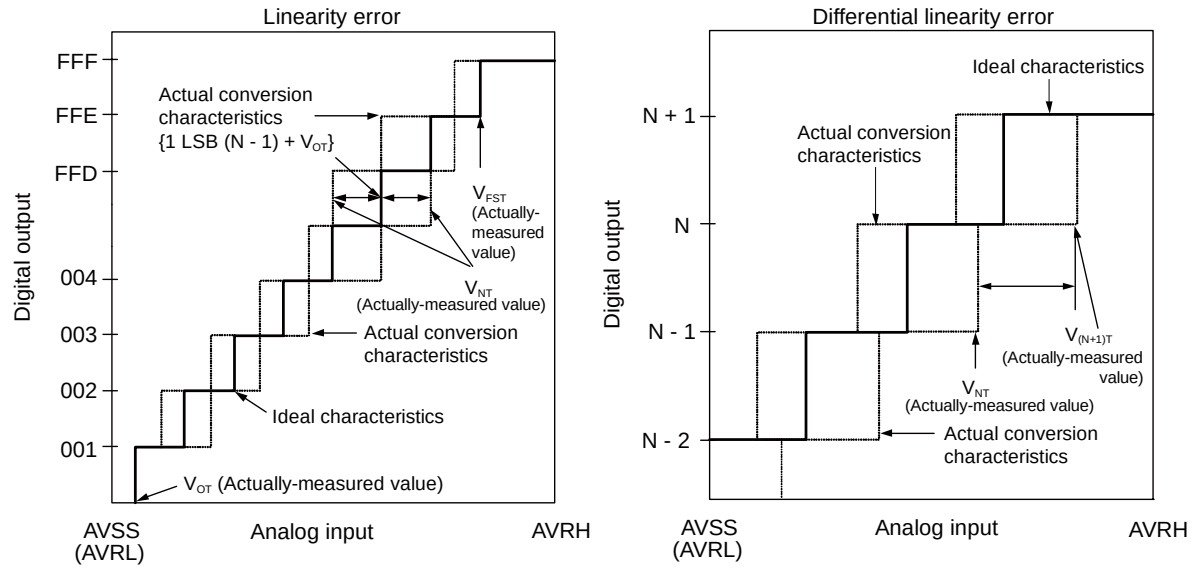
Slave Mode

11.5.2 Definition of Terms

Resolution: Analog variation that is recognized by an A/D converter.

Linearity error : Deviation of the actual conversion characteristics from a straight line that connects the zero transition point ("0000 0000 0000"←→"0000 0000 0001") to the full-scale transition point ("1111 1111 1110"←→"1111 1111 1111").

Differential linearity error: Deviation of the input voltage from the ideal value that is required to change the output code by 1LSB.



$$\text{Linearity error of digital output N} = \frac{V_{NT} - \{1LSB \times (N-1) + V_{OT}\}}{1LSB} \quad [LSB]$$

$$\text{Differential linearity error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1LSB} - 1\ LSB \quad [LSB]$$

$$1LSB = \frac{V_{FST} - V_{OT}}{4094} \quad [V]$$

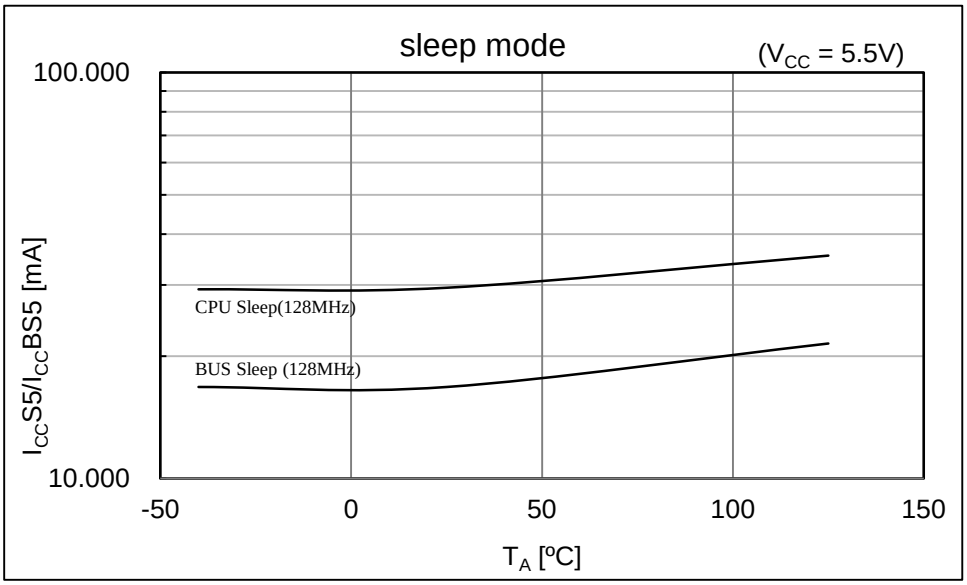
V_{OT}: Voltage at which the digital output changes from "000_H" to "001_H".

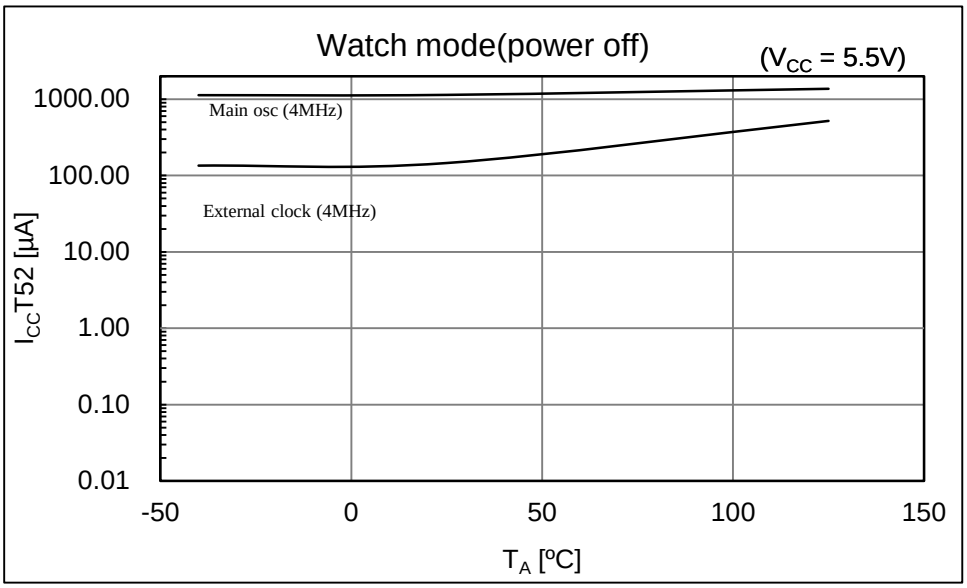
V_{FST}: Voltage at which the digital output changes from "FFE_H" to "FFF_H".

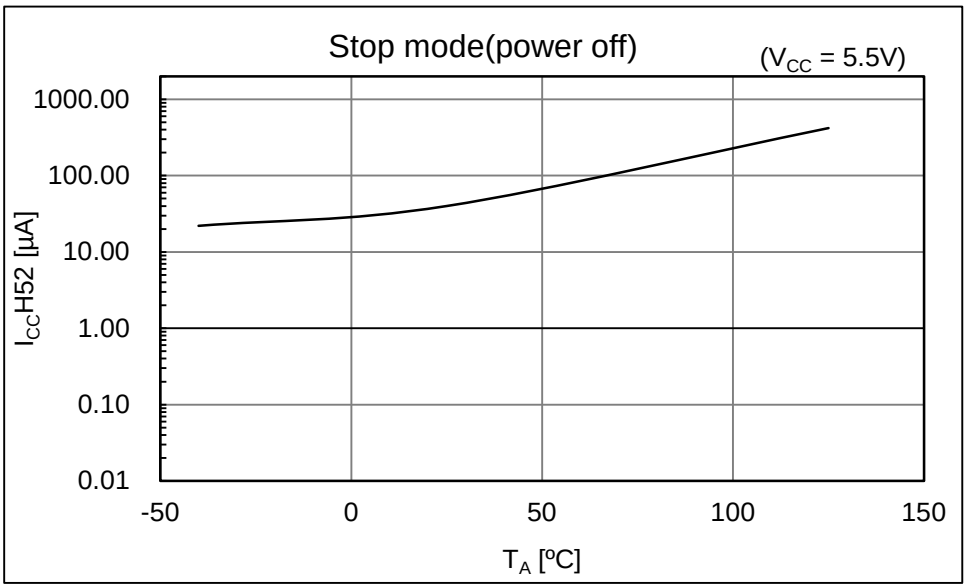
11.5.3 Notes on Using A/D Converter

<About the output impedance of the analog input of external circuit>

When the external impedance is too high, the sampling time for analog voltages may not be sufficient. In this case, it is recommended to connect the capacitor (approx. 0.1 µF) to the analog input pin.


sleep mode
(V_{CC} = 5.5V)
100.000
10.000
$I_{CC}S5/I_{CC}BS5$ [mA]
CPU Sleep(128MHz)
BUS Sleep (128MHz)
-50
0
50
100
150
T_A [ºC]


Watch mode(power off)
(V_{CC} = 5.5V)
1000.00
100.00
10.00
1.00
0.10
0.01
Main osc (4MHz)
External clock (4MHz)
$I_{CC}T52$ [µA]
-50
0
50
100
150
T_A [ºC]


Stop mode(power off)
(V_{CC} = 5.5V)
1000.00
100.00
10.00
1.00
0.10
0.01
$I_{CC}H52$ [µA]
-50
0
50
100
150
T_A [ºC]