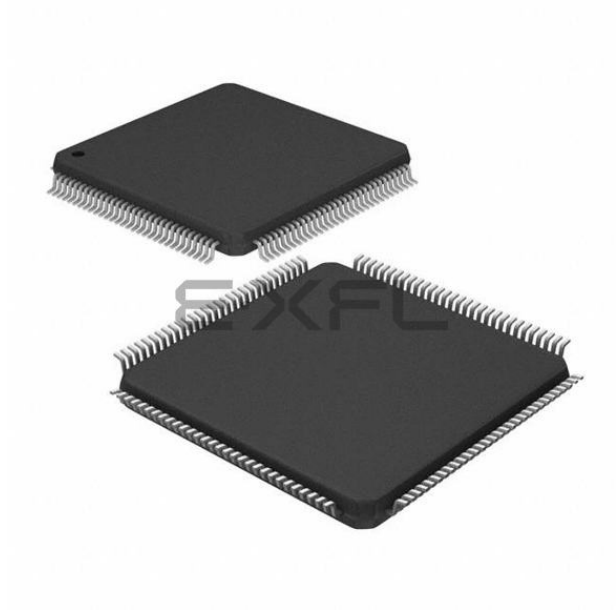
Cypress Semiconductor Corp - MB9BF416RPMC-G-JNE2 Datasheet



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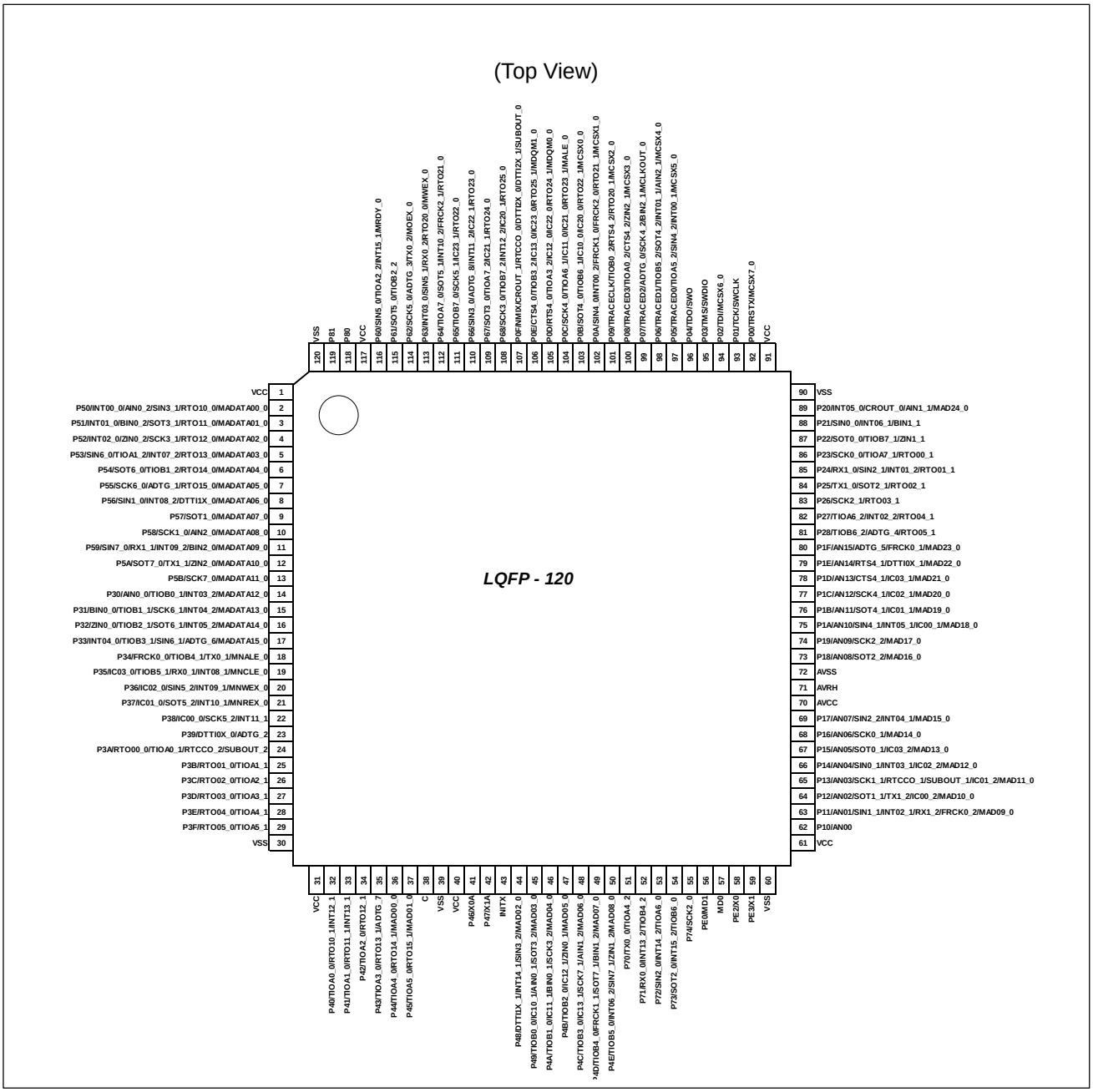
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	144MHz
Connectivity	CANbus, CSIO, EBI/EMI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	103
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	120-LQFP
Supplier Device Package	120-LQFP (16x16)
Purchase URL	https://www.e-xfl.com/product-detail/rochester-electronics/mb9bf416rpmc-g-jne2

LQM120-02



Note:

- *The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.*

4. List of Pin Functions

List of pin numbers

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

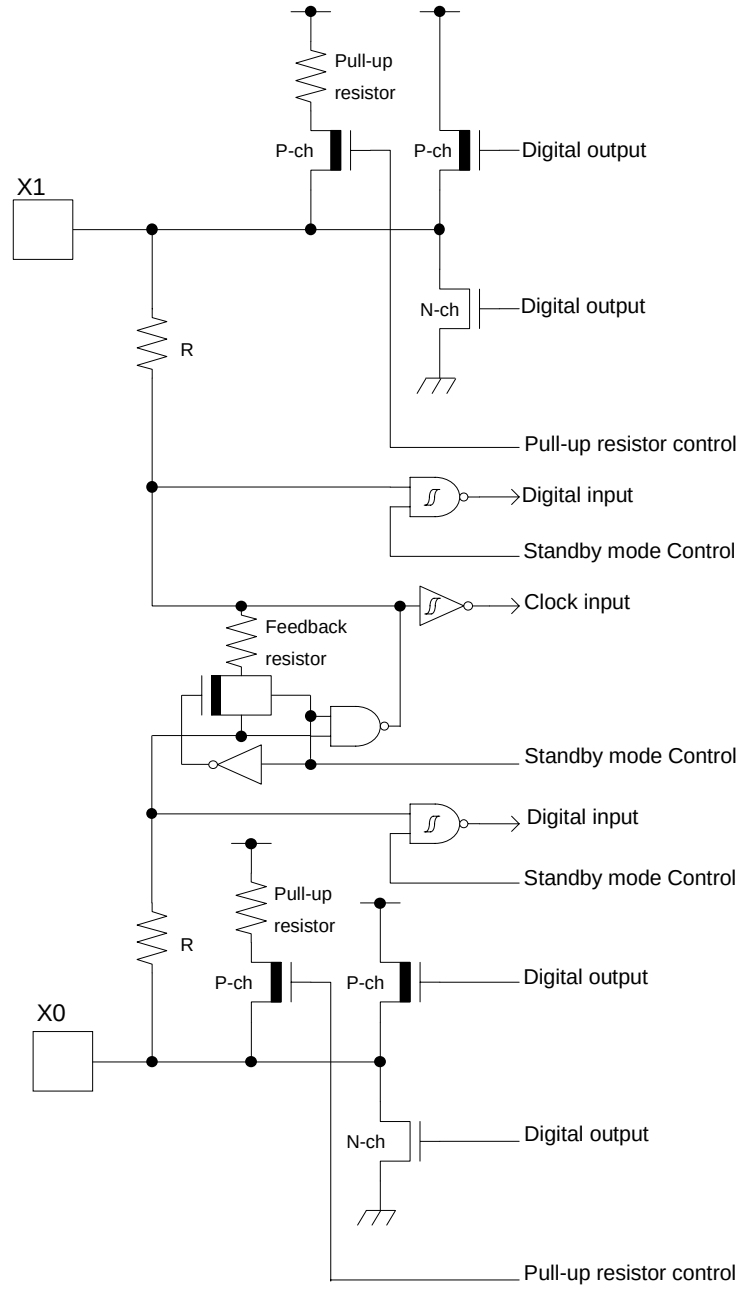
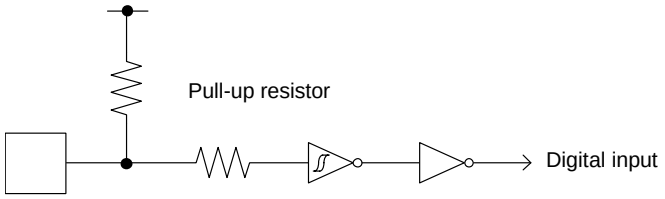
Pin No				Pin Name	I/O circuit type	Pin state type
LQFP-100	FBGA-112	LQFP-120	QFP-100			
1	B1	1	79	VCC	-	
2	C1	2	80	P50 INT00_0 AIN0_2 SIN3_1 RTO10_0 (PPG10_0) MADATA00_0	E	H
3	C2	3	81	P51 INT01_0 BIN0_2 SOT3_1 (SDA3_1) RTO11_0 (PPG10_0) MADATA01_0	E	H
4	B3	4	82	P52 INT02_0 ZIN0_2 SCK3_1 (SCL3_1) RTO12_0 (PPG12_0) MADATA02_0	E	H
5	D1	5	83	P53 SIN6_0 TIOA1_2 INT07_2 RTO13_0 (PPG12_0) MADATA03_0	E	H
6	D2	6	84	P54 SOT6_0 (SDA6_0) TIOB1_2 RTO14_0 (PPG14_0) MADATA04_0	E	I
7	D3	7	85	P55 SCK6_0 (SCL6_0) ADTG_1 RTO15_0 (PPG14_0) MADATA05_0	E	I

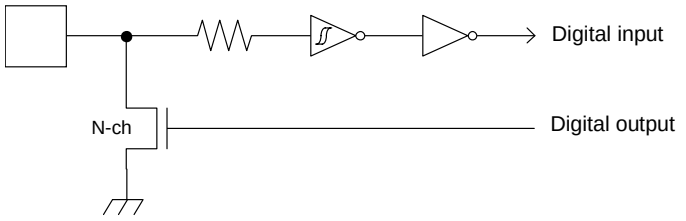
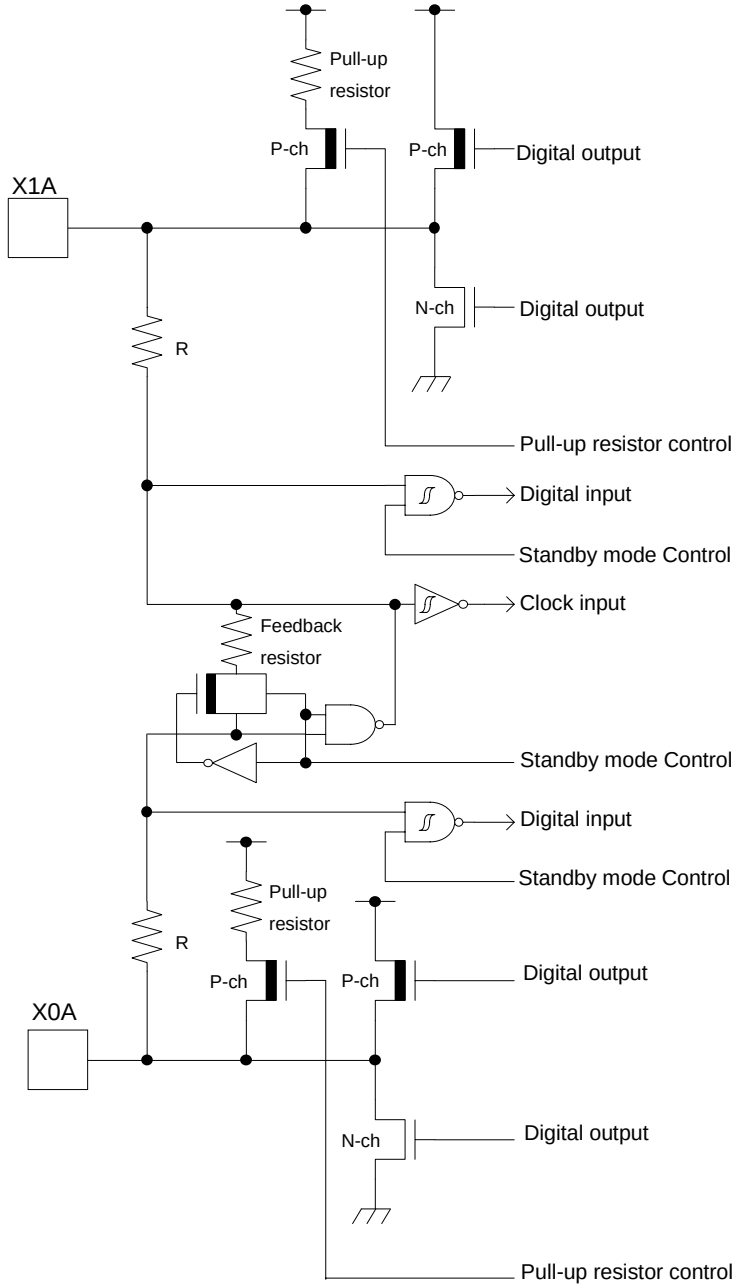
Module	Pin name	Function	Pin No			
			LQFP-100	FBGA-112	LQFP-120	QFP-100
External Interrupt	INT00_0	External interrupt request 00 input pin	2	C1	2	80
	INT00_1		82	C8	97	60
	INT00_2		87	D7	102	65
	INT01_0	External interrupt request 01 input pin	3	C2	3	81
	INT01_1		83	D9	98	61
	INT01_2		-	-	85	-
	INT02_0	External interrupt request 02 input pin	4	B3	4	82
	INT02_1		53	J10	63	31
	INT02_2		-	-	82	-
	INT03_0	External interrupt request 03 input pin	93	D6	113	71
	INT03_1		56	H9	66	34
	INT03_2		9	E1	14	87
	INT04_0	External interrupt request 04 input pin	12	E4	17	90
	INT04_1		59	G9	69	37
	INT04_2		10	E2	15	88
	INT05_0	External interrupt request 05 input pin	74	C10	89	52
	INT05_1		65	F9	75	43
	INT05_2		11	E3	16	89
	INT06_1	External interrupt request 06 input pin	73	C11	88	51
	INT06_2		45	K8	50	23
	INT07_2	External interrupt request 07 input pin	5	D1	5	83
	INT08_1	External interrupt request 08 input pin	14	F2	19	92
	INT08_2		8	D5	8	86
	INT09_1	External interrupt request 09 input pin	15	F3	20	93
	INT09_2		-	-	11	-
	INT10_1	External interrupt request 10 input pin	16	G1	21	94
	INT10_2		-	-	112	-
	INT11_1	External interrupt request 11 input pin	17	G2	22	95
	INT11_2		-	-	110	-
	INT12_1	External interrupt request 12 input pin	27	J4	32	5
	INT12_2		-	-	108	-
	INT13_1	External interrupt request 13 input pin	28	L5	33	6
	INT13_2		-	-	52	-
	INT14_1	External interrupt request 14 input pin	39	K6	44	17
	INT14_2		-	-	53	-
	INT15_1	External interrupt request 15 input pin	96	C4	116	74
	INT15_2		-	-	54	-
	NMIX	Non-Maskable Interrupt input pin	92	B5	107	70

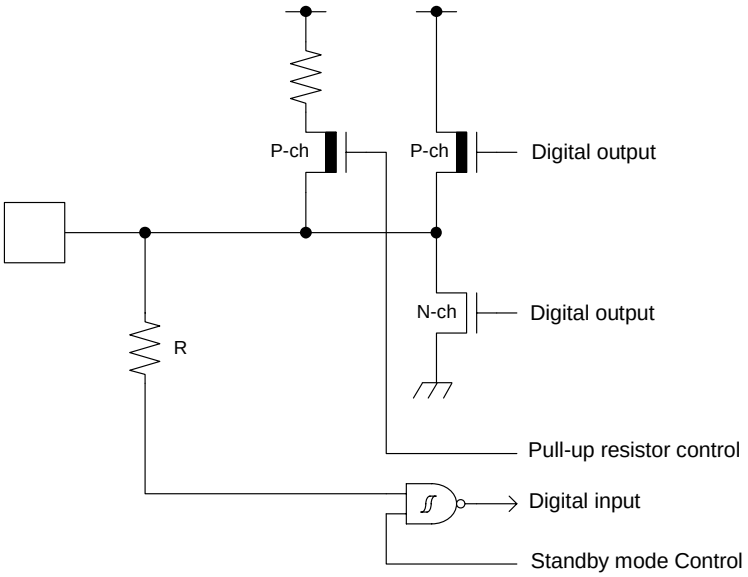
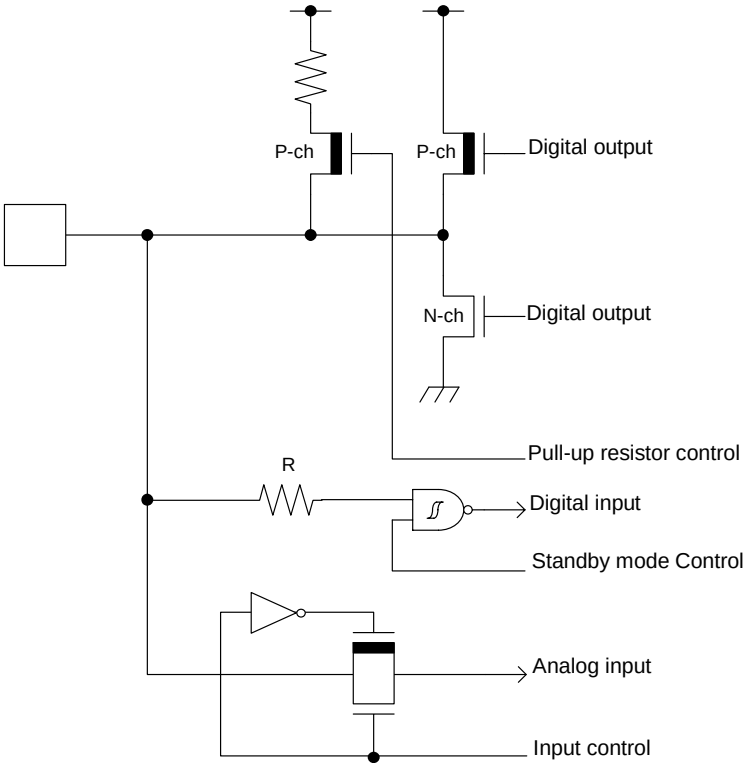
Module	Pin name	Function	Pin No			
			LQFP-100	FBGA-112	LQFP-120	QFP-100
GPIO	P00	General-purpose I/O port 0	77	A9	92	55
	P01		78	B9	93	56
	P02		79	B11	94	57
	P03		80	A8	95	58
	P04		81	B8	96	59
	P05		82	C8	97	60
	P06		83	D9	98	61
	P07		84	A7	99	62
	P08		85	B7	100	63
	P09		86	C7	101	64
	P0A		87	D7	102	65
	P0B		88	A6	103	66
	P0C		89	B6	104	67
	P0D		90	C6	105	68
	P0E		91	A5	106	69
	P0F		92	B5	107	70
	P10	General-purpose I/O port 1	52	J11	62	30
	P11		53	J10	63	31
	P12		54	J8	64	32
	P13		55	H10	65	33
	P14		56	H9	66	34
	P15		57	H7	67	35
	P16		58	G10	68	36
	P17		59	G9	69	37
	P18		63	G8	73	41
	P19		64	F10	74	42
	P1A		65	F9	75	43
	P1B		66	E11	76	44
	P1C		67	E10	77	45
	P1D		68	F8	78	46
	P1E		69	E9	79	47
	P1F		70	D11	80	48
	P20	General-purpose I/O port 2	74	C10	89	52
	P21		73	C11	88	51
	P22		72	E8	87	50
	P23		71	D10	86	49
	P24		-	-	85	-
	P25		-	-	84	-
	P26		-	-	83	-
	P27		-	-	82	-
	P28		-	-	81	-

Module	Pin name	Function	Pin No			
			LQFP-100	FBGA-112	LQFP-120	QFP-100
Multi-function Timer 0	DTTI0X_0	Input signal controlling wave form generator outputs RTO00 to RTO05 of Multi-function timer 0.	18	F4	23	96
	DTTI0X_1		69	E9	79	47
	FRCK0_0	16-bit free-run timer ch.0 external clock input pin	13	F1	18	91
	FRCK0_1		70	D11	80	48
	FRCK0_2		53	J10	63	31
	IC00_0	16-bit input capture ch.0 input pin of Multi-function timer 0. ICxx describes channel number.	17	G2	22	95
	IC00_1		65	F9	75	43
	IC00_2		54	J8	64	32
	IC01_0		16	G1	21	94
	IC01_1		66	E11	76	44
	IC01_2		55	H10	65	33
	IC02_0		15	F3	20	93
	IC02_1		67	E10	77	45
	IC02_2		56	H9	66	34
	IC03_0		14	F2	19	92
	IC03_1		68	F8	78	46
	IC03_2		57	H7	67	35
	RTO00_0 (PPG00_0)	Wave form generator output pin of Multi-function timer 0. This pin operates as PPG00 when it is used in PPG0 output modes.	19	G3	24	97
	RTO00_1 (PPG00_1)		-	-	86	-
	RTO01_0 (PPG00_0)	Wave form generator output pin of Multi-function timer 0. This pin operates as PPG00 when it is used in PPG0 output modes.	20	H1	25	98
	RTO01_1 (PPG00_1)		-	-	85	-
	RTO02_0 (PPG02_0)	Wave form generator output pin of Multi-function timer 0. This pin operates as PPG02 when it is used in PPG0 output modes.	21	H2	26	99
	RTO02_1 (PPG02_1)		-	-	84	-
	RTO03_0 (PPG02_0)	Wave form generator output pin of Multi-function timer 0. This pin operates as PPG02 when it is used in PPG0 output modes.	22	G4	27	100
	RTO03_1 (PPG02_1)		-	-	83	-
	RTO04_0 (PPG04_0)	Wave form generator output pin of Multi-function timer 0. This pin operates as PPG04 when it is used in PPG0 output modes.	23	H3	28	1
	RTO04_1 (PPG04_1)		-	-	82	-
	RTO05_0 (PPG04_0)	Wave form generator output pin of Multi-function timer 0. This pin operates as PPG04 when it is used in PPG0 output modes.	24	J2	29	2
	RTO05_1 (PPG04_1)		-	-	81	-

5. I/O Circuit Type

Type	Circuit	Remarks
A		It is possible to select the main oscillation / GPIO function When the main oscillation is selected. – Oscillation feedback resistor: Approximately 1 MΩ – With Standby mode control When the GPIO is selected. – CMOS level output. – CMOS level hysteresis input – With pull-up resistor control – With standby mode control – Pull-up resistor: Approximately 50 kΩ – I_{OH} = -4 mA, I_{OL} = 4 mA
B		– CMOS level hysteresis input – Pull-up resistor: Approximately 50 kΩ

Type	Circuit	Remarks
C		– Open drain output – CMOS level hysteresis input
D		It is possible to select the sub oscillation / GPIO function When the sub oscillation is selected. – Oscillation feedback resistor: Approximately 5 MΩ – With Standby mode control When the GPIO is selected. – CMOS level output. – CMOS level hysteresis input – With pull-up resistor control – With standby mode control – Pull-up resistor: Approximately 50 kΩ – I_{OH} = -4 mA, I_{OL}= 4 mA

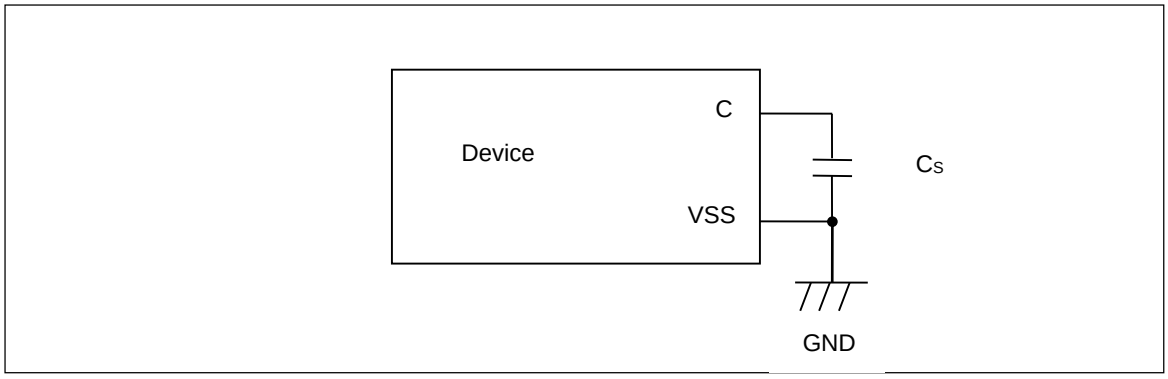
Type	Circuit	Remarks
E		– CMOS level output – CMOS level hysteresis input – With pull-up resistor control – With standby mode control – Pull-up resistor: Approximately 50 kΩ – I_{OH} = -4 mA, I_{OL} = 4 mA – When this pin is used as an I^2C pin, the digital output – P-ch transistor is always off – +B input is available
F		– CMOS level output – CMOS level hysteresis input – With input control – Analog input – With pull-up resistor control – With standby mode control – Pull-up resistor: Approximately 50 kΩ – I_{OH} = -4 mA, I_{OL} = 4 mA – When this pin is used as an I^2C pin, the digital output – P-ch transistor is always off – +B input is available

C Pin

This series contains the regulator. Be sure to connect a smoothing capacitor (CS) for the regulator between the C pin and the GND pin. Please use a ceramic capacitor or a capacitor of equivalent frequency characteristics as a smoothing capacitor.

However, some laminated ceramic capacitors have the characteristics of capacitance variation due to thermal fluctuation (F characteristics and Y5V characteristics). Please select the capacitor that meets the specifications in the operating conditions to use by evaluating the temperature characteristics of a capacitor.

A smoothing capacitor of about 4.7µF would be recommended for this series.



Mode pins (MD0)

Connect the MD pin (MD0) directly to VCC or VSS pins. Design the printed circuit board such that the pull-up/down resistance stays low, as well as the distance between the mode pins and VCC pins or VSS pins is as short as possible and the connection impedance is low, when the pins are pulled-up/down such as for switching the pin level and rewriting the Flash memory data. It is because of preventing the device erroneously switching to test mode due to noise.

Notes on power-on

Turn power on/off in the following order or at the same time.
If not using the A/D converter, connect AVCC = VCC and AVSS = VSS.

Turning on : VCC → AVCC → AVRH

Turning off : AVRH → AVCC → VCC

Serial Communication

There is a possibility to receive wrong data due to the noise or other causes on the serial communication.

Therefore, design a printed circuit board so as to avoid noise.

Consider the case of receiving wrong data due to noise, perform error detection such as by applying a checksum of data at the end. If an error is detected, retransmit the data.

Differences in features among the products with different memory sizes and between Flash products and MASK products

The electric characteristics including power consumption, ESD, latch-up, noise characteristics, and oscillation characteristics among the products with different memory sizes and between Flash products and MASK products are different because chip layout and memory structures are different.

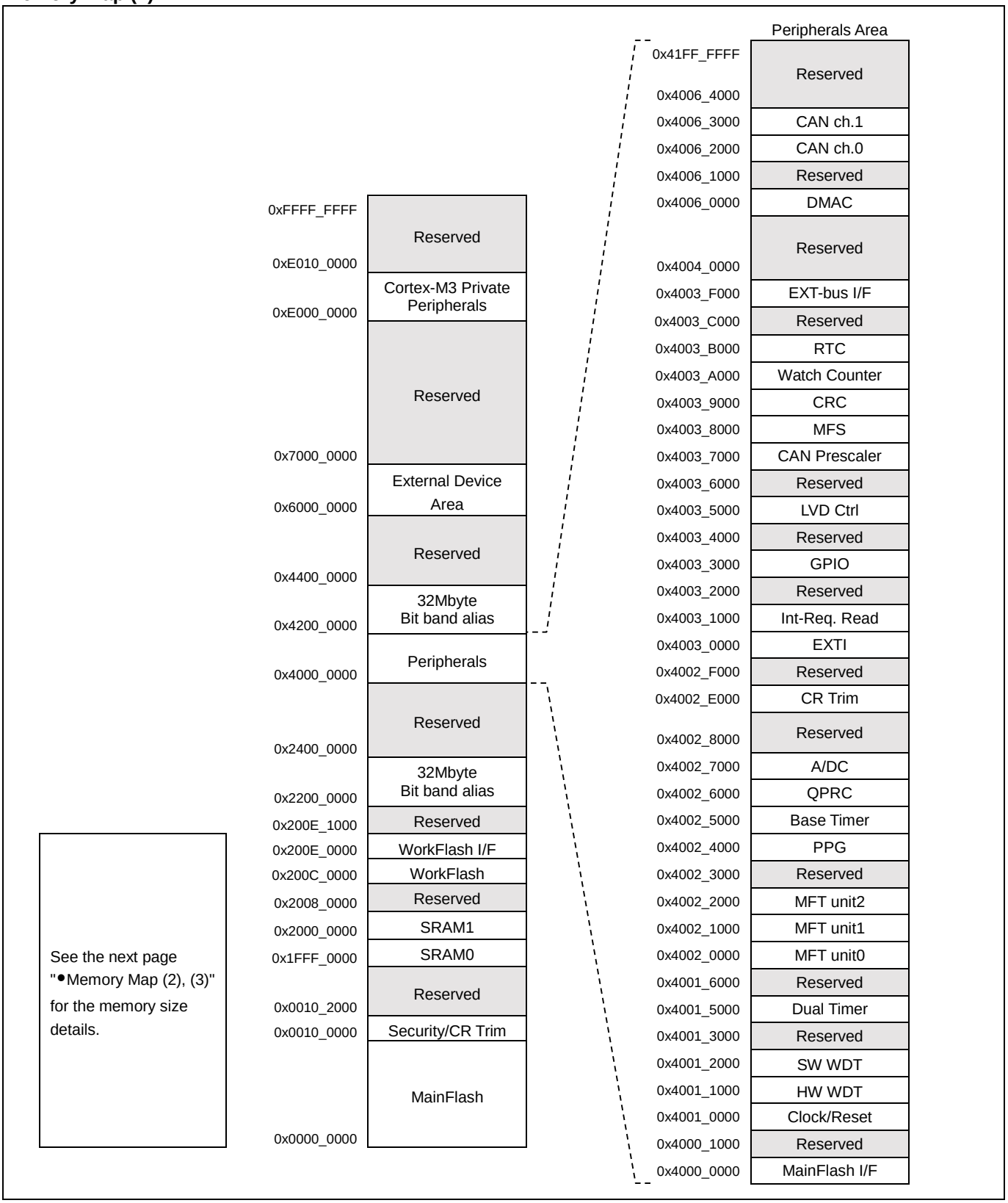
If you are switching to use a different product of the same series, please make sure to evaluate the electric characteristics.

Pull-Up function of 5 V tolerant I/O

Please do not input the signal more than VCC voltage at the time of Pull-Up function use of 5 V tolerant I/O.

10. Memory Map

Memory Map (1)



Pin status type	Function group	Power-on reset or low-voltage detection state	INITX input state	Device internal reset state	Run mode or sleep mode state	Timer mode or sleep mode state	
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable	
		-	INITX=0	INITX=1	INITX=1	INITX=1	
		-	-	-	-	SPL=0	SPL=1
H	External interrupt enabled selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state
	GPIO selected, or other than above resource selected	Hi-Z	Hi-Z/ Input enabled	Hi-Z/ Input enabled			Hi-Z/ Internal input fixed at "0"
I	GPIO selected, resource selected	Hi-Z	Hi-Z/ Input enabled	Hi-Z/ Input enabled	Maintain previous state	Maintain previous state	Hi-Z/ Internal input fixed at "0"
J	NMIX selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state
	GPIO selected, or other than above resource selected	Hi-Z	Hi-Z/ Input enabled	Hi-Z/ Input enabled			Hi-Z/ Internal input fixed at "0"
K	Analog input selected	Hi-Z	Hi-Z/ Internal input fixed at "0"/ Analog input enabled	Hi-Z/ Internal input fixed at "0"/ Analog input enabled	Hi-Z/ Internal input fixed at "0"/ Analog input enabled	Hi-Z/ Internal input fixed at "0"/ Analog input enabled	Hi-Z/ Internal input fixed at "0"/ Analog input enabled
	GPIO selected, or other than above resource selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z/ Internal input fixed at "0"
L	External interrupt enabled selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state
	Analog input selected	Hi-Z	Hi-Z/ Internal input fixed at "0"/ Analog input enabled	Hi-Z/ Internal input fixed at "0"/ Analog input enabled	Hi-Z/ Internal input fixed at "0"/ Analog input enabled	Hi-Z/ Internal input fixed at "0"/ Analog input enabled	Hi-Z/ Internal input fixed at "0"/ Analog input enabled
	GPIO selected, or other than above resource selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z/ Internal input fixed at "0"

Parameter	Symbol	Pin name	Conditions		Value		Unit	Remarks
					Typ*2	Max*2		
Timer mode current	I_{CCT}	VCC	Main Timer mode	T_A = + 25°C, When LVD is off	3.2	6	mA	*1, *3
				T_A = + 85°C, When LVD is off	-	15	mA	*1, *3
			Sub Timer mode	T_A = + 25°C, When LVD is off	0.9	3	mA	*1, *4
				T_A = + 85°C, When LVD is off	-	12	mA	*1, *4
Stop mode current	I_{CCH}		Stop mode	T_A = + 25°C, When LVD is off	0.8	3	mA	*1
				T_A = + 85°C, When LVD is off	-	12	mA	*1

*1: When all ports are fixed.

*2: V_{CC}=5.5 V

*3: When using the crystal oscillator of 4 MHz(Including the current consumption of the oscillation circuit)

*4: When using the crystal oscillator of 32 kHz(Including the current consumption of the oscillation circuit)

Low-Voltage Detection Current

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Typ	Max		
Low voltage detection circuit (LVD) power supply current	I_{CCLVD}	VCC	At operation for interrupt V_{CC} = 5.5 V	4	7	µA	At not detect

Flash Memory Current

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Typ	Max		
Flash memory write/erase current	$I_{CCFLASH}$	VCC	MainFlash At Write/Erase	11.4	13.1	mA	*
			WorkFlash At Write/Erase	11.4	13.1	mA	

*: The current at which to write or erase Flash memory, $I_{CCFLASH}$ is added to I_{CC}.

A/D Converter Current

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = AVRL = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Typ	Max		
Power supply current	I_{CCAD}	AVCC	At 1unit operation	0.47	0.62	mA	
			At stop	0.06	25	µA	
Reference power supply current	I_{CCAVRH}	AVRH	At 1unit operation AVRH=5.5 V	1.1	1.96	mA	
			At stop	0.06	4	µA	

12.4.4 Operating Conditions of Main PLL (In the case of using main clock for input of PLL)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time*1 (LOCK UP time)	t_{LOCK}	100	-	-	µs	
PLL input clock frequency	f_{PLLI}	4	-	16	MHz	
PLL multiple rate	-	13	-	75	multiple	
PLL macro oscillation clock frequency	f_{PLLO}	200	-	300	MHz	
Main PLL clock frequency*2	f_{CLKPLL}	-	-	144	MHz	

*1: Time from when the PLL starts operating until the oscillation stabilizes.

*2: For more information about Main PLL clock (CLKPLL), see CHAPTER 2-1: Clock in FM3 Family PERIPHERAL MANUAL.

12.4.5 Operating Conditions of Main PLL (In the case of using high-speed internal CR)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 85°C)

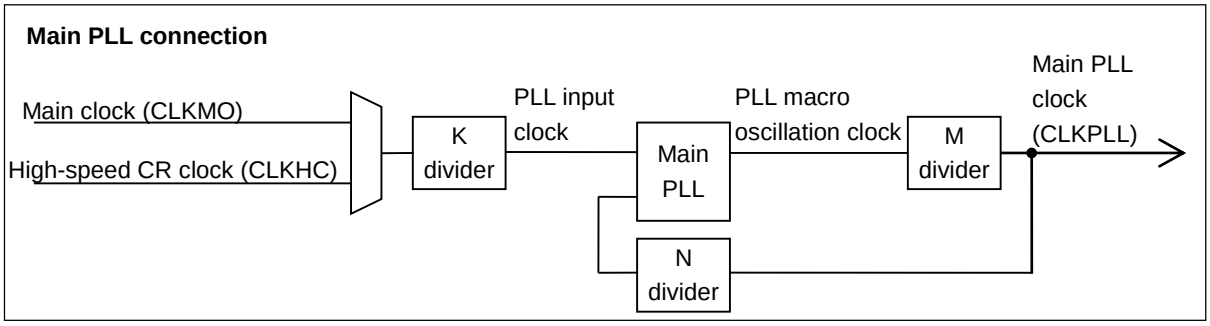
Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time*1 (LOCK UP time)	t_{LOCK}	100	-	-	µs	
PLL input clock frequency	f_{PLLI}	3.8	4	4.2	MHz	
PLL multiple rate	-	50	-	71	multiple	
PLL macro oscillation clock frequency	f_{PLLO}	190	-	300	MHz	
Main PLL clock frequency*2	f_{CLKPLL}	-	-	144	MHz	

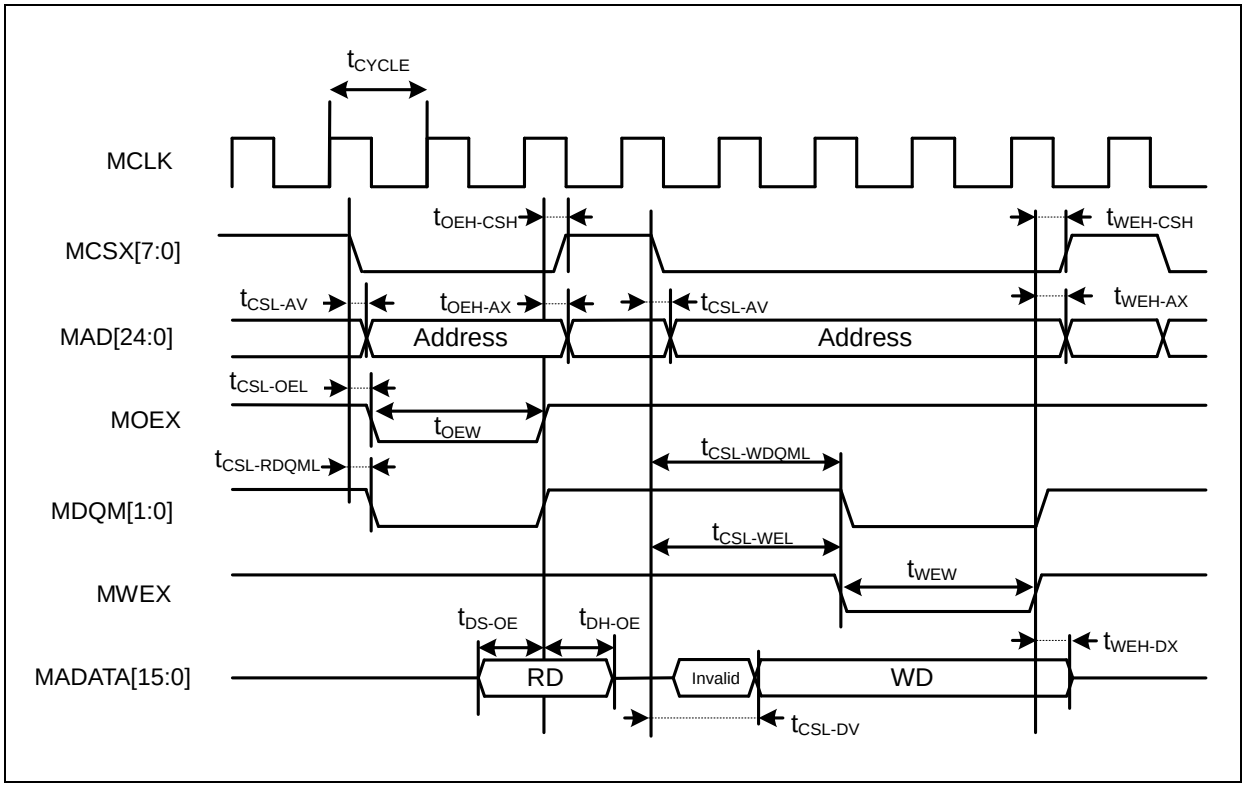
*1: Time from when the PLL starts operating until the oscillation stabilizes.

*2: For more information about Main PLL clock (CLKPLL), see CHAPTER 2-1: Clock in FM3 Family PERIPHERAL MANUAL.

When setting PLL multiple rate, please take the accuracy of the built-in high-speed CR clock into account and prevent the master clock from exceeding the maximum frequency.

Main PLL connection




tCYCLE
MCLK
MCSX[7:0]
MAD[24:0]
MOEX
MDQM[1:0]
MWEX
MADATA[15:0]
tOEH-CSH
tWEH-CSH
tCSL-AV
tOEH-AX
tCSL-AV
tWEH-AX
Address
Address
tCSL-OEL
tOEW
tCSL-RDQML
tCSL-WDQML
tCSL-WEL
tWEW
tDS-OE
tDH-OE
tWEH-DX
RD
Invalid
WD
tCSL-DV

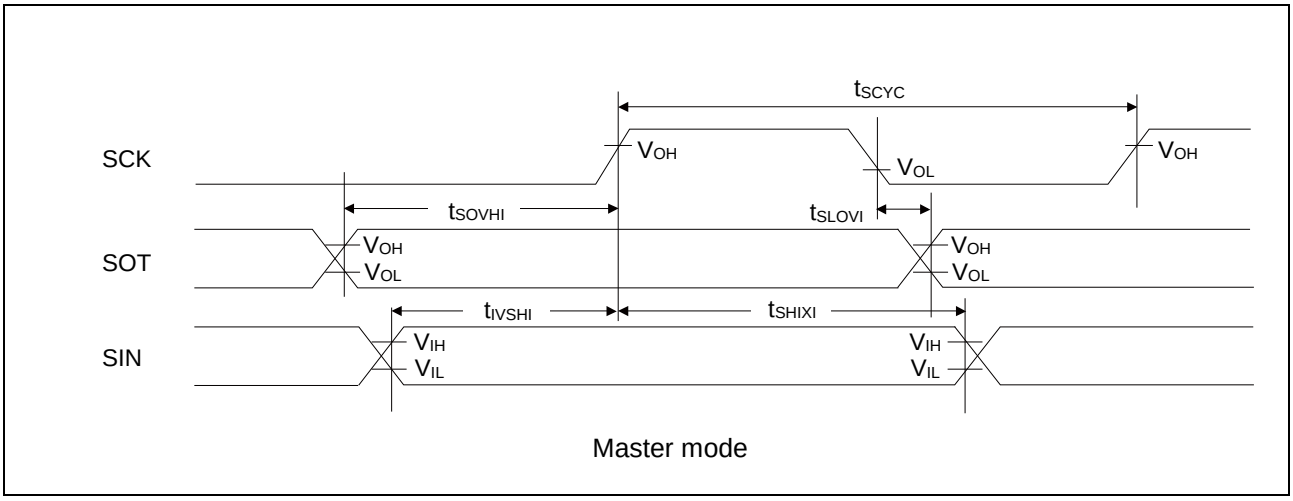
CSIO (SPI = 1, SCINV = 1)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 85°C)

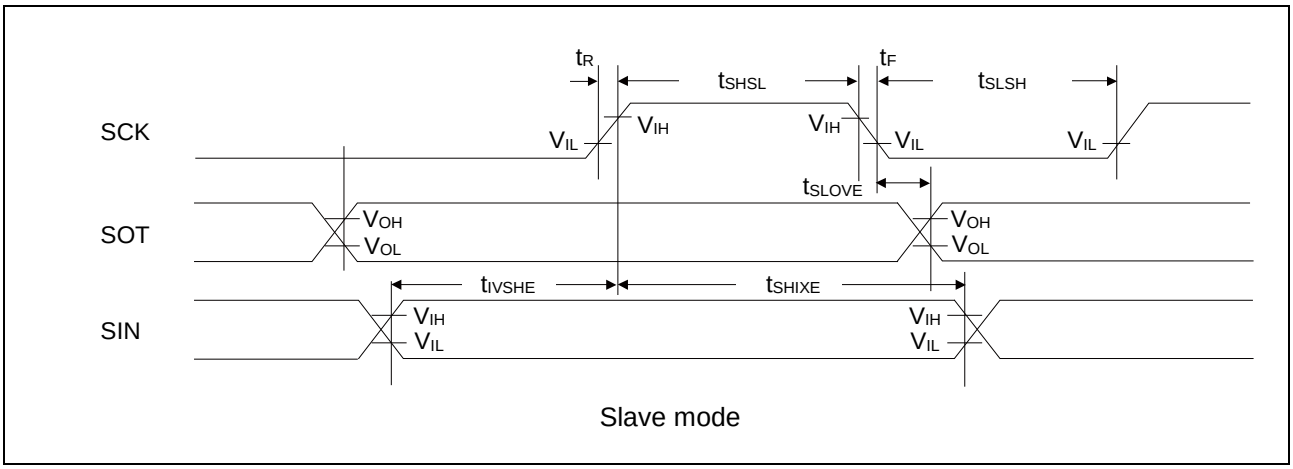
Parameter	Symbol	Pin name	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYC}	SCKx	Master mode	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCKx SOTx		-30	+30	- 20	+ 20	ns
SIN → SCK ↑ setup time	t_{IVSHI}	SCKx SINx		50	-	30	-	ns
SCK ↑ → SIN hold time	t_{SHIXI}	SCKx SINx		0	-	0	-	ns
SOT → SCK ↑ delay time	t_{SOVHI}	SCKx SOTx		$2t_{CYCP}$ - 30	-	$2t_{CYCP}$ - 30	-	ns
Serial clock L pulse width	t_{SLSH}	SCKx	Slave mode	$2t_{CYCP}$ - 10	-	$2t_{CYCP}$ - 10	-	ns
Serial clock H pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK ↓ → SOT delay time	t_{SLOVE}	SCKx SOTx		-	50	-	30	ns
SIN → SCK ↑ setup time	t_{IVSHE}	SCKx SINx		10	-	10	-	ns
SCK ↑ → SIN hold time	t_{SHIXE}	SCKx SINx		20	-	20	-	ns
SCK fall time	t_F	SCKx		-	5	-	5	ns
SCK rise time	t_R	SCKx		-	5	-	5	ns

Notes:

- *The above characteristics apply to CLK synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which Multi-function Serial is connected to, see 8 Block Diagram in this data sheet.
- *These characteristics only guarantee the same relocate port number.*
  For example, the combination of SCKx_0 and SOTx_1 is not guaranteed.
- *When the external load capacitance = 30 pF.*



Master mode

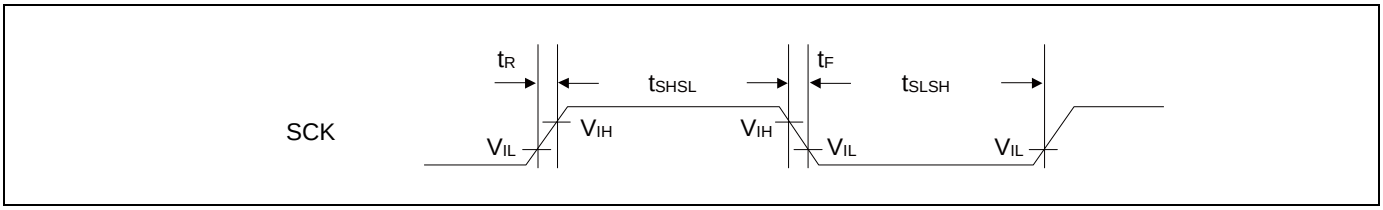


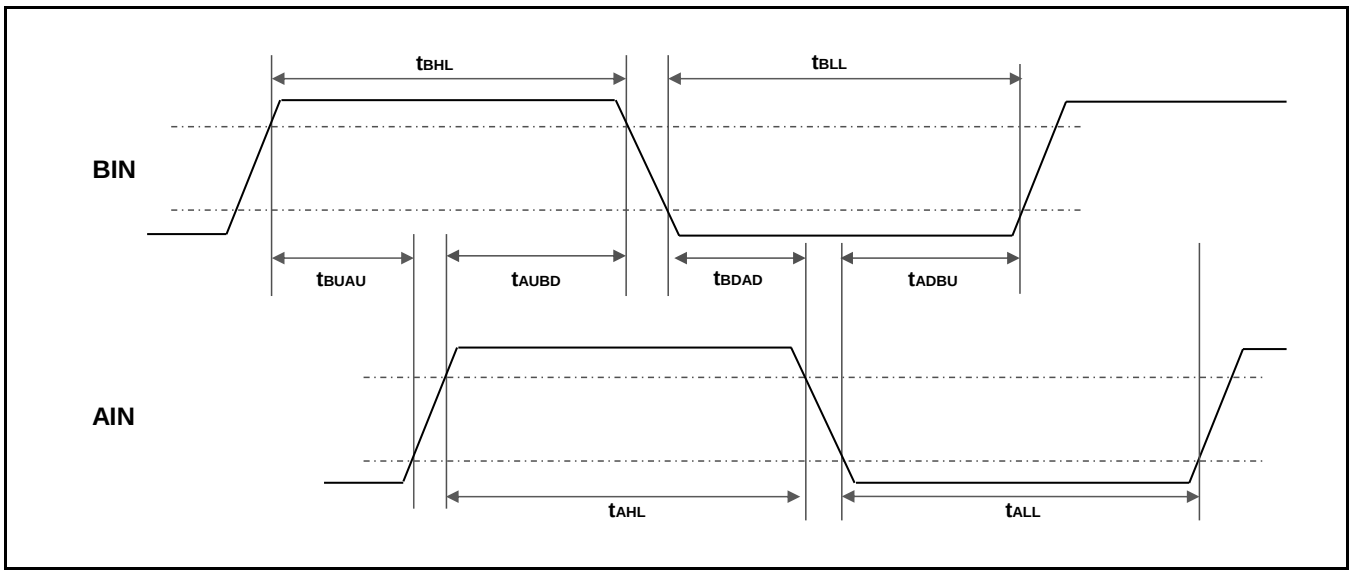
Slave mode

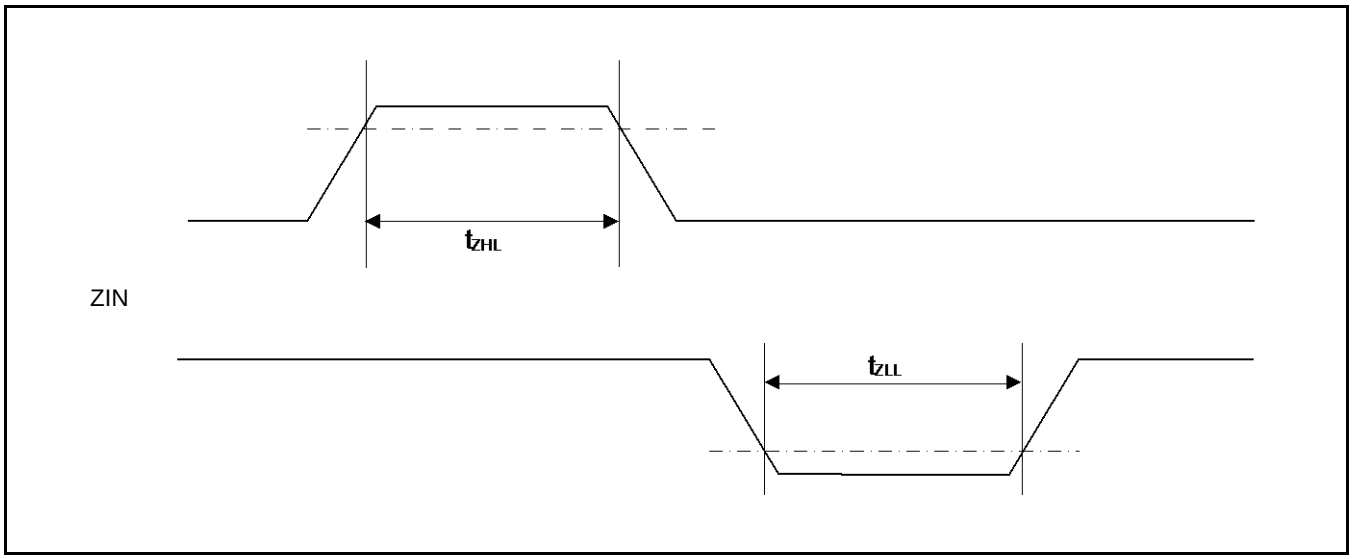
UART external clock input (EXT = 1)

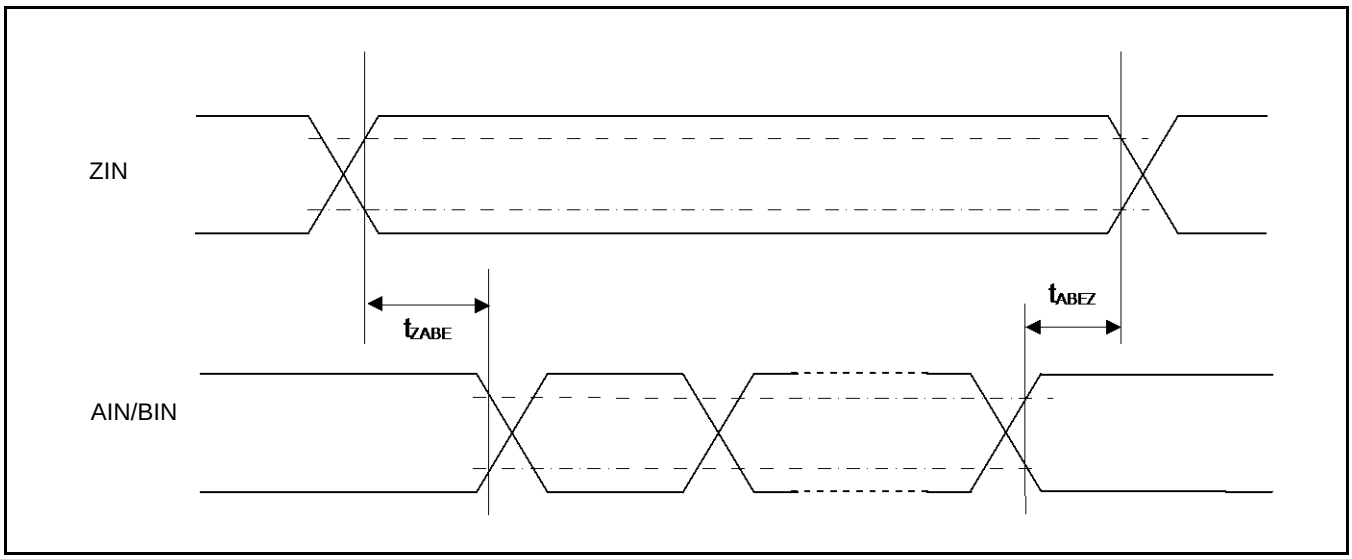
(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Conditions	Min	Max	Unit	Remarks
Serial clock L pulse width	t_{SLSH}	C_L = 30 pF	t_{CYCP} + 10	-	ns	
Serial clock H pulse width	t_{SHSL}		t_{CYCP} + 10	-	ns	
SCK fall time	t_F		-	5	ns	
SCK rise time	t_R		-	5	ns	




BIN
AIN
tBHL
tBLL
tBUAU
tAUBD
tBDAD
tADBU
tAHL
tALL


ZIN
tZHL
tZLL


ZIN
AIN/BIN
tZABE
tABEZ

12.7 MainFlash Memory Write/Erase Characteristics

12.7.1 Write / Erase time

(V_{CC} = 2.7V to 5.5V, T_A = - 40°C to + 85°C)

Parameter		Value		Unit	Remarks
		Typ*	Max*		
Sector erase time	Large Sector	0.7	3.7	s	Includes write time prior to internal erase
	Small Sector	0.3	1.1		
Half word (16-bit) write time		12	384	µs	Not including system-level overhead time
Chip erase time		8	38.4	s	Includes write time prior to internal erase

*: The typical value is immediately after shipment, the maximum value is guarantee value under 100,000 cycle of erase/write.

12.7.2 Erase/write cycles and data hold time

Erase/write cycles (cycle)	Data hold time (year)	Remarks
1,000	20*	
10,000	10*	
100,000	5*	

*: At average + 85°C

12.8 WorkFlash Memory Write/Erase Characteristics

12.8.1 Write / Erase time

(V_{CC} = 2.7V to 5.5V, T_A = - 40°C to + 85°C)

Parameter	Value		Unit	Remarks
	Typ*	Max*		
Sector erase time	0.3	1.5	s	Includes write time prior to internal erase
Half word (16-bit) write time	20	384	µs	Not including system-level overhead time
Chip erase time	1.2	6	s	Includes write time prior to internal erase

*: The typical value is immediately after shipment, the maximum value is guarantee value under 10,000 cycle of erase/write.

12.8.2 Erase/write cycles and data hold time

Erase/write cycles (cycle)	Data hold time (year)	Remarks
1,000	20*	
10,000	10*	

*: At average + 85°C

Page	Section	Change Results
75	■Electrical Characteristics 4. AC Characteristics (4-1) Operating Conditions of Main PLL (4-2) Operating Conditions of Main PLL	· Added Main PLL clock frequency · Added the figure of Main PLL connection
76	■Electrical Characteristics 4. AC Characteristics (6) Power-on Reset Timing	· Added Time until releasing Power-on reset · Changed the figure of timing
78-80	■Electrical Characteristics 4. AC Characteristics (7) External Bus Timing	Modified Data output time
88-95	■Electrical Characteristics 4. AC Characteristics (8) CSIO/UART Timing	· Modified from UART Timing to CSIO/UART Timing · Changed from Internal shift clock operation to Master mode · Changed from External shift clock operation to Slave mode
102	■Electrical Characteristics 5. 12bit A/D Converter	· Added the typical value of Integral Nonlinearity, Differential Nonlinearity, Zero transition voltage and Full-scale transition voltage · Modified Stage transition time to operation permission · Modified the minimum value of Reference voltage
105	■Electrical Characteristics 7. Low-voltage Detection Characteristics (2) Interrupt of Low-voltage Detection	Modified LVD stabilization wait time
106	■Electrical Characteristics 9. WorkFlash Memory Write/Erase Characteristics (1) Write / Erase time	· Modified sector erase time · Modified half word(16-bit) write time
107-110	■Electrical Characteristics 9. Return Time from Low-Power Consumption Mode	Added Return Time from Low-Power Consumption Mode
111	■Ordering Information	Change to full part number
112-115	■Package Dimensions	Deleted FPT-100P-M20 and FPT-120P-M21

NOTE: Please see “Document History” about later revised information.

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