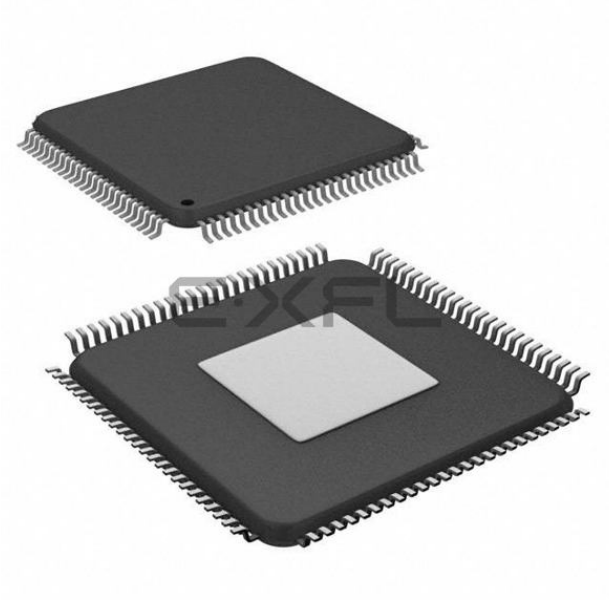

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Details	
Product Status	Obsolete
Core Processor	C166SV2
Core Size	16-Bit
Speed	80MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, SPI, SSC, UART/USART, USI
Peripherals	I²S, POR, PWM, WDT
Number of I/O	75
Program Memory Size	192KB (192K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	26K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP Exposed Pad
Supplier Device Package	PG-LQFP-100-8
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/saf-xe164fn-24f80l-aa

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XE164xN Data Sheet
Revision History: V1.4 2013-02

Previous Versions:
V1.3, 2011-07
V1.2, 2010-04
V1.1, 2009-07
V1.0, 2009-03 Preliminary

Page	Subjects (major changes since last revision)
36	Added AB step marking.
87	Errata SWD_X.P002 implemented: V_{SWD} tolerance boundaries for 5.5 V are changed.
89	Clarified “Coding of bit fields LEVxV” descriptions. Matched with Operating Conditions: marked some coding values “out of valid operation range”.
90	Errata FLASH_X.P001 implemented: Test Condition for Flash parameter N_{ER} corrected

Trademarks

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Table of Contents

1.2 Definition of Feature Variants

The XE164xN types are offered with several Flash memory sizes. Table 2 and Table 3 describe the location of the available Flash memory.

Table 2 Continuous Flash Memory Ranges

Total Flash Size	1st Range[1)]	2nd Range	3rd Range
320 Kbytes	$C0'0000_H$ … $C0'EFFF_H$	$C1'0000_H$ … $C4'FFFF_H$	n.a.
192 Kbytes	$C0'0000_H$ … $C0'EFFF_H$	$C1'0000_H$ … $C1'FFFF_H$	$C4'0000_H$ … $C4'FFFF_H$
128 Kbytes	$C0'0000_H$ … $C0'EFFF_H$	$C4'0000_H$ … $C4'FFFF_H$	n.a.

1) The uppermost 4-Kbyte sector of the first Flash segment is reserved for internal use ($C0'F000_H$ to $C0'FFFF_H$).

Table 3 Flash Memory Module Allocation (in Kbytes)

Total Flash Size	Flash 0[1)]	Flash 1
320	256	64
192	128	64
128	64	64

1) The uppermost 4-Kbyte sector of the first Flash segment is reserved for internal use ($C0'F000_H$ to $C0'FFFF_H$).

The XE164xN types are offered with different interface options. Table 4 lists the available channels for each option.

Table 4 Interface Channel Association

Total Number	Available Channels / Message Objects
6 ADC0 channels	CH0, CH2 … CH5, CH8
11 ADC0 channels	CH0, CH2 … CH5, CH8 … CH11, CH13, CH15
5 ADC1 channels	CH0, CH2, CH4 … CH6
2 CAN nodes	CAN0, CAN1 64 message objects
4 serial channels	U0C0, U0C1, U1C0, U1C1
6 serial channels	U0C0, U0C1, U1C0, U1C1, U2C0, U2C1

2.1 Pin Configuration and Definition

The pins of the XE164xN are described in detail in **Table 5**, which includes all alternate functions. For further explanations please refer to the footnotes at the end of the table. The following figure summarizes all pins, showing their locations on the four sides of the package.

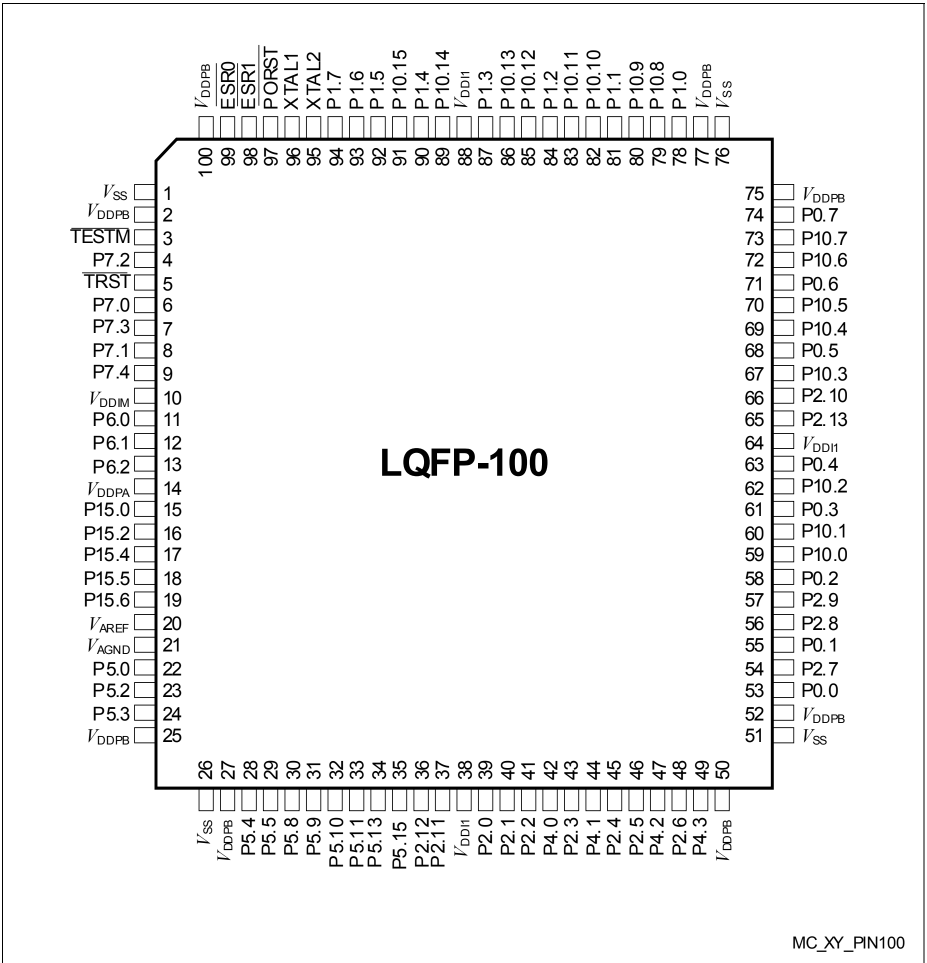

Figure 3 XE164xN Pin Configuration (top view)

Table 5 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
31	P5.9	I	In/A	**Bit 9 of Port 5, General Purpose Input**
	ADC0_CH9	I	In/A	**Analog Input Channel 9 for ADC0**
	ADC1_CH9	I	In/A	**Analog Input Channel 9 for ADC1**
	CC2_T7IN	I	In/A	**CAPCOM2 Timer T7 Count Input**
32	P5.10	I	In/A	**Bit 10 of Port 5, General Purpose Input**
	ADC0_CH10	I	In/A	**Analog Input Channel 10 for ADC0**
	ADC1_CH10	I	In/A	**Analog Input Channel 10 for ADC1**
	BRKIN_A	I	In/A	**OCDS Break Signal Input**
	U2C1_DX0F	I	In/A	**USIC2 Channel 1 Shift Data Input**
	CCU61_T13HRA	I	In/A	**External Run Control Input for T13 of CCU61**
33	P5.11	I	In/A	**Bit 11 of Port 5, General Purpose Input**
	ADC0_CH11	I	In/A	**Analog Input Channel 11 for ADC0**
	ADC1_CH11	I	In/A	**Analog Input Channel 11 for ADC1**
34	P5.13	I	In/A	**Bit 13 of Port 5, General Purpose Input**
	ADC0_CH13	I	In/A	**Analog Input Channel 13 for ADC0**
35	P5.15	I	In/A	**Bit 15 of Port 5, General Purpose Input**
	ADC0_CH15	I	In/A	**Analog Input Channel 15 for ADC0**
36	P2.12	O0 / I	St/B	**Bit 12 of Port 2, General Purpose Input/Output**
	U0C0_SELO4	O1	St/B	**USIC0 Channel 0 Select/Control 4 Output**
	U0C1_SELO3	O2	St/B	**USIC0 Channel 1 Select/Control 3 Output**
	READY	IH	St/B	**External Bus Interface READY Input**
37	P2.11	O0 / I	St/B	**Bit 11 of Port 2, General Purpose Input/Output**
	U0C0_SELO2	O1	St/B	**USIC0 Channel 0 Select/Control 2 Output**
	U0C1_SELO2	O2	St/B	**USIC0 Channel 1 Select/Control 2 Output**
	BHE/WRH	OH	St/B	**External Bus Interf. High-Byte Control Output** Can operate either as Byte High Enable (BHE) or as Write strobe for High Byte (WRH).

Table 5 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
57	P2.9	O0 / I	St/B	**Bit 9 of Port 2, General Purpose Input/Output**
	U0C1_DOUT	O1	St/B	**USIC0 Channel 1 Shift Data Output**
	TxDC1	O2	St/B	**CAN Node 1 Transmit Data Output**
	CC2_CC22	O3 / I	St/B	**CAPCOM2 CC22IO Capture Inp./ Compare Out.**
	A22	OH	St/B	**External Bus Interface Address Line 22**
	CLKIN1	I	St/B	**Clock Signal Input 1**
	TCK_A	IH	St/B	**DAP0/JTAG Clock Input** If JTAG pos. A is selected during start-up, an internal pull-up device will hold this pin high when nothing is driving it. If DAP pos. 0 is selected during start-up, an internal pull-down device will hold this pin low when nothing is driving it.
58	P0.2	O0 / I	St/B	**Bit 2 of Port 0, General Purpose Input/Output**
	U1C0_SCLKOUT	O1	St/B	**USIC1 Channel 0 Shift Clock Output**
	TxDC0	O2	St/B	**CAN Node 0 Transmit Data Output**
	CCU61_CC62	O3	St/B	**CCU61 Channel 2 Output**
	A2	OH	St/B	**External Bus Interface Address Line 2**
	U1C0_DX1B	I	St/B	**USIC1 Channel 0 Shift Clock Input**
	CCU61_CC62INA	I	St/B	**CCU61 Channel 2 Input**

Table 5 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
81	P1.1	O0 / I	St/B	**Bit 1 of Port 1, General Purpose Input/Output**
	U1C0_SELO5	O2	St/B	**USIC1 Channel 0 Select/Control 5 Output**
	U2C1_DOUT	O3	St/B	**USIC2 Channel 1 Shift Data Output**
	A9	OH	St/B	**External Bus Interface Address Line 9**
	ESR2_3	I	St/B	**ESR2 Trigger Input 3**
	U2C1_DX0C	I	St/B	**USIC2 Channel 1 Shift Data Input**
82	P10.10	O0 / I	St/B	**Bit 10 of Port 10, General Purpose Input/Output**
	U0C0_SELO0	O1	St/B	**USIC0 Channel 0 Select/Control 0 Output**
	CCU60_COUT63	O2	St/B	**CCU60 Channel 3 Output**
	AD10	OH / IH	St/B	**External Bus Interface Address/Data Line 10**
	U0C0_DX2C	I	St/B	**USIC0 Channel 0 Shift Control Input**
	U0C1_DX1A	I	St/B	**USIC0 Channel 1 Shift Clock Input**
	TDI_B	IH	St/B	**JTAG Test Data Input** If JTAG pos. B is selected during start-up, an internal pull-up device will hold this pin high when nothing is driving it.
83	P10.11	O0 / I	St/B	**Bit 11 of Port 10, General Purpose Input/Output**
	U1C0_SCLKOUT	O1	St/B	**USIC1 Channel 0 Shift Clock Output**
	$\overline{\text{BRKOUT}}$	O2	St/B	**OCDS Break Signal Output**
	AD11	OH / IH	St/B	**External Bus Interface Address/Data Line 11**
	U1C0_DX1D	I	St/B	**USIC1 Channel 0 Shift Clock Input**
	TMS_B	IH	St/B	**JTAG Test Mode Selection Input** If JTAG pos. B is selected during start-up, an internal pull-up device will hold this pin high when nothing is driving it.

Table 5 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
2, 25, 27, 50, 52, 75, 77, 100	V_{DDPB}	-	PS/B	**Digital Pad Supply Voltage for Domain B** Connect decoupling capacitors to adjacent V_{DDP}/V_{SS} pin pairs as close as possible to the pins. *Note: The on-chip voltage regulators and all ports except P5, P6 and P15 are fed from supply voltage V_{DDPB}.*
1, 26, 51, 76	V_{SS}	-	PS/--	**Digital Ground** All V_{SS} pins must be connected to the ground-line or ground-plane. *Note: Also the exposed pad is connected internally to V_{SS}. To improve the EMC behavior, it is recommended to connect the exposed pad to the board ground. For thermal aspects, please refer to the Data Sheet. Board layout examples are given in an application note.*

1) To generate the reference clock output for bus timing measurement, f_{SYS} must be selected as source for EXTCLK and P2.8 must be selected as output pin. Also the high-speed clock pad must be enabled. This configuration is referred to as reference clock output signal CLKOUT.

3.3 Central Processing Unit (CPU)

The core of the CPU consists of a 5-stage execution pipeline with a 2-stage instruction-fetch pipeline, a 16-bit arithmetic and logic unit (ALU), a 32-bit/40-bit multiply and accumulate unit (MAC), a register-file providing three register banks, and dedicated SFRs. The ALU features a multiply-and-divide unit, a bit-mask generator, and a barrel shifter.

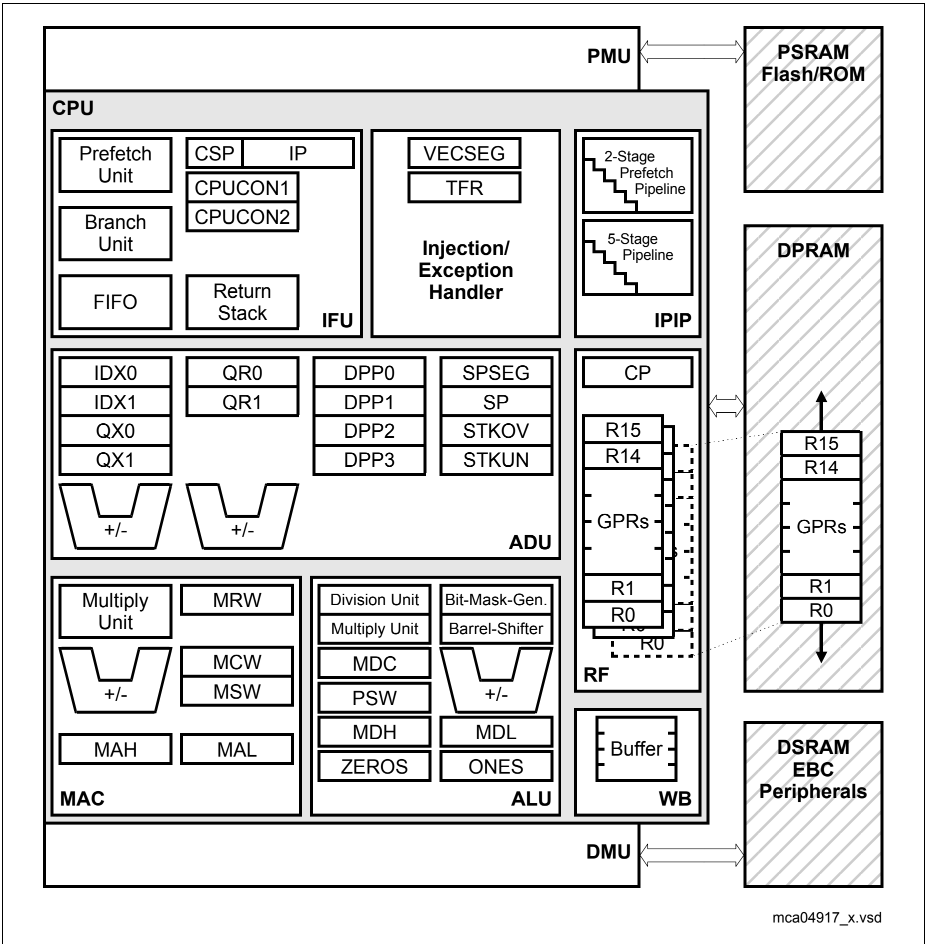

Figure 5 CPU Block Diagram

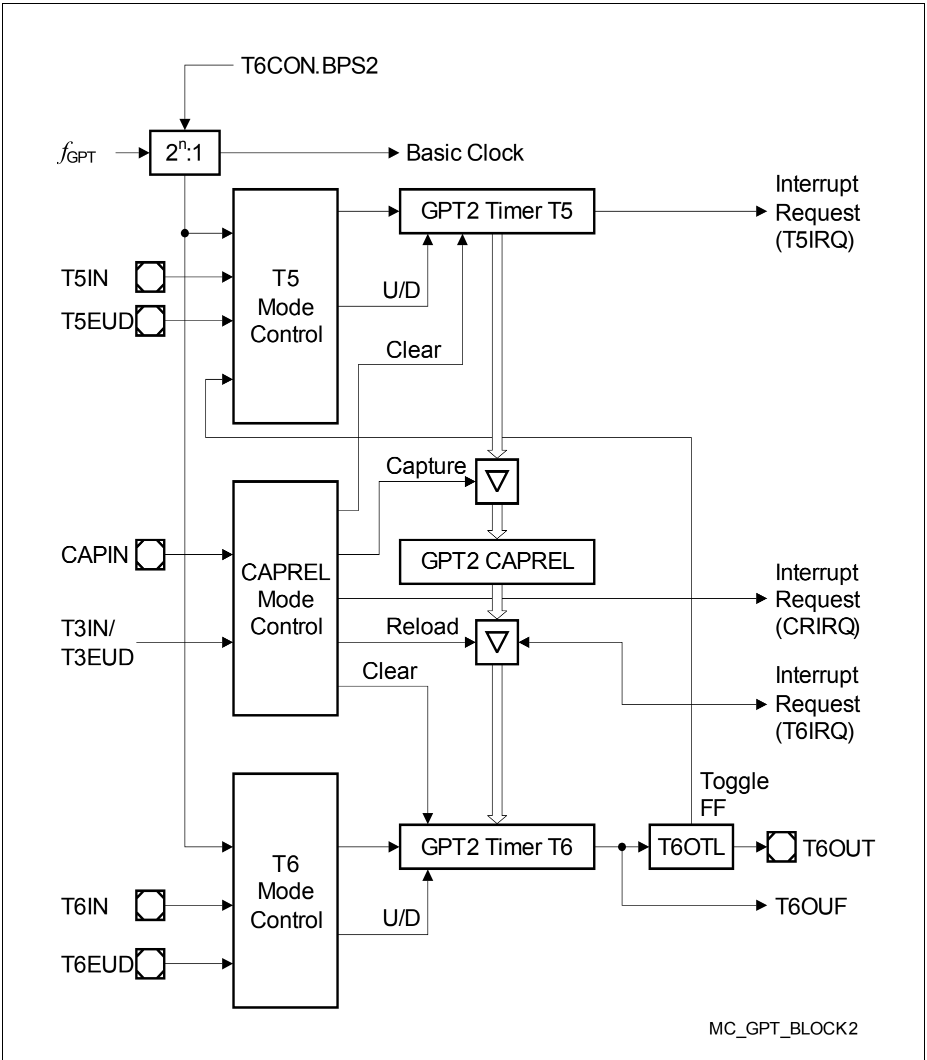

Figure 9 Block Diagram of GPT2

3.13 Universal Serial Interface Channel Modules (USIC)

The XE164xN features the USIC modules USIC0, USIC1, USIC2. Each module provides two serial communication channels.

The Universal Serial Interface Channel (USIC) module is based on a generic data shift and data storage structure which is identical for all supported serial communication protocols. Each channel supports complete full-duplex operation with a basic data buffer structure (one transmit buffer and two receive buffer stages). In addition, the data handling software can use FIFOs.

The protocol part (generation of shift clock/data/control signals) is independent of the general part and is handled by protocol-specific preprocessors (PPPs).

The USIC's input/output lines are connected to pins by a pin routing unit. The inputs and outputs of each USIC channel can be assigned to different interface pins, providing great flexibility to the application software. All assignments can be made during runtime.

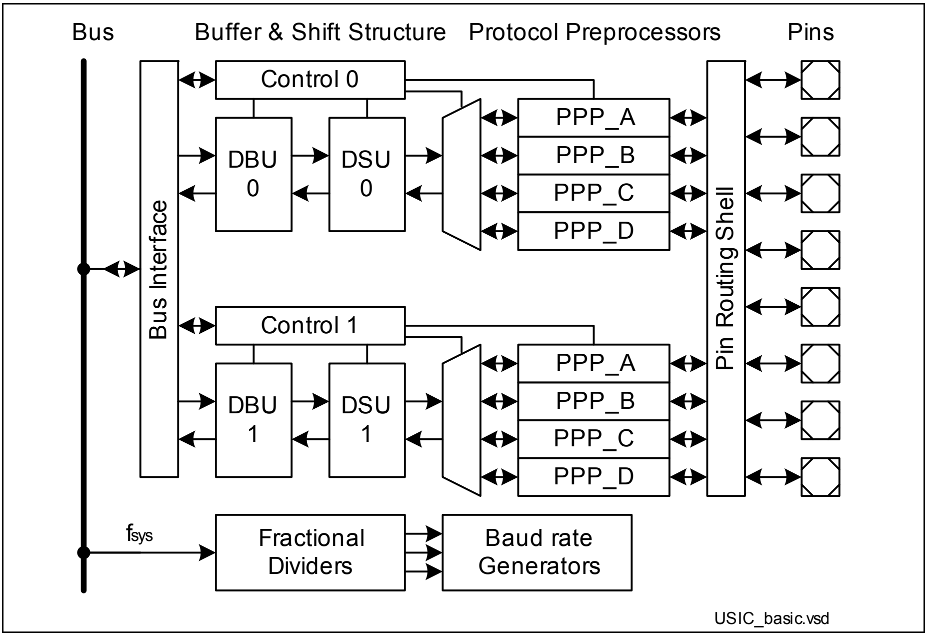

Figure 11 General Structure of a USIC Module

The regular structure of the USIC module brings the following advantages:

- Higher flexibility through configuration with same look-and-feel for data management
- Reduced complexity for low-level drivers serving different protocols
- Wide range of protocols with improved performances (baud rate, buffer handling)

4 Electrical Parameters

The operating range for the XE164xN is defined by its electrical parameters. For proper operation the specified limits must be respected when integrating the device in its target environment.

4.1 General Parameters

These parameters are valid for all subsequent descriptions, unless otherwise noted.

Table 11 Absolute Maximum Rating Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Output current on a pin when high value is driven	I_{OH} SR	-30	–	–	mA	
Output current on a pin when low value is driven	I_{OL} SR	–	–	30	mA	
Overload current	I_{OV} SR	-10	–	10	mA	[1]
Absolute sum of overload currents	$\Sigma\lvert I_{OV}\rvert$ SR	–	–	100	mA	[1]
Junction Temperature	T_J SR	-40	–	150	°C	
Storage Temperature	T_{ST} SR	-65	–	150	°C	
Digital supply voltage for IO pads and voltage regulators	V_{DDP} SR	-0.5	–	6.0	V	
Voltage on any pin with respect to ground (Vss)	V_{IN} SR	-0.5	–	V_{DDP} + 0.5	V	$V_{IN} \leq V_{DDP(max)}$

1) Overload condition occurs if the input voltage V_{IN} is out of the absolute maximum rating range. In this case the current must be limited to the listed values by design measures.

Note: Stresses above the values listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for an extended time may affect device reliability.
During absolute maximum rating overload conditions ($V_{IN} > V_{DDP}$ or $V_{IN} < V_{SS}$) the voltage on V_{DDP} pins with respect to ground (V_{SS}) must not exceed the values defined by the absolute maximum ratings.

4.1.1 Operating Conditions

The following operating conditions must not be exceeded to ensure correct operation of the XE164xN. All parameters specified in the following sections refer to these operating conditions, unless otherwise noticed.

Note: Typical parameter values refer to room temperature and nominal supply voltage, minimum/maximum parameter values also include conditions of minimum/maximum temperature and minimum/maximum supply voltage. Additional details are described where applicable.

Table 12 Operating Conditions

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Voltage Regulator Buffer Capacitance for DMP_M	C_{EVRM} SR	1.0	–	4.7	µF	[1]
Voltage Regulator Buffer Capacitance for DMP_1	C_{EVR1} SR	0.47	–	2.2	µF	[2][1]
External Load Capacitance	C_L SR	–	20[3]	–	pF	pin out driver= default [4]
System frequency	f_{SYS} SR	–	–	80	MHz	[5]
Overload current for analog inputs[6]	I_{OVA} SR	-2	–	5	mA	not subject to production test
Overload current for digital inputs[6]	I_{OVD} SR	-5	–	5	mA	not subject to production test
Overload current coupling factor for analog inputs[7]	K_{OVA} CC	–	2.5×10^{-4}	1.5×10^{-3}	-	I_{OV}< 0 mA; not subject to production test
		–	1.0×10^{-6}	1.0×10^{-4}	-	I_{OV}> 0 mA; not subject to production test

Pullup/Pulldown Device Behavior

Most pins of the XE164xN feature pullup or pulldown devices. For some special pins these are fixed; for the port pins they can be selected by the application.

The specified current values indicate how to load the respective pin depending on the intended signal level. **Figure 13** shows the current paths.

The shaded resistors shown in the figure may be required to compensate system pull currents that do not match the given limit values.

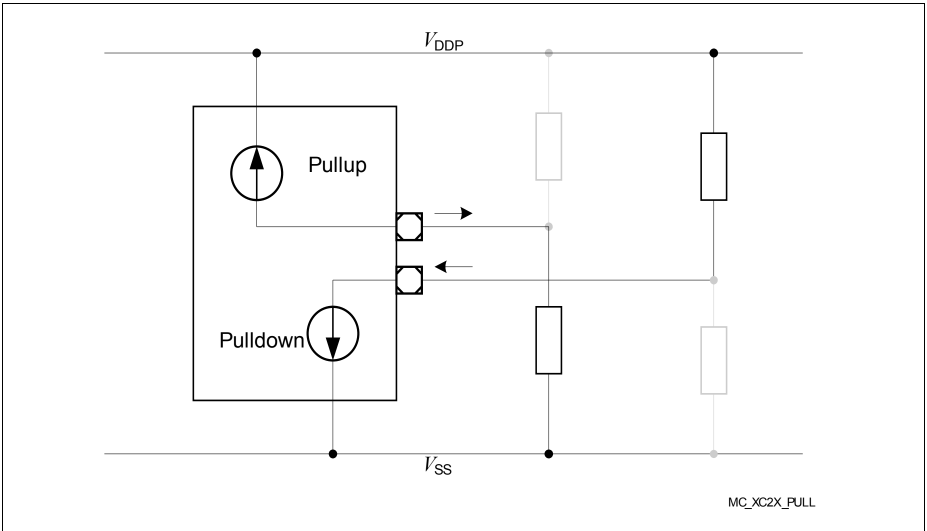

Figure 13 Pullup/Pulldown Current Definition

Table 15 DC Characteristics for Upper Voltage Range (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Output High voltage[7)]	V_{OH} CC	V_{DDP} - 1.0	–	–	V	$I_{OH} \geq I_{OHmax}$
		V_{DDP} - 0.4	–	–	V	$I_{OH} \geq I_{OHnom}$ [8)]
Output Low Voltage[7)]	V_{OL} CC	–	–	0.4	V	$I_{OL} \leq I_{OLnom}$ [8)]
		–	–	1.0	V	$I_{OL} \leq I_{OLmax}$

1) Because each double bond pin is connected to two pads (standard pad and high-speed pad), it has twice the normal value. For a list of affected pins refer to the pin definitions table in chapter 2.

2) Not subject to production test - verified by design/characterization. Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It cannot suppress switching due to external system noise under all conditions.

3) If the input voltage exceeds the respective supply voltage due to ground bouncing ($V_{IN} < V_{SS}$) or supply ripple ($V_{IN} > V_{DDP}$), a certain amount of current may flow through the protection diodes. This current adds to the leakage current. An additional error current (I_{INJ}) will flow if an overload current flows through an adjacent pin. Please refer to the definition of the overload coupling factor K_{OV}.

4) The given values are worst-case values. In production test, this leakage current is only tested at 125 °C; other values are ensured by correlation. For derating, please refer to the following descriptions: Leakage derating depending on temperature (T_J = junction temperature [°C]): I_{OZ} = 0.05 x $e^{(1.5 + 0.028 \times TJ>)}$ [µA]. For example, at a temperature of 95 °C the resulting leakage current is 3.2 µA. Leakage derating depending on voltage level (DV = V_{DDP} - V_{PIN} [V]): $I_{OZ} = I_{OZtempmax}$ - (1.6 x DV) (µA]. This voltage derating formula is an approximation which applies for maximum temperature.

5) Drive the indicated minimum current through this pin to change the default pin level driven by the enabled pull device.

6) Limit the current through this pin to the indicated value so that the enabled pull device can keep the default pin level.

7) The maximum deliverable output current of a port driver depends on the selected output driver mode. This specification is not valid for outputs which are switched to open drain mode. In this case the respective output will float and the voltage is determined by the external circuit.

8) As a rule, with decreasing output current the output levels approach the respective supply level (V_{OL}->V_{SS}, V_{OH}->V_{DDP}). However, only the levels for nominal output currents are verified.

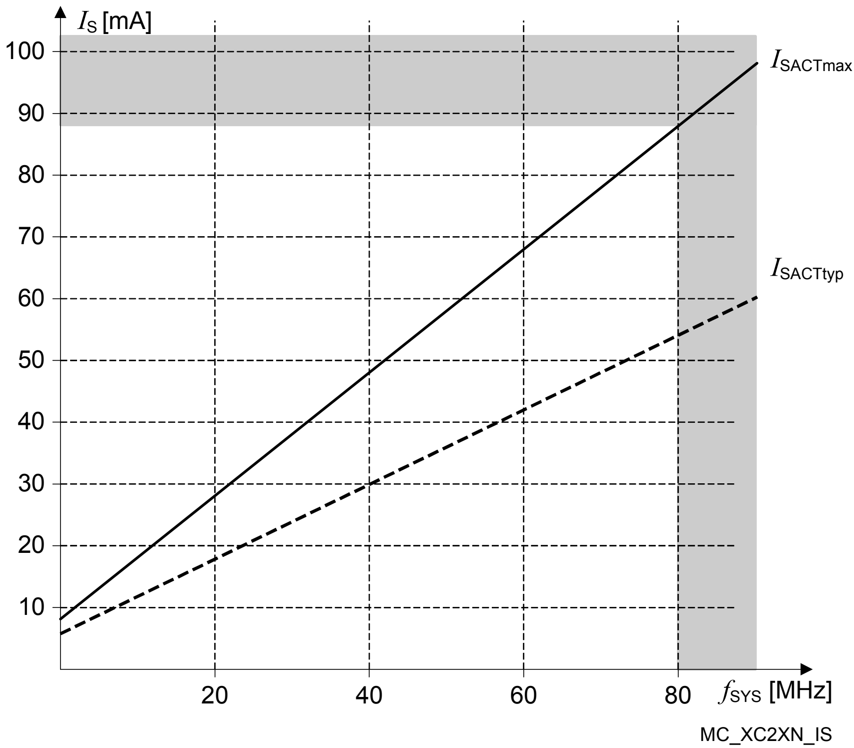

Figure 14 Supply Current in Active Mode as a Function of Frequency

Note: Operating Conditions apply.

Table 18 Leakage Power Consumption

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Leakage supply current [1]	I_{LK1} CC	–	0.03	0.04	mA	T_J= 25 °C[1]
		–	0.5	1.2	mA	T_J= 85 °C[1]
		–	1.9	5.5	mA	T_J= 125 °C[1]
		–	3.9	12.2	mA	T_J= 150 °C[1]

1) All inputs (including pins configured as inputs) are set at 0 V to 0.1 V or at V_{DDP} - 0.1 V to V_{DDP} and all outputs (including pins configured as outputs) are disconnected.

4.7.2 Definition of Internal Timing

The internal operation of the XE164xN is controlled by the internal system clock f_{SYS}.

Because the system clock signal f_{SYS} can be generated from a number of internal and external sources using different mechanisms, the duration of the system clock periods (TCSs) and their variation (as well as the derived external timing) depend on the mechanism used to generate f_{SYS}. This must be considered when calculating the timing for the XE164xN.

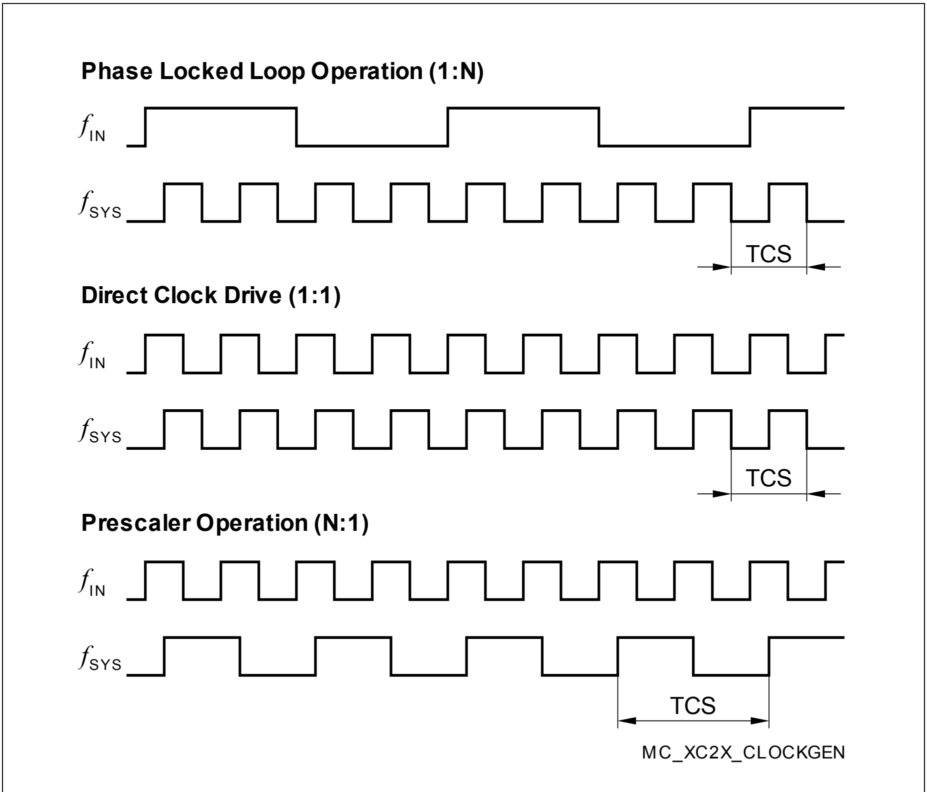

Figure 19 Generation Mechanisms for the System Clock

Note: The example of PLL operation shown in ***Figure 19*** *uses a PLL factor of 1:4; the example of prescaler operation uses a divider factor of 2:1.*

The specification of the external timing (AC Characteristics) depends on the period of the system clock (TCS).

Table 28 Standard Pad Parameters for Lower Voltage Range (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Rise and Fall times (10% - 90%)	t_{RF} CC	–	–	37 + 0.65 x C_L	ns	$C_L \geq$ 20 pF; $C_L \leq$ 100 pF; Driver_Strength = Medium
		–	–	24 + 0.3 x C_L	ns	$C_L \geq$ 20 pF; $C_L \leq$ 100 pF; Driver_Strength = Strong ; Driver_Edge= Medium
		–	–	6.2 + 0.24 x C_L	ns	$C_L \geq$ 20 pF; $C_L \leq$ 100 pF; Driver_Strength = Strong ; Driver_Edge= Sharp
		–	–	34 + 0.3 x C_L	ns	$C_L \geq$ 20 pF; $C_L \leq$ 100 pF; Driver_Strength = Strong ; Driver_Edge= Slow
		–	–	500 + 2.5 x C_L	ns	$C_L \geq$ 20 pF; $C_L \leq$ 100 pF; Driver_Strength = Weak

1) An output current above $|I_{OXnom}|$ may be drawn from up to three pins at the same time. For any group of 16 neighboring output pins, the total output current in each direction (ΣI_{OL} and Σ-I_{OH}) must remain below 50 mA.

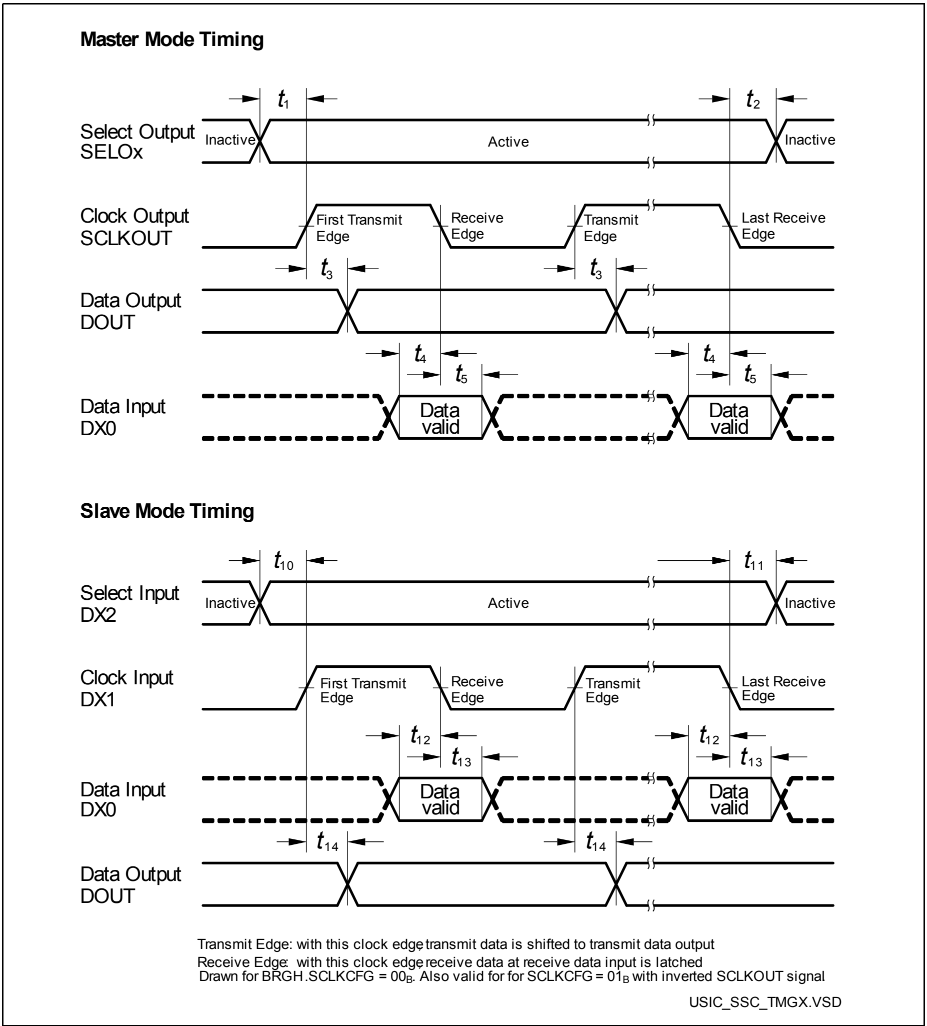

Figure 26 USIC - SSC Master/Slave Mode Timing

Note: This timing diagram shows a standard configuration where the slave select signal is low-active and the serial clock signal is not shifted and not inverted.